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SOA Gate Array Recirculating Buffer for Optical Packet Switching

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Abstract: A compact recirculating buffer using an InP-based 2x2 switch with gain and a fiber delay line is demonstrated at 40 Gb/s. Packet throughput of 98% is measured for up to 8 circulations, or 0.18 μs.
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1. Introduction

Optical buffering is one of the major challenges in realizing the benefits of optical packet switching. However, a compact, scalable, high bit-rate solution has yet to be demonstrated [1]. The majority of optical buffering approaches can be generalized as either feedback or feed-forward buffers, many of which implement two-by-two and one-by-two switches [2, 3]. Although reasonable storage times have been demonstrated, there have not been any practical compact solutions. The buffer presented here is demonstrated without any additional components in the delay loop and can be easily integrated with an on-chip silicon or silica delay. To the authors' knowledge, this device has the best performance for a buffer approach amenable to integration.

2. Buffer design

A recirculating buffer approach is chosen to provide dynamic control of storage times with the granularity of the delay line length. Recirculating buffers have been pursued with success in the past using fiber loops [4, 5] and therefore show promise for a practical buffer if they can be designed to be amenable to integration while not sacrificing performance. The buffer combines a 2x2 InP-based switch with 450 centimeters of fiber or silica delay line (Fig. 1a). The delay line length is chosen to be slightly longer than the length of a packet and its guard bands; thus allowing the greatest resolution in possible delay times.
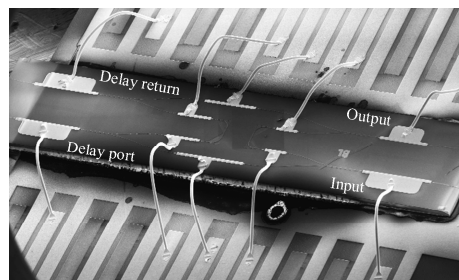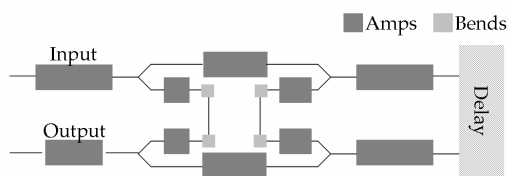

Fig. 1. a) Schematic of 2x2 switch with amplifiers. b) SEM image of the switch affixed and wire-bonded to a submount.

Recirculating buffers place significant performance requirements on the 2x2 switch. To be competitive, the switch must be bit-rate scalable up to 40 Gb/s, have low crosstalk (< -40 dB) and high extinction ratios (>40 dB) for cascadability [6], and be able to switch within packet guard bands. The semiconductor optical amplifier (SOA) gate matrix switch is the most promising switch choice for recirculating buffers because it is fast, meets the crosstalk requirement, and has low insertion loss. During operation, the signal is split toward the two possible ports and the switching amplifier is turned on for the desired path while the other path's amplifier is left off to absorb the remainder. A fabricated switch was previously characterized with good performance up to 40 Gb/s and switching times less than 2 ns [7]. A second generation for integration was fabricated and is shown in Fig. 1b.

The InGaAsP/InP SOA gate matrix switch presented here has an improved integrated amplifier layout and waveguide routing. The switch uses an offset quantum well platform in which the quantum wells are grown above a bulk waveguide layer. This results in an offset between the peak of the mode and the gain region and thereby lowers

the confinement factor. The benefits of this platform include ease of fabrication, the possibility of future integration with other standard photonic integrated circuits, and linear performance at higher output powers due to the lower confinement factor [8]. Many-body gain simulations were performed to optimize the placement and lengths of the amplifiers in order to distribute the gain and minimize saturation. The total gain is designed to exceed the loss by only several dB. Therefore, during the first several circulations there is slight gain until the amplified spontaneous emission (ASE) builds up and detracts slightly from signal gain. The amplifier lengths range from 200 μm long for the switching amplifiers in the shortest path up to 650 μm long for the input amplifier and the amplifiers on both ends of the delay. In addition, the amplifier directly before the delay is flared as it will see the most power. An additional component is the tightly confining, deeply etched bend to avoid crossing waveguides while allowing the input and output ports to be positioned on the side opposite to the delay ports.

3. Measurements

3.1 Measurement setup

The experiments were performed on devices that were soldered and wirebonded to aluminum nitride submounts and subsequently affixed with thermal compound to a copper mount. The submounts were cooled to approximately 18°C. Lensed fibers were used at each of the four ports to couple light on and off the chip. The optical signal (1550 nm) was modulated using an SHF 50 Gb/s BERT with RZ 2^{31}-1 pseudo-random bit sequence (PRBS) data at 40 Gb/s. Packet measurements were made using 40-byte packets which contained identifier strings for characterization. A variable attenuator and a polarization controller were placed in the setup before the device to maintain a TE-polarized input since the quantum well amplifiers are polarization dependent. A 1.2-nm bandpass filter was placed before the receiver to reduce the ASE.

3.2 InP switch

Static measurements and bit error rate testing were performed using continuous data at 40 Gb/s to characterize the performance of the switch. The chip gain from the input port fiber to the delay fiber was approximately 2 dB. The sensitivity degradation for the four port configurations at 40 Gb/s is shown in Fig. 2a. The back-to-back measurement is taken as a reference for the system by bypassing only the device under test with a fiber patch cord. As can be seen in Fig. 2a, the measurements show negative power penalty. This is due to reshaping from the amplifiers and the bandpass filter used to reduce the accumulated ASE. The primary limitation of sensitivity is the ASE that builds up in the amplifiers. The dynamic range of the input power is shown below in Fig. 2b and is greater than 15 dB.
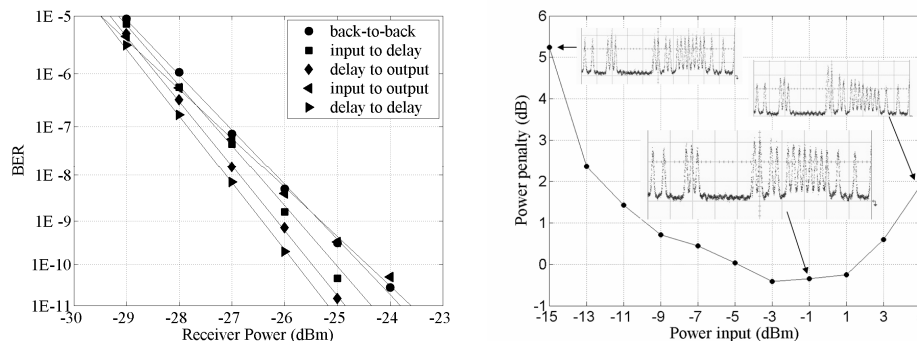

Fig. 2. a) BER vs. optical power at 40 Gb/s RZ 2^{31}-1. b) Operable range of input powers for the path from the input port to the delay port.

3.3 Buffering

The InP-based switch was combined with a fiber delay loop to demonstrate successful optical buffering of packets. The fiber delay was chosen to be 23 ns, which is therefore also the resolution of the storage time. Optical signal-to-noise ratios (OSNR) were measured by taking the difference of the power of the signal and the noise at a wavelength 1 nm away. These calculations were done for a range of the input power to the device for all storage times from 1 to 10 circulations. The back-to-back OSNR was 53 dBm.
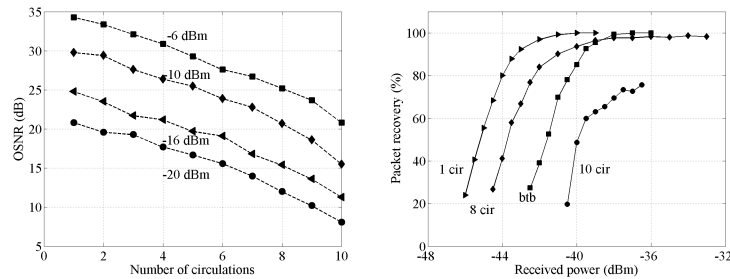
Fig. 3. a) Optical signal-to-noise ratios as a function of number of circulations for a range of input powers. b) Packet recovery percentage as a function of received power for back-to-back and 1, 8, and 10 circulations.

Packet recovery data was then taken to demonstrate that the data was preserved. Due to the size and spacing of the packets, the BERT can not synchronize to the data; therefore bit error rate measurements are not possible. Packet recovery is used as a Layer 2 metric that can predict the buffer's ultimate success in an all-optical router. Forty-byte packets were stored for up to 184 ns with recovery greater than 98%, as shown in Fig. 3b. In addition, the dynamic range of the buffer was tested for 4 circulations and shown to be error-free over an 8 dB range of input power (Fig. 4a). Lastly, a 5-nm bandpass filter was used in the recirculation loop to reduce the ASE buildup. Figure 4b shows the improvement provided by the filter, which increases the maximum storage time to 230 ns.
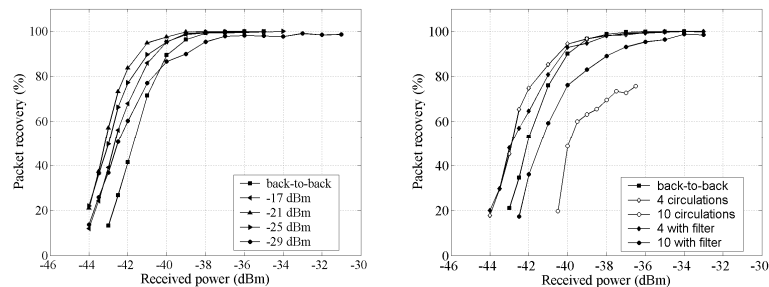

Fig. 4. a) Packet recovery measurements for varying input power for a delay of 4 circulations.
b) Improvement shown in packet recovery by using a bandpass filter in the delay line.

4. Conclusions

The buffer demonstrated here uses an SOA gate array switch that has excellent extinction (40 dB), low crosstalk (-40 dB) and sufficient gain to balance the recirculating losses. The buffer is randomly accessible in time increments of 23 ns and can store packets for up to 184 ns with greater than 98% packet recovery. This approach provides a practical solution to meet the predicted memory needs in future optical routers [9]. The buffer presented offers a compact solution for optical memory that can be easily integrated with a chip delay.

5. References

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