



conversion with both device types at bit rates of 40 Gbps RZ has been reported. In addition, a fully integrated packet forwarding chip (PFC), operating with 40 Gbps payloads and 10 Gbps labels has been successfully demonstrated and used in an optical switch demonstration [1,3]. Finally, multistage tunable wavelength converter MZI-SOA based implementations with on chip signal filtering have been demonstrated as well [5].

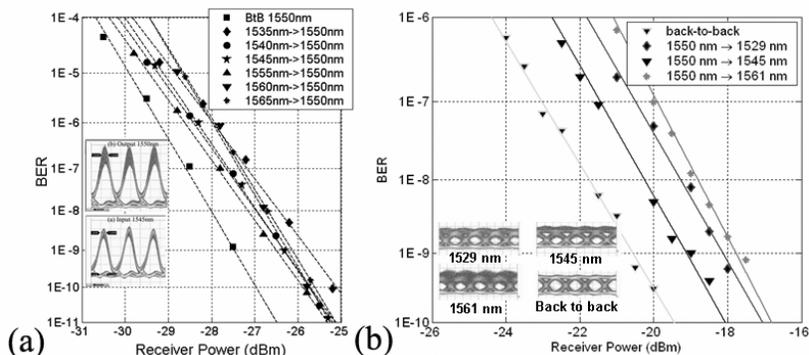


Figure 2 – (a) PFC - Bit error rate results for 40 Gbps RZ operation (b) SAM - Bit error rate results for 40 Gbps NRZ operation

Recently, successful demonstration of the separate absorption and modulation (SAM) approach to wavelength conversion has been accomplished for bit rates up to 40 Gbps [6]. In this method, a transmitter and receiver are monolithically integrated on a single chip. The photodiode is directly connected to the modulator through an on-chip terminated traveling wave electrode, allowing the photocurrent from an absorbed input signal to directly drive an optical modulator. Since the photodiode produces enough photocurrent to drive the optical modulator there is no need for any electrical amplification. Due to the spatial separation of the receiver and transmitter waveguides, SAM wavelength converters have no optical filtering requirements. These devices also have the advantage of lower power consumption and smaller footprints than comparable SOA-based devices. Operation at 40 Gbps with NRZ data shows less than a 2.5 dB power penalty across the 32 nm laser tuning range with no additional power penalty for conversion to the input wavelength. Both Mach-Zehnder and EAM based devices are being investigated [6,7].

### 3. Integrated Optical Buffers

The realization of practical optical memory elements to resolve packet contention is necessary before optical routers can become viable. The most successful optical buffering demonstrations have used either feedback or feed-forward buffers, many of which implement two-by-two or one-by-two switches [8]. Although practical storage times have been demonstrated, there have not been any integrated solutions.

Recently, a simple recirculating buffer that operates without additional control components in the delay loop was presented [9]. This recirculating buffer was based on an InP SOA gate array two-by-two switch and an optical fiber delay loop, 450 centimeters, or 23 ns, in length. The buffer exhibited greater than 40 dB extinction, sub-nanosecond switching, and fiber-to-fiber gain. Up to 184 ns of storage was demonstrated with greater than 98% packet recovery for 40 Gb/s, 40-byte packets, Figure 3. To the authors' knowledge, this device has the best performance for a buffer approach amenable to integration. Further work on all photonic chip based buffers is underway.

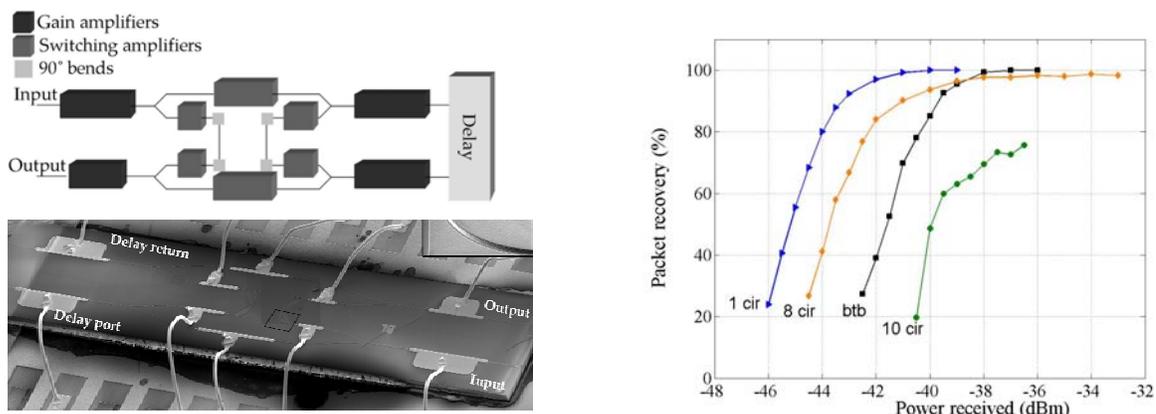
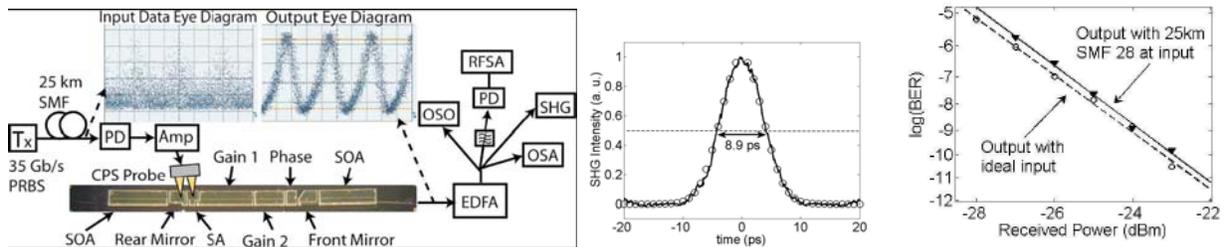


Figure 3 (top-left) Schematic of 2x2 switch with amplifiers (bottom left) SEM image of the switch affixed and wire-bonded to a submount (right) Packet recovery of 98% for up to 8 circulations (184 ns delay).

#### 4. Monolithic Mode-Locked Laser and Optical Amplifier

Mode locked lasers (MLLs) are key components for 3R regeneration applications in optical routers. Some qualities of MLLs utilized in optical clock recovery are their ability to perform jitter reduction, pulse reshaping, and amplification. Since the frequency of mode locking is determined by the cavity length, traditional MLLs with cleaved facets are not reproducible at a specific frequency. This, special MLL designs, compatible with further integration into complex 3R PICs, are of particular interest.

Recently, we have experimentally demonstrated optical clock recovery using a novel mode-locked laser (MLL) [10, 11] monolithically integrated with an output semiconductor optical amplifier. The laser's distributed Bragg reflector (DBR) mirror positions are determined using lithography, allowing for mode locking and clock recovery at the exact frequency of the design (35.00 GHz), which is easily scalable to 40 GHz or higher. The laser design and fabrication platform are compatible with other photonic integrated circuit components, enabling integrated signal processing using these MLLs in the future.



**Figure 4 – (left) Experimental setup for hybrid clock recovery, with eye diagrams of the input and output signals and photograph of the device. The recovered clock appears to have high jitter because of poor OSO triggering. The actual jitter is 1.14 ps (middle) SHG trace of the output pulses. The solid line is the data and the open circles are a Gaussian fit (right) Bit error rates of the output clock that has been gated by the input data and sent to the receiver with a normal input and with input signal degradation**

The device was shown to generate nearly transform limited pulses at 35.0-GHz repetition rate with pulse widths tunable between 3.5 and 8.5 ps, over 12 dB extinction ratio (ER), and 8.3 dBm average output power. Both all-optical [10] and hybrid [11] clock recovery were tested for this device. Among other regenerative capabilities, the device performed optical clock recovery with 50% jitter reduction from a degraded input signal with low ER. By combining this type of MLL with a nonlinear optical gate such as a Mach Zehnder SOA structure or SAM device, a fully integrated 3R regenerator can be created.

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