1.5mW/Gbps Low Power Optical Interconnect Transmitter Exploiting High-Efficiency VCSEL and CMOS Driver

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Abstract: We demonstrate a low power optical interconnect transmitter which employs a 990nm VCSEL with high efficiency and low threshold current, and a 130nm CMOS driver. The power dissipated by the transmitter is 15.1 mW at 10 Gbps.

OCIS codes: (060.2360) Fiber optics links and subsystems; (200.4650) Optical Interconnects;

1. Introduction

Requirements for interconnects in computing systems are getting harder to satisfy without employing optical technologies, as the performance keeps growing with the evolution of CMOS technologies as well as system architectures. The emphasis of system designs has been shifting toward reducing power consumption from increasing performance. The total system power, including the power required for cooling as well as for computation, is reaching to or even exceeding the limit of power supply when the system performance is increased. One main advantage of optical compared to electrical interconnects, in addition to the benefit of long-distance transmission at high data rate with optics, is a high data rate density, which provides large bandwidth through a small volume or area. This results in an efficient flow of cooling air through systems as well as tight integration of optical interconnects with electronic chips. As the bandwidth and channel count of interconnects has to be increased for evolving system performance and architecture, these benefits of optical interconnects are crucial.

Reduction of the power consumed by optical interconnects is critical to increase the aggregate interconnect bandwidth for further system performance improvement. Several efforts have been made to realize high data rates with low power dissipation, and recent breakthroughs have been made by deploying CMOS technology for high-speed laser diode drivers (LDDs) and high-speed transimpedance amplifiers plus limiting amplifiers (TIA/LIAs) [1, 2]. VCSELs have already demonstrated their inherent advantage of low-power and high-speed operation, suited for light sources of optical interconnects, and more emphasis has been placed on design optimization for high-speed operation [3]. In this talk, we design and demonstrate a very low power optical interconnect by focusing on reducing the power dissipation of the whole optical link, instead of decreasing the power consumed by each component individually. More specifically, we focus on the design of optical transmitters, which consist of the VCSELs and LDDs, to realize high optical modulation amplitude (OMA) with small modulation current, enabling reductions of the power dissipated by the LDD and TIA/LIA. The low power design presented in this talk can be also applied to any short-reach datacom and telecom transmitters based on VCSELs.

2. Low power optical interconnect design

An optical interconnect, shown in Fig. 1, has to be designed to meet the requirements of input and output electrical signals, such as a voltage amplitude and data rate. The VCSEL drive current and the optical link budget, however, have more freedom to be designed as long as error-free transmission is achieved and the swing voltage requirements are met. One approach to minimize the total power dissipation of an optical interconnect is to decrease the VCSEL modulation current, while simultaneously increasing the transmitted OMA. The reduced modulation current lowers the power dissipated by the LDD both in the pre-driver and output stages. Increased OMA further enables a reduction in the TIA/LIA power consumption due to lower required gain. Increasing the differential quantum efficiency (DQE) of a VCSEL provides larger OMA with smaller modulation current. One way to increase the DQE of a VCSEL is to decrease its internal loss, which also reduces its threshold material gain. The reduced threshold gain results in decreased power dissipation in the LDD output stage due to lowered bias current while supporting high-speed operation and enough optical average power. The DQE of a VCSEL can also be increased by decreasing the reflectivity of the output mirror, but at the expense of increased bias current.

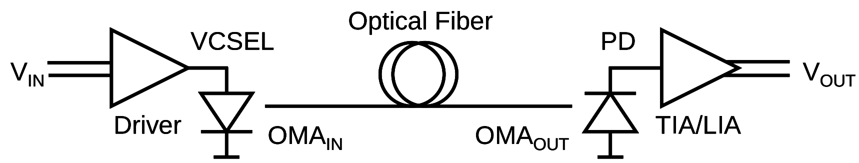


Fig.1. Optical interconnect diagram.

3. Results

One of the authors' group has demonstrated high-efficiency and high-speed 990nm VCSELs [4]. The low internal loss attributed to a short tapered oxide aperture brings both high DQE and high modulation efficiency. The VCSELs were characterized at room temperature before building a transmitter module as shown in Fig. 2. The detailed performance of the VCSELs has been already described in [4]. Some key characteristics for a 6μm-aperture device are the DQE at a bias current of 2.0 mA = 56 %, the threshold current = 0.35 mA, the threshold current density = 1.2 kA/cm^2, the series resistance at 2.0 mA = 150 Ω, and the 3dB modulation bandwidth at 2.0 mA = 11.5 GHz. The measured emission wavelength was 987 nm.

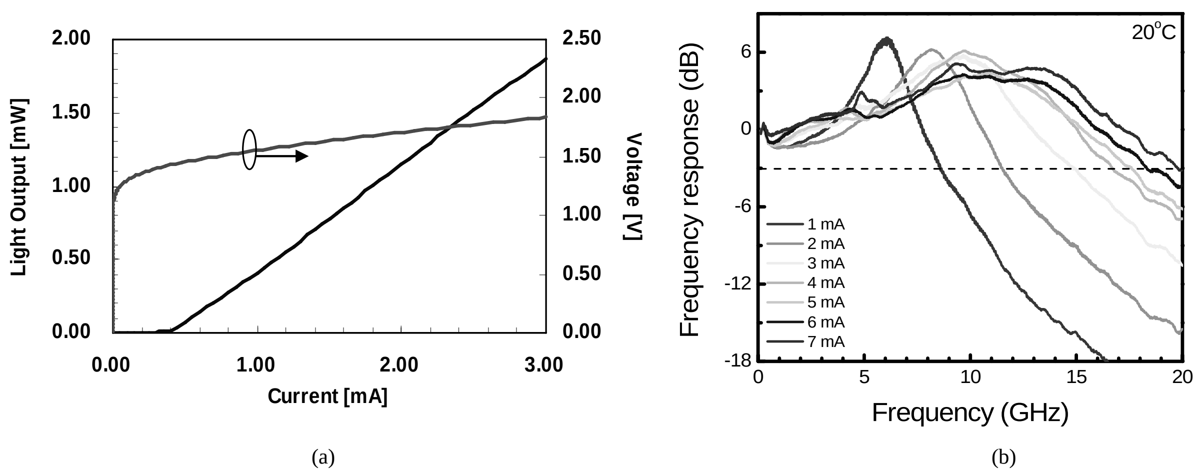
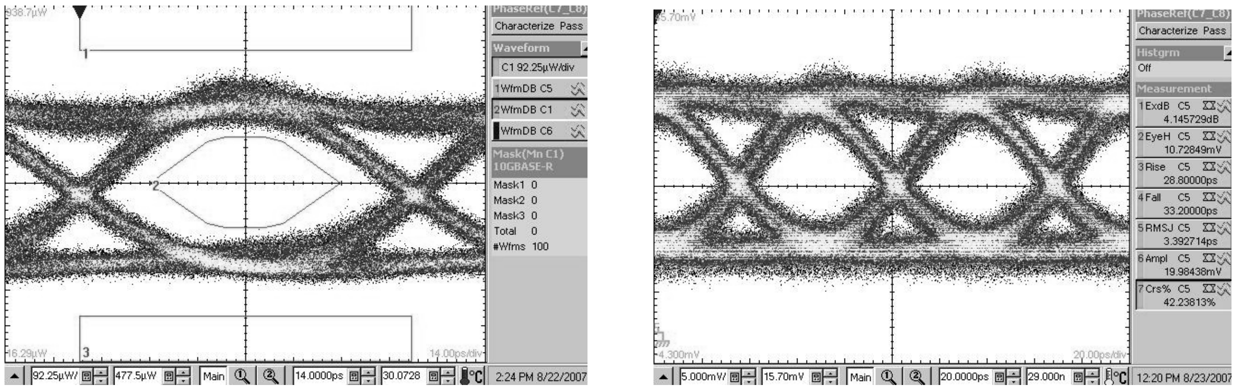


Fig.2. (a) DC LIV characteristics, and (b) small-signal frequency response of 990nm, 6-μm aperture, bottom emitting VCSEL.

A transmitter module was built with a LDD fabricated in the IBM CMOS8RF technology (130 nm) and a 6μm-aperture VCSEL, both mounted on a test card. The VCSEL is backside emitting, so the card was modified by drilling a 1mm-diameter hole. The light coming out of the VCSEL through the hole was collected with a lensed multimode fiber. High-speed electrical signals were fed into the LDD using a Cascade GSSG air-coplanar probe. RF electrical signals were generated by an SHF 40 G/s pattern generator, while optical signals were detected by a 17-GHz bandwidth Newport photodiode and characterized with a Tektronics digital signal analyzer.

Optical eye diagrams were taken with various operational conditions of the transmitter. Fig. 3(a) was taken at 10 Gbps with supply voltages of the LDD pre-amplifier and output stage of 1.2 V and 2.4 V, respectively. The OMA was -0.8 dBm, and the extinction ratio was 4.0 dB. Such large OMA decreases the required receiver gain, which likely translates into a reduction of receiver power dissipation. The light was obtained through 500μm-thick substrate, and the OMA can be larger if the VCSEL is top emitting. For the 10Gb Ethernet eye mask, no mask hits were detected with +15% margin for 2^7 -1 PRBS over 100 waveforms. The measured current of the pre-amplifier and the output stages was 4.0 mA and 4.3 mA, respectively, meaning the total power dissipation of the transmitter was 15.1 mW, or 1.5 mW/Gbps at 10 Gbps. This is the lowest power dissipation for a 10-Gb/s-class optical transmitter ever reported [2]. The LDD utilized in this experiment was not specifically designed for such low modulation and bias currents, and therefore may be optimized in future LDD designs for further power reduction. Further power reduction is expected by employing 90nm CMOS technology instead of 130nm to achieve higher speed and lower power.

The optical eye diagram was measured also for a transmitter with a 4µm-aperture device and the same CMOS LDD. Fig. 3(b) is the eye diagram at 15 Gbps, and at this rate, the total power consumption is 13.6 mW, or 0.9 mW/Gbps, with an OMA of -1.6 dBm. Although the observed eye diagram is relatively noisy, which may be attributed to modal noise, this result indicates the potential of optical interconnect transmitters operating beyond 10 Gbps and dissipating power less than 1.0 mW/Gbps.



(a) 10Gbps eye diagram with 6µm VCSEL

(b) 15Gbps eye diagram with 4µm VCSEL

Fig.3. Measured optical eye diagrams of transmitters with two sizes of VCSELs and the same CMOS LDD with bias conditions optimized for low power dissipation. (a) is with 10Gb Ethernet mask with +15% margin.

4. Conclusion

We have demonstrated a low power optical interconnect transmitter exploiting a high-efficiency VCSEL and a CMOS LDD. In this experiment, a 990nm VCSEL with a DQE of 56% is employed, and operation at 10 Gbps with an OMA of -0.8 dBm was demonstrated at a record-low power dissipation of 15.1 mW, or 1.5 mW/Gbps. The transmitter also indicated the potential of the 15Gbps operation at a power dissipation of 0.9 mW/Gbps. The low power optical interconnect design approach discussed in this paper can be applied to any level of optical interconnects, such as discrete optical transceiver modules or waveguide-based optical interconnects on printed circuit boards [5, 6], and it will accelerate the deployment of optical interconnects into high-performance computing systems. The low power design presented in this talk also enables the power reduction of VCSEL-based optical transmitters for short-reach datacom and telecom.

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5. References

[1] C. Schow, F. Doany, O. Liboiron-Ladouceur, C. Baks, D. Kuchta, L. Schares, R. John, and J. Kash, “160-Gb/s, 16-channel full-duplex, single-chip CMOS optical transceiver,” in *Tech. Dig. Optical Fiber Communication Conf.*, Anaheim, CA, March 2007.

[2] C. Kroemer, G. Sialm, C. Berger, T. Morf, M. L. Schmatz, F. Ellinger, D. Erni, G.-L. Bona, and H. Jackel, “A 100-mW 4 x 10 Gb/s transceiver in 80-nm CMOS for high-density optical interconnects,” *IEEE J. Solid-State Circuits*, **40**, pp. 2667-2679, 2005.

[3] N. Suzuki, H. Katakeyama, K. Fukatsu, T. Anan, K. Yashiki, and M. Tsuji, “25-Gbps operation of 1.1-mm-range InGaAs VCSELs for high-speed optical interconnects,” in *Tech. Dig. Optical Fiber Communication Conf.*, Anaheim, CA, March 2006.

[4] Y.-C. Chang, C. S. Wang, and L. A. Coldren, “High-efficiency, high-speed VCSELs with 35 Gbit/s error-free operation,” *Electron. Lett.*, **43**, pp. 1022-1023, 2007.

[5] F. E. Doany, “160-Gb/s, bidirectional parallel optical transceiver module for board-level interconnects using a single-chip CMOS IC,” in *Proc. 57th Electron. Comp. and Technol. Conf.*, Reno, NV, May 2007.

[6] S. Nakagawa, Y. Taira, H. Numata, K. Kobayashi, K. Terada, Y. Tsukada, “High-density optical interconnect exploiting build-up waveguide-on-SLC board,” submitted to *58th Electron. Comp. and Technol. Conf.*, Lake Buena Vista, FL, May 2008.