Ultra-compact, high-yield intra-cavity contacts for GaAs/AlGaAs-based vertical-cavity surface-emitting lasers

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A novel method of fabricating compact intra-cavity contacts with high yield for GaAs/AlGaAs-based vertical-cavity surface-emitting lasers is presented. By carefully tailoring the composition of high-aluminum content layer, a highly selective Al_2O_3 etch-stop layer can be formed simultaneously with the oxide aperture during wet thermal oxidation. With this technique, contact metals can be uniformly deposited on deeply embedded contact layers over large substrate areas. Utilizing this embedded etch-stop design, dual intra-cavity contacted three-terminal vertical-cavity surface-emitting lasers were fabricated, demonstrating submilliampere threshold currents, over 54% differential quantum efficiencies and over 9 mW output powers. © *2013 American Vacuum Society*. [http://dx.doi.org/10.1116/1.4769856]

I. INTRODUCTION

Over the past few years, vertical-cavity surface-emitting lasers (VCSELs) have become the most commercially successful GaAs/AlGaAs-based semiconductor lasers due to their versatility in the communication and sensing areas.[1] The main driving force is the emerging need for high-speed, highly efficient laser sources to power the optical links in data centers and high performance computing (HPC) systems. Compared to edge-emitting semiconductor lasers, VCSELs have the advantages of small footprint, high-speed modulation with low power consumption, capability of two-dimensional array fabrication, and a circular beam shape for efficient fiber coupling. Researchers also showed that by replacing the legacy AlGaAs/GaAs quantum wells (QWs) with strained InGaAs/GaAs quantum wells as the active region, it is possible to achieve higher data rate and lower power dissipation (less than a pJ/bit).[2,3]

In addition to diode VCSELs, multi-terminal VCSELs have also drawn some recent interest due to their new functionalities and applications, such as direct gain modulation for potentially higher speed,[4] polarization switching,[5] and direct loss modulation.[6] The third terminal is often inserted in the form of extra intra-cavity contact layer, adding complexity to the epitaxial growth and the device fabrication.

The strength of the GaAs/AlGaAs material system for VCSELs is the wide bandgap range available on a lattice-matched platform, so stacks of distributed Bragg reflectors (DBRs) mirrors can be grown epitaxially. Typical mirror thickness requires etching depths of several microns to reach the deeply embedded intra-cavity contact layers, limiting the adoption of intra-cavity contacts on the mass production level, since a laser monitor has to be used to stop the dry etch at the desired layer.

However, even with the assist of a laser monitor, it is still very challenging to obtain high device yield on a large wafer due to the fact that nearly all the dry-etching techniques, including reactive ion etch (RIE) and inductively coupled plasma etch (ICP), create a depth gradient where edge parts get etched more than the center part of the wafer. In order to accommodate this etch gradient the thickness of the intra-cavity contact layer can be increased as long as it is exactly an odd multiple of the designed wavelength in that material (1/4-λ, 3/4-λ, 5/4-λ, 7/4-λ, etc., in GaAs) to maintain the phase matching conditions of DBR mirrors. However, this leads to two significant negative impacts on the device performance:

(i) Higher threshold current and lower differential quantum efficiency (DQE). The thicker contact layers needed for process control, the more dopants have to be placed in the high electric field regions within the cavity, resulting in higher free carrier absorption loss that increases the internal loss α_i, which leads to higher threshold gain g_{th} providing the same confinement factor Γ and mirror loss α_m [Eq. (1)]. To compensate for this effect, higher threshold current I_{th} is required for the increased threshold gain g_{th} [Eqs. (2) and (3)]. Here, A represents the active area, and g_o and J_{tr} are the gain parameters.

$$\Gamma g_{th} = \alpha_i + \alpha_m, \tag{1}$$

$$I_{th} = A \cdot J_{th}, \tag{2}$$

$$g_{th} = g_0 \ln \frac{J_{th}}{J_{tr}}, \tag{3}$$

$$\eta_d = \eta_i \frac{\alpha_m}{\alpha_i + \alpha_m}. \tag{4}$$

The differential quantum efficiency η_d, given the same injection efficiency η_i, will also be reduced since internal

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loss α_i is increased [Eq. (4)]. These two effects result in a lower output power at a given biasing current, which is a common disadvantage for multi-terminal VCSELs.

(ii) Lower differential gain and lower direct modulation speed. Higher threshold current means lower differential gain a [Eq. (5)]. Longer effective cavity length means larger mode volume V_P. Both of these effects reduce the small signal modulation bandwidth f_{3dB} [Eq. (6)].

$$a \propto \left.\frac{\partial g}{\partial J}\right|_{J_{th}} = \frac{g_0}{J_{th}}, \tag{5}$$

$$f_{3dB} \propto \sqrt{a/V_P}. \tag{6}$$

It is possible to stop the etch on AlGaAs by adding a small amount of SF_6 to chloride-based etch chemistry,[7] but the gas has to be turned on just before the target layer. Since a deep etch (3–4 μm) would produce a large nonuniformity (80 nm for 2%), this technique would not work over large areas even with the assist of a laser monitor.

In this paper, a novel method will be proposed to make thin intra-cavity contact layers through the incorporation of an etch-stopping mechanism, which is essential to enhance the performance of multi-terminal VCSELs and make them feasible for mass production.

II. OBSERVATION OF ETCHING UNIFORMITY

A. RIE loading effect

To quantify the dry-etch nonuniformity in a RIE system, a 2 in. semi-insulating GaAs wafer was diced into quarters and then patterned with SPR220-7 photoresist.

The etch tool was a home-built RIE system with pure Cl_2 as the only reactant. The wafers were mounted by MUNG II, a type of silicon based thermal vacuum grease, to a silicon backing wafer which was water cooled to regulate the temperature. Before turning on the reactant gas, the etch chamber was pumped down to 1×10^{-7} Torr background pressure range, to minimize background O_2 and H_2O concentrations. The intake of Cl_2 was regulated by a mass flow controller (MFC) to maintain a constant flow rate of 7.2 sccm, with the chamber pressure kept at 1.6 mTorr. Etching proceeded for 10 min with 40 W of RIE power.

The first sample was etched alone. The second sample was surrounded by dummy pieces of GaAs wafers when loading into the etch chamber. Following the etch, both samples were then soaked in 1165 stripper to remove the photoresist. Step heights were measured using a DekTek 6 profilometer across the whole wafer to determine etch rate and uniformity. The results are shown in Fig. 1. For the 2 in. quarter GaAs that was etched alone, an average etch rate of 195 nm/min was observed at the center of the wafer, while the edge was etched around 20% faster than the center. For the other quarter that was accompanied by dummy GaAs wafers, an average etch rate of 104 nm/min was observed at the center of the wafer, while the edge was etched around 10% faster than the center. By surrounding the target wafer with dummy pieces of the same material, the etching uniformity can be significantly improved, with the trade-off of lower etch rate.

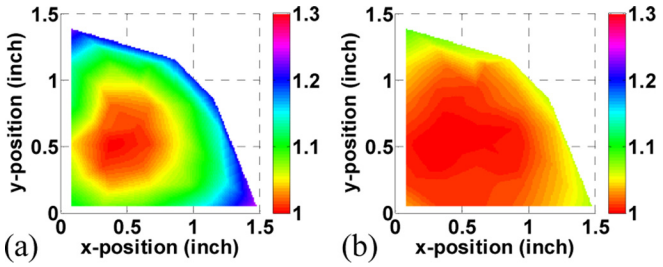

FIG. 1. (Color online) RIE etch uniformity map of (a) stand-alone 3 in. GaAs quarter wafer, normalized to 195 nm/min etch rate; (b) 3 in. GaAs quarter wafer surrounded by dummy GaAs pieces, normalized to 104 nm/min etch rate.

However, even the uniformity variation can be lowered to 10%, an intra-cavity GaAs contact layer will still need to be 500 nm thick for a common 5 μm deep etch, which is about 1.75-λ thick for a 980 nm VCSEL or 2-λ thick for a 850 nm VCSEL. To further reduce the required thickness of intra-cavity contact layers while maintaining good yield, an etch-stopping process is necessary.

B. Oxidized AlGaAs as the etch-stop layer

The formation of robust, high-quality native oxide on silicon embarked the tremendous commercial success of Si integrated circuit technology. On the other hand, a similarly robust oxide for compound semiconductors was not found until 1990,[8] when researchers discovered that the selective lateral wet thermal oxidation of high aluminum content semiconductors could form a mechanically stable aluminum oxide, Al_2O_3. Over the years, this process has been employed in the fabrication of various electronics and photonic devices, among which VCSELs have benefited the most and achieved performance leaps.[9]

This aluminum oxide provides not only an insulating layer to funnel the current into the active region, thus greatly enhance the injection efficiency, but also provides a low-to-high-to-low index contrast at the aperture, confining the optical mode in a similarly way as an optical lens does. In other words, both electrical and optical confinements can be achieved with the same structure. Moreover, this Al_2O_3 layer is impervious to Cl_2-based dry-tech, making it a good candidate for the etch-stop layer.

In Sec. III, we will propose a three-terminal VCSEL designed and fabricated with an embedded Al_2O_3 layer, which enables a compact cavity design and improved DC characteristics.

III. EXPERIMENTAL SETUP

A. Device design

To demonstrate the etch-stopping process, a bottom-emission, dual intra-cavity contacted 3-terminal VCSEL design was chosen. The schematic is shown in Fig. 2. The lower p-contact layer is a 7/4 -λ thick p-type GaAs with δ-

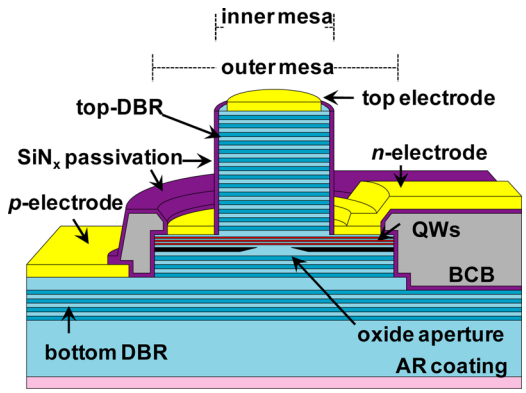

FIG. 2. (Color online) Schematic of a compact cavity three-terminal VCSEL.

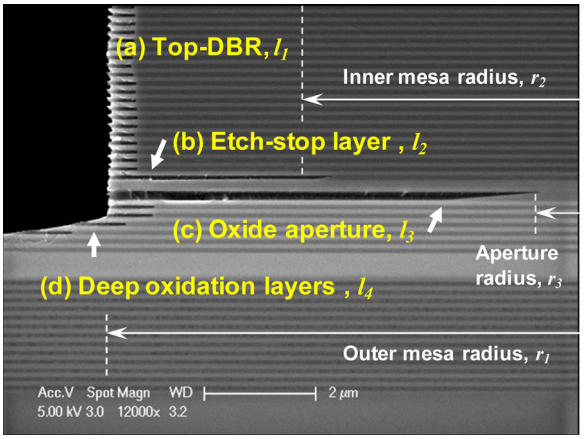

FIG. 3. (Color online) SEM cross-sectional image of various oxide layers incorporated in the VCSEL structure; (a) sidewall-oxidation of the GaAs/$Al_{0.9}Ga_{0.1}As$ top DBR pairs; (b) etch-stop layer modified from the first GaAs/$Al_{0.9}Ga_{0.1}As$ DBR; (c) tapered oxide aperture layer; (d) deep oxidation layers.

doping at the optical nodes to enhance conductivity while minimizing optical loss. The upper *n*-contact layer is a 160 nm thick GaAs active layer that includes three $In_{0.18}Ga_{0.82}As$ quantum wells with δ-doped silicon in the four adjacent GaAs barriers, so the actual *n*-contact layer is about 1/4 -λ thick. The *n*-type δ-doping provides free carriers in the quantum wells and forms two-dimensional electron gas (2DEG), so the carriers and be injected laterally into the active region with lower resistance.[10] An embedded etch-stop layer will be formed directly on top of the *n*-contact layer to facilitate the dry-etch and be removed later with a selective wet-etch.

A two-step etch is needed for the double mesa structure. The outer mesa is formed with the first RIE etch, which stops at the *p*-contact layer. After the outer mesa etch, a wet thermal oxidation step creates the oxide aperture as well as the etch-stop layer. Afterward, the inner mesa mask is defined on top of the mesas, and then bottom *p*-contact layer is coated with thick photoresist. Hence, only the doughnut-shaped region between the inner and outer mesa circumferences will be etched by the second RIE etch, which will stop at the embedded Al_2O_3 etch-stop layer.

During the wet thermal oxidation step, different compositions of AlGaAs in the mesa structure will be oxidized at different rates. These oxides can be categorized into four groups, as shown in Fig. 3: top-DBR oxidation (with a length of l_1), etch-stop layer (with a length of l_2), oxide aperture (with a length of l_3), deep oxidation layer (with a length of l_4). It is very critical to tailor the layer compositions according to the device geometries, such as the inner mesa radius r_1, the outer mesa radius r_2, and the aperture radius r_3. The importance and design rules of each of the four oxides are discussed below.

(a) The high aluminum content layers in the top-DBR will oxidize partially into ring oxides, which mask the second RIE etch and create an unwanted "coliseum wall" around the outer mesa circumference. The higher aluminum content in the top-DBRs, the deeper the sidewall oxidation and the thicker the coliseum wall will be, which is harder to be removed. On the other hand, higher aluminum content provides higher index contrast for each period of the GaAs/AlGaAs DBRs, facilitating the optical confinement in the longitudinal direction. As a result, there is a design trade-off between fabrication ease and confinement strength.

(b) The etch-stop oxide has to extend long enough to provide enough coverage as the etch-stop [Eq. (7)], but shorter than the oxide aperture in order not to create extra optical loss to the cavity [Eq. (8)]

$$l_2 > r_1 - r_2, \tag{7}$$

$$l_2 < l_3. \tag{8}$$

This etch-stop layer can be created by inserting a layer of AlAs to the first period of the top-DBR, so the oxidation rate is faster than the rest of the top-DBR.

(c) The oxide aperture has to be the longest, since it is the oxide layer that actually provides optical and electrical confinement. A taper oxide design was chosen as it confines the optical mode very effectively without introducing extra cavity-loss.[11]

(d) The deep oxidation layers reduce the parasitic capacitance between the two intra-cavity contact layers. Its design is less critical than the other three oxides'.

To achieve the desired device geometry, calibration samples were grown and processed, with these four groups of oxides verified with scanning electron microscopy (SEM). The optimized designs through iterations were summarized in Table I.

B. Material growth

Once the layer design was decided, the complete VCSEL structure was grown on 3 in. semi-insulating GaAs (100) substrate on a Veeco GenIII MBE system equipped with a custom-designed CBr4 digital doping system[12] for *p*-type dopant control. The overall epitaxial thickness is around 9 μm.

C. Device fabrication

For precise control of the outer mesa dimension, a three-level mask was used to define the patterns, including

TABLE I. Oxide design.

Category	Layer design	Thickness (Å)	Oxidation length l (μm) vs time t (min)	Oxide shape
Top DBR	GaAs	546		
	Linear grading	160		
	$Al_{0.9}Ga_{0.1}As$	654		
	Linear grading	160	$l_1 = 0.0567\,t - 0.1866$ ($R^2 = 0.9798$)	Blunt
Etch-stop layer	GaAs	505		
	Parabolic grading	200		
	AlAs	96		
	$Al_{0.93}Ga_{0.07}As$	524		
	Parabolic grading	200	$l_2 = 0.0085\,t^2 + 0.2541\,t - 0.2283$ ($R^2 = 0.9999$)	Tapered (taper length around 0.3 μm)
Tapered oxide aperture	*p*-AlAs	100	$l_3 = 0.0158\,t^2 + 0.5358\,t - 1.0612$ ($R^2 = 0.9999$)	Tapered (taper length around 1.4 μm)
	p-$Al_{0.93}Ga_{0.07}As$	1367		
Deep oxidation layer	*p*-GaAs	563		
	p-parabolic grading	280		
	p-$Al_{0.93}Ga_{0.07}As$	458		
	p-parabolic grading	280	$l_4 = 0.0926\,t - 0.2388$ ($R^2 = 0.9996$)	Blunt

Note: Parabolic curve fitting worked better for the etch-stop layer and the tapered oxide aperture.

2500 nm silicon nitride (SiN_x) deposited on the GaAs/AlGaAs base structure with plasma-enhanced chemical vapor deposition (PECVD), followed by 100 nm Cr and 900 nm SPR955CM-0.9 photoresist (PR) defined by stepper lithography. The Cr was etched in a Panasonic ICP etcher at 15C substrate temperature using a low power Cl_2/O_2 based recipe with a PR-to-Cr selectivity of 1:1. The PR was removed and the SiN_x mask was defined in the Panasonic ICP etcher with a CF_4/O_2-based recipe with SiN_x-to-Cr selectivity of 30:1. After solvent cleaning, the sample was etched in a parallel plate RIE etcher with pure Cl_2 down to the lower *p*-type intra-cavity contact, with the assist of a laser monitor.

After the outer mesa was formed [Fig. 4(a)], the sample was cleaned with solvent and pure ammonia hydroxide to remove the natural oxides on the sidewall and then directly transferred into a tube furnace for wet thermal oxidation. The oxidation conditions for a target oxide aperture length of 8 μm were 410 °C for 12′30″ [Fig. 4(b)].

After the oxidation, the inner mesa pattern was defined by SPR220-7 photoresist. The Panasonic ICP etcher was used to etch these patterns on the remaining SiN_x hard mask. The CF_4/O_2 recipe for SiN_x etch had a superior SiN_x-to-GaAs selectivity of 90:1, so the amount of GaAs machined away by the SiN_x dry-etch was negligible. The SPR220-7 masking the SiN_x layer was then stripped away, and a new layer of SPR220-7 was coated and then partially developed window to expose the semiconductor between the inner mesa and the outer mesa circumferences [Fig. 4(c)]. This PR layer was used to protect the bottom area from being attacked by the second RIE etch. A small wafer cut from the original VCSEL epitaxial wafer was mounted next to the actual wafer for laser-monitoring. The second RIE with pure Cl_2 was performed to etch down to the etch-stop oxide, with extra overetch time to ensure good etching uniformity. The selectivity between AlGaAs and Al_2O_3 was measured to be greater than 50:1 in such kind of etching chemistry. After the inner mesa etch, the PR was removed with 1165 stripper, leaving behind the unwanted coliseum wall structures resulting from the top-DBR oxidation [Fig. 4(d)]. The AZ-400 K developer, a combination of potassium hydroxide and surfactants, was used to remove the coliseum walls as well as the etch-stop oxide layers, revealing the thin intra-cavity contact layer [Fig. 4(e)]. At this point, both intra-cavity contact layers were exposed with no observable surface damage.

Afterward, a bilayer photoresist was used to lift-off the 200/200/5000 Å of Ti/Pt/Au Ohmic contact on *p*-layer. The *p*-GaAs layer was then partially removed with patterned wet-etch to reduce to pad capacitance [Fig. 4(f)]. 2000 Å of PECVD silicon nitride was used to cover the whole device, followed by lithography and dry-etch to open vias to the ring *n*-contact layer and the top of the inner mesa [Fig. 4(g). This process is commonly used by heterojunction bipolar transistor (HBT) researchers to create semi-self-aligned dielectric spacers,[13] allowing contact metal to be put direct next to the mesa ankle. A 800/300/3000 Å of AuGe/Ni/Au ring Ohmic contact and a 800/300/3000 Å of AuGe/Ni/Au top contact were then deposited, followed by a rapid thermal annealing step for contacts at 410 °C for 2 min in forming gas [Fig. 4(h)].

After annealing, a layer of Cyclotene 4022-25 photosensitive benzocyclobutene (BCB) was spun on, lithographically defined, and then cured in an oven. 2000 Å of PECVD SiN_x was deposited to form a adhesive layer, then both vias to the *n*-contact metal and *p*-contact metal were opened by dry-etch [Fig. 4(i)], followed by the final Ti/Au pad metallization step. The backside of the GaAs wafer was then polished and anti-reflection (AR) coated [Fig. 4(j)] to allow emission through the substrate.

IV. RESULTS AND DISCUSSION

The fabrication results were checked with a SEM to verify the details, with some of the intermediate results shown

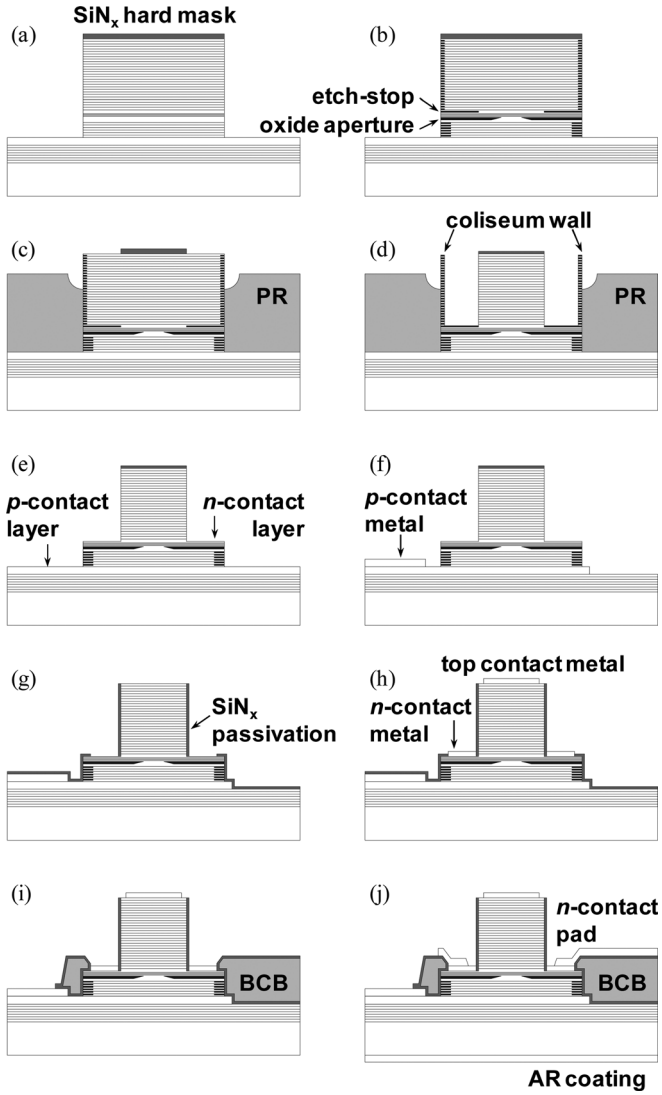

FIG. 4. Process flow for ultracompact dual intra-cavity contacted VCSEL; (a) outer mesa etch; (b) oxidation; (c) inner mesa hard-mask etch and photoresist protective layer definition; (d) inner mesa etch, leaving behind the coliseum wall of GaAs/AlGaAs stacks; (e) coliseum wall and etch-stop layer removal; (f) *p*-contact metal deposition and *p*-contact layer partial removal. (g) SiN_x passivation, and via etch (h) *n*-contact metal deposition, top-contact metal deposition, contact annealing, (i) BCB planarization and curing, (j) *n*-contact pad deposition, back-side polishing, and AR coating.

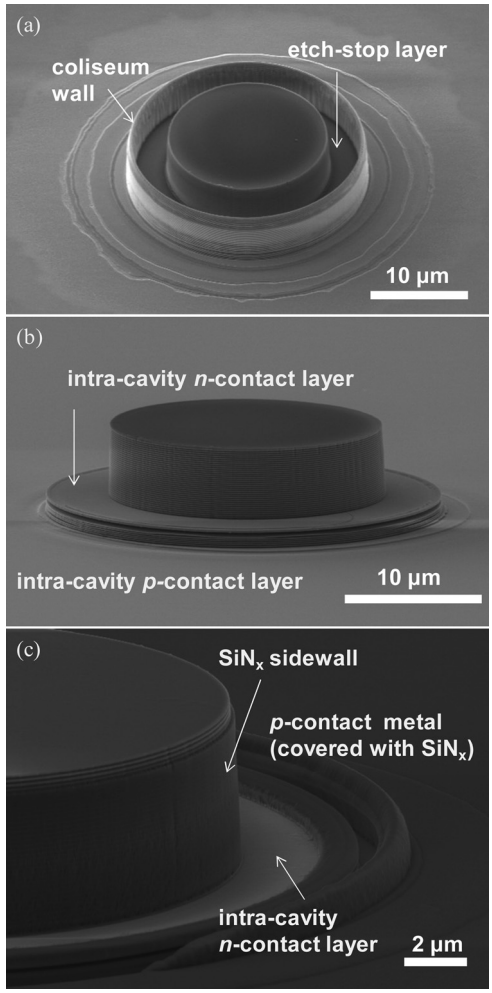

FIG. 5. SEM images of some intermediate steps of the process flow: (a) after inner mesa etch and the removal of thick protective photoresist. (b) After the coliseum wall removal with AZ-400 K developer, revealing both intra-cavity contact layers. (c) After blanket SiN_x passivation and via opening, showing the semi-self-aligned spacer and the open contact layers.

in Fig. 5. After the inner mesa etch, the residual coliseum wall structure [Fig. 5(a)] is removed with AZ-400 K developer dip, exposing the smooth intra-cavity *n*-contact layer [Fig. 5(b)]. The top-DBR and the intra-cavity *n*-contact layer are isolated with a vertical SiN_x sidewall [Fig. 5(c)].

The fabricated devices were characterized with continuous-wave (CW) operation at 20 °C, with a forward bias provided between the *n*-electrode and the *p*-electrode. Figure 6 shows the voltage and output power versus current (*L–I–V*) curves for devices with 3, 4, 5, 6, 7 μm of aperture diameters. The lasing wavelength is around 990 nm. All devices have a submilliampere threshold current and a differential quantum efficiency above 54%, corresponding to a slope efficiency of 0.68 (W/A). The threshold voltage is around 1.53 V, only 290 mV higher than the photon energy.

Only the 3 μm device supports single-mode operation up to 1.5 mA of bias current. With a dual intra-cavity contact configuration, the current tends to flow near the rim of the aperture, favoring higher-order modes in a large device. The

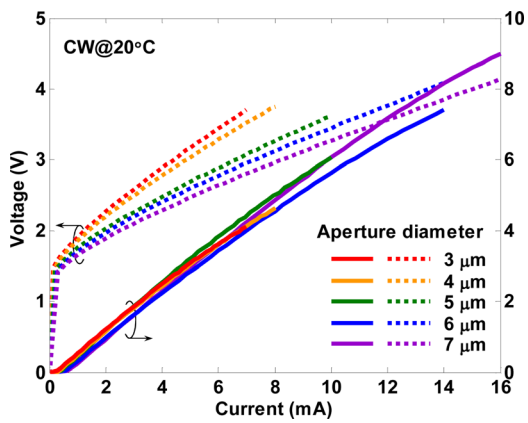

FIG. 6. (Color online) Voltage and output power vs current (*L–I–V*) curves for devices with different aperture diameters.

TABLE II. Device parameter and performance results.

Device aperture (μm)	3	7
Inner mesa diameter, r_2 (μm)	17	21
Outer mesa diameter, r_1 (μm)	24	28
Slope efficiency (mW/mA)	0.68	0.69
DQE	0.54	0.55
Threshold current, I_{th} (μA)	223	648
Threshold voltage, V_{th} (V)	1.53	1.54
Series resistance (Ω)	298	156
Maximum output power (mW)	4.11	9.00
Peak wall-plug efficiency	0.28	0.26

Note: DC measurements done at 20 °C.

series resistance decreases monotonically as the aperture diameter increases, from 298 Ω on a 3 μm device to 156 Ω on a 7 μm device. All devices have a peak wall-plug efficiency higher than 25%. The highest output power of 9 mW is achieved with a 7 μm device.

The direct current (DC) results of the smallest 3 μm device and the largest 7 μm device are listed in Table II.

V. CONCLUSIONS

We have demonstrated a novel method of making compact intra-cavity contacts. By changing the aluminum content above the contact layer, an embedded Al_2O_3 etch-stop layer can be formed along with the oxide aperture, without additional cost for device fabrication. After dry-tech, this Al_2O_3 etch-stop layer as well as the residual structures can be easily removed using AZ-400 K developer, without introducing extra damage to the mesa structure. Blanket PECVD SiN_x deposition and ICP etch creates a self-aligned sidewall, which allows the contact metal to be deposited directly next to the mesa ankle to reduce lateral resistance. This method can also be applied to fabricate all the other GaAs-based electronic and photonic devices, including HBTs, high electron mobility transistors, DBR lasers, and distributed feedback lasers.

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