Integrated Photonics for Low-Power Packet Networking

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(Invited Paper)

***Abstract*—Communications interconnects and networks will continue to play a large role in contributing to the global carbon footprint, especially in data center and cloud-computing applications exponential growth in capacity. Key to maximizing the benefits of photonics technology is highly functional, lower power, and large-scale photonics integration. In this paper, we report on the latest advances in the photonic integration technologies used for asynchronous optical packet switching using an example photonic integrated switched optical router, the label switched optical router architecture. We report measurements of the power consumed by the photonic circuits in performing their intended function, the electronics required to bias the photonics, processing electronics, and required cooling technology. Data is presented to show that there is room (potentially greater than 10 ×) for improvement in the router packet-forwarding plane. The purpose of this exercise is not to provide a comparison of all-optical versus electronic routers, rather to present a data point on actual measurements of the power contributions for various photonic integration technologies of an all-optical packet router that has been demonstrated and conclude, where the technology can move to reduce power consumption for high-capacity packet routing systems.**

***Index Terms*—Optical communications, optical packet switching, photonic integration.**

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I. Introduction

THE predicted carbon footprint of data communications networks and data centers to the global IT sector contributes almost one-half of the total expected contribution. With predicted exponential growth in capacity due to consumer applications like video demand taking off, technologies that can save power in the network communications, and data center infrastructures will be critical. Photonics has the potential based on fundamentally different power scaling laws, to enable high capacity and bandwidth systems to scale in a different manner than how systems are architected today based on electronic integrated technologies. The power savings from using photonics technologies will need to come about from rearchitecting these systems as well as pushing the state of the art in photonic integration. In this paper, we focus on results from the DARPA-funded label switched optical router (LASOR) project to illustrate how photonics can be used to offset power and footprint limits that will be imposed for high-capacity future routers and communications system. We will describe how the LASOR project systematically addresses, through design and measurements, the largest power consumer in today's router architectures as the fiber bit rate and router capacity increases. We will also describe how photonic circuits, positioned in the proper functions in a packet-based system provide better power scaling behavior as the line bit rate increases relative to electronic solutions that rely on heavy parallelism and fast transistors. In order to begin to understand, the potential photonic ICs (PICs) can have on the power consumption of packet switched systems, it

Fig. 1. Contributions of IT sectors to the global carbon footprint.

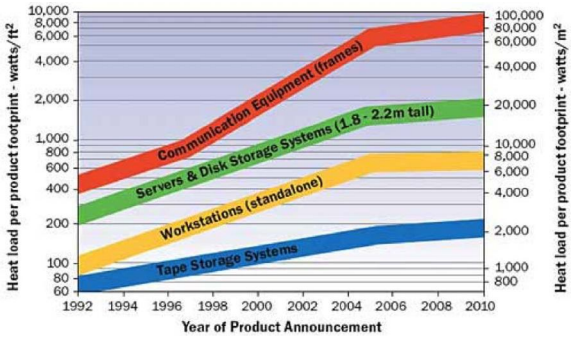

Fig. 2. Intel study showing the dominant contribution of communications equipment in data centers to the heat load per product footprint [1].

is important to build and measure prototype systems based on real PIC technologies.

II. Carbon Footprint of IT Systems

IT systems continue to increase demands on energy supplies as computer usage, network bandwidth, data storage, and applications continue to increase at an ever-expanding rate. The problem has become quite severe, on the order of other major global emissions contributors including the global aviation industry. A study done on the global footprint by subsector in 2009, shown in Fig. 1, demonstrates the impact of PCs, peripherals and printer, and the telecommunications and data center infrastructures. The global telecommunications and data center infrastructures are expected to subsume almost half of the IT contributions to carbon footprint.

The heat-load contributions to data centers as a function of data centers release date was reported by Intel and is shown in Fig. 2, where the breakdown of the heat load per footprint illustrates that communications equipment continues to be an increasingly dominant contribution. New technologies, such as photonics, have the potential to flatten out or reduce this growth when architected properly into systems and integrated using next generation photonics integrated technologies, as discussed further on.

III. Power Limitations of Today's Communications Systems—System Scalability and the Power Spreading Problem

The energy problem due to the communications infrastructure will grow as continued increase in IP traffic growth pushes demands on communications equipment. As shown in Fig. 3 increases in IP traffic growth due in particular to consumer

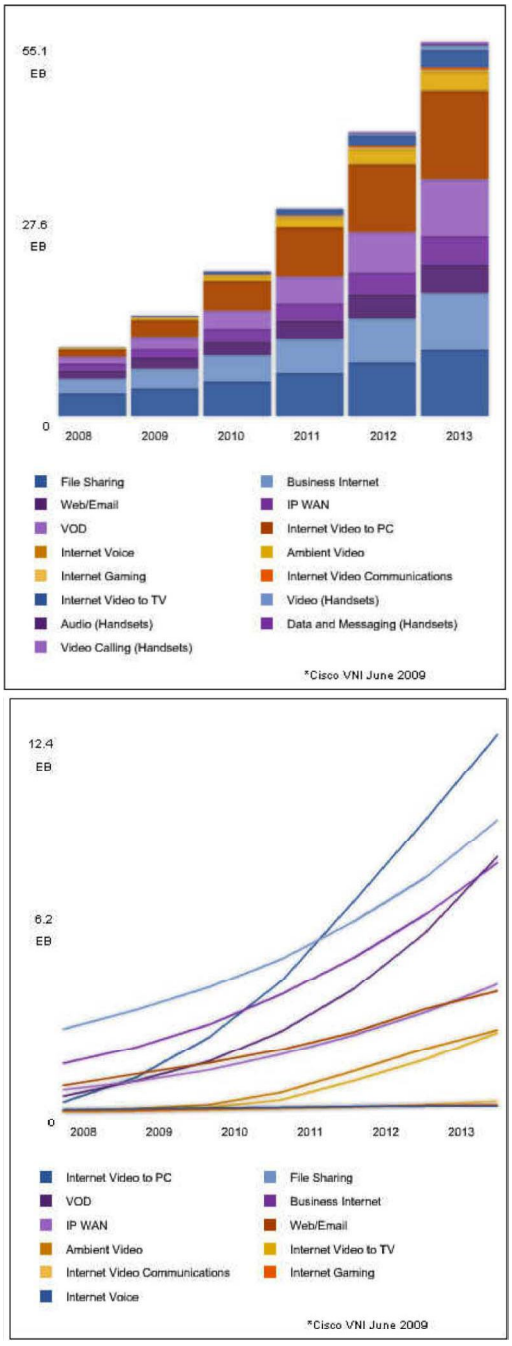

Fig. 3. Projected IP traffic growth due to video and new high bandwidth demands (Graphs courtesy of Cisco Visual Networking Index http://www.cisco.com/en/US/netsol/ns827/networking_solutions_sub_solution.html).

demand for services like video are projected to increase by a factor of fivefold by 2013.

The system bandwidth of high-capacity systems that need to support this growth, like routers, data centers, and telecommunications infrastructure, rely on continued improvements in electronic technologies in terms of metrics like megahertz-gate per milliwatt and megabits per second per watt in order to keep the system power flat, while providing for continual scaling in system bandwidth (BW).

As shown in Fig. 4, the power/performance efficiency improvements of high-performance electronic communication

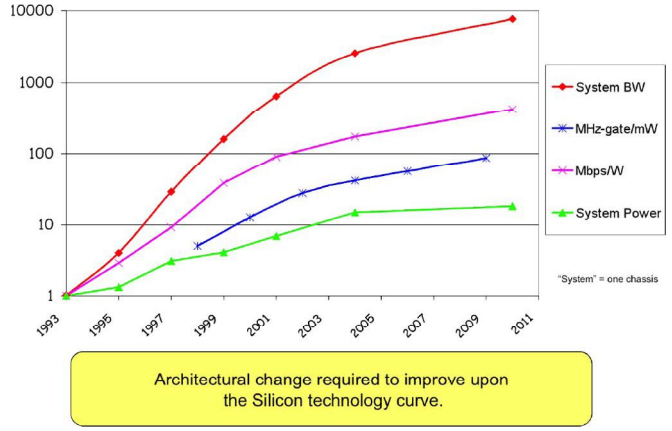

Fig. 4. Historical growth of high-end router capacity and improvements in power efficiency (relative to products of 1993) and dependence on continued improvements in electronic component efficiency.

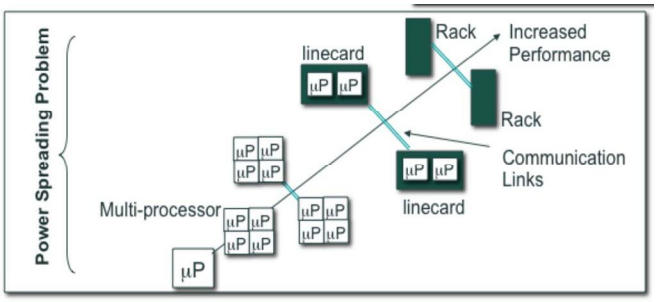

Fig. 5. Effect of power-spreading problem on system footprint and power dissipation.

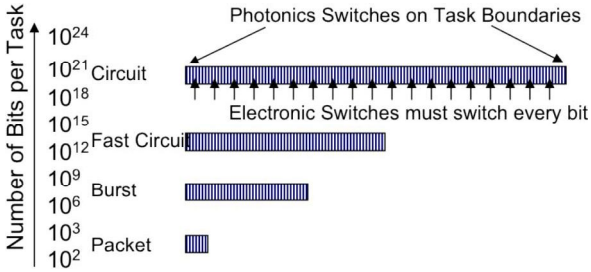

Fig. 6. Scaling of switching energy as a function of the size of switched information for photonics versus electronics.

systems are bound to the efficiency improvements of the underlying silicon technology. To scale systems at a higher rate than the component technology requires architectural innovation and/or a compromise in one or more areas of system functionality such as performance, programmability, or physical size/density. However, this architectural workaround is difficult to sustain long-term and fundamental improvements in the underlying technology is required to overcome projected shortfalls.

The capacity of single-rack Internet routers has grown by approximately threefold every 18 months and is limited by the power that can be delivered to, and dissipated from, a single rack of equipment. Power consumption has grown with capacity, and the largest single-rack routers today consume over 10 kW. Architecting electronic core routers with higher capacities continues to burden all aspects of system design and underlying technologies including switch fabric capacity and packet processing, such as forwarding, queuing, and buffering. Today's state-of-the-art core routers utilize multirack designs in order to spread the system power over multiple racks, reducing the power density, and push aggregate capacities to 100 s of Tb/s. However, these systems require as many as six optoelectronic conversions per input/output and multirack configurations dominated by interface cards. For example, a 25 Tb/s router with 128 40 Gb/s I/O ports can require 768 40Gb/s actual or equivalent optoelectronic/electrooptic (OE/EO) conversions, whose power dissipation and footprint increase with number of ports and bit rate per port.

One reason for the tradeoff in system BW (where system BW is defined as router capacity or throughput with a given packet loss rate and offered load at the input) with physical size/density even with faster and denser electronics is related to the power-spreading problem, as illustrated in Fig. 5. Today's transistors exhibit a fixed leakage current that is based on current manufacturing technology pervasive in the existing semiconductor processing foundry infrastructure that is very expensive to change on a large-scale basis even with fundamental improvements in transistor technology. Additionally, running transistors at ever increasingly high clock speeds adds to the power dissipation problem making multicore solutions more desirable. Since the power footprint of a system is practically constrained, single-chip solutions quickly become multichip solutions with an added power overhead for interchip communications, followed by the need to move to multiline card and multirack solutions, each with additional added communications power overhead between cards, shelves, and racks.

IV. Potential Impact of Photonics on Power Scaling Laws

Photonics has the potential to change the power scaling laws of high bandwidth systems through proper architectural choices that combine photonics with electronics to optimize performance, power, footprint, and cost. The major types of data in a communications system are shown in Fig. 6 with circuit switching at one extreme of granularity and packet switching at the other extreme. Traditionally, digital electronics is used to switch these data units, and transistors must switch and expend energy at the bit rate for every bit. The faster the bit rate, the more energy is expended per bit and the longer the task the more energy is expended per task (e.g., circuit, burst (including packet flows), and packet).

Using analog photonics to switch or tasks requires switching only at the task boundaries. However, there does exist a tradeoff between the switching energy and the bias power depends on the photonics technology used. While electronics has very low switching energy and bias power, certain photonics technologies, like microelectromechanical system (MEMS) can have lower bias power while other technologies like semiconductor optical amplifiers (SOAs) require higher bias powers today. The tradeoff between initial bias power, switching energy, and

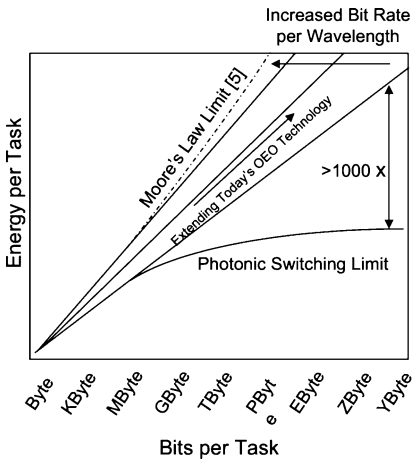

Fig. 7. Energy used to switch task for electronics and photonics as a function of task length.

switching at the bit level or task boundary leads to qualitative behaviors illustrated in Fig. 6. Today's photonics and electronics dissipate roughly the same power for smaller tasks. The total bit level switching energy per task dominates the bias power for longer task for electronics as is shown in the curve "extending today's OE optic (OEO) technology." As the bit rate is increased for electronics, the power to switch transistors increases and the task curve moves to the left approaching Moore's law limit. Photonics (analog) has a qualitatively different behavior, where the energy per task is dominated by the bias power and does not increase significantly as the bit rate and task length increases. This is shown qualitatively in the photonics limit curve in Fig. 7. It is important to note that the curves in Fig. 7 represent switching in the data plane and do not include a dominant component of processing packet forwarding or connection setup.

V. Example System--LASOR: A Label Switched Optical Router

For purposes of the power analysis of PIC for this paper, the LASOR project [1], [3]–[5], funded by DARPA MTO, is presented as an example optical packet switching system, where the power dissipation of the integrated photonics and surrounding electronics has been quantified. The purpose of this exercise is not to provide a firm comparison of all-optical versus electronic routers as this is a very complex and problem with rapidly moving data points. The purpose of this paper is rather to present a data point on actual measurements of the power contributions for various components of an all-optical packet router that has been demonstrated and conclude, where the technology can move to.

An optical label switched network and the LASOR node block diagram are shown in Figs. 8 and 9. For the LASOR project, we have target 64 × 64 ports per packet routing section of the line cards shown in Fig. 9. In order to reach 100 Tb/s per node, 20 line cards are required. The number of fiber input and output ports will depend on the wavelength division multiplexing (WDM) channel plan at the node inputs and outputs and the bit rate per wavelength. Each LASOR node consists of WDM interfaces

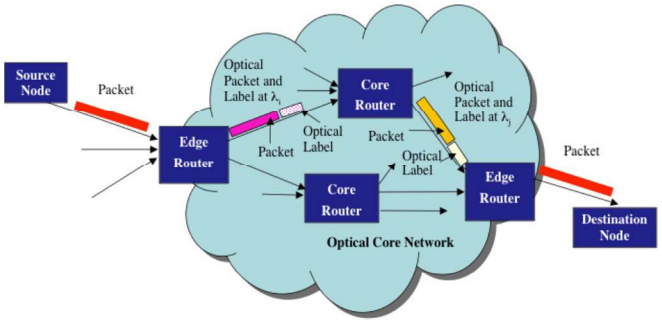

Fig. 8. High-level diagram of an optical label switched packet network and the interface to legacy systems.

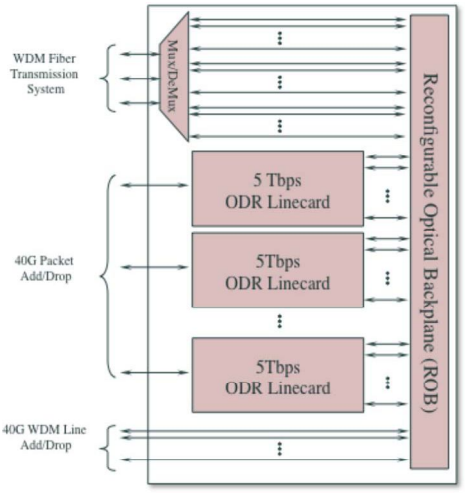

Fig. 9. LASOR optical routing node block diagram.

to transmission lines, optical WDM wavelength add/drop ports, and optical packet add/drop ports. Wavelengths from the transmission system can be quasi-statically connected to any choice of wavelength add/drop or optical data router (ODR) line card ports using a MEMS switch interconnect backplane.

The PIC components and subsystems presented in this paper comprise the LASOR ODR line card shown in Figs. 9 and 10. The primary building blocks that have been integrated using PIC technology include an optical payload envelope detector (PED), optical label burst mode recovery, an optical packet synchronizer (OPS), an optical random access memory (ORAM), a packet-forwarding chip (PFC), an arrayed-waveguide grating router (AWGR), a monolithic tunable optical router (MOTOR), and a 3R regenerative wavelength converter matched to the output line transmission system.

One of the key areas for optical routers is optical buffers and is among the most challenging technology to integrate. The ability to fabricate PIC buffers of a certain complexity must match the network buffer requirements for a router. One of these requirements is the depth of the optical packet buffers required for lossless packet routing (here lossless refers to the loss of packets that are dropped from buffers).

Electrical routers use electrical RAM to implement buffers that resolve contention and congestion, as shown in Fig. 11.

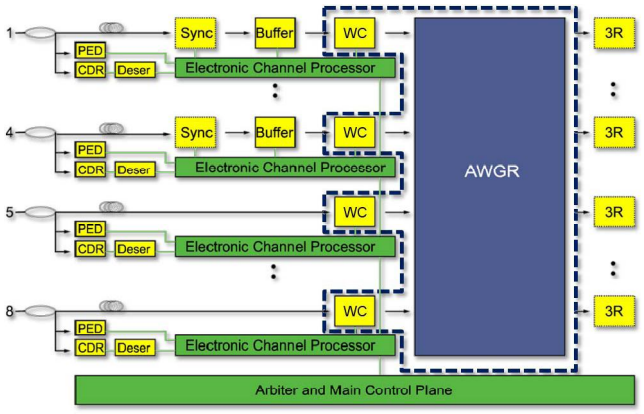

Fig. 10. Main components of the 8 × 8 LASOR ODR. The wavelength conversion (WC) element is the PFC PIC and the buffer is the ORAM PIC described in the following.

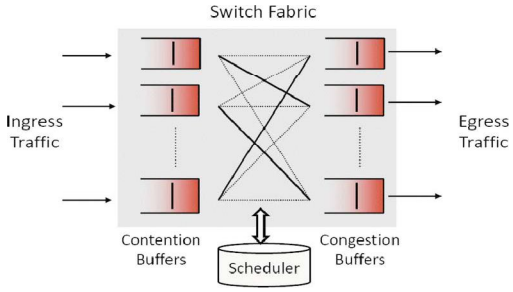

Fig. 11. Buffering in a combined input/output queuing (CIOQ) router. Input buffers store packets when there is internal contention. Output buffers store packets when output links are congested.

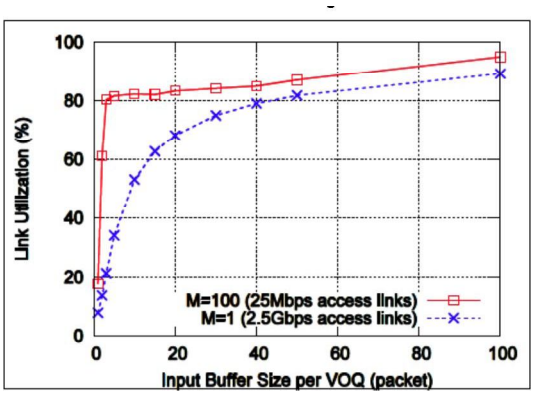

Fig. 12. Link utilization versus input and output buffer sizes. With 25 Mb/s access links, five-packet virtual output queues (VOQs) and 15-packet output buffers make the utilization above 80%.

This capacity is currently not feasible with any proposed optical buffering approach. But research has shown that much smaller buffering capacities are adequate, on the order of 10–20 packet deep buffers, within the reach of today's PIC technology. Analysis, simulations, and experiments show that if access links run slower than backbone links, the traffic is smoothed, and hence, only 10–20 packet buffers per output port are needed for 80% throughput, as shown in Fig. 12 [6]–[8].

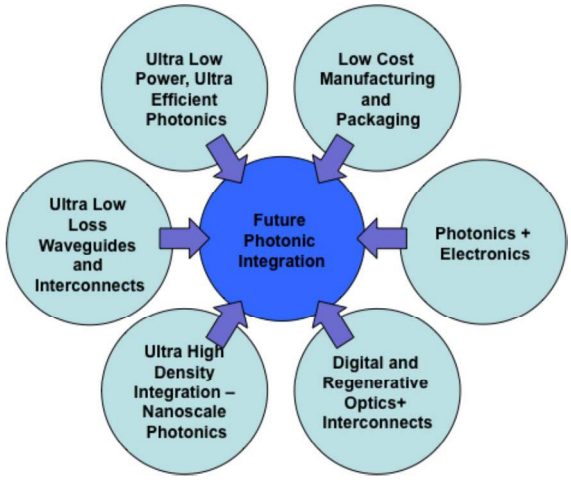

Fig. 13. Enabling technologies to allow for future photonic integration.

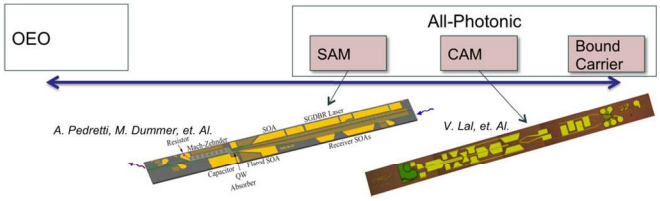

Fig. 14. All-photonic PICs using the SAM and CAM approach.

VI. Low-Power PICs

Photonic integration has the potential to save power for packet routing systems and other applications. However, in order for PIC technology to make in-roads to real systems and be an energy efficient, cost effective, and manufacturable technology that scales to a large number of on-chip components, multiple key issues must be addressed [9]–[11]. As shown in figure, new generation of PICs will require advances in ultralow power sources, detectors and amplifiers, ultralow-loss waveguides and interconnects, ultrahigh density components, digitally regenerative optics, efficient integration of electronics and photonics, and low cost packaging and manufacturing as well as high-yield PICs (see Fig. 13).

Under the LASOR program, we have investigated two categories of all-photonic devices, as depicted in Fig. 14. We define a spread of approaches to lie along a line that has OEO that lies at one extreme. We define OEO, where not only are photons converted to electrons and *vice versa*, but digital manipulation, using electronic transistors or logic gates, occurs between the optical input and output. We define three subcategories of *all-photonic*, where the first two, photocurrent-driven wavelength converters (SAM) and concurrent absorption and modulation wavelength converters (CAM) involve interactions of photons with free carriers and the third involves interaction of photons with bound carriers. The term all-photonic is used for all-optical, CAM, and SAM, since all processes that involve photons controlling photons involve intermediate interaction with electrons, either bound or free.

TABLE I
LASOR PIC FUNCTIONS AND PERFORMANCE

Function	Integration Platform	Performance Summary	Est. PIC Power (W)
Monolithic Tunable Optical Router (MOTOR)	InP, CAM	640 Gbps routing capacity, 8 inputs 8 outputs, 40Gbps per input, 2R regenerative, C-band tunable	16
Optical Payload Envelope Detection (PED)	InP, Si/InP, CAM, SAM	40 Gbps variable length, asynchronous payloads. C-Band operation. 300 ps recovered payload envelope rise time and 30ps rms jitter over 10dB dynamic input power range.	3
Optical Packet Synchronizer (OPS)	InP/Silica, Si/InP, CAM	4-stage synchronizer with the relative delay through any configuration of the synchronizer given as $T(n) = n \times \Delta$ ($n = 0, 1, 2 \ldots 15$), where $\Delta = 800$ps and the tuning range is 12.8ns. Packet rate reconfiguration.	4
Burst Mode CDR	Si/InP Hybrid, CAM	10Gbps asynchronous labels. < 20 bit lock time and > 380 bit hold time. BER < 10^{-12} and 0% header los over 0.8dB Dynamic Range at input.	0.750
Optical Random Access Memory (ORAM)	InP/Silica, Si/InP, CAM	23ns delay, 40dB ER, <1ns load/unload switch times. 184ns storage of 40Byte 40Gbps packets with > 98% packet recovery after storage.	3.5
Packet Forwarding Chip (PFC)	InP, CAM, SAM	40Gbps asynchronous, variable length payload fast switchable wavelength conversion and 10Gbps optical label re-write. C-band operation. -27dBm sensitivity. <2dB PP.	2

SAM devices utilize separate absorption and modulation sections, where the input light is absorbed/detected and used to remodulate the light onto a new optical signal via an externally modulated laser and these two sections are connected by a simple wire or electron waveguide. CAM devices utilize colinear optical and electronic waveguides, where the input photons directly interact with electrons as in a SOA to produce a modulation effect transferring the input optical data onto a new outbound optical signal. Bound carrier devices utilize nonlinear polarization interaction between the photon and a bound electron to produce new optical signals, such as with four-wave mixing in optical fibers or second harmonic generation in, e.g., lithim niobate.

In this paper, we focus on two types of all-photonic PICs integrated under the LASOR project, the SAM and CAM types. Table I lists the PIC devices that are covered in this paper, the integration platform used, a performance summary and list of relevant references for each.

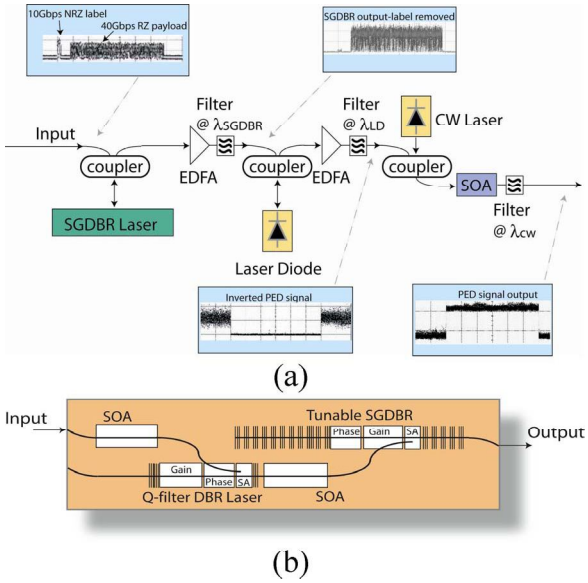

Fig. 15. All-optical PED principal, operation and PIC.

A. Optical PED

The PED function [12] is used to determine the location of the optical packet boundaries with high precision without processing the individual bits, saving power as the length of the packet increases and the bit rate increases.

The PED output is used to create a precise time reference of the payload in the electrical domain relative to the optical domain in order to make synchronization, buffering, label erasure and rewrite, and forwarding operations.

An all-photonic CAM implementation of the PED function provides very rapid rise and fall times of the envelope signal as well as low jitter. A discrete all-optical PED implementation along with on optical packet and the resulting optical envelope is shown in Fig. 15(a). Integration of the optical PED function onto a monolithic chip is shown in Fig. 15(b) [13]. The components are similar to those used in the PFC and the optical clock recovery chip.

B. Burst-Mode Optical Clock and Data Recovery

The task of recovering and processing headers in an asynchronous optical packet switching system poses many unique challenges. At each node input, the optical packet arrival time and the optical packet length are not known ahead of time. In the LASOR system, optical packets consist of payloads that are preceded by optical headers used to compute forwarding and new header information at each node. In order to process the optical headers using electronics, the header clock and data must be recovered burst mode (asynchronously) with a minimum of overhead bits (preamble). The recovered clock phase and frequency accuracy must result in error-free label recovery or the packet will be incorrectly routed. A conflicting requirement to rapid clock recovery is maintaining accurate clock frequency and phase over the length of packets that can vary in length from 40 to 1500 B, after the header terminates. We have

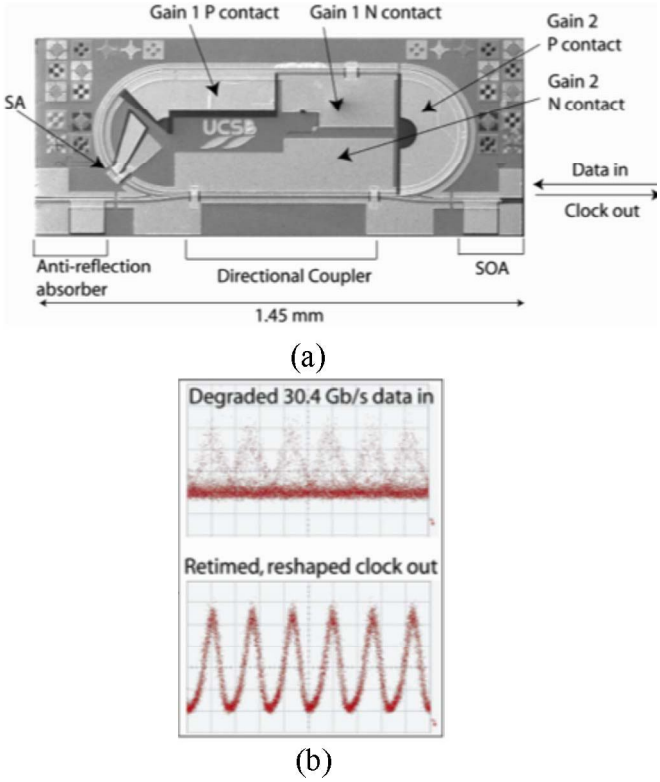

Fig. 16. (a) Si/InP ring laser used as 3R regenerative burst mode clock recovery (b) significantly improves degraded RZ data and will retimes and reshape the clock.

developed a nested feedback approach that addresses this issue and is amenable to integration [14].

A hybrid silicon evanescent ring mode-locked laser PIC has been demonstrated that realizes the rapid optical clock recovery portion of the clock and data recovery (CDR) [17]. The device, shown in Fig. 16, is capable of generating a reshaped and retimed clock signal from 30.4 Gb/s data, even when the input data is severely degraded. Interestingly enough, increasing the repetition rate of integrated ring lasers to 100 GHz and beyond becomes simpler with PIC technology as the size of the cavity becomes smaller, and therefore, more stable.

For input data with 3.8 dB extinction ratio (ER) and 14 ps of jitter, the recovered clock has an ER over 10 dB and 1.7 ps of jitter. Experiments show that the laser suppresses any noise that is outside the locking range (6 MHz). This implies that by carefully designing similar devices with predetermined locking ranges, it should be possible to reliably manufacture mode-locked lasers that can reduce jitter in compliance with International Telecommunications Union (ITU) specifications, suppressing jitter outside only specific frequency offsets from the carrier frequency.

Since the laser's ring cavity is defined using photolithography, it is possible to match the repetition rate of the laser to a specific data rate in future designs, which is essential for practical applications. The ring configuration also allows for integration with optical amplifiers and demonstrates potential for more complex PICs utilizing this mode-locked laser.

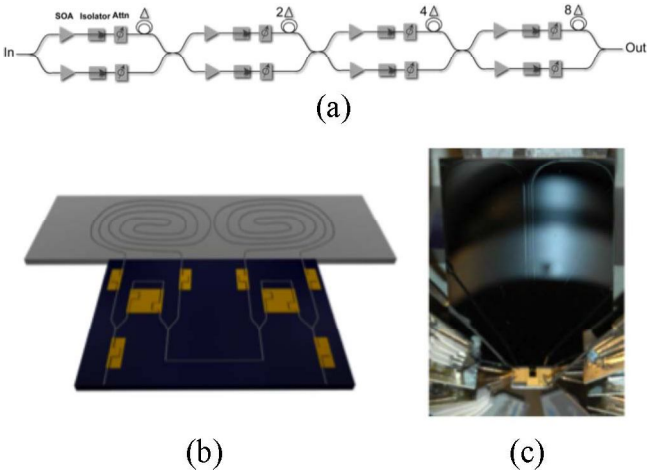

Fig. 17. (a) Optical synchronizer parallel path feedforward designed that can be integrated (b) using InP for the switching structure and silicon for the delay sections. (c) It shows a realized synchronizer.

When data is injected, most of the laser characteristics, such as output power, wavelength, pulsewidth, ER, and spectral width are unchanged from passive mode-locking conditions. The input data pulses modulate the carriers in the absorber and laser cavity and if the data rate matches the repetition rate of the laser, the laser pulses become synchronized to the data, generating a clock signal.

C. Optical Packet Synchronizer

Since packets arrive asynchronously at the router inputs, alignment to a local clock frame using optical synchronizers is required for efficient optical buffer management and output link utilization.

The optical synchronizer is based on a feedforward design that utilizes SOAs and a binary increasing length combination of optical delay lines, as shown in Fig. 17(a). Active monolithic 2×2 InP offset quantum-well (QW) SOA-based switches are used to select the required delays and compensate for delay lines losses.

The delays, fabricated using silica-on-silicon delay lines, are butt coupled to the 2×2 SOA switches shown schematically in Fig. 17(b) and in the chip form in Fig. 17(c). Requirements for the 2×2 switches include high switching ER ($>$40 dB), low crosstalk ($<-$40 dB), and fast switching times ($<$2 ns). The delay lines were chosen to be slightly longer than a 40-B packet (8 ns) at 40 Gb/s with an added 2 ns guard band to accommodate the SOA switching time.

D. Optical Random Access Memory

There are two major approaches to storing light: slowing light down (by decreasing its group velocity), or increasing the length of the waveguide. In [18], various buffering approaches were compared and the conclusion was that ORAM based on slow light was fundamentally limited to below 40 Gb/s and below 40 B packets. Our approaches are based on the latter technique [19], [20].

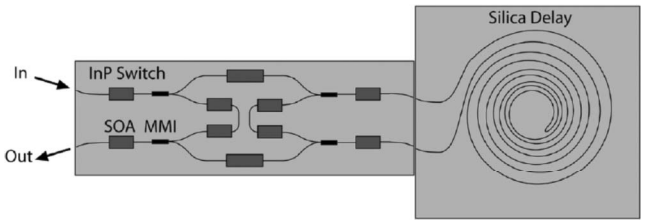

Fig. 18. InP 2 × 2 switch butt coupled to a silica delay line.

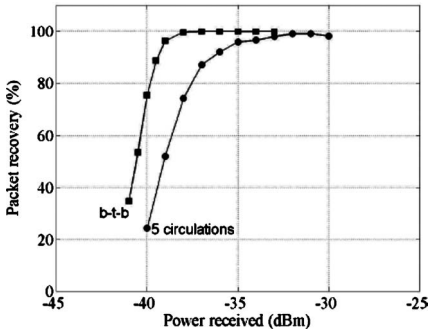

Fig. 19. Packet recovery for five recirculations shows up to 98% packet recovery.

One PIC design, we have implemented a 2 × 2 switch on InP butt coupled to a silica delay line, as shown in Fig. 18. Depending on the bias condition of the SOAs, the signal can be routed from the ''in'' port to the ''out'' port either with or without delay. The delay was a 2 m (12.8 ns) long waveguide that at 40 Gb/s provides 40 B of memory. Fig. 19 shows packet recovery against received power for this device. A packet recovery rate of 98% was achieved after five circulations.

Decreasing the delay loss, the loss between passive and active regions and regeneration (2R or 3R) are all approaches that can be used to increase the buffer hold time. While the propagation loss of the silica waveguide is very low (<0.04 dB/cm) and the ER of the InP switch is high (>40 dB), the butt couple can lead to reflections and the two chips have to be packaged. An integrated solution is required.

To address the loss-coupling issue between the active and passive sections, an integrated buffer was fabricated on the hybrid silicon platform [15]. Similar to the aforementioned design, a 2 × 2 switch is used to route a signal from the input to the output either with or without delay. Because of higher propagation losses (∼2 dB/cm) compared to the silica-on-silicon, only delays of 7.6 cm (1.1 ns) were realized [2], which is more useful for packet synchronization than for memory. Fig. 20 shows the integrated buffer storing a packet for 1.1 ns.

For the earlier platform, a major part of the propagation loss in the integrated buffer is introduced in the definition of the amplifiers (III–V processing). To address this issue, proper passivation is needed to realize longer delay lines.

The latest generation of LASOR optical buffers in the hybrid silicon platform with a modification that the delay line (1.1 m) is protected by SiO_2 and SiN passivation layers to protect the delay line during the III–V processing. In addition, 2R regenerators for reamplification and reshaping have been integrated to amplify and filter the signal. A photograph of the first fabricated chip is shown in Fig. 21.

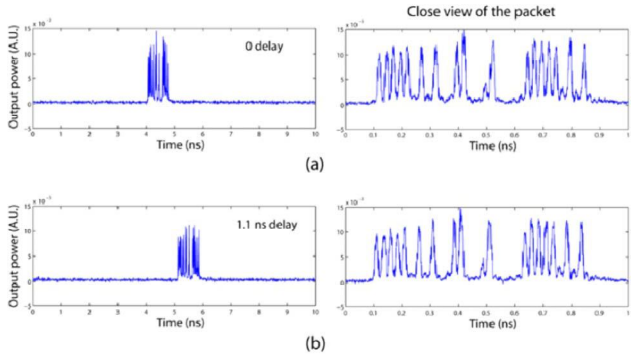

Fig. 20. Optically buffered packet (a) with no delay (b) and 1.1 ns of delay.

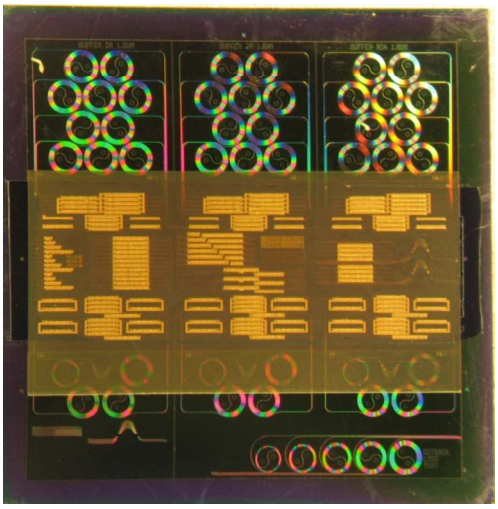

Fig. 21. Integrated buffer with 2R regenerators on an silicon-on-insulator substrate. A total of three buffers having 1.1 m of delay each are shown. In addition, various test structures and shorter buffers are on these chips.

E. Optical Wavelength Converters

Optical wavelength converters are used in LASOR for packet forwarding and are one of the two basic building blocks for the switching fabric in addition to an AWGR. PIC realizations have demonstrated wide tunable laser function, fast wavelength switching, and wavelength conversion without any electrical signal conditioning at data rates of 40 Gb/s. In the LASOR project, we have developed, demonstrated, and incorporated into the final router test bed two types of devices: concurrent absorption and modulation devices (such as Mach–Zehnder interferometric (MZI)-SOA wavelength converters), and separate absorption and modulation devices (such as a photocurrent driven externally modulated laser architecture). This level of integration significantly improves the performance, mainly through insertion loss reduction between the components, which translates into lower chip bias needs, and thus, lower thermal dissipation.

The overall power consumption for both device types was dominated by the need for devices cooling, and more than half

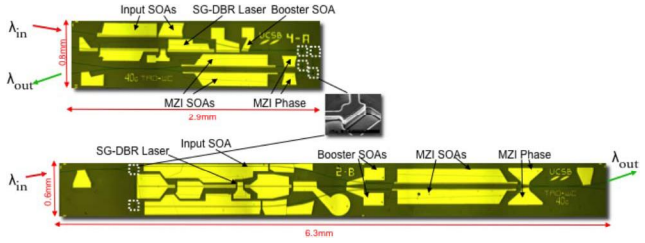

Fig. 22. Folded and unfolded versions of 40 Gb/s fast widely tunable CAM differential pulse MZI-SOA wavelength converters.

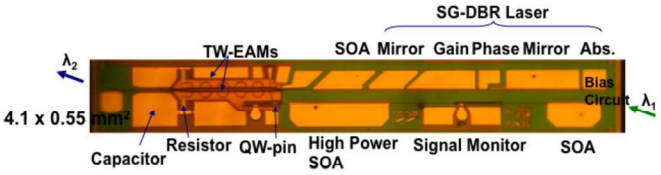

Fig. 23. SAM version of the monolithic fast widely tunable 40 Gb/s wavelength converter.

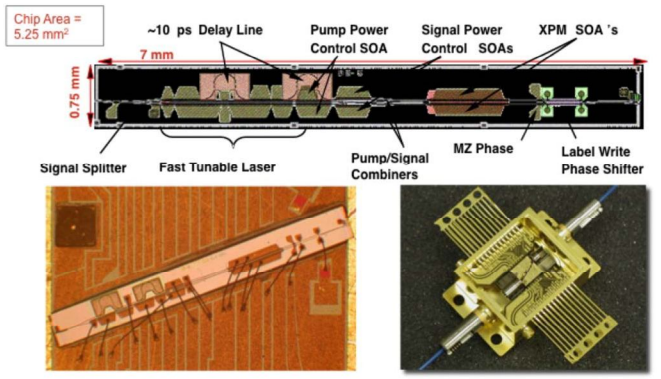

Fig. 24. Differential 40 Gb/s PFC with integrated optical label rewrite (upper), mounted chip on carrier (lower left) and packaged (lower right).

of the total power (2–2.5 W) was used up by the thermoelectric cooler.

Improvements that can be made to make these devices more power efficient have to do with reduction of insertion losses, reduction of on-chip losses, and possible optimization of the chip integration platform, to allow for hotter operation of the devices without performance degradation (which would reduce the need for cooling).

1) Concurrent Absorption and Modulation Wavelength Converters: In these device types, the interaction of photons and electrons happens in adjacent waveguides, where the optical mode overlaps the optical confinement and gain modulation region at the same time (as in an SOA), and the wavelength conversion function is performed through nonlinear behavior in the SOA between the optical mode and the carrier population. This interaction affects both phases and power levels of the signals, which is converted into an amplitude response through a use of an interferometer. In LASOR program, we have demonstrated five generations of tunable CAM wavelength converters operating at 40 Gb/s, with the goal of improving their efficiency, and reducing the footprint.

Two implementations are shown in Fig. 22. Both designs are based on a differentially driven SOA-based MZI. A folded compact version of the device (top, 2.9 mm $\times$ 0.8 mm), and a more advanced design in terms of ability to independently control the phase and amplitude (bottom, 6.3 mm $\times$ 0.6 mm) are shown. The power dissipation on chip was dominated by the nonlinear SOAs in the branches of the MZ ($\sim$1.2 W). The power consumption did scale with bit rate, since higher SOA bias currents were needed at 40 Gb/s to speed up the response of the carriers (0.8 W at 10 Gb/s and 1.2 W at 40 Gb/s).

2) Photocurrent-Driven Wavelength Converters: This type of fast widely tunable wavelength converter operates by detecting the optical input using a preamplified photodiode. The photodiode electrode is shared with an optical modulator electrode, which is adjacent to the widely tunable laser, as shown in Fig. 23. Five different generations of these devices were explored, with performance continually improving, and with maximum data rate reaching 40 Gb/s return to zero (RZ), after implementation of low capacitance, traveling wave electrodes.

Constant bias set-point operation of these devices was demonstrated across the data rates of 2.5 to 40 Gb/s, implying the possibility of constant power consumption. However, it is possible to optimize the biasing conditions for lower bit rates, and thus, reduce the consumption in this region of operation. Another advantage of this approach is that it does not use large MZI-SOAs, which improves this chip's efficiency significantly. Besides common improvements already discussed, these device types would benefit from more optimized photodetectors (PDs) and modulators. We are now seeing much lower waveguide losses in both the deeply etched structures as well as the QW intermixing (QWI) structures, and we have more ideas, which the modeling indicates should get us to significantly better devices

F. Packet Forwarding Chip

CAM and SAM wavelength converters are used as a building block for the PFCs of the optical switching fabric. The PFC adds to the differential tunable wavelength converter, the function of label modulation is added to the tunable wavelength converter platforms. By using small modifications to the wavelength converter platforms, higher level of integration was achieved with additional power saving. The PFCs illustrates the benefits of integrated photonics, through all the functions it provides: light splitting and amplification, new tunable wavelength generation, label erase function, label rewrite function, and payload wavelength conversion, all at 40 Gb/s line rate, and with less than 6 W (see Fig. 24). Two of the most important features of monolithic integration are stability of phase sensitive delays and preservation of photons by reducing losses normally required moving onto and off of several photonic chips.

G. Monolithic Tunable Optical Router

The MOTOR chip was the next step in evolution of moving the LASOR switching fabric onto a single chip, further improving performance, footprint, and power consumption. Improved energy efficiency is achieved by scaling the number of

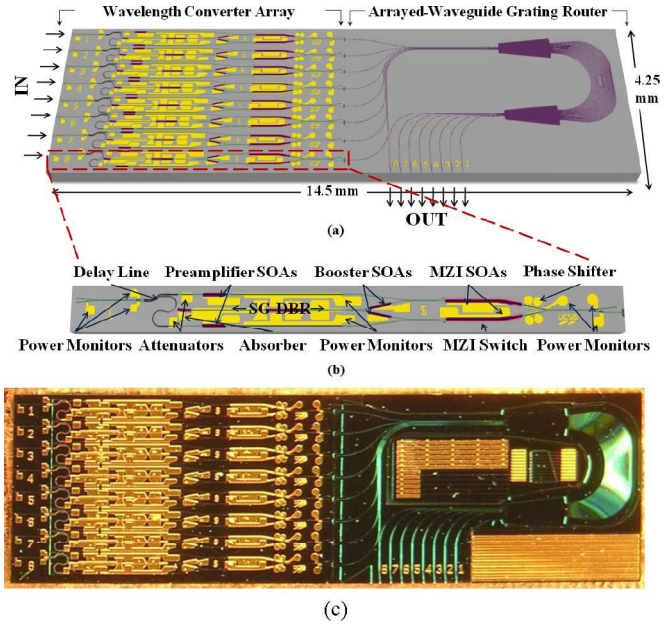

Fig. 25. (a) Diagram of the MOTOR PIC illustrating eight input full functioning PFCs connected to a low loss 8 × 8 AWGR. (b) Details of the individual PFCs. (c) Photomicrograph of the device.

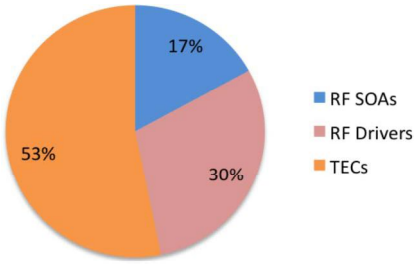

Fig. 26. OPS estimated power consumption breakdown of the total measured power consumption of 7.5 W.

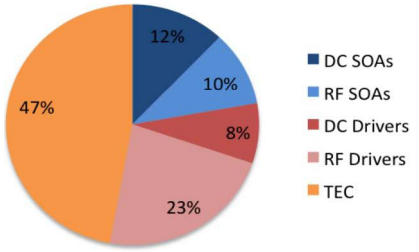

Fig. 27. ORAM estimated power consumption breakdown of the total measured power consumption of 7.7 W.

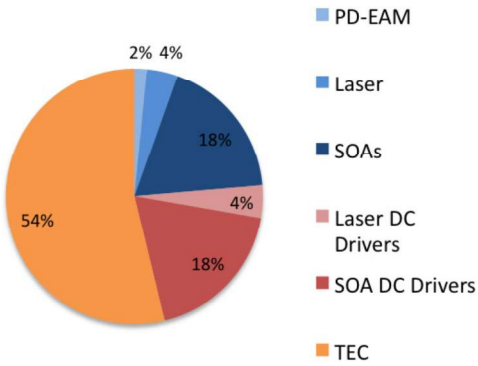

Fig. 28. PFC estimated power consumption breakdown of the total measured power consumption of 5.6 W.

photonic elements in a given chip. These large-scale PICs replace many of the high-loss fiber-to-fiber connections between optical components with low-loss waveguide transitions, reducing the amount of power required for functions like signal amplification to compensate for optical losses. For a function with complexity of that of the optical switching fabric, monolithic integration has fairly significant impact.

We demonstrated integration of the elements within the dotted line in Fig. 10. The chip is called a MOTOR chip. The first generation consisted of an array of eight 40 Gb/s wavelength converters and a passive AWGR. The device is one of the most functionally complex InP photonic ICs ever reported, with more than 200 integrated elements in a single chip, including multiple SOAs, a widely tunable sampled grating distributed Bragg reflector (SG-DBR) laser, a passive differential delay line, variable optical attenuators, an AWGR, and phase shifters. Single-channel 40 Gb/s wavelength conversion and channel switching required less than 2 W drive power and showed a power penalty as low as 4.5 dB with a 2^{31-1} pseudorandom binary sequence data signal. MOTOR chip was part of the final technology demo, whose goal was to prove the extent of integration possible in the router optical switch fabric. Therefore, the MOTOR chip consisted of eight CAM PFC chips, integrated with an AWGR, forming an 8 × 8 optical switch fabric with total capacity of 640 Gb/s and less than 50 W power consumption. At the time of the demonstration, this was one of the most complex PIC chips designed to date (see Fig. 25).

VII. Power and Bit-Switching Analysis

The power consumed by the synchronizers and buffers were measured. For the top port, the power consumed by the synchronizer and buffer was 8.2 and 7.7 W, respectively. It is important to note that the calculations include the power needed to drive the photonic devices as well as the power required to regulate the temperature of each device. Photonics are highly temperature dependent, therefore, temperature controllers are required for proper operation. Furthermore, the photonic devices require electronic drivers to make the devices operational, so the power consumed in the drivers must go hand in hand with the power consumed in the optics. In order to further investigate, where the majority of power is consumed in the optical technologies, power estimates were calculated for the synchronizer and buffer. Packaged components were used that had the optical devices, electronic drivers, and temperature controllers powered by a common power supply. The power consumption of the optical devices can be estimated assuming that the power consumed was at maximum biasing of the SOAs, and the rest was consumed by electronic power dissipation and temperature control.

The results for the estimated breakdown of power consumed in the OPS, optical buffer, and PFC are shown in Figs. 26–28.

A majority of the power is not consumed in the photonics, but rather in the electronic drivers and temperature controllers. All of the photonic devices required SOAs for switching as well as to compensate for losses due to coupling, splitting, and propagation. If these losses can be reduced, then fewer and smaller SOAs can be used, which would reduce power. Additionally, more efficient SOA technology will further reduce power consumption. It should be noted that in the LASOR experiment, the electronic drivers for operating photonic devices were not optimized for low-power operation.

Using state-of-the-art efficient electronic technologies will reduce this measured component. Most photonic devices are currently highly temperature dependent, therefore, temperature regulation is required, which consumes the majority of power. If alternative means of temperature control that draw less power are implemented or temperature-independent photonics are used, then the power consumed by the photonic devices can be reduced drastically. It should be noted that although the use of synchronous buffers increases total power consumption compared to architectures that do not implement synchronization, overall control logic complexity is reduced that may reduce electronic power consumption.

A rough calculation of the switching energy per bit for the LASOR system demonstration technology can be estimated by the 110 W required to route 640 Gb/s or approximately 0.2 nJ/bit (see Fig. 29). It is important to note this switching energy is achieved with first generation PICs and nonpower optimized support electronics. Compared to the 3 nJ/bit switching energy for today's state-of-the-art router, the initial LASOR work shows potential for orders of magnitude improvement. It is important to emphasize that the LASOR technologies are used as a proof of principle and first-order analysis for power and energy and strict conclusions should not be drawn from these numbers, rather the potential for trends by architecting new packet systems that combine PIC and electronic technologies.

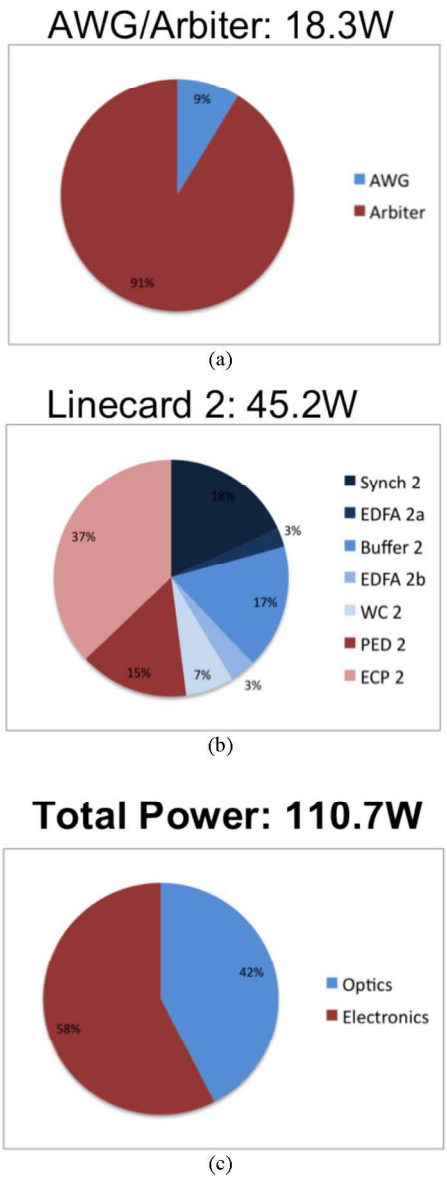

Fig. 29. Power consumption breakdown for the (a) arbiter, (b) line card, and (c) total power consumption for a two line card router.

VIII. Summary and Conclusion

In this paper, we have reviewed the role communications interconnects and networks play in the future contribution to the global carbon footprint, especially in data center and cloud-computing applications, which are expected to grow exponentially in traffic. We have also described the potential power consumption savings by integrating photonic technology into system architecture designs along with electronics technology. Key to maximizing the benefits of photonics technology is photonics integration. In the context of an example packet routing system, the DARPA/MTO funded LASOR project, we have reviewed the key PIC functions that have been realized and the power contributions of these PIC technologies as more and more functions are integrated onto a single chip.

We have also quantified, through measurements, the power consumed by the photonics in performing their intended function, the electronics required to bias the photonics, processing electronics, and required cooling technology. In moving the optical forwarding, buffering and other data plane functions to photonics, the dominant contributions to power in packet routing have moved from the forwarding plane to the packet-processing plane.

There is still much room (potentially greater than 10×) for improvement in the forwarding plane in the PIC technology and supporting electronics, however, moving forward the focus will most likely need to be on investigating photonic technologies that can impact the power consumption of the packet forwarding processing plane and in reducing cooling requirements in the data forwarding plane as well as higher levels of monolithic integration.

In the future, as the bit rates increase to 100 Gb/s and beyond, and coherent transmission technologies are employed, LASOR type technologies will need to scale to these new rates and be adapted to new modulation formats. There is also the potential for the Internet to utilize packet sizes greater than 1500 B (e.g., 5000 B super packets), and all the LASOR technologies will work as the packet size increases. The major issue

will be with optical buffering that will require larger storage delays with lower loss waveguides and regenerative buffers. Work is underway to design, fabricate, and test these new LASOR technologies and reports of progress will appear in future publications.

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Matt Dummer, photograph and biography not available at the time of publication.

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John Garcia, photograph and biography not available at the time of publication.

Brian Koch, photograph and biography not available at the time of publication.

Vikrant Lal, photograph and biography not available at the time of publication.

Erica Lively, photograph and biography not available at the time of publication.

John Mack, photograph and biography not available at the time of publication.

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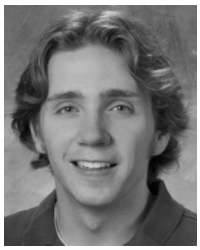

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Matt Sysak, photograph and biography not available at the time of publication.