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High-efficiency, high-speed VCSELs with deep oxidation layers

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High-efficiency, high-speed VCSELs with deep oxidation layers

Y.C. Chang, C.S. Wang, L.A. Johansson, and L.A. Coldren

In this paper, a novel method to reduce the parasitics of vertical-cavity surface-emitting lasers (VCSEL) using deep oxidation layers is proposed. Using this method, we demonstrate high-efficiency, high speed 980 nm, tapered-aperture VCSELs with a –3 dB frequency of 17.9 GHz, the highest bandwidth without using proton implantation.

Introduction: High-efficiency, high-speed VCSELs are in high demand for optical interconnects because they have small footprints, dissipate less power, can be easily fabricated into arrays, and are cost effective. The bandwidth of a VCSEL is determined by the intrinsic laser properties as well as the extrinsic parasitics. Various methods have been proposed to lower the parasitics so that the modulation bandwidth can reach the laser intrinsic limit [1–4]. Proton implantation is widely used to kill the parasitic capacitance associated with the thin oxide aperture capacitance and junction capacitance. The highest two VCSEL modulation bandwidths reported are 21.5 GHz [4] and 20 GHz [5] and they were both proton-implanted. Proton implantation significantly complicates the fabrication since very thick mask is needed to block the high energy protons. For example, 6 μm thick photoresist is needed to block 300 keV protons which penetrate ~2.5 μm in $Al_{0.5}Ga_{0.5}As$ [6]. In this paper, we propose a new method to reduce the parasitic capacitance using deep oxidation layers. By increasing the aluminium fraction of the first several *p*-distributed Bragg reflectors (DBR), deep oxidation layers can be formed simultaneously with the oxide aperture. These deep oxidation layers increase the equivalent capacitor thickness, thus reducing the capacitance. This method is simple and the fabrication remains unchanged. Using this method, we demonstrate high-efficiency, high-speed 980 nm VCSELs with differential efficiency up to 68%, peak wall-plug efficiency of 37%, and modulation bandwidth of 17.9 GHz.

Device structure and fabrication: Fig. 1 shows the schematic cross-section of the VCSEL. The sample was grown on a semi-insulating GaAs (100) substrate by molecular beam epitaxy. The bottom mirror consists of a 14-period undoped GaAs/AlAs DBR, followed by a five-quarter wavelength thick silicon-doped *n*-contact layer, and a 4-period *n*-type GaAs/$Al_{0.9}Ga_{0.1}As$ DBR. The highly-doped *n*-contact layer is placed 4 periods away from the cavity to lower the optical loss as well as to reduce the effective cavity length for high speed consideration. The active region has three InGaAs/GaAs quantum wells embedded in a $Al_{0.3}Ga_{0.7}As$ separate confinement heterostructure layer. The oxide aperture consists of 100 Å AlAs followed by 1430 Å $Al_{0.82}Ga_{0.18}As$ in order to form a tapered tip. The lens-like effect of this tapered aperture decreases optical losses for increased efficiency [7]. The top mirror consists of a 30-period carbon-doped GaAs/AlGaAs DBR, followed by a highly-doped *p*-contact layer. The aluminum fraction of the first two periods of the DBRs is increased from 85% to 93% in order to form the deep oxidation layers. This also increases the refractive index contrast, and, consequently, reduces the mode volume.

The fabrication began by etching cylindrical mesas ranging from 20.5 to 30 μm in diameter down to the *n*-contact layer using reactive ion etch. The oxide apertures were then formed by wet oxidation, resulting in a ~8 μm oxidation depth with a 4.5 μm taper length from either side. The two deep oxidation layers above the oxide aperture were formed simultaneously as shown in the SEM in Fig. 2. The two $Al_{0.93}Ga_{0.07}As$ layers oxidized 4.2 μm in depth, 3 μm deeper than the rest $Al_{0.85}Ga_{0.15}As$ layers. Ti/Pt/Au and AuGe/Ni/Au were evaporated for *p*- and *n*-contacts, respectively. Benzocyclobutene (BCB) was applied, patterned to open windows, and fully cured. The BCB was used for planarization, passivation, and capacitance reduction purposes. Then Ti/Au was deposited on top of BCB as pad metal. Finally, an antireflection coating was deposited to reduce the backside reflection.

Results: Fig. 3 shows the voltage and output power versus current (L-I-V) curves for a 4 μm diameter device which has the highest bandwidth. The device has a differential efficiency of 68% and a low threshold current of 0.18 mA. This low threshold current indicates that incorporating deep oxidation layers does not add extra scattering loss and degrade the device performance. This is because the optical modes are mainly confined by the tapered oxide aperture and do not see the oxidation layers. The threshold voltage is 1.53 V, only 270 meV larger than quasi-Fermi level separation. This indicates our bandgap engineering scheme effectively eliminates the heterobarriers at the DBR interfaces. The series resistance is ~240 Ω, resulting from the insufficient doping levels of the DBRs near the active region. The peak wall-plug efficiency is 37% at a current of 1 mA and the max output power is 5.7 mW at a bias current of 9.5 mA.

Small-signal modulation responses were measured on-wafer using a RF probe and a calibrated vector network analyzer. Output power was collected using a 50 μm multimode fiber and a high-speed photodetector. The frequency responses for the 4 μm diameter device under different bias currents are shown in Fig. 3. The maximum electrical –3 dB frequency is 17.9 GHz at a bias current of 4.75 mA, corresponding to only 10 mW of power dissipation. This is the highest bandwidth for a VCSEL without using proton implantation. Although the bandwidth is still limited by the parasitics, it is mainly due to the relatively high series resistance and can be reduced by increasing the doping.

Conclusion: A novel method using deep oxidation layers to reduce the parasitics of a VCSEL is proposed. By incorporating the deep oxidation layers into our devices, we demonstrated high-efficiency, high-speed 980 nm VCSELs with bandwidth 17.9 GHz

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Figure captions:

Fig. 1 Schematic cross-section of the VCSEL

Fig. 2 Cross-section SEM of the VCSEL

Fig. 3 L-I-V curves for a 4 μm diameter device at 20°C

Fig. 4 Small-signal modulation responses for a 4 μm diameter device under different bias currents at 20°C

Figure 1

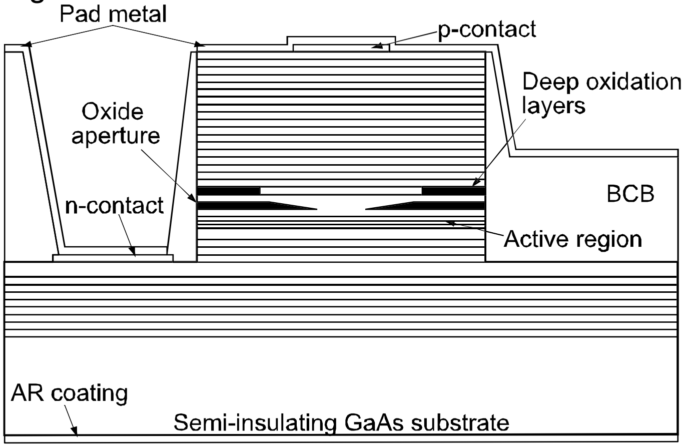

Pad metal
p-contact
Deep oxidation
layers
Oxide
aperture
n-contact
BCB
Active region
AR coating
Semi-insulating GaAs substrate

Figure 2

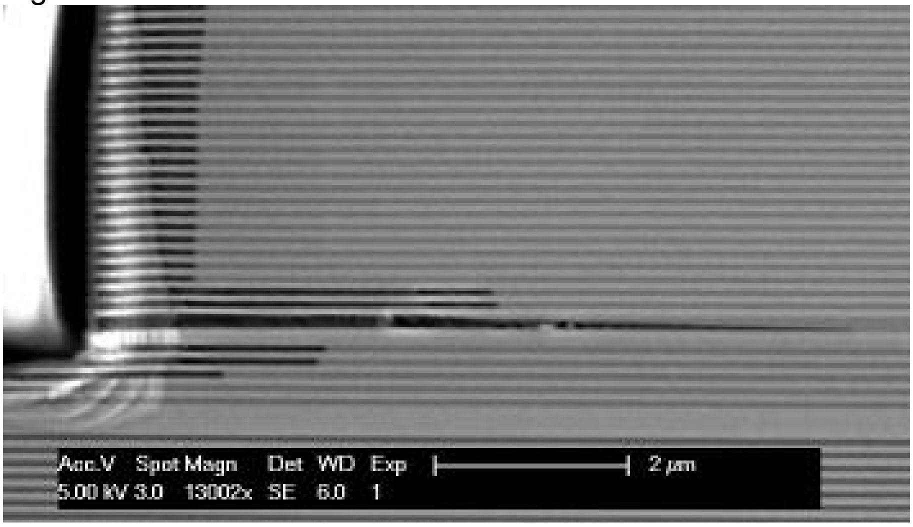


Figure 3

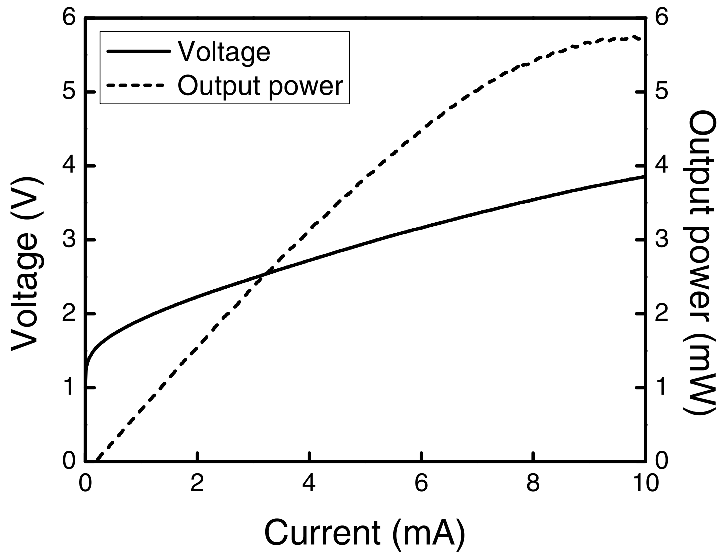
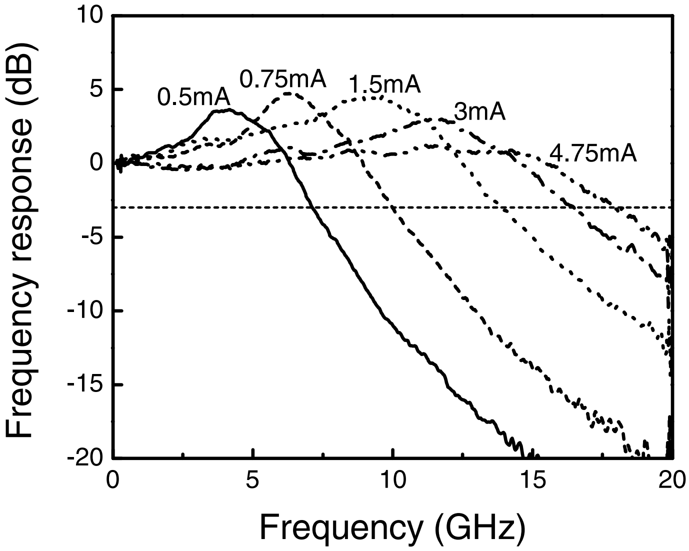

Voltage
Output power
Voltage (V)
Output power (mW)
Current (mA)
0
1
2
3
4
5
6
0
2
4
6
8
10

Figure 4


0.5mA
0.75mA
1.5mA
3mA
4.75mA
Frequency response (dB)
Frequency (GHz)
10
5
0
-5
-10
-15
-20
0
5
10
15
20