Small-dimension power-efficient high-speed vertical-cavity surface-emitting lasers

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Small-dimension power-efficient high-speed oxide-confined 980 nm vertical-cavity surface-emitting lasers (VCSELs) with record-high bandwidth/power-dissipation ratio of 12.5 GHz/mW have been demonstrated. The devices show a modulation bandwidth of 15 GHz at a bias current 0.9 mA, corresponding to only 1.2 mW power dissipation.

Introduction: Recently, VCSELs have received considerable interest for short-distance optical interconnects owing to their small footprint, natural occurrence in arrays and, most importantly, cost effectiveness. Two of the main challenges for the devices to be used in board-to-board and chip-to-chip interconnects are speed and power dissipation. For directly modulated lasers, higher speed can be achieved with higher bias current at the expense of higher power dissipation. High power dissipation can be fatal in these compact systems with limited power budgets and stringent thermal restrictions. Most of the high-speed VCSELs have diameters from 6 to 8 µm and have threshold currents of 0.3 mA or above [1–3]. For these devices, 15 GHz bandwidth, which should enable 20 Gbit/s operation, was achieved at a current of at least 1.5 mA, but usually a much higher current was required owing to their high threshold currents and large mode volumes. Smaller devices are potentially faster and require less power, and thus are more suitable for optical interconnects. One of the obstacles for small devices to have high speed is the parasitics. By implementing deep oxidation layers [4] and optimising the doping schemes, we were able to reduce the parasitics to enable high-speed operation for smaller devices. Our 3 µm diameter device shows 15 GHz bandwidth at a bias current of 0.9 mA, corresponding to only 1.2 mW power dissipation. A bandwidth/power-dissipation ratio of 12.5 GHz/mW is achieved for 15 GHz, the highest ever reported.

Device structure and fabrication: Fig. 1a shows a schematic cross-section of the VCSEL. The layer structure is similar to our previous device [4] except that the following modifications were made to address the issues with parasitics. First, the number of deep oxidation layers was increased from two to five to further reduce the parasitic capacitance. Secondly, the overall *p*-doping concentration was increased to reduce the series resistance, especially in the first several periods of the DBRs above the active region, which account for most of the resistance. Fig. 1b shows a top view scanning electron micrograph (SEM) of a fabricated VCSEL. The devices were fabricated using the process given in [4] with the following improvements. After the *p*- and *n*-contact metals were deposited, the *n*-GaAs contact layer (RF ground) beneath the *p*-pad metal (RF signal) was first etched away using citric acid/hydrogen peroxide to eliminate the pad capacitance. The benzocyclobutene (BCB) between the *n*-pad metal and the *n*-metal was removed for better RF grounding and heat spreading. The dimension of the *p*-pad metal is also reduced to 40×70 µm. Before anti-reflection (AR) coating, the backside was lapped to remove residues accumulated throughout earlier processing steps.

Results: Figure 2 shows the voltage, output power and temperature rise against current (*L-I-V-T*) curves for a 3 µm diameter device, which is the smallest device and has the highest bandwidth/power-dissipation ratio. The device has a differential quantum efficiency of 53%, which is slightly lower than expected. This may have resulted from the lapping process, which roughens the output surface. The threshold current is only 0.155 mA, less than half the values for most high-speed VCSELs. The threshold current does not increase considerably from the higher doping concentration because the modes are better confined in the longitudinal direction and have less overlap with the highly doped DBRs. This is due to the increased number of the deep oxidation layers, which have higher aluminum fraction and larger index contrast in the region of the mode. The threshold voltage is 1.48 V, which is very low for such a small device, and it is only 220 meV larger than the quasi-Fermi level separation. The series resistance is $\sim 220 \, \Omega$. The peak wall-plug efficiency is 30% at a

current 1 mA. The thermal impedance of the device is 2.88°C/mW, calculated by measuring the wavelength shift at different stage temperature and at different bias [5]. The maximum output power is 3.6 mW at a bias current of 8.6 mA, corresponding to a temperature rise of 77°C.
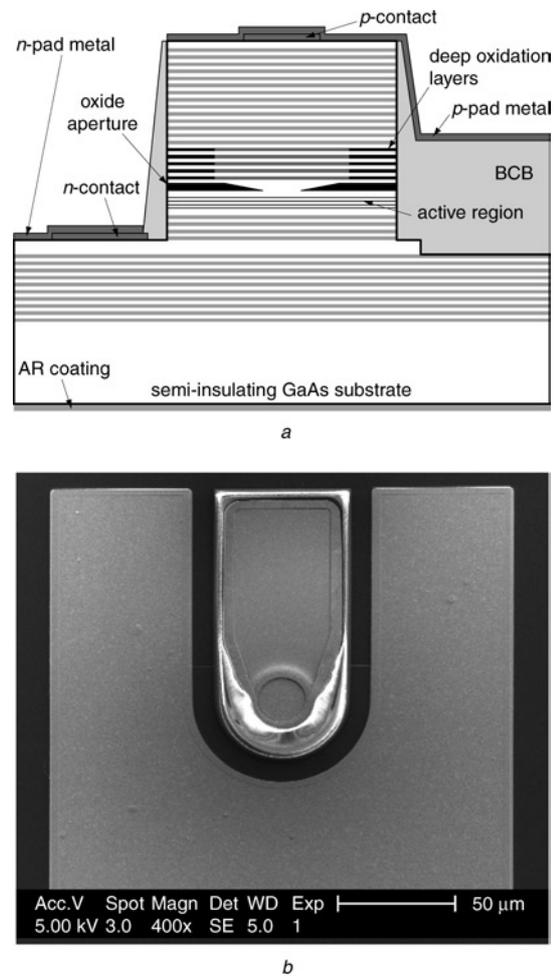
Fig. 1 *Schematic cross-section of VCSEL, and top view SEM of VCSEL*
a Cross-section of VCSEL
b SEM of VCSEL
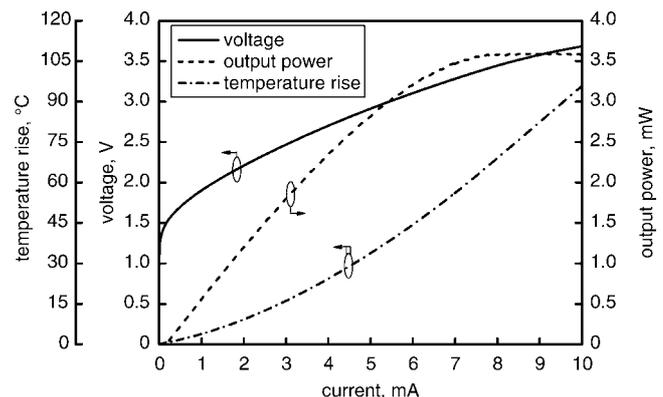
Fig. 2 *L-I-V-T curves for 3 µm diameter device at stage temperature 20°C*

Small-signal modulation responses were measured on-wafer using an RF probe and a calibrated Agilent PNA network analyser E8364A. Output power was collected by a 50/125 multimode fibre and measured using a New Focus 25 GHz photodetector coupled to a New Focus 20 GHz amplifier. The frequency responses for the 3 µm diameter device under different bias currents are shown in Fig. 3. An electrical −3 dB bandwidth of 15 GHz is achieved at a bias current 0.9 mA, corresponding to 1.6 mW input power and 1.2 mW dissipated power. Methods have been proposed to reduce the thermal impedance and alleviate the thermal degradation [3, 6]. With 1.2 mW power

dissipation, the temperature rise is only 3.5°C and should have negligible thermal impacts on the device performances. The modulation current efficiency factor (MCEF) for the device is 16.8 GHz/√mA, equal to the highest previously reported value [7]. The high MCEF is mainly due to the stronger mode confinement in both lateral and longitudinal directions.
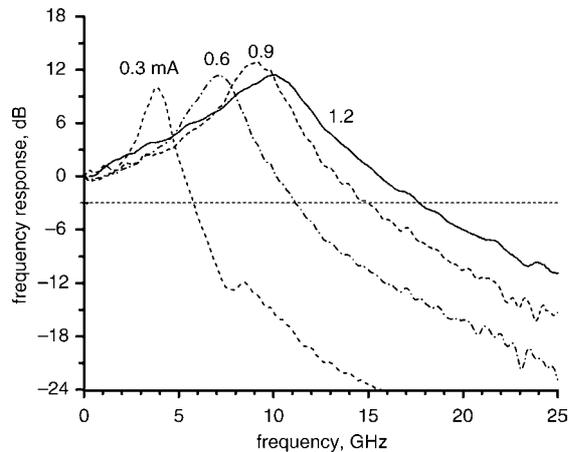
Fig. 3 *Small-signal modulation responses for 3 μm diameter device under different bias currents at stage temperature 20°C*

The modulation responses at higher bias currents were measured, and although they extended to higher frequencies, they also showed sharp drops at low frequency, usually below 0.5 GHz. This may be caused by mode partition inside the device and spatial mode filtering from our measurement setup. This supposition is supported by the fact that the photocurrent from the photodetector was relatively noisy at high VCSEL bias currents. By better controlling the higher order modes or by collecting all of the light, for example with a backside microlens [8], a usable bandwidth > 20 GHz should be attainable.

Conclusions: Small-dimension, power-efficient high-speed VCSELs with 12.5 GHz/mW bandwidth/power-dissipation ratio have been demonstrated. 15 GHz bandwidth is achieved at 0.9 mA for 1.2 mW power dissipation. This high bandwidth with reduced power dissipation makes these devices more suitable for optical interconnect applications than previous designs.

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