Efficient, High-Data-Rate, Tapered Oxide-Aperture Vertical-Cavity Surface-Emitting Lasers

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(Invited Paper)

***Abstract*—New advances in high-efficiency, high-speed 980-nm vertical-cavity surface-emitting lasers (VCSELs) are presented. The tapered oxide aperture was optimized to provide additional mode confinement without sacrificing its static low-loss performance. The pad capacitance was reduced by using benzocyclobutene, removing the n-contact layer, and shrinking the pad dimension. The mesa capacitance was also lowered by using a thicker oxide aperture and deep oxidation layers. With all these improvements, our devices demonstrated >20 GHz bandwidth, the highest for 980 nm VCSELs, and 35 Gb/s operation at only 10 mW power dissipation, corresponding to the highest reported data rate/power dissipation ratio of 3.5 Gb/(s·mW).**

***Index Terms*—Optical interconnects, optical modulation, oxidation, semiconductor lasers, vertical-cavity surface-emitting lasers (VCSELs).**

I. Introduction

In THE PAST several years, vertical-cavity surface-emitting lasers (VCSELs) have received renewed interest due to their applications in optical interconnects, which are becoming widely used, partially because of possible reductions in system power dissipation. Due to the intensive worldwide research efforts, the performance of VCSELs, particularly in high-speed aspect, has made tremendous progress in just the past few years. In 2006, 25 Gb/s operation was first reported by Suzuki *et al.* [1]. In 2007, data rates of 30, 35, and 40 Gb/s were consecutively demonstrated by Yashiki *et al.* [2], Chang *et al.* [3], and Anan *et al.* [4], respectively. In 2007, data rate of VCSEL was pushed from 25 to 40 Gb/s, a significant progress.

Table I summarizes the state-of-the-art high-speed VCSEL structures and results in three different wavelengths: at 850 nm, 30 Gb/s was reported by Johnson in 2008 [5]; at 980 nm, we reported 35 Gb/s; at 1.1 μm, 40 Gb/s was reported by Anan. By examining the structures of these record VCSELs, we can see what the requirements to achieve high-speed operation are. Thick low-dielectric-constant materials such as silicon oxide, benzocyclobutene (BCB), and polymide have to be used for reducing the pad capacitance. The mesa capacitance has to be lowered by either ion implantation or deep oxidation layers. The optical modes need to be confined by oxide aperture or buried tunnel junction. On the other hand, there are unique features for each device. For example, highly strained InGaAs/GaAs quantum wells (QWs) are used in Anan's devices to achieve high differential gain.

Compared with the other two devices that operate best at $\sim$6 μm, our devices can be much smaller due to their lower cavity losses associated with the lens-like tapered aperture [6]. Therefore, the threshold current of our devices is much lower at 0.14 mA for a 3-μm-diameter device, and because the resonance frequency varies inversely with the square root of the photon volume, our devices are fast at small biases, achieving a 20 GHz bandwidth at just 2 mA. In addition, smaller devices with low cavity losses are more power efficient, which is very important for optical interconnect applications. A data rate of 35 Gb/s was demonstrated at 4.4 mA with only 10 mW power dissipation, corresponding to a record data rate/power dissipation ratio of 3.5 Gb/(s·mW). All these results are enabled by carefully designing the tapered oxide aperture for low loss and high confinement, optimizing the distributed Bragg reflector (DBR) mirror, incorporating the deep oxidation layers, and reducing the pad capacitance.

The paper is organized as follows. Section II presents the theoretical background for directly modulated VCSELs. The device designs are covered in Section III. Section IV shows the device fabrication. The results and discussion are given in Section V. Finally, Section VI concludes the paper.

II. Theoretical Background

For directly current-modulated VCSELs, the bandwidth is determined by the intrinsic laser properties as well as the extrinsic parasitics. To make our discussion easier, we will consider them separately using the cascaded two-port model [7], shown in Fig. 1, to isolate the parasitics from the intrinsic laser. The intrinsic laser is defined as the active region approximately in the apertured area where carriers and photons interact via absorption and emission. The parasitics, defined between the intrinsic laser and driving circuit, are split into the pad parasitics and chip parasitics at the metal contacts.

The input variables of the VCSEL are the drive voltage v_d and current i_d. The voltage and current seen by the intrinsic laser are v_a and i_a, respectively. The output variables are the output power p and frequency shift $\Delta\nu$. For short-distance optical interconnects, dispersion is negligible and $\Delta\nu$ will not be discussed. The currents entering the pad and chip parasitics are i_p and i_c, respectively.

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TABLE I
STATE-OF-THE-ART HIGH-SPEED VCSELS

Wavelength (nm)	Authors	Features	Achievements
850	R. Johnson *et al.* [5]	• Thick silicon oxide • Proton implantation • Oxide aperture	• I_{th}=0.75 mA for 6 µm devices • 19 GHz bandwidth • 30 Gb/s operation at 8 mA
980	Y.-C. Chang *et al.* [3]	• BCB • Deep oxidation layers • Low-loss high-confinement tapered oxide aperture	• I_{th}=0.14 mA for 3 µm devices • >20 GHz bandwidth • 35 Gb/s operation at 4.4 mA
1100	T. Anan [4]	• Polymide • Ion implantation • Buried tunnel junction • Optimized active region	• I_{th}<1 mA for 6 µm devices • 24 GHz bandwidth • 40 Gb/s operation at 5 mA

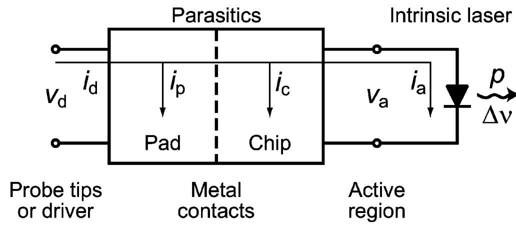


Fig. 1. Cascaded two-port model of diode laser.

A. Intrinsic Laser Limitations

The dynamic behaviors of diode laser are commonly analyzed using small-signal frequency response. For diode laser, the modulation response can be approximated as [8]

$$H_{\rm int}(\omega) \equiv \frac{p(\omega)}{i_{\rm a}} = \frac{A}{\omega_{\rm r}^2 - \omega^2 + j\omega\gamma} \qquad (1)$$

where A is an amplitude factor, ω is the angular modulation frequency, $\omega_{\rm r} = 2\pi f_{\rm r}$ is the relaxation resonance frequency, and γ is the damping factor.

The relaxation resonance frequency is the natural oscillation frequency between the carriers and photons in the laser cavity and can be approximately expressed as

$$\omega_{\rm r} = \left[\frac{v_{\rm g} a N_{\rm p}}{\tau_{\rm p}}\right]^{1/2} = \left[\frac{v_{\rm g} a}{q V_{\rm p}} \eta_{\rm i} (I - I_{\rm th})\right]^{1/2} \qquad (2)$$

where $v_{\rm g}$ is the group velocity, a is the differential gain at threshold, $N_{\rm p}$ is the photon density, $\tau_{\rm p}$ is the photon lifetime, q is the electronic charge, $V_{\rm p}$ is the mode volume, $\eta_{\rm i}$ is the injection efficiency, I is the bias current, and $I_{\rm th}$ is the threshold current.

The relaxation resonance frequency basically determines how fast an intrinsic laser can be modulated, provided that the damping is not severe. To improve the high-speed performance, the relaxation resonance frequency must be increased. As shown in (2), higher differential gain and larger photon density increase the relaxation resonance frequency. Several approaches have been shown to increase the differential gain, such as using quantum dots active region [9], adding strain in the QW [10], and p-doping the active region [11]. The photon density can be increased by increasing the current that contributes to the photon number $\eta_{\rm i}(I - I_{\rm th})$ and/or reducing the mode volume. The mode volume can be reduced using dielectric DBRs [2] in the longitudinal direction and photonic crystals [12] in the lateral direction.

Since the relaxation resonance frequency increases with the bias current, a figure of merit to evaluate how efficient an intrinsic laser can be modulated is the D-factor [13]

$$D \equiv \frac{f_{\rm r}}{(I - I_{\rm th})^{1/2}} = \frac{1}{2\pi}\left[\frac{v_{\rm g} a}{q V_{\rm p}} \eta_{\rm i}\right]^{1/2}.$$

To evaluate the device's overall high-speed performanace, modulation current efficiency factor (MCEF) is used

$$\text{MCEF} \equiv \frac{f_{3\,\rm dB}}{(I - I_{\rm th})^{1/2}}$$

where $f_{3\,\rm dB}$ is the 3-dB frequency. If the parasitics and damping are small, MCEF $\approx 1.55D$.

The damping factor γ is given as

$$\gamma = v_{\rm g} a N_{\rm p}\left[1 + \frac{\Gamma a_{\rm p}}{a}\right] + \frac{1}{\tau_{\Delta N}} + \frac{\Gamma R'_{\rm sp}}{N_{\rm p}} \qquad (3)$$

where Γ is the confinement factor, $a_{\rm p} = -\partial g/\partial N_{\rm p}$, $\tau_{\Delta N}$ is the differential carrier lifetime, and $R'_{\rm sp}$ is the spontaneous emission rate into the modes. At high photon density, the first term on the right-hand side dominates, and γ increases proportional to $N_{\rm p}$, and hence, $f_{\rm r}^2$. The proportionality between γ and $f_{\rm r}^2$ is the K-factor, which determines the theoretical maximum 3-dB frequency

$$f_{3\,\rm dB}|_{\rm max} = \sqrt{2}\frac{2\pi}{K}.$$

B. Extrinsic Parasitic Limitations

When dealing with high-frequency devices, parasitics are always a concern. Parasitics divert the modulated current $i_{\rm d}$ from entering the intrinsic laser due to $i_{\rm p}$ and $i_{\rm c}$. In most cases, it is desirable to minimize the parasitics so that the intrinsic bandwidth can be achieved.

Fig. 2 shows a cross-sectional schematic of an oxide-confined VCSEL superimposed with its parasitic elements. The pad capacitance $C_{\rm p}$ represents all the capacitances between the signal and ground from the probe tips/driver to the metal contacts. The value of $C_{\rm p}$ varies from tens to hundreds of femtofarads, depending on the pad layout and the materials between the

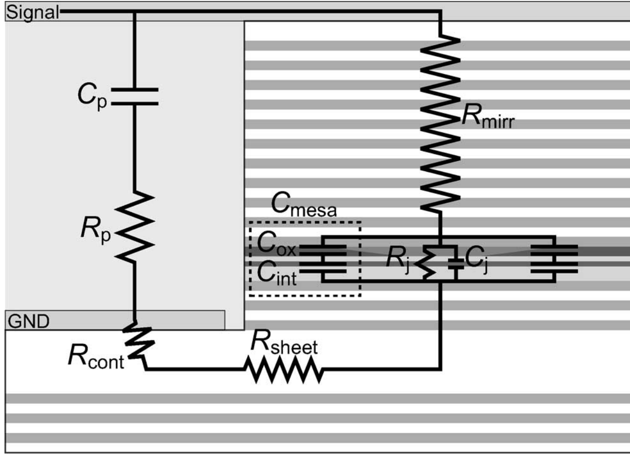


Fig. 2. Cross-sectional schematic of VCSEL superimposed with its parasitics.

pads. Typical high-speed VCSELs employ thick low-dielectric-constant materials such as polymide or BCB underneath the signal pad to reduce C_p. The pad resistance R_p accounts for the pad loss. Since it is usually relatively small, in the ohms range, compared with the impedance of C_p at the frequency of interest, it is sometimes omitted in the small-signal model.

The mirror resistance R_mirr includes the resistances from both the n- and p-DBRs. R_sheet represents the sheet resistance in the n-contact layer, and R_cont is the contact resistance for both contacts. All these resistances, usually dominated by R_mirr, can be grouped together into $R_\mathrm{m} = R_\mathrm{mirr} + R_\mathrm{sheet} + R_\mathrm{cont}$ in the small-signal model. The mesa capacitance C_mesa is the oxide capacitance C_ox in series with the capacitance associated with the intrinsic region below the aperture C_int. C_mesa depends on the pillar size and the thicknesses of the oxide and intrinsic layer.

The capacitance C_j represents the diode junction capacitance in the apertured area where current flows. It is the sum of the depletion capacitance and diffusion capacitance. Under normal forward bias condition, C_j is dominated by the diffusion capacitance, which models the modulation of the carriers stored in the intrinsic separate-confinement heterostructure (SCH) region [14]. It has been shown that the diffusion capacitance depends not only on the carrier lifetime but also on the length/grade of the intrinsic SCH region [15]. By decreasing the doping setback and grading the SCH, the diffusion capacitance can be reduced. To simplify our model, C_mesa and C_j are grouped together into $C_\mathrm{m} = C_\mathrm{mesa} + C_\mathrm{j}$. Lastly, the intrinsic laser is represented by the junction resistance R_j.

Fig. 3 illustrates the small-signal model of VCSEL and the RF driving source. Here, we have implicitly assumed that VCSEL is driven by the instrument. The RF driving source consists of a voltage source v_s and a characteristic impedance of Z_0, which is included to account for the power reflection due to impedance mismatch.

The effects of the parasitics can be described by the transfer function $H_\mathrm{ext}(\omega)$ [16]

$$H_\mathrm{ext}(\omega) \equiv \frac{\text{current flowing into the intrinsic diode}}{\text{voltage from the voltage source}} = \frac{i_\mathrm{a}(\omega)}{v_\mathrm{s}}.$$

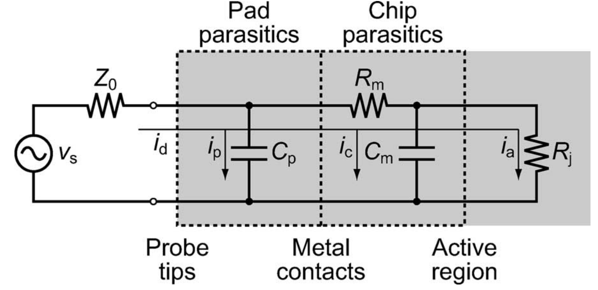


Fig. 3. Small-signal model with the driving source. The VCSEL is grayed.

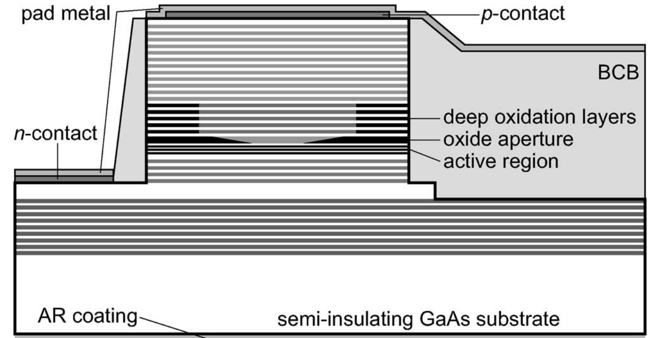


Fig. 4. Schematic cross section of our devices.

The frequency at which $|H_\mathrm{ext}(\omega)|^2/|H_\mathrm{ext}(0)|^2 = 1/2$ is defined as the parasitic 3-dB frequency ω_rc. This transfer function can be approximated by a single-pole low-pass filter function

$$H_\mathrm{ext}(\omega) = \frac{B}{1 + j(\omega)/(\omega_0)} \tag{4}$$

where B is a proportional constant and ω_0 is the parasitic roll-off frequency, which may be different from ω_rc.

The overall electrical modulation frequency response $H(\omega)$ is given as

$$H(\omega) \equiv \left|\frac{p(\omega)}{v_\mathrm{s}}\right|^2 = \left|\frac{i_\mathrm{a}(\omega)}{v_\mathrm{s}}\frac{p(\omega)}{i_\mathrm{a}(\omega)}\right|^2 = |H_\mathrm{ext}(\omega)H_\mathrm{int}(\omega)|^2$$
$$= \left(\frac{B^2}{1 + (\omega/\omega_0)^2}\frac{A^2}{(\omega_\mathrm{r}^2 - \omega^2)^2 + \gamma^2\omega^2}\right) \tag{5}$$

which gives the commonly used three-pole formula for fitting the frequency response to extract ω_r, γ, and ω_0.

III. Device Structure

Our devices are n-intracavity, bottom-emitting, oxide-confined VCSELs emitting at 980 nm wavelength, as shown in Fig. 4. For 980 nm emission, strained InGaAs/GaAs QW, which has lower transparency and higher differential gain, can be used. Bottom emission offers the possibility of backside microlenses, which can collimate the output beams, and thus, improve the alignment tolerance and reduce the packaging costs [17]. In addition, direct driver integration can be realized using flip-chip bonding that eliminates the parasitics associated with the bonding wires.

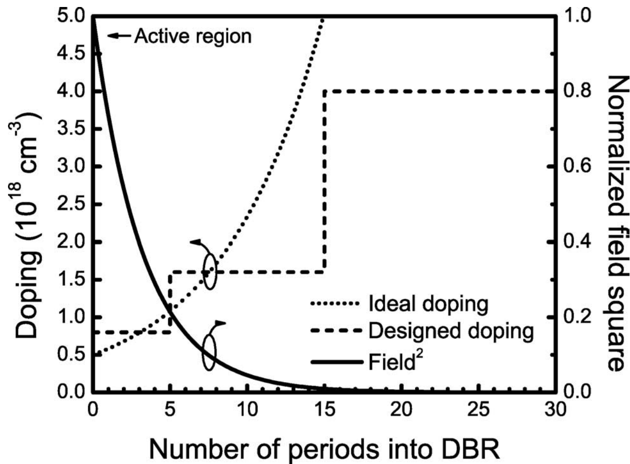


Fig. 5. Average doping profile for each DBR period.

Our devices have a 14-period undoped GaAs/AlAs DBR, followed by a five-quarter-wavelength-thick silicon-doped n-GaAs contact layer, and a four-period n-type GaAs/$Al_{0.9}Ga_{0.1}As$ DBR. The highly doped n-contact layer is placed four periods away from the cavity in consideration of optical loss and longitudinal mode confinement. The active region has three InGaAs/GaAs QWs embedded in the SCH layer. On top of the SCH is the oxide aperture, followed by a 30-period carbon-doped p-mirror, which has 5 periods of GaAs/$Al_{0.93}Ga_{0.07}As$ DBR for the deep oxidation layers and 25 periods of GaAs/$Al_{0.85}Ga_{0.15}As$ DBR. The top layer is a highly doped p-contact layer.

In the remaining part of this section, we will discuss the components of our VCSELs, namely the DBR mirror, oxide aperture, deep oxidation layers, and cavity structure.

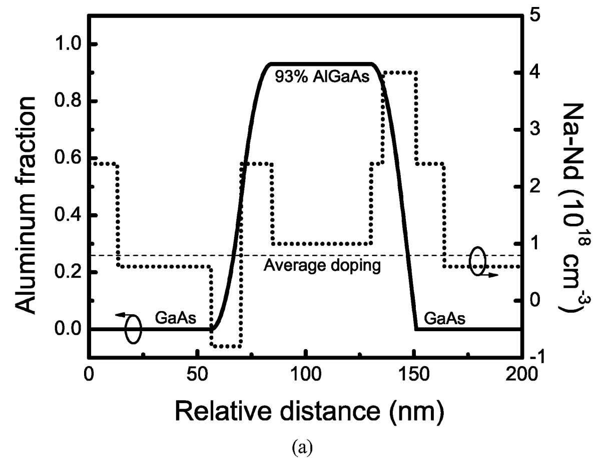
A. DBR Mirror

A major tradeoff in designing VCSELs is the electrical resistance and optical loss by the free carrier concentration, controlled by the doping. Due to higher free carrier absorption loss and lower mobility of holes, p-mirror usually employs more sophisticated design scheme, and we will focus on its design here.

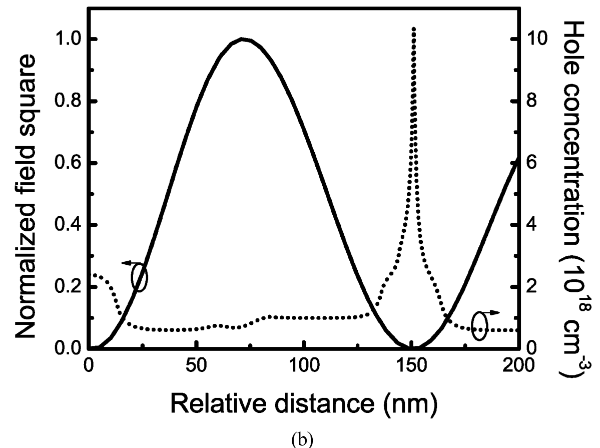
First, the average doping concentration for each DBR period is determined by maintaining a constant loss–resistance product across the whole p-mirror. For the first-order approximation, the ideal doping concentration $\rho(z)$ should be [18]

$$\rho(z) \propto \psi(z)^{-1/2}$$

where $\psi(z)$ is the electric field square profile and can be determined using 1-D transfer matrix calculation. Fig. 5 plots the average doping concentration for each DBR period in our devices. Three different doping levels were used to approximate the calculated ideal doping profile. The doping is the lowest near the active region, where the electric field is the highest, for maintaining reasonable optical losses. As moving toward the top contact layer, the doping increases to reduce the resistance.



(a)



(b)

Fig. 6. (a) Grading and doping. (b) Normalized electric field square and simulated hole concentration in one DBR period.

Once the average doping concentration has been determined, the doping profile within the period can be designed. Bandgap engineering was used to eliminate the heterobarriers in the valence band at the interfaces, and simultaneously maintain minimal optical losses. Fig. 6 shows our low-doped DBR design. The horizontal dash line in Fig. 6(a) is the average doping concentration obtained from Fig. 5. The dopings in GaAs and AlGaAs layers are slightly adjusted to compensate the difference in the mobility.

We can also take advantages of the standing-wave effects in VCSELs. At the standing-wave peaks, biparabolic grade and modulation doping were used to flatten the valence band [19]. No excess holes are produced with this scheme so that the optical loss is minimized. On the other hand, uniparabolic scheme was used at the standing-wave nulls [20]. The abrupt change of the slope of the composition at 150 nm creates an accumulation of holes, which improves the resistance without adding extra optical loss.

B. Oxide Aperture

Tapered oxide apertures, which have been demonstrated to have low optical scattering losses [6], are used in our devices for electrical and optical confinement. The thickness of the

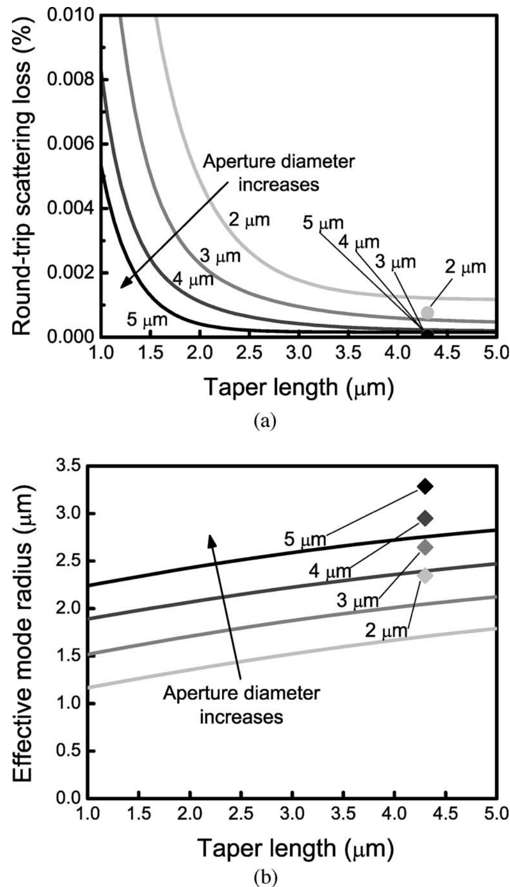


Fig. 7. (a) Round-trip optical scattering loss and (b) effective mode radius versus taper length for different device sizes, ranging from 2 to 5 μm in diameter. These curves were calculated assuming that the effective indexes in the unoxidized and fully oxidized sections are 3.254 and 3.113, respectively. The simulated results are superimposed for the original taper aperture, plotted as circles (scattering loss) in (a) and diamonds (effective mode radius) in (b).

aperture was increased from the standard quarter-wavelength-thick to half-wavelength-thick for lowering the chip parasitic capacitance.

As discussed earlier, the mode volume has to be reduced to efficiently achieve high-speed operation. However, there is a tradeoff between the optical scattering loss and mode confinement. Blunter taper provides better mode confinement and also creates more loss. In order to find the optimal design, simulations based on the model given in [6] were performed and the results are plotted in Fig. 7 [21].

Fig. 7(a) shows the simulated round-trip optical scattering loss for different taper lengths and the aperture diameters of interest, ranging from 2 to 5 μm. As expected, the optical scattering loss increases rapidly as the taper length goes below the critical length L_{c}, which is smaller for larger diameter devices. Taper length of 4 μm was conservatively chosen so that the scattering losses for all the devices are still within the flat region. The circles in the figure are the simulated results for our original aperture, which has a quarter-wavelength thickness and 4.3 μm taper length. The original aperture was optimized for low optical scattering loss and has experimentally demonstrated negligible optical scattering loss down to 1.5-μm-diameter devices. As can

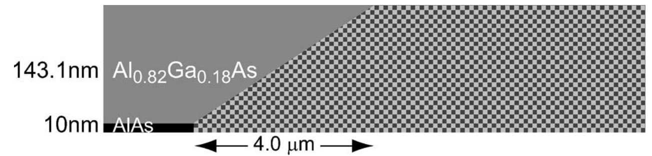


Fig. 8. Tapered oxide aperture design in our devices.

be seen, the optical scattering loss does not increase considerably from our original aperture design.

On the other hand, the mode confinement does improve greatly compared with the original aperture. Fig. 7(b) plots the corresponding effective mode radius, which is defined as the $1/e^2$ radius for an equivalent Gaussian mode with the same total power and peak amplitude. The diamonds in the figure are the results of our original aperture. Take 3 μm devices as an example, the effective mode radius reduced from 2.64 to 2.01 μm. This corresponds to a 1.73 times mode volume reduction and a 31% increase in D-factor.

Fig. 8 shows our aperture design, which consists of a 10-nm pure AlAs layer and a 143.1-nm $Al_{0.82}Ga_{0.18}As$ layer. This design gives a taper length of ~4 μm.

C. Deep Oxidation Layers

Due to the alternating layers in the DBRs, VCSELs inherently have higher series resistances, and if no precaution is taken, the bandwidth is likely to be parasitic-limited. One approach to relieve the parasitic limitation is to reduce the capacitance, specifically C_{mesa}. However, the thicknesses of the oxide aperture and the intrinsic semiconductor below the oxide are restricted by the cavity design and cannot be increased easily. In order to lower C_{mesa}, additional thick nonconducting layers have to be created inside the mesa, and this is commonly done using proton implantation. For bottom-emitting VCSELs with semiconductor top mirror, energy of several hundreds electronvolts is needed for the protons to reach the active region. This, in turn, requires fairly thick masking layers to block these high-energy protons, which inevitably complicates the fabrication process and increases the costs.

Another approach to form the nonconducting layers is to use oxidation. One example is to use double oxide apertures [22], which have different optical waveguiding than the single aperture and need to be considered. We proposed the deep oxidation layers [23], which can be formed simultaneously with the oxide aperture. By increasing the Al fraction of the AlGaAs layers for the first several DBR periods in the top mirror, these layers will penetrate further during oxidation, as shown in Fig. 9. These deeply oxidized layers effectively increase the equivalent capacitor thickness, and thus, reduce the capacitance.

There are several advantages with this approach. First, it is simple and can be easily incorporated into any oxide-confined VCSEL with a semiconductor top mirror. Second, no process modification is required. Third, the index contrast in the unoxidized region where optical modes exist also increases due to these higher Al content layers, which improves the longitudinal mode confinement. Fourth, compared with proton implantation,

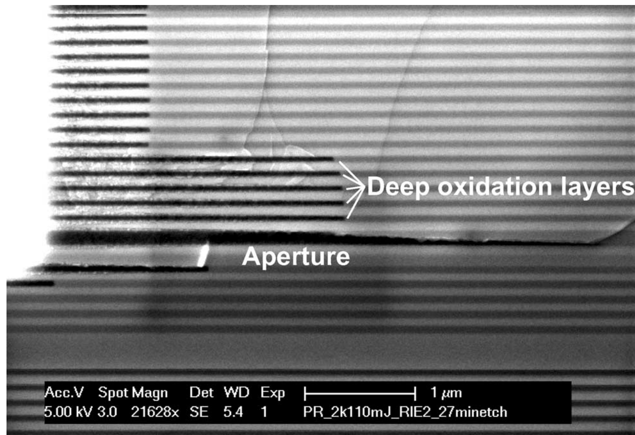


Fig. 9. Cross-sectional SEM showing five deep oxidation layers and the oxide aperture.

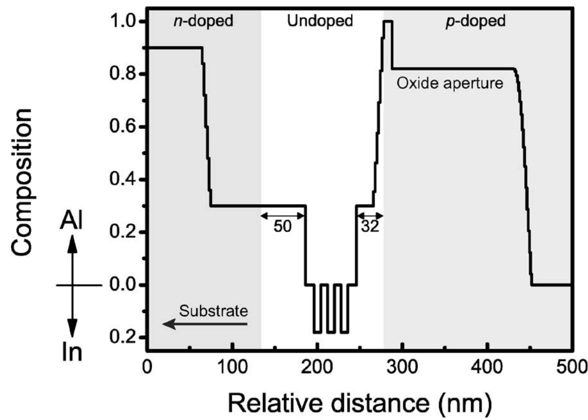


Fig. 10. Cavity structure of our devices.

this approach requires thinner nonconducting layers to achieve the same C_{mesa} due to the smaller dielectric constant of the oxide than the semiconductor. This is favorable in consideration of the resistance because of the distance that the current has to funnel is reduced.

In order not to perturb the optical modes, the length of the deep oxidation layers was conservatively chosen to be 5 μm, which can be achieved with $Al_{0.93}Ga_{0.07}As$ layers in our device structure. Five deep oxidation layers were incorporated in our devices.

D. Cavity

Fig. 10 shows the cavity design of our devices. The active region is sandwiched by two $Al_{0.3}Ga_{0.7}As$ SCH layers. The thickness of the bottom SCH is 111 nm, and the n-doping ($\sim 2 \times 10^{17}$ cm^{-3}) is set back 50 nm to minimize the carrier transport effects [24] and maintain a reasonable loss. The top SCH layer has a thickness of 20 nm and is undoped to reduce the current spreading underneath the oxide aperture [25]. However, the layers that form the oxide aperture are doped p-type at $\sim 6 \times 10^{17}$ cm^{-3} to reduce the resistance from the apertured area.

IV. Device Fabrication

The sample was grown on a semi-insulating GaAs (1 0 0) substrate by molecular beam epitaxy. The fabrication flow is shown in Fig. 11. The fabrication began by etching cylindrical mesas ranging from 21 to 30 μm in diameter to expose the n-GaAs contact layer using reactive ion etch. The oxide apertures were then formed by wet oxidation, resulting in a $\sim$9 μm oxide aperture with $\sim$4 μm taper length. The deep oxidation layers were also formed at the same time. Ti/Pt/Au and AuGe/Ni/Au were evaporated for the p- and n-contacts, respectively. The part of the n-GaAs contact layer (ground) that lies beneath the p-pad (signal) is removed to reduce the pad capacitance. BCB, sandwiched between silicon nitride, was patterned and fully cured. Then, vias were opened to expose the contacts, followed by depositing Ti/Au as pad metal. The signal pad is only 40×70 μm^2 for low capacitance. Finally, antireflection coating was applied to reduce backside reflection. Fig. 12 shows a top-view SEM of the fabricated device.

V. Device Results

A. L–I–V–P Curves

Fig. 13 plots the voltage, output power, and power dissipation against current (L–I–V–P) curves for the 3-μm-diameter device. The device has a slope efficiency of 0.67 W/A, corresponding to a differential quantum efficiency (DQE) of 54%. The threshold current is only 0.144 mA, comparatively low for typical high-speed VCSELs, which have diameters from 5 to 8 μm. The low threshold current along with high slope efficiency indicates that the internal loss in our devices is low. This means that our tapered oxide aperture does not introduce excess optical scattering losses even down to 3-μm-diameter devices.

The threshold voltage, a good measure of the excess voltage drop from the heterobarriers of the DBRs, is 1.47 V. It is very low for such a small device, only 220 meV larger than the photon energy. This low threshold voltage is the consequence of our optimized p-doping scheme as well as the low threshold current. The series resistance is approximately 250 Ω at 4.4 mA. The series resistance is relatively high due to the deep oxidation layers that restrict the current conducting area. The thermal impedance is 3.3 °C/mW. At a bias current of 4.4 mA, the power dissipation and temperature rise are 10 mW and 33 °C, respectively. This device has a peak wall-plug efficiency of 31% at 1 mA and a maximum output power of 3.1 mW at a bias current of 7 mA.

Fig. 14 plots the threshold current and DQE versus the stage temperature for another 3 μm device that has a slightly lower DQE at 20 °C. Even though the gain-cavity offset in our devices was not optimized for high-temperature operation [26], they perform relatively well at elevated temperatures. The threshold current increases from 0.13 mA at 20 °C to 0.34 mA at 110 °C, corresponding to a 2.6 times increase. The DQE decreases from 50% at 20 °C to 38% at 110 °C, corresponding to a 25% reduction.

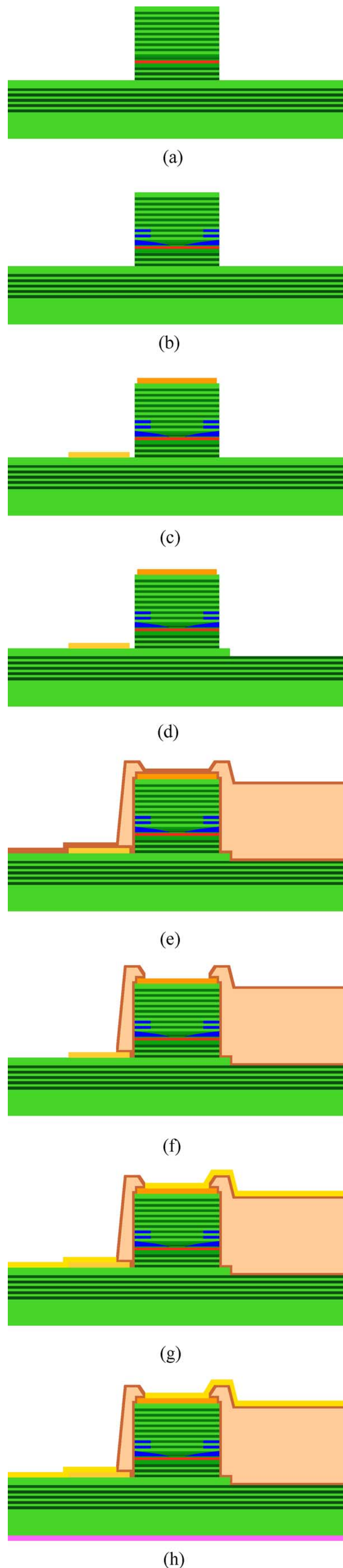


Fig. 11. Process flow. (a) Mesa etch. (b) Oxidation. (c) p- and n-metal deposition. (d) n-contact layer removal. (e) BCB pattern. (f) Via open. (g) Pad metal deposition. (h) Antireflection coating.

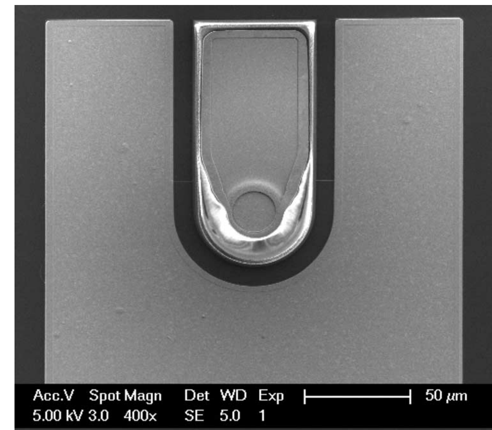


Fig. 12. Top-view SEM of the fabricated device.

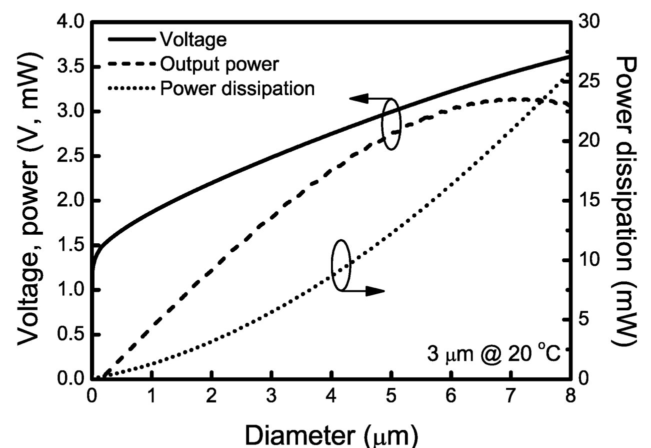


Fig. 13. L–I–V–P curves for 3 μm devices at 20 °C.

B. Spectrum

Fig. 15(a) shows the spectra for the 3-μm device at different bias currents. The device lases multimode, side-mode suppression ratio (SMSR) <30 dB, except for the lowest bias current at 1 mA. To see how the distribution of power between modes evolves as the current increases, Fig. 15(b) plots the intensities of the fundamental and second-order modes as a function of the bias current. The intensity of the fundamental mode increases quickly for the current smaller than 0.5 mA and then slowly saturates. On the other hand, the second-order mode increases rapidly as the current increases from 1.4 to 2 mA. Single-mode operation is maintained only below 1.4 mA, and the device practically operates with two modes in the bias condition of interest. Consequently, the photon density of the fundamental mode does not scale with current after 1.5 mA, when the second-order mode begins to consume a significant fraction of the additional current. This results in a reduction in the obtainable relaxation resonance frequency, as will be discussed in the next section.

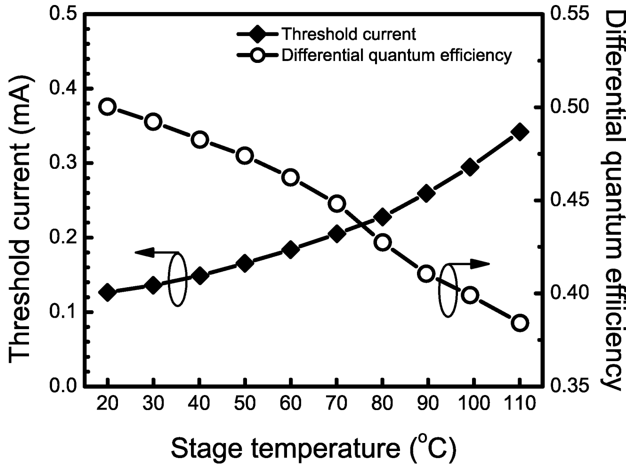
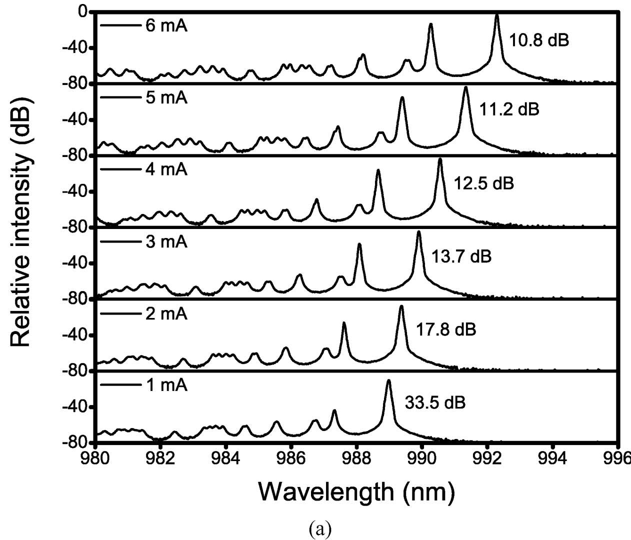
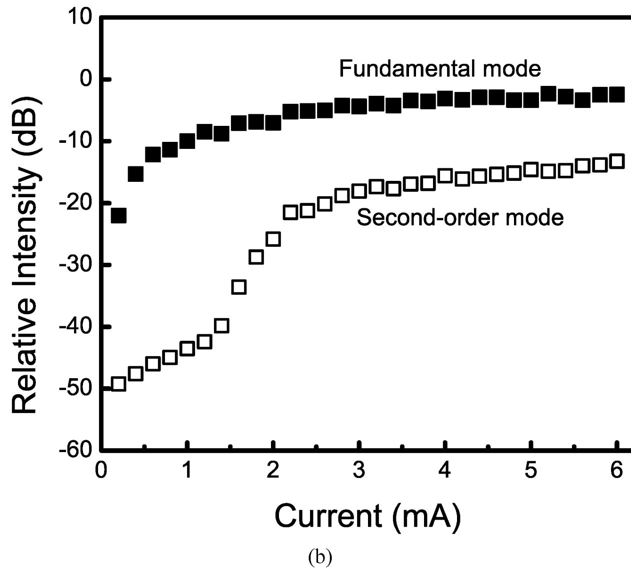


Fig. 14. Threshold current and DQE versus stage temperature for 3-μm-diameter devices.

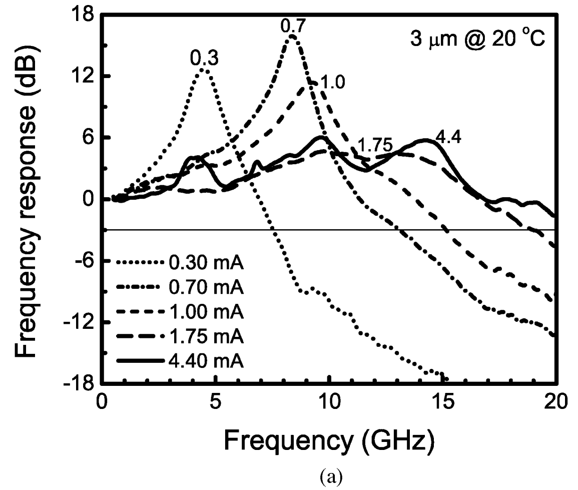


(a)

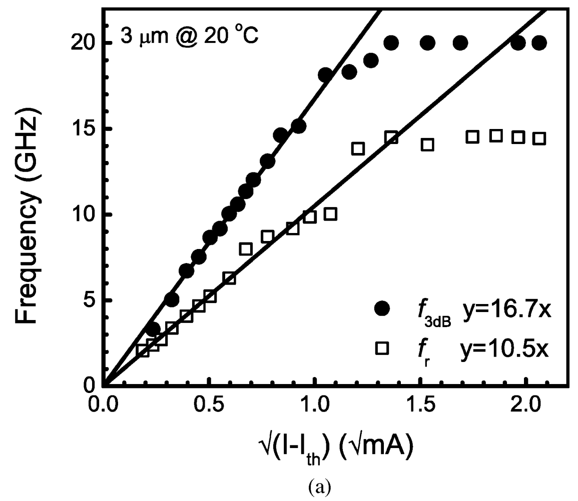


(b)

Fig. 15. (a) Spectra with the corresponding SMSR labeled for 3 μm device at different bias currents. (b) Intensities for the fundamental and second-order modes versus bias current.



(a)



(a)

Fig. 16. (a) Normalized electrical frequency responses at different bias currents for 3-μm-diameter device. (b) Relaxation resonance frequency (f_r), determined from relative intensity noise measurements, and 3-dB frequency ($f_{3\,\mathrm{dB}}$) versus $(I - I_{\mathrm{th}})^{1/2}$.

C. Small-Signal Modulation Bandwidth

Fig. 16(a) plots the small-signal modulation responses for the 3 μm device at different bias currents. To ensure that the device was actually operated with small-signal modulation, the input RF power was chosen to be -40 dBm.

As shown in the figure, bandwidth of 15 GHz, which should enable 20 Gb/s operation, is achieved with a bias current of 1 mA. The corresponding power consumption and dissipation are only 1.87 and 1.29 mW, respectively. The estimated temperature rise at this bias current is less than 5 °C and should have negligible thermal impacts on the device performance. Bandwidth exceeding 20 GHz has also been demonstrated for currents larger than 2 mA. Although this is the record bandwidth for 980 nm VCSELs to date, the high-current data clearly show a saturation effect that accompanies the buildup of power in higher order modes as the total photon density spreads from the fundamental mode to these higher order modes. Simple small-signal modeling fitted only to the lower current data indicates bandwidths in excess of 25 GHz if the higher order modes are

not allowed. The ripples in the Fig. 16(a) higher current data are believed to be due to multimode effects, because they were not significant at lower currents, but it is also possible that some optical reflections still remain in the test system.

Fig. 16(b) plots the relaxation resonance frequency and 3-dB frequency versus the square root of the current above threshold. The extracted D-factor is 10.5 GHz/mA$^{1/2}$, higher than typical high-speed VCSELs. This is because our tapered oxide aperture effectively confines the mode laterally. The MCEF is 16.7 GHz/mA$^{1/2}$, which is very close to the highest reported value of 16.8 GHz/mA$^{1/2}$ for QW-based VCSELs [27]. The ratio of the slopes of $f_{3\,\mathrm{dB}}$ to f_{r} is 1.59, close to the theoretical value of 1.55, indicating that the damping is not severe in our devices at low bias currents. This has also been revealed in Fig. 16(a), as the resonance peaks are quite strong.

Since our devices were not optimized for high-temperature operation, the threshold current increases, and the injection efficiency and differential gain decrease at elevated temperatures. However, according to the static performance shown in Fig. 14, we expect that our devices would not degrade significantly up to the commonly specified 85 °C.

D. Impedance

To understand how the parasitics affect the high-speed performance of our devices, the values of the parasitic elements need to be determined. This is commonly done by curve-fitting the measured S_{11} data to the small-signal model, as shown in Fig. 3. It should be noted that to reduce the number of the fitting parameters, this model was simplified by assuming that the resistances between the oxide aperture layer and the deep oxidation layers are relatively small compared with R_{j} so that all the capacitances in the mesa can be grouped together into C_{m}.

In the small-signal model, C_{p} and R_{m} are assumed to be bias-independent, which neglects the heating effects, and C_{m} and R_{j} are assumed to be bias-dependent. The following procedure was used to do the fitting. First, all the parasitic elements are allowed to vary for each bias current, and the estimated ranges of C_{p} and R_{m} can be obtained. Then, C_{p} and R_{m} are determined so that they give the best overall fitting for all the currents. Finally, C_{m} and R_{j} can be obtained using the fitted C_{p} and R_{m}.

For the 3-μm device, the fitted C_{p} and R_{m} are 29 fF and 103 Ω, respectively. Table II lists the extracted C_{m} and R_{j} and the calculated parasitic 3-dB frequency f_{rc} for different bias currents. C_{m} increases with current due to the increased diffusion capacitance and R_{j} decreases as current increases. Due to the small size of our device, R_j and R_m are inherently larger than typical high-speed VCSELs that have larger device sizes. To compensate this, the capacitive elements in our devices were minimized so that most of the modulation current can enter the intrinsic laser. By removing the n-contact layer, inserting BCB, and reducing the pad dimension, C_{p} was greatly reduced. With the incorporation of the deep oxidation layers and thicker oxide aperture, C_{m} is also relatively small.

To understand how these two features reduce C_{m}, a simple calculation based on the schematic shown in Fig. 17 was performed. Assume that the dielectric constants of the oxide and semiconductor are 4 and 12.2 [28], respectively. For the region of $10.5 \geq r > 5.5$ μm, the capacitance C_1 is C_{dox} (from the deep oxidation layers), C_{ox1}, and C_{int1} connected in series. Using the parallel-plate capacitance approximation, C_{dox}, C_{ox1}, and C_{int1} are calculated to be 29.7, 63.5, and 208.7 fF, respectively. For the region of $5.5 \geq r > 1.5$ μm, the capacitance C_2 is calculated to be 46.4 fF.

TABLE II
EXTRACTED C_{m} AND R_{j} AND CALCULATED PARASITIC 3-dB Frequency f_{rc} for 3 μm Device at Different Bias Currents

Current (mA)	1.0	2.0	3.0	4.5	6.0
R_{j} (Ω)	274.4	192.7	168.2	146.5	126.7
C_{m} (fF)	57.1	66.7	75.4	87.9	100.0
f_{rc} (GHz)	27.0	25.9	24.6	22.8	21.8

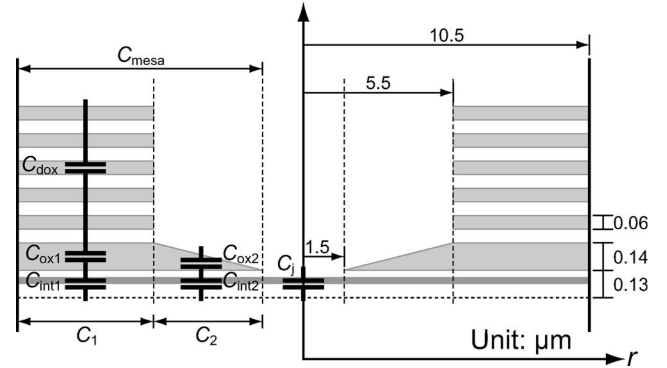


Fig. 17. Various components for C_{mesa} in our devices. The lengths are labeled for 3-μm-diameter devices.

By increasing the aperture thickness from quarter-wavelength to half-wavelength with the same taper length, we were able to reduce C_{mesa} from 118.3 to 76.8 fF. Assuming that everything else remains unchanged, this corresponds to an increase of f_{rc} from 12.9 to 17.3 GHz, a 34% increase. The inclusion of the deep oxidation layers further lowers C_{mesa} from 76.8 to 46.4 fF, corresponding to an increase of f_{rc} from 17.3 to 22.8 GHz. By implementing a thicker oxide aperture as well as the deep oxidation layers, we were able to greatly reduce the chip parasitic capacitance. However, our devices are still partially limited by the parasitics as f_{rc} is in the range of 22–27 GHz.

In order to further reduce the chip parasitic capacitance, C_{j} has to be lowered. For typical edge emitters that are usually operated at tens of milliamperes, R_{j} is very small and C_{j} is negligible. However, for VCSELs that require less current to operate, C_{j} cannot be neglected. Fig. 18 plots the extracted C_{m} as a function of the bias current. All the data fit in a line. Similar trend has also been found in the literature [29] and can be explained using the following simple argument:

$$C \equiv \frac{dQ}{dV} = \frac{di\,\Delta t}{dv} = \frac{di\,\Delta t}{di(V_{\mathrm{T}}/I_{\mathrm{bias}})} \propto I_{\mathrm{bias}} \qquad (6)$$

where di and dv are the small-signal modulation current and voltage, respectively, and V_{T} is the thermal voltage ∼26 meV at room temperature. Here, we have assumed ideal diode equation for the relation between di and dv.

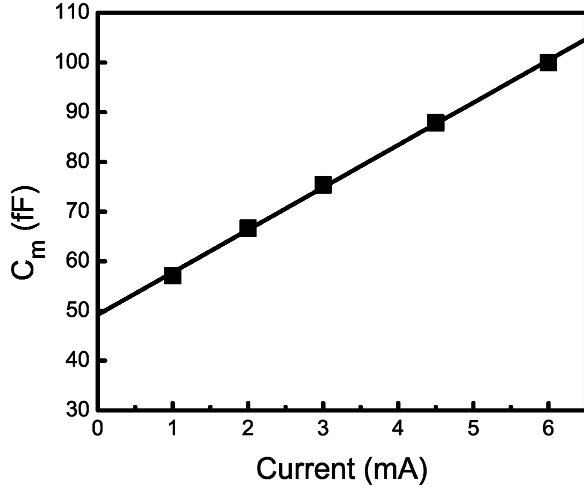


Fig. 18. Extracted C_{m} versus the bias current for 3 μm device.

For the bias current of 4.5 mA, which is close to the condition for the large-signal modulation experiments, a considerable portion of C_{m} comes from C_{j}. Therefore, carefully designing the SCH region is needed to lower the parasitics.

E. Bit Error Rate and Eye Diagram

Fig. 19 shows the test setup for large-signal modulation experiments. The nonreturn-to-zero (NRZ) signal with $2^7 - 1$ word length from the pattern generator (SHF 12100A) was amplified using a 38-GHz SHF 806E amplifier with 26 dB gain, and then attenuated 6 dB using a fixed attenuator to reduce the voltage swing to ~0.84 $V_{\mathrm{p\text{-}p}}$. The RF signal was combined with the dc bias through a 65-GHz Anritsu V255 bias tee and fed to the device using a 67-GHz ground-signal-ground RF probe. The output power was collected into a 1-m standard 9/125 fiber attached with a dual-lens focuser. Standard telecom 9/125 fiber was used for equipment compatibility. The eye diagram was measured using an Agilent 86109A oscilloscope with an internal 30 GHz photodiode. To measure the bit error rate (BER), the optical signal was attenuated using a variable optical attenuator (VOA) and then fed to a 25-GHz New Focus 1414 photodiode coupled with a 40-GHz SHF 810 amplifier and finally sent to the error analyzer (SHF 11100A). The coupling efficiency under the BER testing was approximately 27%, estimated by the photocurrent from the photodiode and the L–I curve.

Fig. 20 shows the BER curve at 35 Gb/s for the 3 μm device. The bias current was 4.4 mA. The inset of the figure shows the optical eye diagram at 35 Gb/s and the eye is clearly open with an extinction ratio of 5.4 dB. In the BER curve, all the data points except the lowest one were taken with a VOA. Due to the ~3 dB insertion loss of the VOA, the BER in the range of 10^{-11} and 10^{-7} could not be measured. Thus, the lowest data point at a received power of -4.7 dBm was taken without the VOA. At a bias current of 4.4 mA, the power consumption and dissipation, excluding the RF driver circuitry, are only 12.5 and 10 mW, respectively. This corresponds to a data rate/power dissipation ratio of 3.5 Gb/(s·mW).

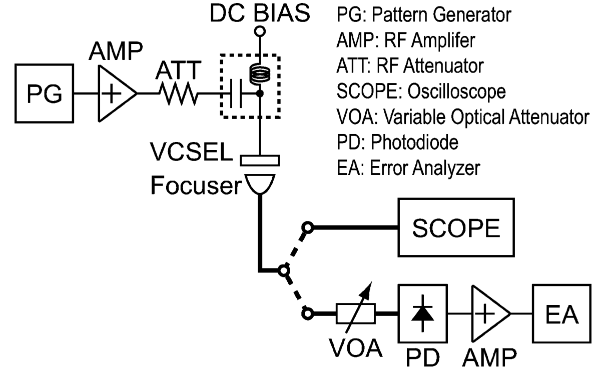


Fig. 19. Experiment setup for BER and eye diagram.

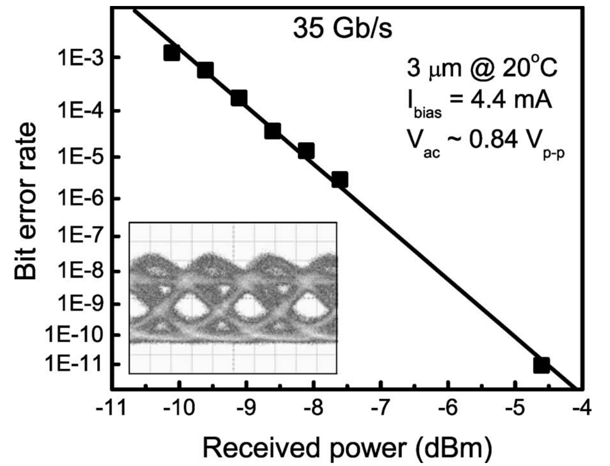


Fig. 20. Bit error curve at 35 Gb/s for 3-μm-diameter device. The device was biased at 4.4 mA and a RF voltage swing of 0.84 $V_{\mathrm{p\text{-}p}}$ was used. The inset shows the corresponding optical eye diagram with an extinction ratio of 5.4 dB.

One concern with small devices is the high current density that can cause reliability problems. At 4.4 mA where the BER testing was performed, the current density, $J = I/\text{area}$, is indeed quite high at over 60 kA/cm^2. The rationale to, or trying to, go with small devices is that ideally, the relaxation resonance frequency should be independent of the size of the device. This can be seen if we rewrite (2) as

$$\omega_{\mathrm{r}} = \left[\frac{\Gamma v_{\mathrm{g}} a}{q L_{\mathrm{a}} A}\eta_{\mathrm{i}} A(J - J_{\mathrm{th}})\right]^{1/2} = \left[\frac{\Gamma v_{\mathrm{g}} a}{q L_{\mathrm{a}}}\eta_{\mathrm{i}}(J - J_{\mathrm{th}})\right]^{1/2}$$

where A is the apertured area, L_{a} is the total thickness of the QWs, and $J_{\mathrm{th}} = I_{\mathrm{th}}/A$. Here, we have assumed that the confinement factor Γ is size-independent. Moreover, small devices require less power to operate. As shown earlier, our 3 μm devices can achieve a 15-GHz bandwidth at 1 mA, corresponding to a current density of 14 kA/cm^2. Further optimization of the devices and testing setup may bring the current density of 60 kA/cm^2 down to a more reasonable value.

VI. Conclusion

High-efficiency, high-speed, oxide-confined 980 nm VCSELs are demonstrated. We first considered the factors that determine the bandwidth and tried to address them in our device design. To

improve the intrinsic laser response, an optimized tapered oxide aperture was used for better mode confinement and higher photon density. The parasitic limitations were lowered by using the deep oxidation layers, thicker oxide apertures, and reducing the pad capacitance. These designs enabled us to use smaller 3 μm devices, which have a threshold current of 0.14 mA. In addition, our devices achieved >20 GHz bandwidth for current >2 mA and 35 Gb/s operation at only 10 mW power dissipation, corresponding to a data rate/power dissipation ratio of 3.5 Gb/(s·mW). By analyzing the results, we also pointed out some potential improvements such as single modeness and the reduction of the junction capacitance.

Acknowledgment

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References

[1] N. Suzuki, H. Hatakeyama, K. Fukatsu, T. Anan, K. Yashiki, and M. Tsuji, "25-Gbps operation of 1.1-μm-range InGaAs VCSELs for high-speed optical interconnections," presented at the Opt. Fiber Commun. Conf., Anaheim, CA, Mar. 5–10, 2006, Paper OFA4.

[2] K. Yashiki, N. Suzuki, K. Fukatsu, T. Anan, H. Hatakeyama, and M. Tsuji, "1.1-μm-range tunnel junction VCSELs with 27-GHz relaxation oscillation frequency," presented at the Opt. Fiber Commun. Conf., Anaheim, CA, Mar. 25–29, 2007, pp. 1–3, Paper OMK1.

[3] Y.-C. Chang, C. S. Wang, and L. A. Coldren, "High-efficiency, high-speed VCSELs with 35 Gbit/s error-free operation," *Electron. Lett.*, vol. 43, no. 19, pp. 1022–1023, 2007.

[4] T. Anan, N. Suzuki, K. Yashiki, K. Fukatsu, H. Hatakeyama, T. Akagawa, K. Tokutome, and M. Tsuji, "High-speed InGaAs VCSELs for optical interconnects," presented at the Int. Symp. VCSELs Integr. Photon., Tokyo, Japan, 2007, Paper. E3.

[5] R. H. Johnson and D. M. Kuchta, "30 Gb/s directly modulated 850 nm datacom VCSELs," presented at the Conf. Lasers Electro-Opt., San Jose, CA, 2008, Paper. CPDB2.

[6] E. R. Hegblom, D. I. Babic, B. J. Thibeault, and L. A. Coldren, "Scattering losses from dielectric apertures in vertical-cavity lasers," *IEEE J. Sel. Topics Quantum Electron.*, vol. 3, no. 2, pp. 379–389, Apr. 1997.

[7] R. S. Tucker, "High-speed modulation of semiconductor lasers," *J. Lightw. Technol.*, vol. LT-3, no. 6, pp. 1180–1192, Dec. 1985.

[8] L. A. Coldren and S. W. Corzine, *Diode Lasers and Photonic Integrated Circuits*. New York: Wiley, 1995.

[9] Y. Arakawa and A. Yariv, "Quantum well lasers–gain, spectra, dynamics," *IEEE J. Quantum Electron.*, vol. QE-22, no. 9, pp. 1887–1899, Sep. 1986.

[10] I. Suemune, "Theoretical study of differential gain in strained quantum well structures," *IEEE J. Quantum Electron.*, vol. 27, no. 5, pp. 1149–1159, May 1991.

[11] J. D. Ralston, S. Weisser, I. Esquivias, E. C. Larkins, J. Rosenzweig, P. J. Tasker, and J. Fleissner, "Control of differential gain, nonlinear gain and damping factor for high-speed application of GaAs-based MQW lasers," *IEEE J. Quantum Electron.*, vol. 29, no. 6, pp. 1648–1659, Jun. 1993.

[12] P. O. Leisher, C. Chen, J. D. Sulkin, M. S. B. Alias, K. A. M. Sharif, and K. D. Choquette, "High modulation bandwidth implant-confined photonic crystal vertical-cavity surface-emitting lasers," *IEEE Photon. Technol. Lett.*, vol. 19, no. 19, pp. 1541–1543, Oct. 2007.

[13] D. Tauber, G. Wang, R. S. Geels, J. E. Bowers, and L. A. Coldren, "Large and small signal dynamics of vertical cavity surface emitting lasers," *Appl. Phys. Lett.*, vol. 62, no. 4, pp. 325–327, 1993.

[14] Y. Liu, W.-C. Ng, F. Oyafuso, B. Klein, and K. Hess, "Simulating the modulation response of VCSELs: The effects of diffusion capacitance and spatial hole-burning," *Inst. Electr. Eng. Proc. Optoelectron.*, vol. 149, no. 4, pp. 182–188, Aug. 2002.

[15] J. Strologas and K. Hess, "Diffusion capacitance and laser diodes," *IEEE Trans. Electron Devices*, vol. 51, no. 3, pp. 506–509, Mar. 2004.

[16] K. Y. Lau and A. Yariv, "Ultra-high speed semiconductor lasers," *IEEE J. Quantum Electron.*, vol. QE-21, no. 2, pp. 121–138, Feb. 1985.

[17] D. A. Louderback, O. Sjölund, E. R. Hegblom, J. Ko, and L. A. Coldren, "Flip-chip bonded arrays of monolithically integrated, microlensed vertical-cavity lasers and resonant photodetectors," *IEEE Photon. Technol. Lett.*, vol. 11, no. 3, pp. 304–306, Mar. 1999.

[18] E. R. Hegblom, "Engineering oxide apertures in vertical cavity lasers," Ph.D. dissertation, Univ. California, Santa Barbara, CA, Mar. 1999.

[19] M. G. Peters, B. J. Thibeault, D. B. Young, J. W. Scott, F. H. Peters, A. C. Gossard, and L. A. Coldren, "Band-gap engineered digital alloy interfaces for lower resistance vertical-cavity surface-emitting lasers," *Appl. Phys. Lett.*, vol. 63, no. 25, pp. 3411–3413, 1993.

[20] K. L. Lear and R. P. Schneider, Jr., "Uniparabolic mirror grading for vertical cavity surface emitting lasers," *Appl. Phys. Lett.*, vol. 68, no. 5, pp. 605–607, 1996.

[21] Y.-C. Chang and L. A. Coldren, "Optimization of VCSEL structure for high-speed operation," in *Proc. IEEE 20th Int. Semicond. Laser Conf., 2006. Conf. Dig. 2008*, Sorrento, Italy, Sep. 14–18, pp. 159–160, Paper. ThA1.

[22] P. Westbergh, J. Gustavsson, A. Haglund, H. Sunnerud, and A. Larsson, "Large aperture 850 nm VCSELs operating at bit rates up to 25 Gbit/s," *Electron. Lett.*, vol. 44, no. 15, pp. 907–908, 2008.

[23] Y.-C. Chang, C. S. Wang, L. A. Johansson, and L. A. Coldren, "High-efficiency, high-speed VCSELs with deep oxidation layers," *Electron. Lett.*, vol. 42, no. 22, pp. 1281–1282, 2006.

[24] R. Nagarajan, M. Ishikawa, T. Fukushima, R. S. Geels, and J. E. Bowers, "High speed quantum-well lasers and carrier transport effects," *IEEE J. Quantum Electron.*, vol. 28, no. 10, pp. 1990–2008, Oct. 1992.

[25] E. R. Hegblom, N. M. Margalit, B. Thibeault, L. A. Coldren, and J. E. Bowers, "Current spreading in apertured vertical-cavity lasers," *Proc. IEEE*, vol. 3003, pp. 176–180, 1997.

[26] D. B. Young, J. W. Scott, F. H. Peters, M. G. Peters, M. L. Majewski, B. J. Thibeault, S. W. Corzine, and L. A. Coldren, "Enhanced performance of offset-gain high-barrier vertical-cavity surface-emitting lasers," *IEEE J. Quantum Electron.*, vol. 29, no. 6, pp. 2013–2022, Jun. 1993.

[27] K. L. Lear, A. Mar, K. D. Choquette, S. P. Kilcoyne, R. P. J. Schneider, and K. M. Geib, "High-frequency modulation of oxide confined vertical cavity surface emitting lasers," *Electron. Lett.*, vol. 32, no. 5, pp. 457–458, 1996.

[28] S. Adachi, "GaAs, AlAs, and $Al_x Ga_{1-x} As$: Material parameters for use in research and device appications," *J. Appl. Phys.*, vol. 58, no. 3, pp. R1–R29, 1985.

[29] A. N. AL-Omari and K. L. Lear, "Polyimide planarized vertical-cavity surface-emitting lasers with 17.0-GHz bandwidth," *IEEE Photon. Technol. Lett.*, vol. 16, no. 4, pp. 969–971, Apr. 2004.

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Prof. Coldren is a Fellow of the Optical Society of America (OSA) and the Institute of Electrical Engineering (IEE). He was the recipient of the 2004 John Tyndall Award. He was a member of the National Academy of Engineering. He has presented dozens of invited and plenary talks at major conferences.