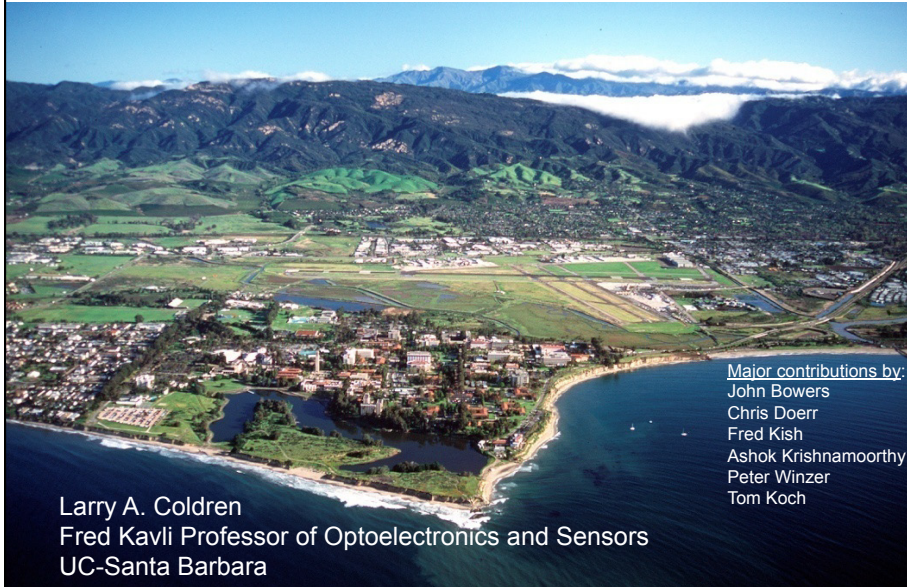




Photonic Integrated Circuits as Key Enablers for Datacom, Telecom and Sensor Systems



Larry A. Coldren
Fred Kavli Professor of Optoelectronics and Sensors
UC-Santa Barbara

Major contributions by:
John Bowers
Chris Doerr
Fred Kish
Ashok Krishnamoorthy
Peter Winzer
Tom Koch



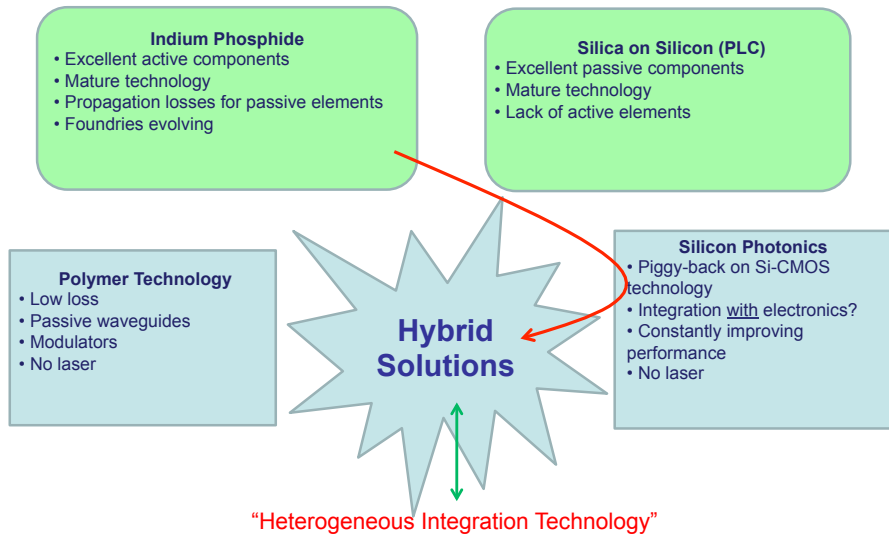
What's the problem?

CLEO 2014

Size, Weight, Power, Cost, Performance, Reliability

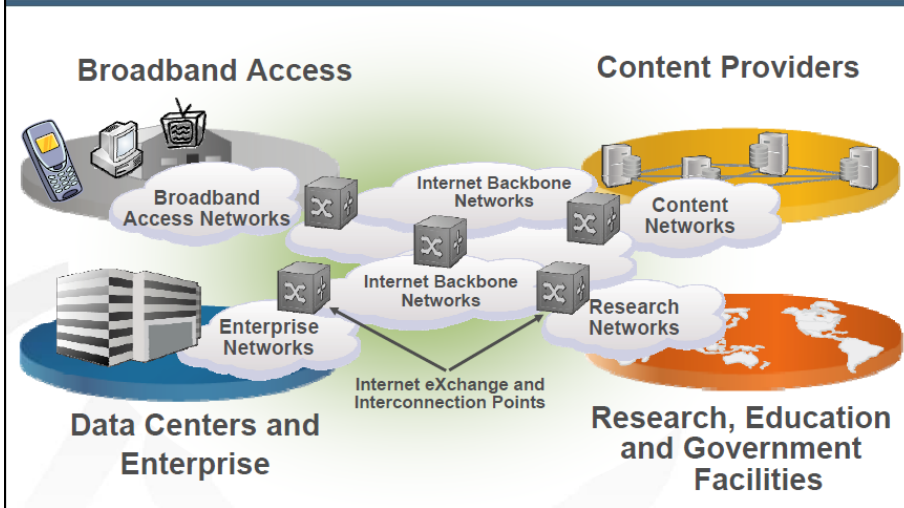
Where?

- Communication
 - Long haul
 - Metro, campus
 - Data centers, Supercomputers
- Sensing/instrumentation
- Computing



- 1970's - OEICs on GaAs for high-speed computing
- 1980's – InP photonics/fiber; integration & tunables for coherent → Reach
- 1990's – Widely-tunables, laser-mods, small-scale int. for WDM and cost
- 1990's – VCSELs for datacom and optical interconnection
- 2000 - Bubble: Explosion of strange ideas, bandwidth-demand satisfied by DWDM → crash; but bandwidth needed by 2010.
- 2000's – InP PICs & PLCs expanded and matured; increasing use of VCSELs in high-speed datacom and computing interconnects
- 2006+ – Emergence of Si-PICs with several different goals: low-cost OEICs; high-performance PICs; or stop Moore's-Law saturation
- 2008+ - Use of advanced modulation formats/coherent receivers for improved Spectral Efficiency—need for integration at both ends of links
- 2010's – Increased InP-PIC use; maturity of Si-photonics solutions; improved VCSEL performance; heterogeneous integration approaches
- 2014 -- Quandary regarding future design choices

- The Ethernet ecosystem—it's nearly all optical (fiber)
- Need higher bandwidth & performance with lower SWAP-C



- > 50 MW power requirements
- Requires many Gb/s of bandwidth—need 100Gb-Ethernet
- Need 0.1 – 3 m in rack and 1 – 2000 m interconnects between racks



Oil & Gas



Structures



Aerospace



Medical--OCT

Bragg gratings:

- Temperature
- Pressure
- Displacement / Strain
- Damage/Delamination

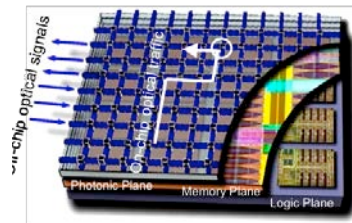
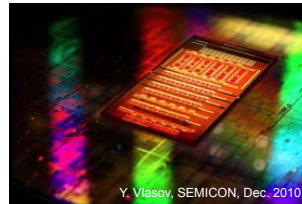
Coherent Fiber Sensing

- Distributed Acoustics
- Vibration
- Flow
- Intrusion
- Perimeter Monitoring



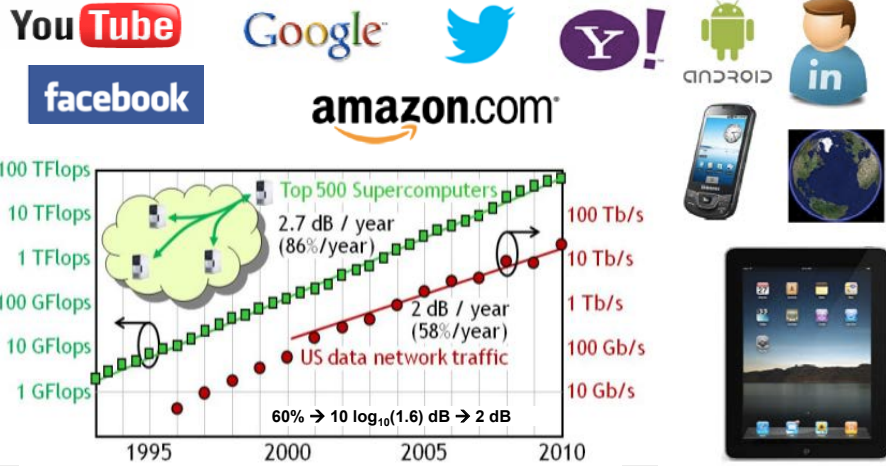
New lasers, such as all-semiconductor very high-speed swept lasers (>kHz rates), are enabling new methodologies (photo courtesy of Insight Photonic Solutions)

- A motivator for Si-Photonics
 - High bandwidth density with WDM
- Packaging is critical for total cost
 - Optical coupling to SMF?
 - WDM DFB integration and coupling?
 - Thermal management?
 - WDM reduces cost/Gb/s of connector and packaging
- Reliability?



Courtesy S. Nakagawa, IBM

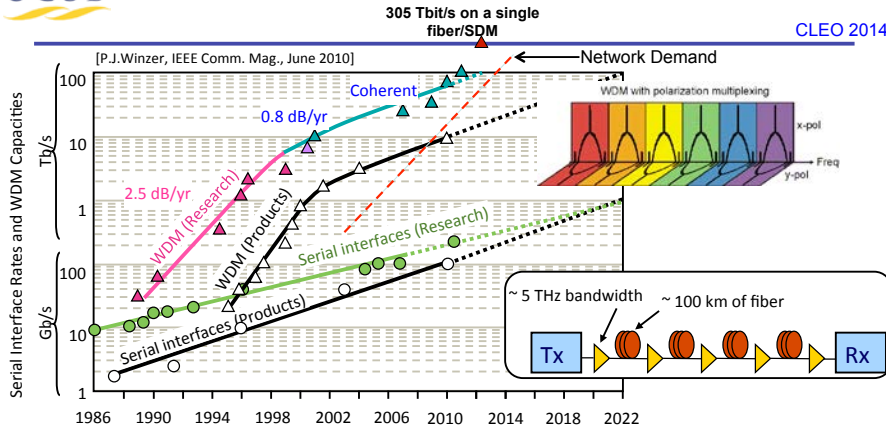
Exponential Growth of Network/Data-Center Traffic and Supercomputer Needs



Exponential network traffic growth is driven by high-bandwidth digital applications
G4, Video-on-demand, HD-TV, wireless backhaul, cloud computing & services

Courtesy P. Winzer

Scaling spectral efficiency through WDM, Coherent, ?



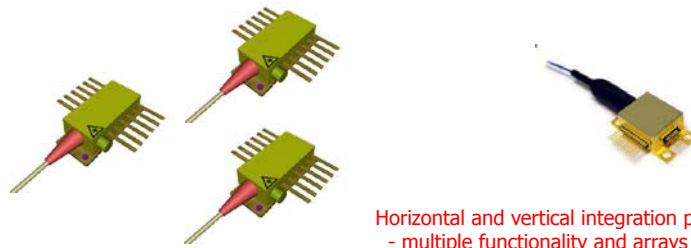
~10 Terabit/s WDM systems are now commercially available
~100+ Terabit/s WDM systems have been demonstrated in research (Coherent)

EDFA enabled WDM (wavelength division multiplexing) in 1990s

Growth of WDM system capacities has noticeably slowed down

Courtesy P. Winzer

- Reduced size, weight, power (SWAP)
- Improved performance (coupling losses, stability, etc.)
- Improved reliability (fewer pigtails, TECs, fiber alignment optics, etc...), although chip yield may not be highest
- Cost (in volume)



Horizontal and vertical integration possible
 - multiple functionality and arrays of chips in one

After C. Joyner, infirera

- **Small footprint**
 - No lenses between elements
 - Strongly confining waveguides
- **Low power**
 - Avoid 50-ohm lines (if close to electronics); only one cooler/PIC
- **Performance**
 - Cannot optimize components separately → need common design rules
 - Only one input/output coupling, but still need mode X-former or optics
 - Can usually avoid isolators on-chip, but still need at output
 - Phase delays for interference and feedback stable and small
- **Low price (need large market to realize)**
 - Fewer touch points
 - No mechanical adjustments—packaging still issue
 - Less test equipment
 - Less material



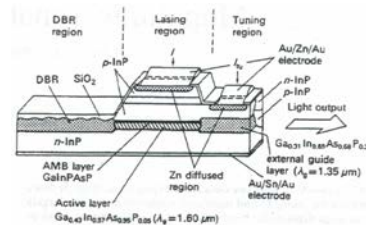
Based on C. Doerr inputs, OFC 2014, ACACIA

Partially transmissive mirrors (couplers) and active-passive integration needed

→ DBR gratings and vertical couplers

- Tunable single frequency
- Combined integration technologies

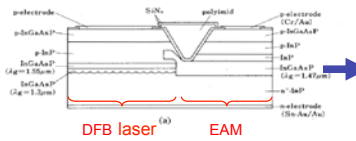
Y. Tohmori, Y. Suematsu, Y. Tushima, and S. Arai, "Wavelength tuning of GaInAsP/InP integrated laser with butt-jointed built-in DBR," *Electron. Lett.*, 19 (17) 656-7 (1983).



→ EML = electroabsorption-modulated laser

- Still in production today

M. Suzuki, et al., *J. Lightwave Technol.*, LT-5, pp. 1277-1285, 1987.



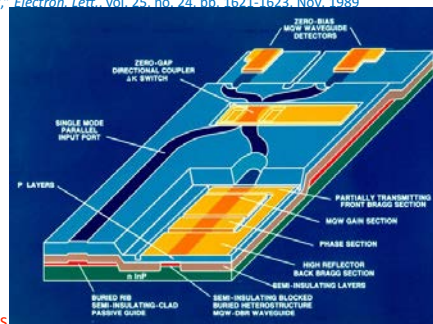
• In the 1980's coherent communication was widely investigated to increase receiver sensitivity and repeater spacing. It was also seen as a means of expanding WDM approaches because optical filters would not be so critical.

Y. Yamamoto and T. Kimura, "Coherent optical fiber transmission systems," *IEEE J. Quantum Electron.*, vol. 17, no. 6, pp. 919-925, Jun. 1981.

• This early coherent work drove early photonic integration efforts—Stability; enabled phase-locking

T. L. Koch, U. Koren, R. P. Gnall, F. S. Choa, F. Hernandez-Gil, C. A. Burrus, M. G. Young, M. Oron, and B. I. Miller, "GaInAs/GaInAsP multiple-quantum-well integrated heterodyne receiver," *Electron. Lett.*, vol. 25, no. 24, pp. 1621-1623, Nov. 1989

Integrated Coherent Receiver (Koch, et al)

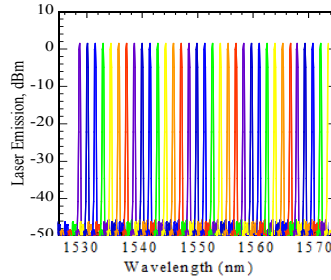
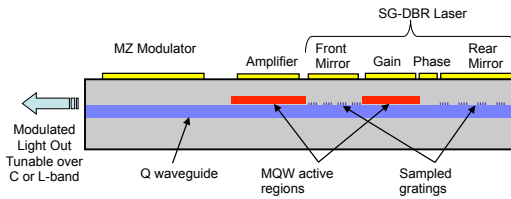


- The EDFA enabled simple WDM repeaters
- (just amplifiers) and coherent was put on the shelf
- But, some aspects of Photonic Integration continued → e.g., Tunable Lasers

SGDBR+X widely-tunable transmitter:

- Foundation of PIC work at UCSB (UCSB'90-- → Agility'99-'05 → JDSU'05→)

"Multi-Section Tunable Laser with Differing Multi-Element Mirrors," US Patent # 4,896,325 (January 1990)



- Vernier tuning over 40+nm near 1550nm
- SOA external to cavity provides power control
- Currently used in many new DWDM systems (variations)
- **Integration technology for much more complex PICs**

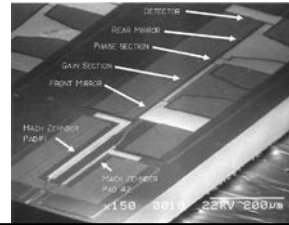
ILMZ TOSA (~ 18mm)



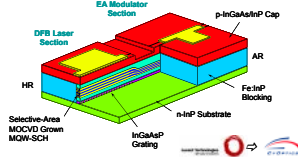
JDSU

6 section InP chip

J. S. Barton, et al., "JSLC, TuB3, Garmish, (Sept, 2002)

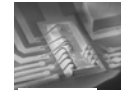
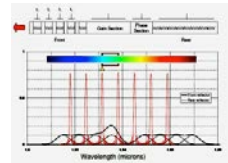
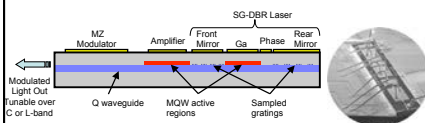


EML's:



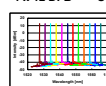
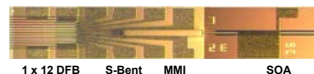
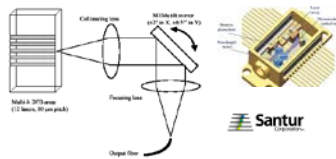
into XFP transceivers, etc.

Tunables & Selectable Arrays:



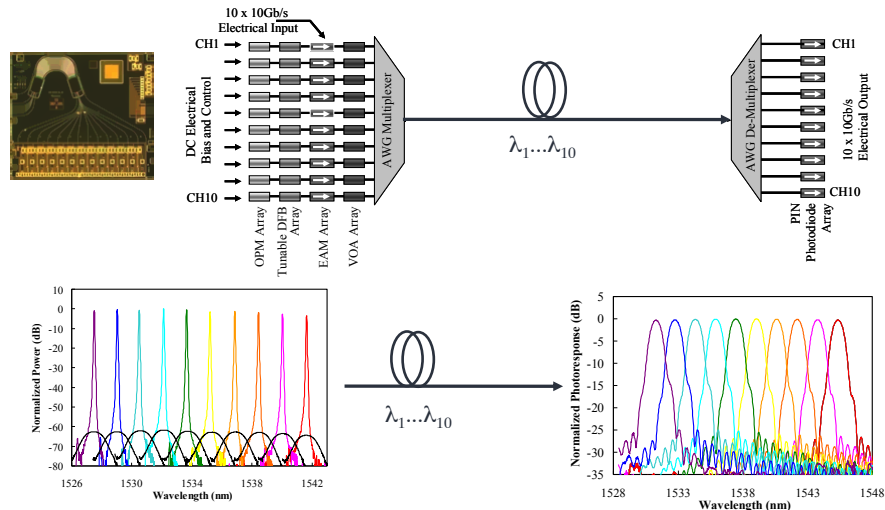
oclaro

UCSB → AGILITY → JDSU



FURUKAWA ELECTRIC

courtesy of T. Koch



courtesy of F. Kish



Binary modulation formats

(1 bit/symbol):

– Optical duobinary / PSBT

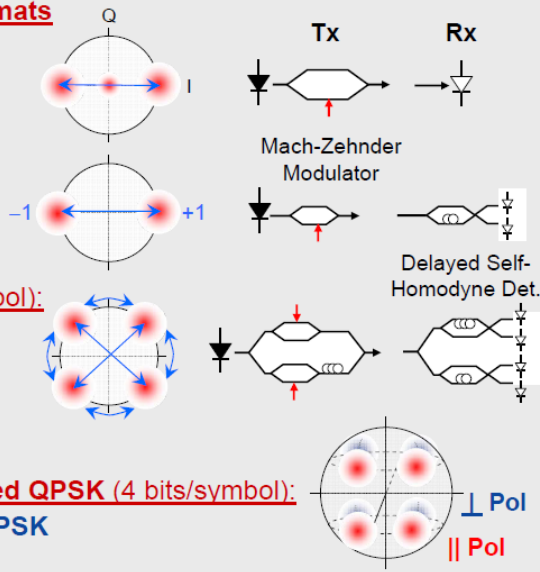
– NRZ- / RZ-DPSK (“bipolar” ASK)

Quaternary (2 bits/symbol):

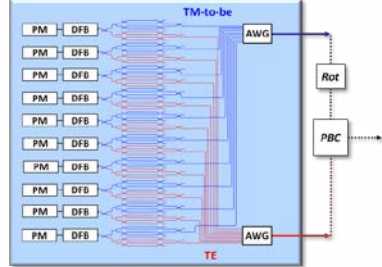
– NRZ- / RZ-DQPSK

Polarization-multiplexed QPSK (4 bits/symbol):

– Dual-Polarization QPSK



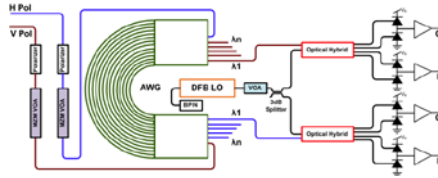
Tx PIC Architecture (5 x 114 Gb/s)



- > 450 Integrated Functions
- 8 Different Integrated Functions



Rx PIC Architecture (5x 114Gb/s)

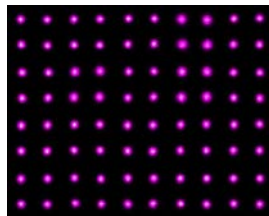


- > 150 Integrated Functions
- 7 Different Integrated Functions

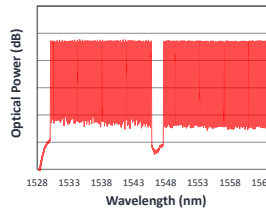
courtesy of F. Kish



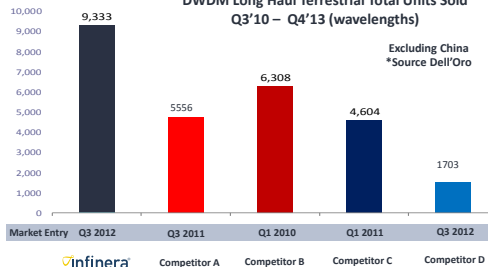
500 Gb/s Tx→Rx Contiguous Super-Channel



500Gb/s PIC-based Transport / Switching System



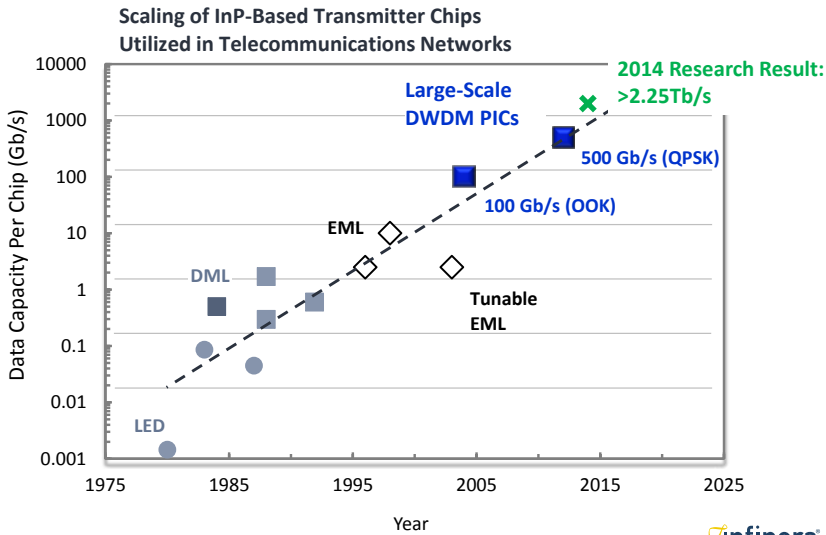
DWDM Long Haul Terrestrial Total Units Sold Q3'10 – Q4'13 (wavelengths)



Infinera has 25% of all 100G LH ports ever sold since 3Q-10 (31% excluding China)

courtesy of F. Kish

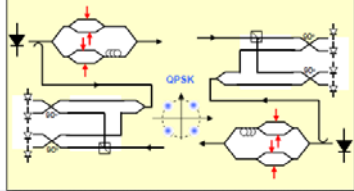




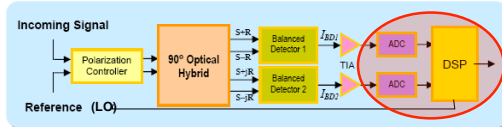
courtesy of F. Kish

Intradyne Coherent Detection

- Phase and polarization diversity
- Frequency-locked local oscillator
- Digital signal processing of received electrical signals
 - Electronic CD compensation
 - Electronic polarization demultiplex
 - Adaptive PMD compensation

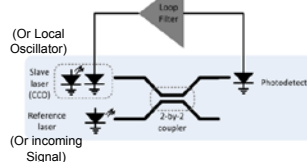


Typical Intradyne receiver architecture



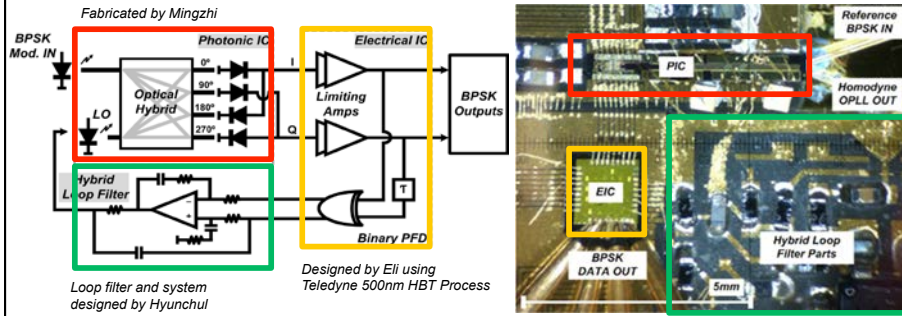
But for short-modest reach:

Homodyne receiver architecture



- Use Phase-locked Homodyne detection instead of power-hungry and costly Intradyne?
 - Integrated Costa's loop homodyne receivers with widely-tunable LOs have been explored
 - High-speed A/Ds & DSPs require lots of power and are expensive to design, especially as data rate increases
 - Short feedback loops narrow LO linewidth and enable rapid and robust phase locking.
 - Some impairments can be removed with much slower, lower-power, lower-cost signal-processing.

Homodyne OPLL + Costas Loop → 1 cm² footprint



Photonic IC: SGDBR laser, optical hybrid, and un-balanced PDs

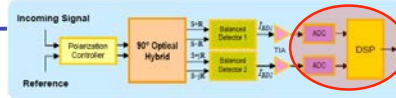
Electronic IC: limiting amplifiers and phase & frequency detector (PFD)

Hybrid loop filter: Feed-forward technique, op-amplifier and 0603 SMDs

Mingzhi Lu, et. al., *Optics Express*, Vol. 20, Issue 9, pp. 9736-9741 (2012)

Main Achievements:

VS →

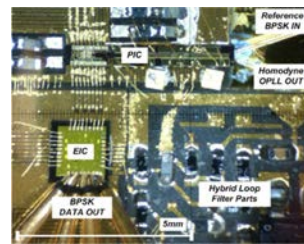


1. Stable Homodyne OPLL

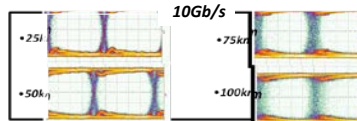
- **10x10mm²** Integration on single carrier (*Smallest*)
- **1.1GHz** closed loop bandwidth (*Widest*)
- **120ps** loop propagation delay (*Shortest*)
- **100kHz** narrow-linewidth (*Same as ref. laser*)
- **-100dBc/Hz@above 50kHz** phase noise
- **600ns** frequency pull-in time (*First time*)
- **<10ns** phase lock time (*First time*)
- **2.6°** temperature fluctuations while locked

2. BPSK Coherent Optical Receiver

- **First** demonstration for integrated optical Costas loop
- **40Gb/s** coherent BPSK data reception no latency
- **Error-free** up to 35Gb/s BPSK data (< 10⁻¹² BER)
- **QPSK possible**

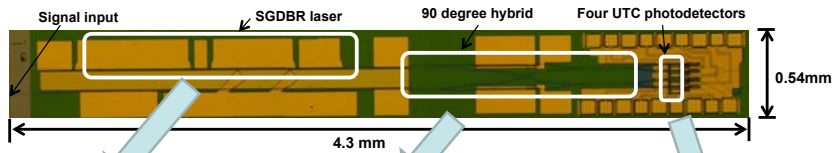


40Gb/s Back-to-back

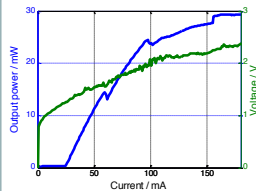


Mingzhi Lu, et. al., *Optics Express*, Vol. 20, Issue 9, pp. 9736-9741 (2012)

InP Widely-tunable Coherent Receiver PIC (Homodyne or Intradyn—also for Optical Synthesis)



SG-DBR laser



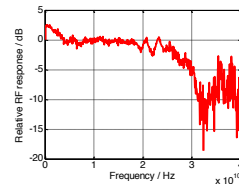
- 30 mW output power
- 40 nm tuning range
- 25 mA threshold current

90 deg hybrid

- 1x2 MMI couplers
- Directional couplers
- Phase shifters

↓
No phase error
4% power imbalance

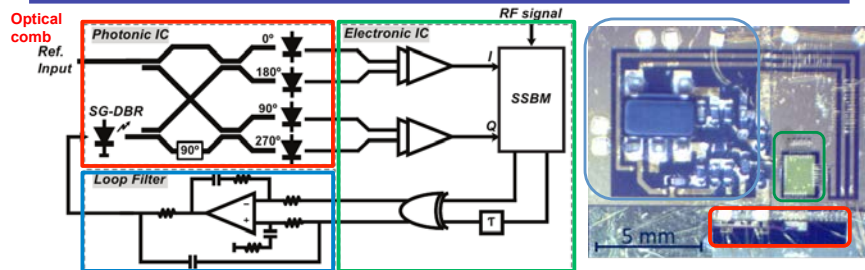
UTC photodetectors



- 29 GHz 3-dB bandwidth with -2V bias
- 18 mA saturation current at -5V bias.

Mingzhi Lu, et. al., Optics Express, Vol. 20, Issue 9, pp. 9736-9741 (2012)

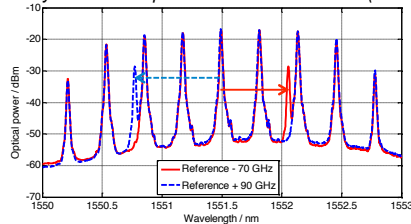
Optical Frequency Synthesis with OPLL



- Reference input is now a stabilized comb
- The circuit selects one comb line and offset locks from it to the next line using an RF synthesizer input
- Photonic IC same as for receiver
- Electronic IC incorporates single-sideband mixer and RF input for offset locking
- Loop filter similar to receiver

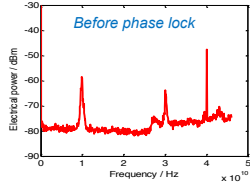
Mingzhi Lu, et. al., OFC, paper W1G.4(2014)

Synthesizer output + reference comb lines (40 GHz)

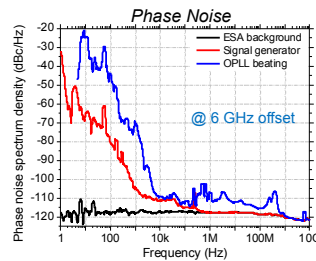
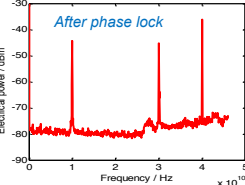


- Very low phase noise : $< 0.03 \text{ rad}^2$ phase error variance
- ~ 500 MHz loop bandwidth
- $\pm 25 \text{ GHz}$ offset locking capture range
- 160 GHz output frequency sweep range demonstrated

10GHz offset/40GHz comb spacing



10GHz offset/40GHz comb spacing



Mingzhi Lu, et. al., OFC, paper W1G.4(2014)

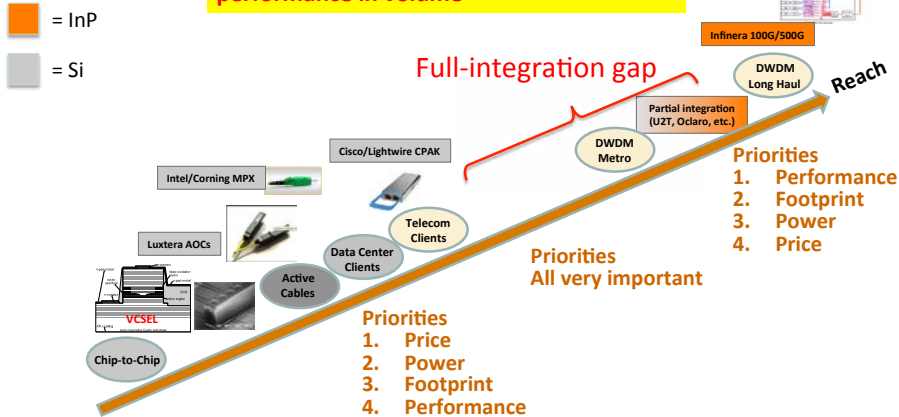
Balanced Receiver

- Laser – SGDBR (40 nm tunability)
- Frequency Error Sensor – Asymmetric MZI
- Filter FSR = 10 GHz

- Open loop $\rightarrow > 5 \text{ MHz}$ linewidth
- Closed loop $\rightarrow 150 \text{ kHz}$ linewidth

A. Sivanathan, et al, OFC, 2013

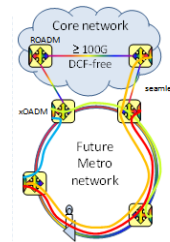
Metro challenge: deliver full integration with good price, power, footprint, and performance in volume



Based on C. Doerr inputs, OFC 2014, ACACIA

Metro architecture renewal

- Growing faster than LH because traffic increasingly staying within the metro area
 Source: Bell Labs "Metro Network Traffic Growth: An Architecture Impact Study"
- Metro may account for 58% of all IP traffic by 2017
 Source: Cisco "The Zettabyte Era—Trends and Analysis"
- Transitioning from opaque topology to higher level of transparency w/ ROADMs
 Source: OIF "OIF Carrier WG Requirements for Intermediate Reach 100G DWDM for Metro Type Applications"

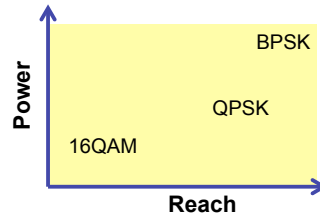


Source: OIF Carrier WG Requirements for Intermediate Reach 100G DWDM for Metro Type Applications

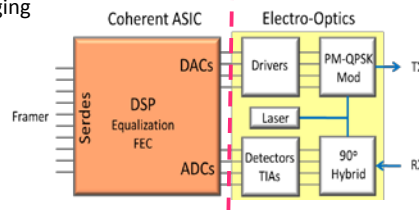
Based on C. Doerr inputs, OFC 2014, ACACIA

Key Technologies and Challenges for 100G Coherent Metro Transceiver

- Possible modulation formats
 - PM-BPSK, PM-QPSK, PM-16QAM
 - PM-BPSK is over-kill for metro distance, too spectrally inefficient for metro applications
 - PM-16QAM is too sensitive to fiber non-linearity, limited distance.
 - PM-QPSK is good compromise between performance, cost and power
- Key Transceiver Technologies
 - ASIC, DSP, **Photonic Integration**, Packaging
- Transceiver Power Consumption determines Form-factor
 - Heat dissipation is the real challenge



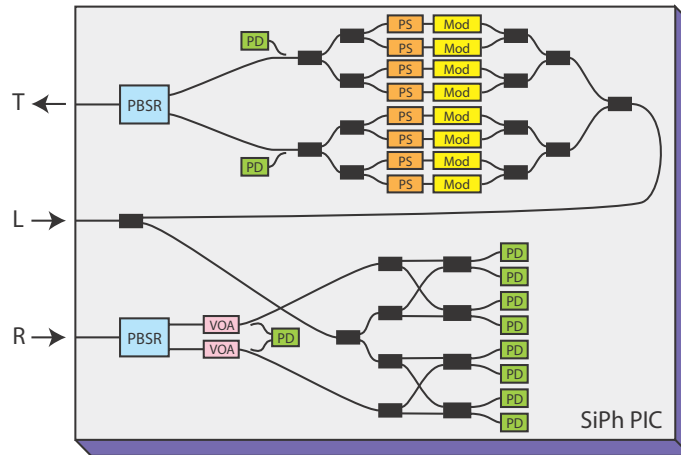
Analog pluggable / Digital pluggable



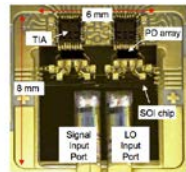
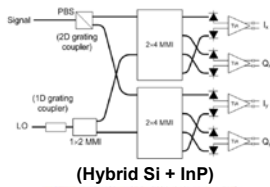
InP – Si PIC comparison

InP	Si
<ul style="list-style-type: none"> Expensive material <ul style="list-style-type: none"> In is scarce (hasn't affected chip cost) Medium yield <ul style="list-style-type: none"> W.g. material from epitaxy (excellent vertical dimension control) Small footprint <ul style="list-style-type: none"> High index contrast in 1D Efficient laser & PD No good native oxide Low dark current (lattice-matched) Small wafers <ul style="list-style-type: none"> Brittle material Modulator temp. sensitive <ul style="list-style-type: none"> But more efficient (could use depletion also) 	<ul style="list-style-type: none"> Cheap material <ul style="list-style-type: none"> 27% Earth's crust is Si High yield <ul style="list-style-type: none"> W.g. material from original boule (excellent lateral pattern control) Extremely small footprint <ul style="list-style-type: none"> High index contrast in 2D No native laser or PD Excellent native oxide Medium dark current (Ge) <ul style="list-style-type: none"> Not key in coherent Large wafers <ul style="list-style-type: none"> Strong material Modulator temp. insens. <ul style="list-style-type: none"> But weaker effect

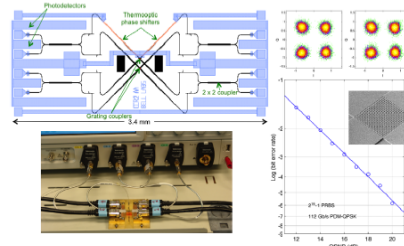
Laser is shared between Tx and Rx, allowing Tx and Rx to be integrated together, reducing assembly parts, time, and testing



Based on C. Doerr inputs, OFC 2014, ACACIA



Chip dimension: 2 x 6 mm

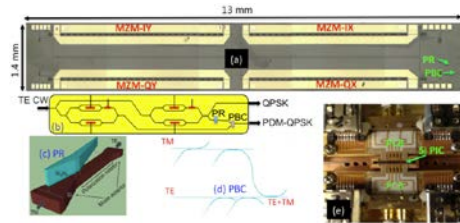


Chip dimension: 1.4 x 3.4 mm

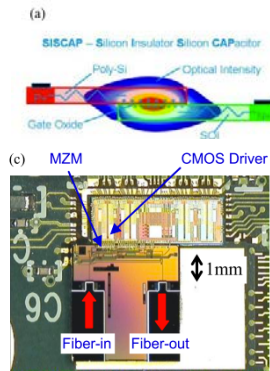
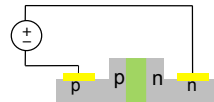
C. R. Doerr, et al., J. Lightwave Tech, 2010 (ALU).
C. R. Doerr, et al., IEEE PTL, 2011.

Y. Painchaud, et al., OFC 2013 (Teraxion)

Based on C. Doerr inputs, OFC 2014, ACACIA

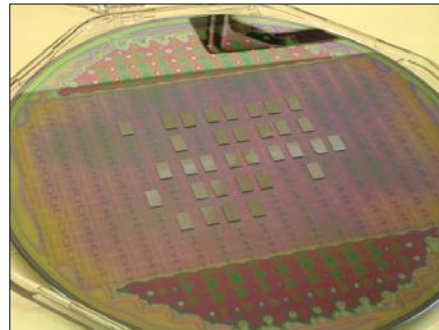
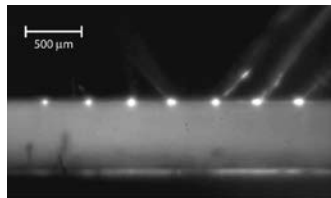
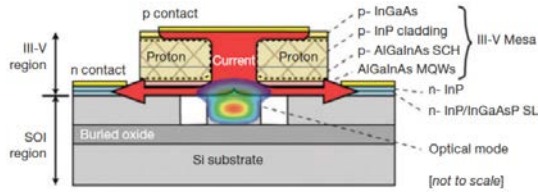


P. Dong, L. Chen, et al., *Opt. Exp.*, 2012.



B. Milivojevic, et al., *OFC, OTh1D.1*, 2013.

Based on C. Doerr inputs, *OFC 2014*,



Heck et al. *JSTQE* 2013

FP, ring, DFB, and DBR lasers
(Fang, *IEEE PTL*, 20, 2008)

ring
DBR
DFB

19 dB/mm amplifier
(Kurczveil, *SPIE PW*, 2011)

AMP
detector

>20 GHz photodetector
(Faralli, *OSA OE*, 20, 2012)

Microring laser

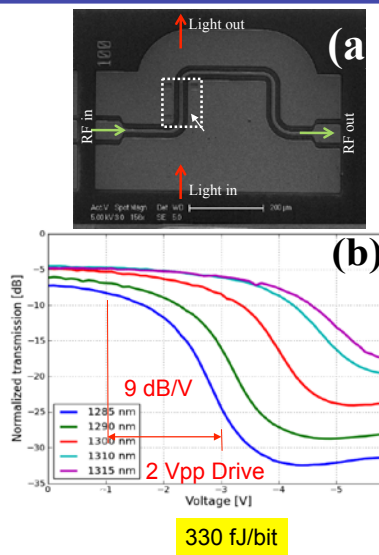
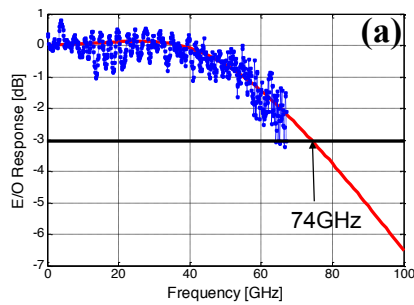
Bus WG
235 μm
179 μm
2.5 μm

74-GHz EAM, 27-GHz MZI modulators
(Chen, *OSA OE*, 19, 2011; Tang, *OSA OE*, 20, 2012)

MZM
EAM
Light out
Active Part
RF in
RF out

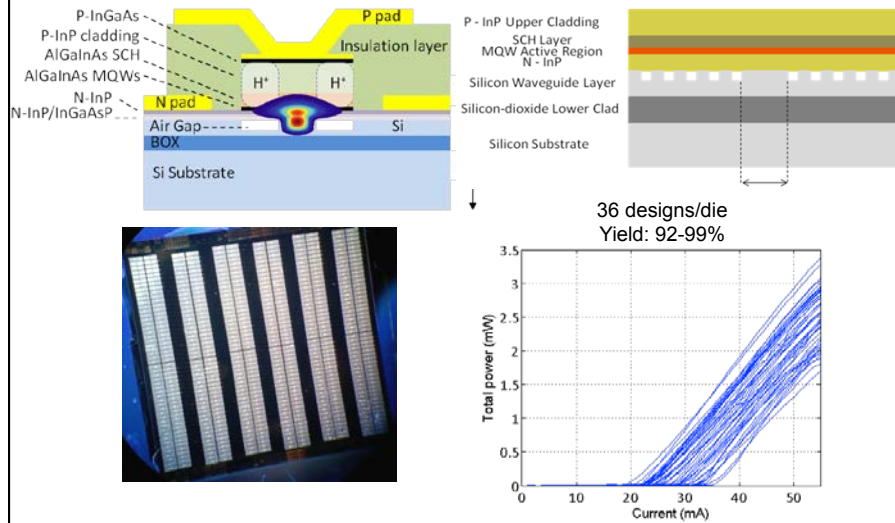
Microring resonator laser
(Liang, *GFP*, 2009)

- Segmented electrode
- Length: 100 μm
- >67 GHz Bandwidth



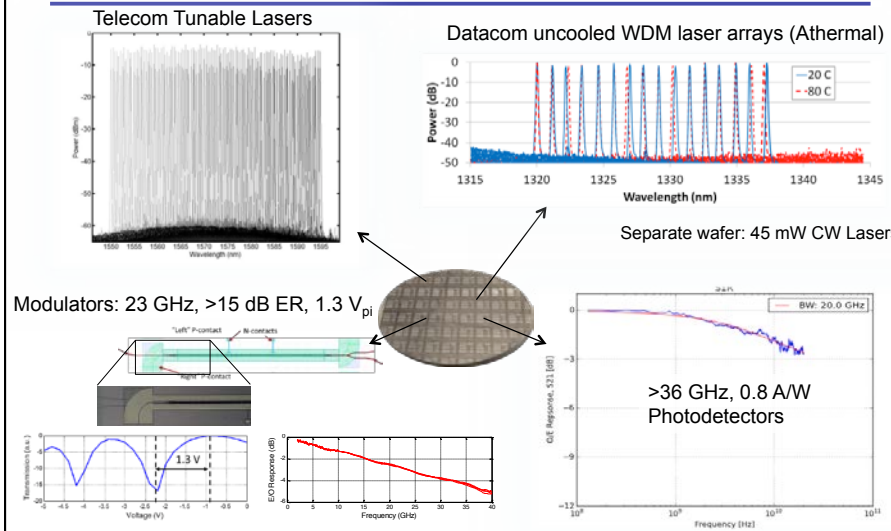
Tang, Peters, Bowers OFC Postdeadline 2012

Distributed feedback laser structure



S. Srinivasan, N. Julian, J. Peters, D. Liang, J. E. Bowers, "Reliability of Hybrid Silicon Distributed Feedback Lasers," *JSTQE* 19, (4), July/August 2012

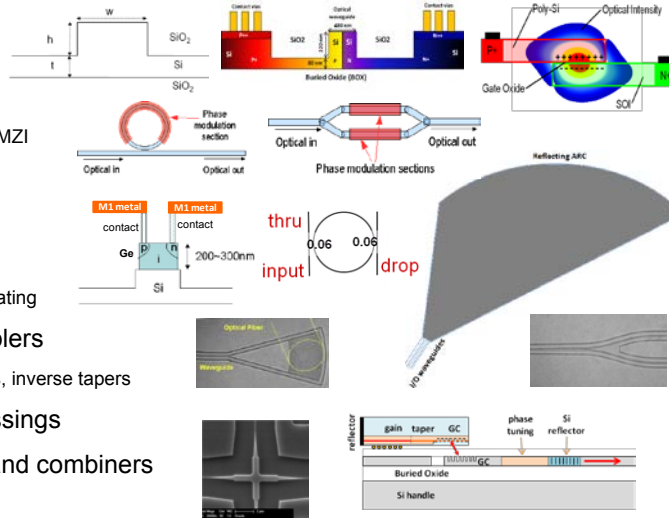
Hybrid-Si PIC Integration (Aurion)



Brian Koch *et al.*, OFC Postdeadline 2013

Si photonic device building blocks

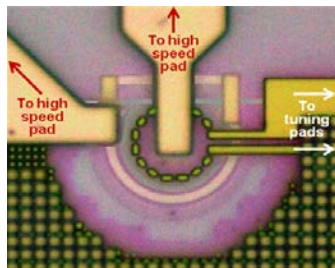
- Waveguides
 - Rib, wire
- Modulators
 - Ring resonator, MZI
- Photodetectors
 - Ge-on-Si
- Mux/demux
 - Ring, Echelle grating
- Optical I/O couplers
 - Grating couplers, inverse tapers
- Waveguide crossings
- Optical slitters and combiners
- Laser source



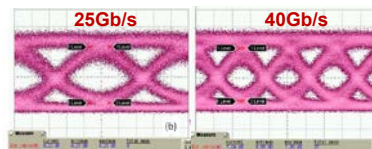
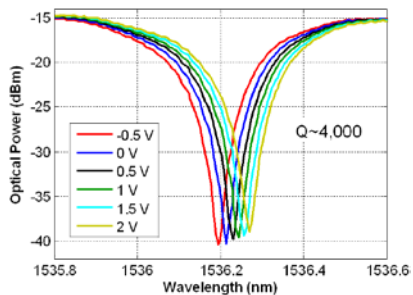
Approved for Public Release; Distribution Unlimited

40 Gb/s ring modulator

G. Li, *Opt. Express* 19 (21), 2011
G. Li, *Group IV Photonics*, 2012



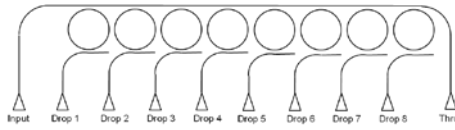
Radius	5 μm
Driving voltage	2 V
Capacitance	22 fF
ER @40Gb/s	7.0 dB
ON-state loss	5 dB
Tuning efficiency	0.12 nm/mW



Proof-of-concept at 40Gb/s with an extinction ratio = 7dB

Approved

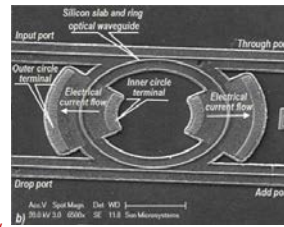
Ring mux/demux



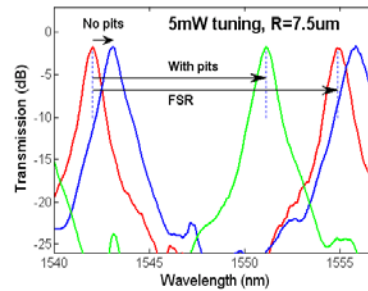
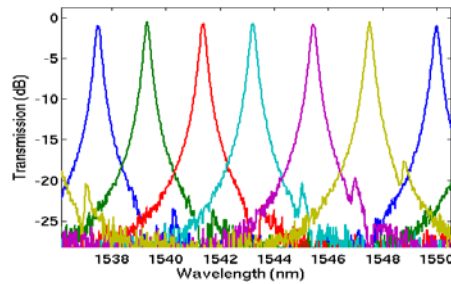
J. Cunningham, *Opt Ex*, 18 (18), 2010

I. Shubin, *Opt. Quan. Elec.*, 2012

A. Krishnamoorthy, *IEEE Photon. J.*, 3(3), 2011



- Optimize bus-ring coupling gap for small loss and small crosstalk
- Thermal tuning to align the channels

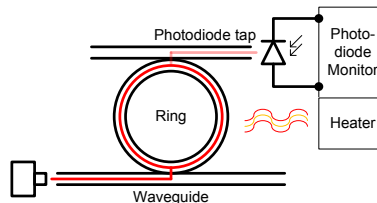


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ORACLE
Ashok Krishnamoorthy, OIC (2014) 43

Controlling the ring modulator

- Three components to feedback system
 - Monitor the ring output with a dedicated photodiode (1% tap)
 - Constantly compare power level with the fixed reference
 - Drive the local heater to push ring back to reference

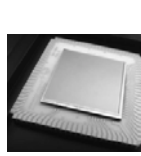


- Establish fixed reference at bring-up & periodically refresh

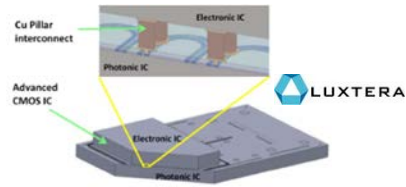
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ORACLE
Ashok Krishnamoorthy, OIC (2014) 44

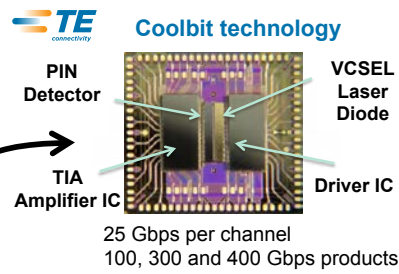
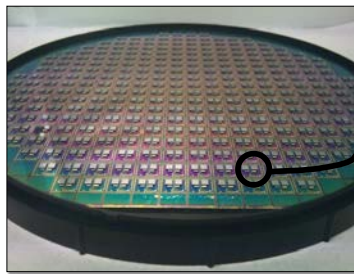
“Flip-chip” photonics + CMOS examples



Megapixel GaAs MQW/CMOS QWIP

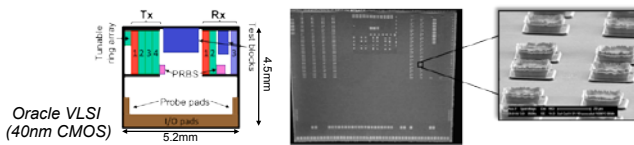


Luxtera hybrid integrated Nx28 Gbps Chipset

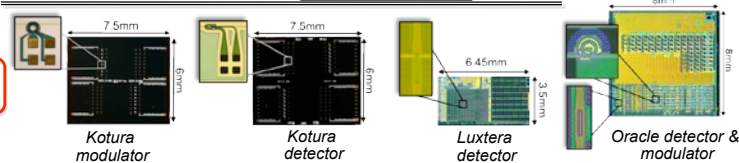


Hybrid integration technology

VLSI chip



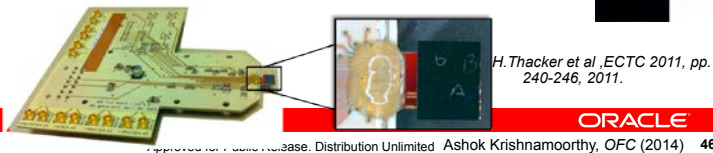
Photonic chip



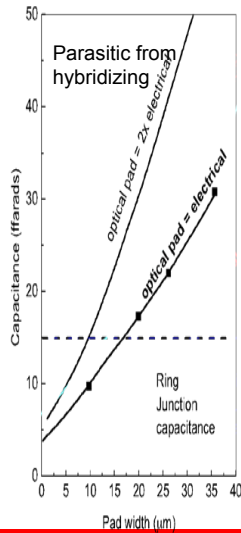
Hybrids



Assembled test vehicle



Hybrid integration scaling



Hybrid approach parasitics become smaller than device junction as pad shrinks

Hybrid can outperform (monolithic) in speed, power, density, and TTM

Optimization enables/requires electronics-photonics co-design

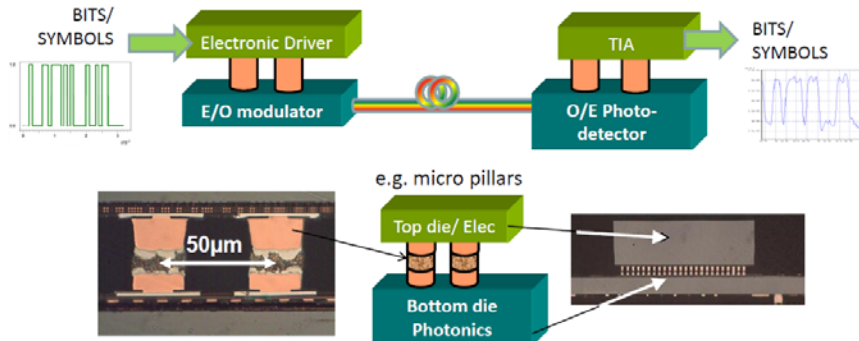
3D (or Heterogeneous) integration → Integration

ORACLE

Approved for Public Release. Distribution Unlimited Ashok Krishnamoorthy, OFC (2014) 47

Back end E/O integration

- Preferred due to differences in nodes /size : Opto versus Elec
- 3D CMOS integration processes
 - With high throughput
 - Reduced parasitic capacitance between optics and electronics



leti

ECOC 2013, Workshop 3 – Device integration - Si Photonics, Sylvie Menezo

8

© IZA. All rights reserved.

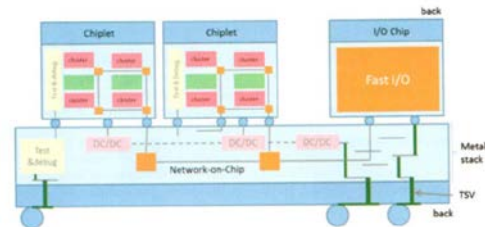


Figure 1: Schematic view of the interposer concept.

- Chiplet—generic high-performance computing or memory die
- I/O chip—electrical or optical inputs and outputs to other interposers or boards or?
- Active Interposer—power and flexible interconnect architecture

The “active-interposer” concept for high-performance chip-to-chip connections

S. Cheramy, et al, *Chip Scale Review*, 18 (3) (May/June,2014).

- PICs are desirable for modest to high volume communication, sensing and instrumentation functions, where size, weight, power and cost (SWAP-C) reductions are desired.
- PICs are important because of the inherently stable phase relationships and possibly seamless interfaces between elements.
- PICs generally bring better reliability once properly designed; yield and some aspects of performance may be compromised.
- PICs, (heterogeneously) integrated with EICs, are needed to reduce transmission line parasitics, to provide intimate (phase adjusted) control, or to provide near instantaneous feedback.
- Single-crystal (e.g. CMOS) integration may not be as desirable as heterogeneous (3D, Hybrid) integration (unless high volume). Still may want to use silicon “system in a package” technology.

Photonic Integrated Circuits with Wavelength Tunable Lasers

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ABSTRACT

Efforts to develop monolithic tunable lasers required the integration of several different waveguide elements, such as gain, phase modulator, and grating mirror sections. With this suite of components, more complex photonic ICs became possible.

In the 1980's coherent communication was widely investigated to increase receiver sensitivity and repeater spacing in optical fiber systems. It was also seen as a means of expanding WDM approaches because optical filters would not be so critical. This early coherent work drove early photonic integration efforts because of the phase stability such integration brings; it also drove work on tunable lasers for use both in local oscillators, which could be tuned across many channels in a single receiver, and also for use in flexible transmitters.

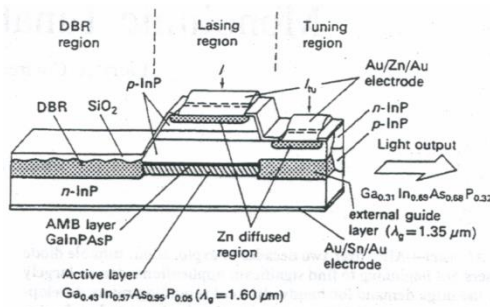


Fig. 1. Early tunable DBR laser [1].

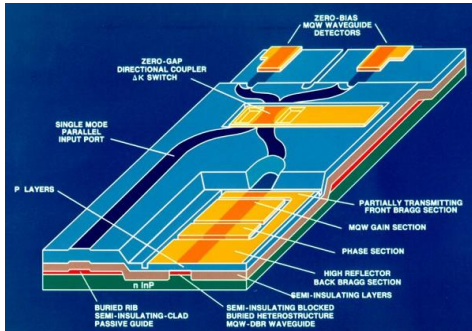


Fig. 2. Integrated heterodyne receiver [3].

laser should fail; however later (in the 2000s), once reliability and cost were competitive, it became the dense WDM source of choice. In fact, many applications besides fiber optic communications listed such a device as desirable. So, the exploration of such components continued throughout the 1990s, and with this exploration, the development of many new photonic IC elements continued. For example, grating-assisted vertical couplers, Y-branch couplers, sampled-grating DBRs, super-structure DBRs, and MMI couplers were perfected during this time [4].

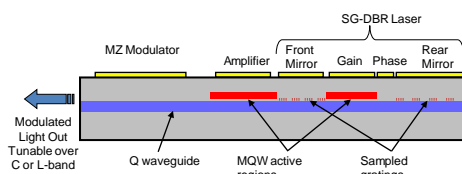


Fig. 3. SG-DBR + SOA + MZM [5].

Some of the earliest efforts to make single-chip tunable lasers resulted in technologies to integrate a variety of active and passive waveguide components that have enabled many of the photonic integrated circuits becoming technologically important today. Because of the interest in fiber optic communication systems, these were mainly based upon the InGaAsP/InP materials system, so that will be the focus of this paper. Seminal examples include work on tunable DBR structures from Prof. Suematsu's group illustrated in Fig. 1 [1] as well as some developments in coupled cavities by reactive dry etching technology from the author's group [2].

By the end of the 1980's photonic integration in these materials had been explored to the point where complete coherent receivers were attempted on a single chip as illustrated by the work of Koch and Koren [3] in Fig. 2. However, with the advent of the Er-doped fiber amplifier (EDFA), the desperate need to stretch the reach between repeaters in WDM systems waned, as all channels could now be amplified in an analog way without the need for optical demux/receivers; multichannel electronic amplification; mux/optical transmitters—so-called O/E/O.

Nevertheless, the desire to have widely-tunable lasers for dense WDM remained; a single laser that could be tuned to any channel across the entire C or L-band, perhaps 200 channels, was still a dream. Initially, it was considered just as a universal spare if a DFB

Figure 3 shows the SG-DBR laser integrated with an SOA and a Mach-Zehnder modulator (MZM) [5]. This was first developed in the author's group with heavy influence from Agility Communications, a company started by former students of UCSB that continued to closely collaborate. Following the acquisition by JDSU, this basic structure has become a very popular small PIC, because of its small size and large capability. It can be tuned over 40 nm, with over 20 mW of fiber-coupled output—leveled by the SOA,

the MZM can operate up to and above 25 Gb/s with low drive voltage and tailorable chirp.

In recent years, more complex PICs have been investigated for many applications, such as optical switching (including wavelength conversion)[6], free-space beam sweeping [7], and coherent communication [8,9] —all depending upon widely-tunable lasers for their functionality. Figure 4 illustrates an integrated Optical Phase Locked Loop (OPLL) circuit that contains a PIC and closely integrated Costa's-loop electronic feedback circuit, which can function either as a coherent receiver or as a frequency synthesizer [10], depending upon the nature of the feedback circuit. The receiver is shown. It provided error-free BPSK operation up to 40 Gb/s without careful temperature ($\sim 3^\circ\text{C}$) or vibration control on a $\sim\text{cm}^2$ area ceramic substrate. As shown in Fig. 4(c), the PIC itself contains a widely-tunable local oscillator, a 90° hybrid, and 4-UTC photodiodes, so one might call it alone an integrated coherent receiver; but of course, its I, Q, I' and Q' outputs are only descrambled when phase-locked to the incoming carrier of the signal. [This can also be done with an ADC/DSP circuit, but this would be much more expensive, bulky, power hungry, and with FEC, high latency.]

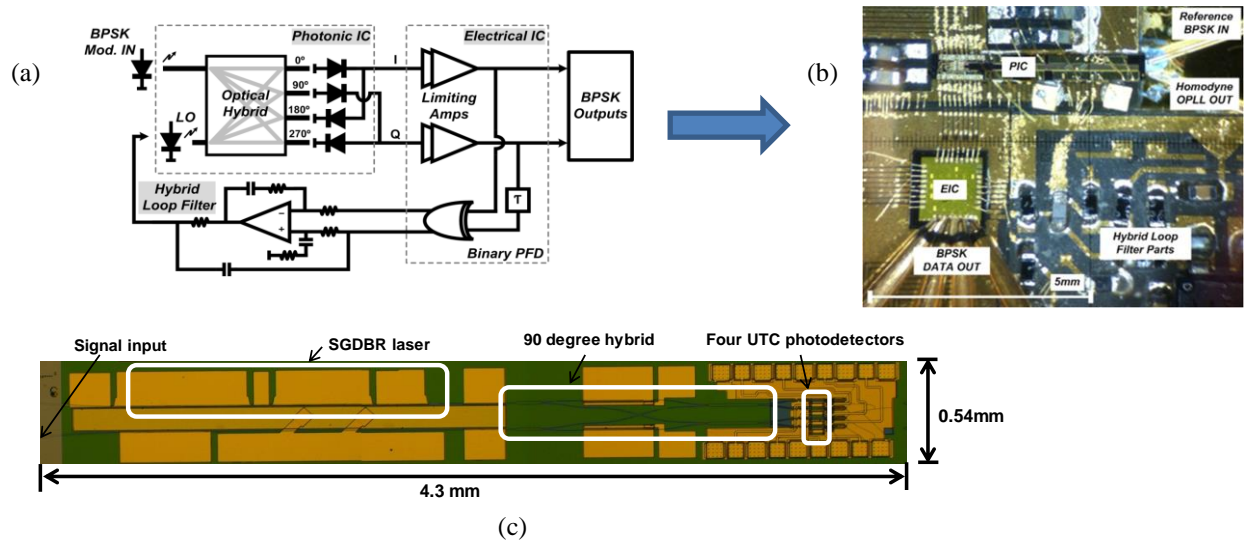


Fig. 4. (a) OPLL schematic; (b) OPLL photo; (c) expanded PIC photo [9].

References

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An Integrated Heterodyne Optical Phase-locked Loop with Record Offset Locking Frequency

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and Larry A. Coldren^{1,3}

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Abstract: A highly-integrated optical phase-locked loop (OPLL) is realized by photonic and electronic integration. The experiment shows the full functionality of this heterodyne OPLL and 25 GHz offset locking frequency is achieved.

OCIS codes: (250.5300) Photonic integrated circuits; (060.2840) Heterodyne; Optical phase-locked loop;

Ever since the first optical phase-locked loop (OPLL) was demonstrated in 1965, a lot of effort has been devoted to the development of OPLLs. Much of the motivation has been to achieve what has been achieved in the electrical domain, where almost every electronic system that we are using today relies on phase locked loops (PLLs) to realize their basic functions, such as frequency/phase synthesis, clock recovery, RF down/up-conversion. The realization of PLL in the optical domain, i.e. OPLL, may bring a fundamental change to the way how optical systems are designed and may also lead to many applications in the area of optical coherent communication and optical sensing [1].

The early work on OPLLs was mainly based on free-space optics and fiber pigtailed devices [2][3], and the resulting system size was large and the stability was generally poor, mainly because of a large loop delay. The loop delay directly relates to the loop bandwidth, and consequently the loop stability and phase noise suppression range. Control theory indicates that for a second-order type-II loop, the loop delay and bandwidth must satisfy, $\tau \cdot B_n < 0.12 \text{ ns} \cdot \text{GHz}$, for absolute loop stability [4]. For example, in order to achieve a loop bandwidth of 1 GHz, the maximum allowable loop delay is 120 ps, which corresponds to 36 mm of optical propagation in free space. Because of difficulties due to limited loop delay, OPLLs are historically regarded as one of the most unstable optical systems. Any perturbation such as mechanical vibration, might lead to a malfunction of such OPLLs. However recently, the situation has changed [5][6][7][8]. Several prototypes of highly integrated OPLLs have been demonstrated by the authors with high stability and other desirable characteristics [7][8]. Integration has provided orders of magnitude reductions in the loop bandwidth, and in addition, novel single-sideband mixer (SSBM) and phase/frequency detector (PFD) designs have increased the offset frequency range and OPLL stability as well [7].

In this paper, we demonstrate an integrated OPLL with a record laser offset frequency of 25 GHz. The system architecture is shown in Fig. 1. It is composed of three parts: a photonic IC (PIC), an electronic IC (EIC) and a loop filter (LP).

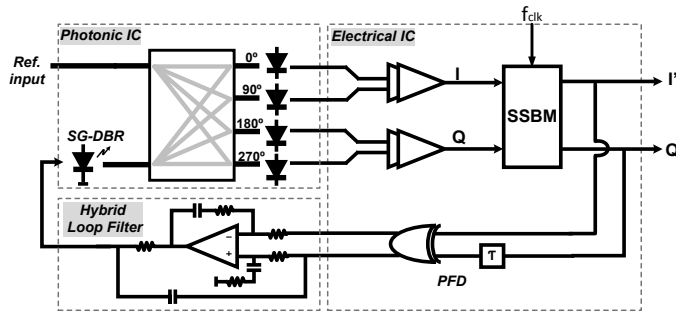


Fig. 1. Architecture of the heterodyne OPLL.

On the PIC, we integrate a widely-tunable sampled-grating DBR (SG-DBR) laser, a star-coupler-based optical 90 degree hybrid [7], four single-ended uni-travelling-carrier (UTC) photodetectors, and microstrip transmission lines. The SG-DBR laser acts as the widely-tunable slave laser. By injecting current into the back and front mirrors, the laser can be tuned over a 40 nm range. Meanwhile, the current injection into the phase section can tune the laser wavelength finely within one cavity mode, which is around 40 GHz, and this is used to phase lock the SGDBR laser so that its frequency is determined to Hz-level offset accuracy from the reference. On the EIC, trans-impedance limiting amplifiers, a delay line, an XOR gate and an SSB mixer are integrated [9]. The delay line and the XOR gate

together act as a phase/frequency detector. The loop filter is built on a common Aluminium Nitride carrier, using a voltage feedback operational amplifier as an active filter and integrator. The beat signal from the on-PIC photodetectors are finally negatively fed back to the SG-DBR laser phase section through the EIC and the loop filter.

The loop delay for the closely integrated hybrid PIC-EIC-LP circuits is approximately 200 ps, in which 40 ps is from the PIC, >100 ps is from the EIC and 50 ps from the loop filter and interconnections.

The PIC is fabricated with a centered-QW structure, and quantum well intermixing is used to define active and passive areas. UTC photodetector layers are regrown by MOCVD after active/passive definition. Surface ridge waveguides are used for all devices on chip. A star coupler is chosen as a 90-degree hybrid, where in-phase and quadrature signals are generated. Microstrip transmission lines are also integrated. The details about the PIC design and fabrication can be found in [10]. Measurements show the full functionality of the PIC. The SG-DBR laser covers 40 nm, and UTC photodetectors have a RF bandwidth of 35 GHz [10]. A picture of the photonic IC is shown in Fig. 2.

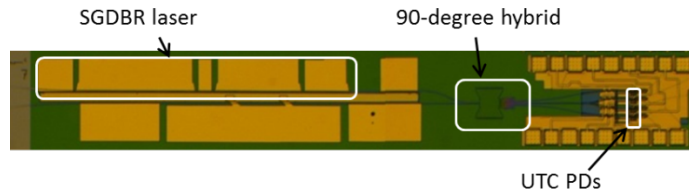


Fig. 2. A microscope picture of the PIC.

The EIC is fabricated at Teledyne Scientific using 500 nm InP-HBT technology. The unit gain frequency is 300 GHz. The working frequency of the designed EIC is up to 50 GHz.

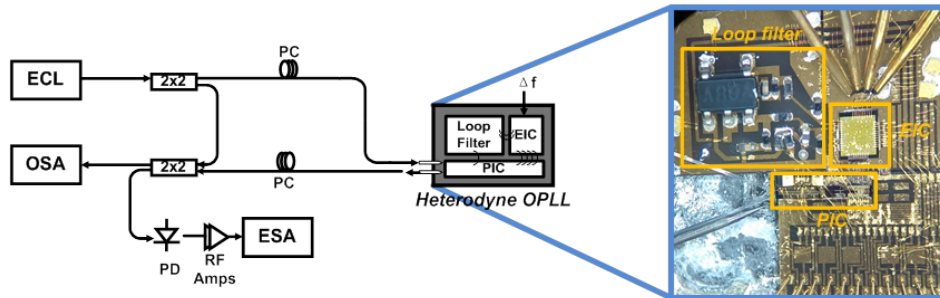


Fig. 3. The schematic of the OPLL test setup and a microscope picture of the heterodyne OPLL. (ECL: external cavity laser, OSA: optical spectrum analyzer, ESA: electrical spectrum analyzer, PC: polarization controller.)

Schematics of the OPLL test bed can be found in Fig. 3 and a microscope picture is also shown. The designed loop bandwidth is around 500 MHz. Using lensed fiber, the reference laser (an Agilent widely-tunable laser) signal was coupled into the PIC, and the SG-DBR laser signal was coupled out from the back mirror for monitoring purposes. The optical spectrum of the SG-DBR laser and the reference laser was measured by an optical spectrum analyzer (OSA) and their beat tone measured by an electrical spectrum analyzer (ESA) via a high speed photodetector. The offset locking frequency is defined by RF signal generator frequency, which is twice of the desired offset frequency of this heterodyne OPLL [9].

The experiment shows phase locking between the on-PIC SG-DBR laser and the incoming reference laser. The beating tone of the locked lasers is shown in Fig. 4 with an offset frequency of 12 GHz. According the Fig. 4, the closed loop bandwidth is around 500 MHz, which is in accordance with our design, and the phase noise within 500 MHz is well suppressed. By only tuning the RF signal generator frequency, frequency pull-in and phase locking are achieved at the same time. As long as the desired locking frequency is within a laser cavity mode spacing, by turning on the OPLL, the SG-DBR laser output frequency will be pulled towards the desired frequency, and it will finally be phase locked automatically. Total pull-in and locking times are sub-microsecond. The maximum offset frequency that we achieve in this experiment is 25 GHz, as limited by the RF synthesized signal generator, since the SSB mixer requires double the offset frequency [9] and only a 50 GHz signal generator is available for this experiment. A series of electrical spectra are shown in Fig. 5, where the offset frequencies vary from 5 GHz to 25 GHz.

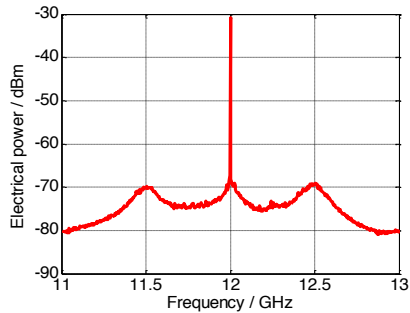


Fig. 4. Beating tones of the two lasers when the offset frequency are 12 GHz, measured with 100 kHz resolution bandwidth.

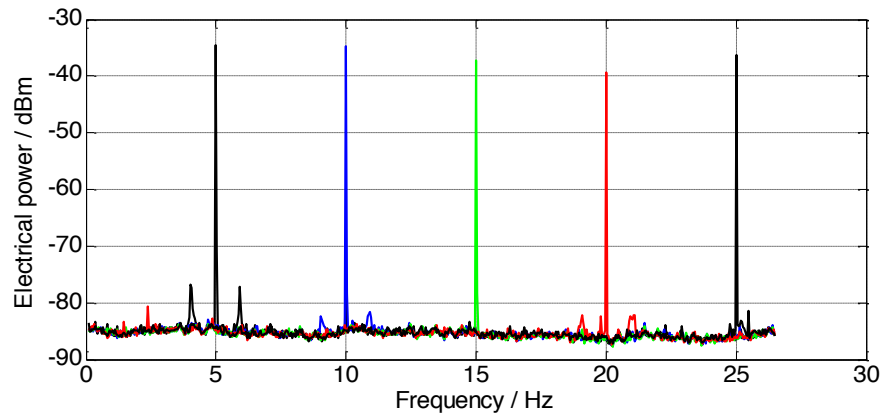


Fig. 5. Shows the beating tones of the two lasers when they are phase locked at various frequency offsets: 5 GHz, 10 GHz, 15 GHz, 20 GHz, and 25 GHz. The resolution bandwidth is 100 kHz.

Acknowledgement

This work was mainly supported by DARPA CIPHER—PICO project. A portion of this work was done in the UCSB nanofabrication facility, part of the National Science Foundation (NSF) funded NNIN network. The EIC is fabricated at Teledyne Scientific and Imaging Company.

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A Highly-Integrated Optical Frequency Synthesizer Based on Phase-locked Loops

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Abstract: The first highly-integrated optical synthesizer is realized by photonic integration and optical phase-locking technique. Preliminary results show >160 GHz output frequency range and a relative frequency accuracy as defined by the RF signal.

OCIS codes: (250.5300) Photonic integrated circuits; (060.2840) Heterodyne; Optical phase-locked loop; optical frequency synthesis

Frequency synthesis is widely used in many electronic systems. By using a synthesizer, arbitrary RF frequencies that are coherent to a single reference signal are generated. High frequency RF signals are therefore obtained with a similar phase noise to that of a crystal oscillator or other low noise sources. The coherent RF tone generated by RF synthesis enables RF signal up/down-conversion and coherent detection, and is the core technology for numerous applications, including radio receivers, mobile telephones, satellite receivers, GPS systems, radar, etc. Although RF frequency synthesizers are widely used commercially, its counterpart, an optical synthesizer is far from mature. In this paper, the first highly-integrated optical frequency synthesizer is proposed and demonstrated.

For a typical RF synthesizer architecture, a phase-locked loop (PLL) is usually the key element. Frequency dividers and multiplexers in the PLLs are key components for generating a signal with a different frequency from the reference. However, in the optical domain, efficient and integrated frequency dividers and multiplexers are not available. Moreover, the demanded frequency range is relatively small compared to the absolute optical frequency. Using dividers and multiplexers for optical synthesis is not realistic. In this work, the first integrated optical frequency synthesizer is achieved by phase-locking a tunable CW laser to an optical comb, which is generated from a narrow linewidth reference laser [1][2].

The basic idea of this integrated synthesizer is explained in Fig. 1 [1]. The continuous-wave laser A is a single fixed-wavelength narrow-linewidth laser, which is used as the reference laser in this system. Stable and narrow-linewidth comb lines are then generated from this fixed-wavelength laser through modulators. The comb lines are then used as the reference for the heterodyne optical phase-locked loop (OPLL). A RF frequency f_{RF2} is applied on the electronic IC (EIC) of the OPLL to introduce a frequency offset, which is $f_{RF2}/2$ [3]. By tuning the slave laser mirror and phase section currents as well as f_{RF2} , the slave laser can phase-lock the frequency of $f_i \neq f_{RF2}/2$, where $i=1,2,3,4,\dots$. As long as the heterodyne OPLL offset frequency range is larger than half of the comb line spacing, the optical synthesizer can cover all the frequencies within the comb range. Moreover, the SG-DBR linewidth will be the same as CW laser A, because of the linewidth ‘cloning’ of OPLL [4]. Importantly, switching between frequencies can be achieved much more quickly and accurately (Hz-level) than with freely-running tunable lasers, and thermal effects over a few degrees are not an issue, because of the rapid (submicrosecond or even nanosecond) phase locking.

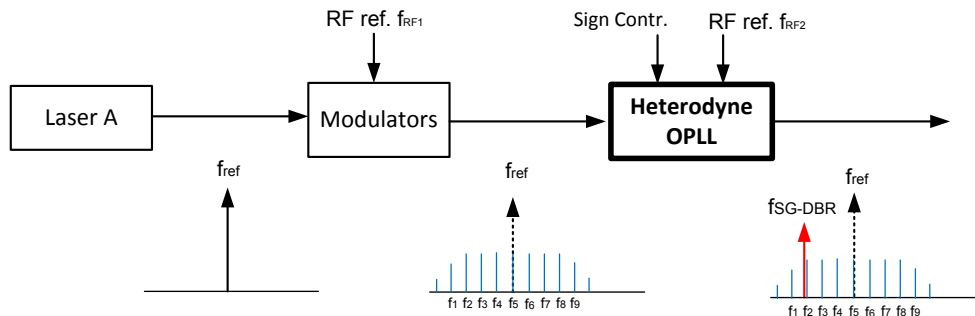


Fig. 1. The architecture of the optical frequency synthesizer.

The key building block of this system, the heterodyne OPLL [5], has the structure shown in Fig. 2, including three parts: a photonic IC (PIC), an EIC and a loop filter built of discrete components. The PIC is based on the InGaAsP/InP integration platform, and it is composed of a widely-tunable sampled-grating DBR (SG-DBR) laser, a star-coupler-based 90-degree hybrid, four high-speed uni-travelling-carrier (UTC) photodetectors, and transmission lines [6]. The SG-DBR laser covers a 40 nm spectral range, and the UTC photodetectors have a 35 GHz 3-dB RF bandwidth. The EIC is based on Teledyne's 500-nm InP HBT technology, and has a working frequency higher than 50 GHz. TIAs, a single-sideband mixer (SSBM) and a phase/frequency detector are integrated. The details of this EIC can be found in [3]. The loop filter electronics ensures the loop property. In this case, a dual-path type II loop is used. The size of the whole OPLL system is $\sim 10 \times 10 \text{ mm}^2$. The designed loop bandwidth is $\sim 500 \text{ MHz}$.

The details of test setup are shown in Fig. 3. First, an optical comb is generated from the reference laser by applying modulations using a phase modulator (PM) and a Mach-Zehnder modulator (MZM), both of which are driven by 40 GHz RF signals that are generated from active frequency doublers. The output of the MZI is amplified by an Erbium-doped fiber amplifier (EDFA), and then propagated through a long fiber where the comb is flattened due to nonlinear effects. An optical filter with a 2.4-nm FWHM bandwidth is used to filter out the amplified spontaneous emission (ASE) noise. The comb is then coupled into the PIC as the reference for the OPLL as shown in Fig. 3.

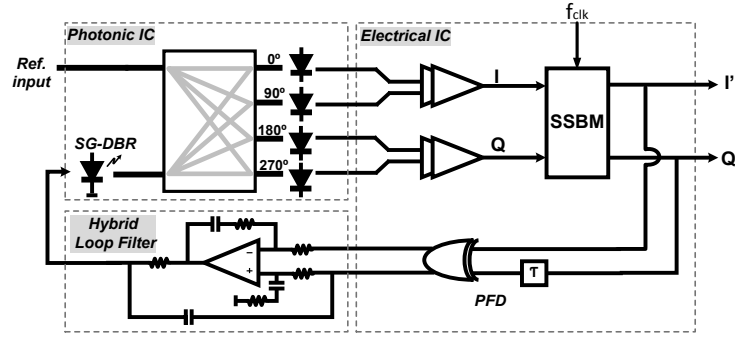


Fig. 2. The architecture of the heterodyne OPLL.

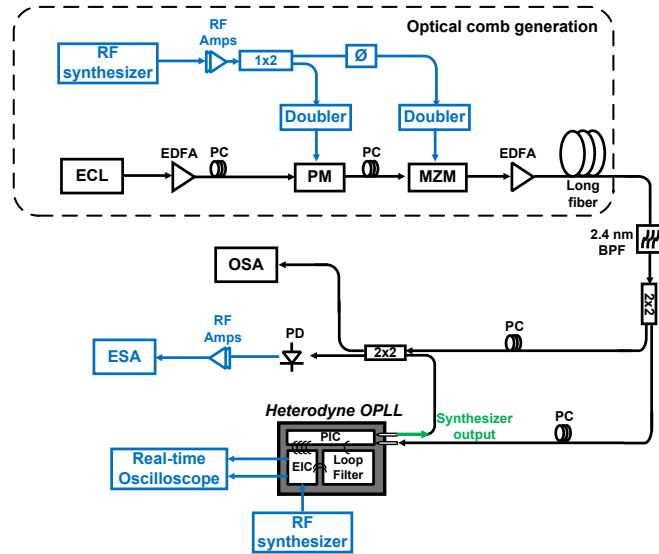


Fig. 3. The test setup of the optical synthesizer. The blue lines indicate RF connection, and the black lines are optical fiber connections. (ECL: external cavity laser, ESA: electrical spectrum analyzer, OSA: optical spectrum analyzer.)

The measurement indicates a 25 GHz offset locking range of the heterodyne OPLL, which means that this optical synthesizer can cover the whole frequency spectrum within the comb range as long as the line spacing is no larger than 50 GHz. A 40 GHz comb spacing is chosen in this case.

We have successfully phase locked the SG-DBR laser to the comb lines. Fig 4(a) shows the optical spectra when the SG-DBR laser locks to two of the comb lines, respectively, with a 10 GHz offset. The electrical spectra are

shown in Fig. 4(b) & (c) as well. As we can see, the RF beating tones show that the offset frequency is exactly 10 GHz, which is +90 GHz and -70 GHz from the reference laser frequency. That is, >160 GHz range is covered. The narrowness of the RF tones on the ESA also verifies the coherence between the SG-DBR laser and the reference laser. To the best of our knowledge, this is the first time that a prototype of a real optical synthesizer has been demonstrated.

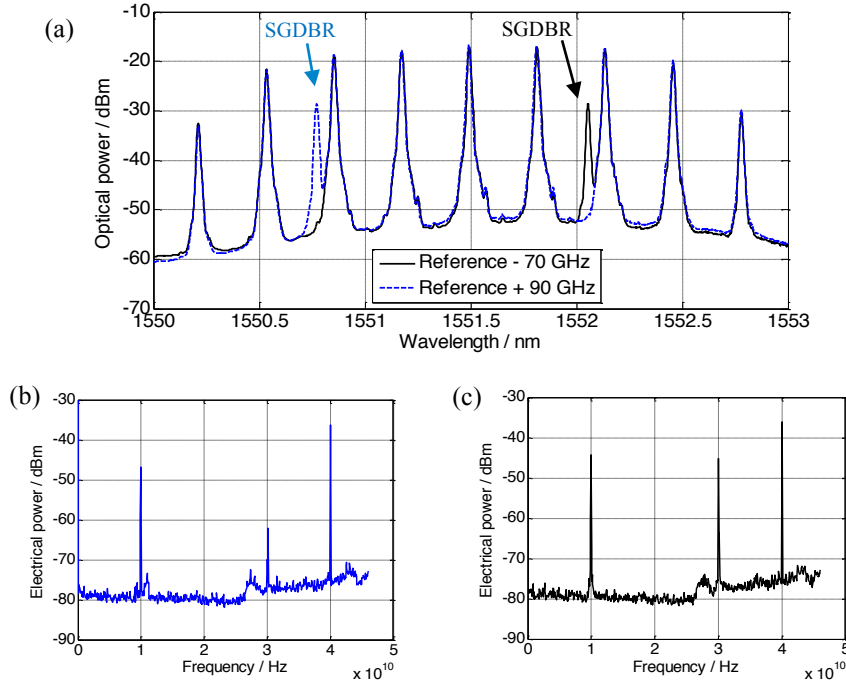


Fig. 4. Optical synthesizer measurement results. (a) optical spectra when the output is +90 and -70 GHz off the reference wavelength. The RBW is 0.01 nm. (b) and (c) RF spectra when the output is +90 and -70 GHz, respectively, measured on the ESA shown in Fig. 3. The RBW is 100 kHz.

Acknowledgement

This work was mainly supported by the DARPA CIPHER—PICO project. A portion of this work was done in the UCSB nanofabrication facility, part of the National Science Foundation (NSF) funded NNIN network. The EIC is fabricated at Teledyne Scientific and Imaging Company.

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Phase-Locked Coherent Optical Interconnects for Data Links

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In large-scale digital systems, propagation delay and power consumption of the interconnects are vastly larger than that of the transistors themselves [1,2]. Reduced power consumption, and increased capacity is required for interconnects, whether on-chip, between circuit boards, or within large data centers. Here we will consider coherent optical interconnects for high-capacity, sub-km links within data centers. At the other extreme of interconnect length, we will also briefly consider alternative approaches for reduced $CV^2/2$ switching energy of VLSI interconnects.

Within data centers, optical links can readily provide $\gg 100$ Gb/s capacity using wavelength-division and polarization multiplexing. Coherent links [3] offer more complex constellations, increased spectral efficiency, and greater capacity. Most long-haul coherent links [3] use free-running local oscillator (LO) lasers; the receiver uses digital signal processing (DSP) to both equalize dispersion and correct LO phase fluctuations. In few-km links, dispersion need not be compensated; if the LO laser is then phase-locked to the received signal, DSP can then be eliminated to greatly reduce receiver cost and DC power.

In phase-locked [4,5] coherent receivers, the LO laser phase is locked to the received signal. In optical PLLs (OPLLs) [6,7,8], wide ~ 1 GHz loop bandwidths are necessary to suppress the LO laser's phase noise, and, as noted by Coldren [6,7,8] photonic integration (PIC) is required to provide the needed small component propagation delays. Because the signal and LO lasers may be initially offset by 5-50GHz, broadband (DC \sim 50GHz) phase-frequency [9] difference detectors force the loop to lock. By these techniques we have demonstrated 35Gb/s coherent phase-locked BPSK receivers [6] (fig. 1a).

Used in WDM transmitters, OPLLs can further improve spectral efficiency. Using broadband digital *SSB* mixing [9], the OPLL forces a frequency offset of controlled sign between the reference and slave lasers, generating optical frequency offsets, and WDM channel separations, at the ~ 1 ppm. precision of a microwave synthesizer (fig. 1b). This is *optical frequency synthesis*. Cascading such offset OPLLs, precise WDM combs can be generated.

In coherent receivers, WDM signals can be demultiplexed electrically [10] (fig. 2), replacing many WDM receivers with one PIC and one electrical IC. WDM signals at 25GHz separation become electrical subcarriers at 25GHz separation, and are downconverted to DC. There are large potential power-savings; initial demonstrations [10] used several-Watt ICs, but power can be saved using CMOS time-domain mixers [11] and charge-steering logic [12]. Today's ICs support 600 GHz bandwidths [13], hence one such electrical IC might recover 48 WDM channels at 25 GHz channel spacing.

On-chip interconnect $CV_{DD}^2/2$ dissipation is a central barrier to improved digital systems [1,2]. Though tunnel FETs offer reduced V_{DD} , projected I_{on} is small [14], hence logic will be slow. Alternatives to the widely-studied tunnel FET thus warrant greater consideration. By operating finFETs near threshold (fig. 3) for low V_{DD} , and then increasing the fin height-spacing ratio [15,16] to offset the loss in on-current arising from the low V_{DD} , low $CV_{DD}^2/2$ dissipation, and moderately high drive current per unit IC area, hence low gate delay, can be obtained simultaneously. At the expense of two supplies and three PMOS thresholds, $CV_{DD}^2/2$ dissipation can also be reduced using circuit techniques with low-static-dissipation interconnect buffers with voltage gain (fig. 4). Here long interconnects are driven by gates with a low V_{DD} , producing a 200 mV swing. The interconnect receivers must have shifted V_{th} to maintain low I_{off} , hence have low I_{on} . Buffer gate delay is minimized by using only short interconnects ($< 1 \mu\text{m}$) between the line receivers and normal 500-mV- V_{DD} logic stages.

Work supported by DARPA PICO and NSF-NEB program. A portion of this work was performed in UCSB nanofabrication facility, which is part of the NSF-funded NNIN network, and in the MRL Central Facilities supported by the MRSEC Program of the NSF under Award MR05-20415

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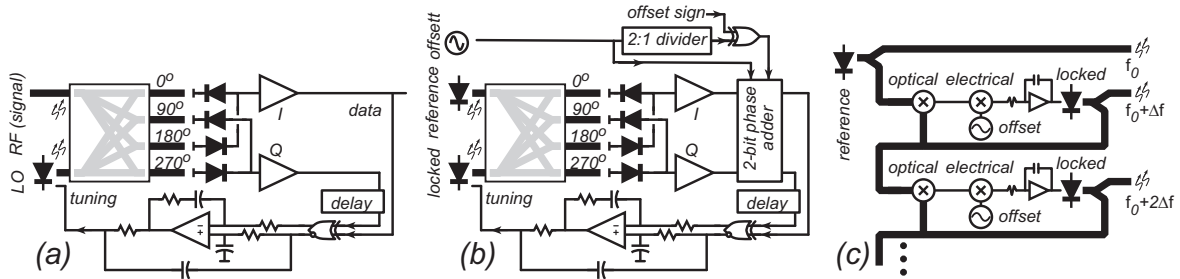


Figure 1: Phase-locked optical components: coherent BPSK optical receiver (a), optical frequency synthesizer (b), and precision generation, by optical frequency synthesis, of wavelength channel spacings within WDM (c).

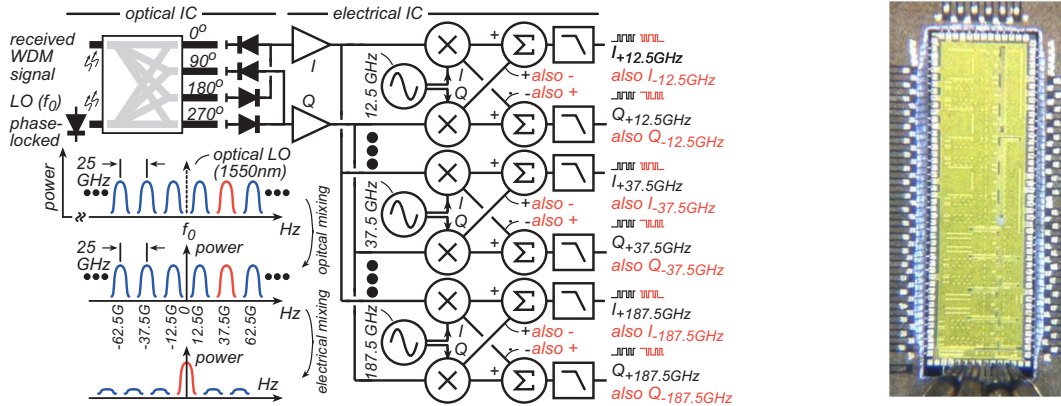


Figure 2: Receiver for demodulation of optical wavelength-division-multiplexing demodulation in the electrical domain; block diagram (left) and die photograph of prototype six-channel receiver (right).

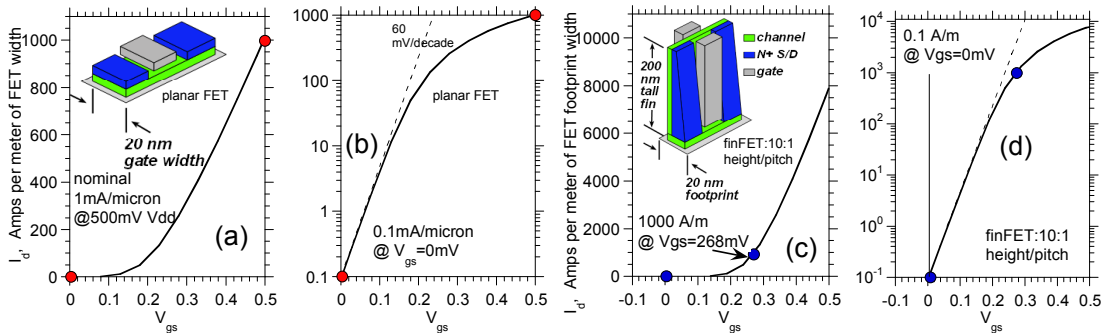


Figure 3: Simulated (a,b) characteristics of a planar ballistic FET with $I_{on}=1000\text{A/m}$ and $I_{off}=0.1\text{A/m}$ for a 500 mV supply. With a 10:1 height/pitch ratio, the same on- and off-current per unit footprint width (c,d) can be obtained with a 268 mV supply

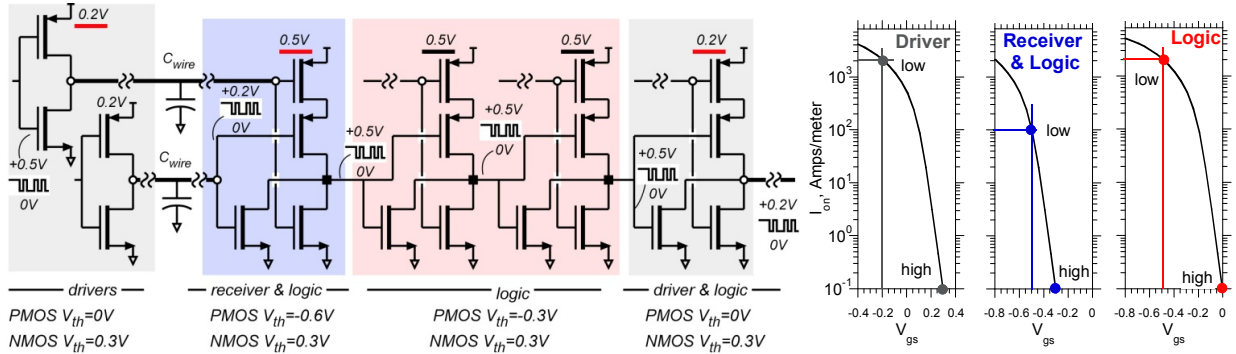


Figure 4: Voltage-gain buffering for reduced interconnect $CV^2/2$ dissipation. Long interconnects are driven by gates with a low V_{DD} , producing a 200 mV swing. Interconnect receivers have shifted V_{th} to maintain low I_{off} , hence have low I_{on} . Gate delay is minimized by using only short interconnects between the line receivers and 500-mV- V_{DD} logic stages.

Flexible, compact WDM receivers using cascaded optical and electrical down-conversion

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Abstract: We propose a super-channel flexible wavelength division multiplexing (WDM) receiver architecture. The receiver, which requires no optical filtering, only a pair (I and Q phases) of coherent optical detectors, and an electrical receiver system, can simultaneously recover multiple wavelength-multiplexed channels using cascaded optical and electrical down-conversion. The receiver data capacity increases in proportion to the number of electrical sub-carrier channels. The proposed receiver concept has been described using a six-channel WDM receiver, and a two-channel (± 25 GHz) receiver IC, which is a key block of the WDM receiver, has been successfully demonstrated with two and three 2.5Gb/s binary-phase-shift-key (BPSK) modulated channels.

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OCIS codes: (060.1660) Coherent communications; (250.5300) Photonic integrated circuits; (350.4010) Microwaves.

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1. Introduction

High spectral efficiency and high channel capacity wavelength division multiplexing (WDM) systems such as Tb/s super-channels [1–4] are needed to meet future demands for high data rate transmission. For these systems, simple hardware and low DC power consumption are both desirable. Moreover, WDM systems with elastic and flexible channel allocations have been proposed to aid in adapting to variations in network traffic and conditions [5,6].

A conventional coherent WDM receiver consists of a fixed- or flexible-grid optical demultiplexing filter and an array of coherent receivers, as is shown in Fig. 1(a) [1–4]. The photonic IC (PIC) is complex, containing the optical filter and an array of coherent receivers, each coherent receiver containing a local oscillator (LO) laser, a 90 degree optical hybrid, and a pair of balanced photodiodes (PDs). Each pair of PICs and electronics requires its own high-speed electrical interface [1,7]. The large number of components and interfaces can increase manufacturing costs and decrease manufacturing yield. The number of PIC components can be reduced by high-speed and high-resolution analog-digital-converters (ADCs) and digital-

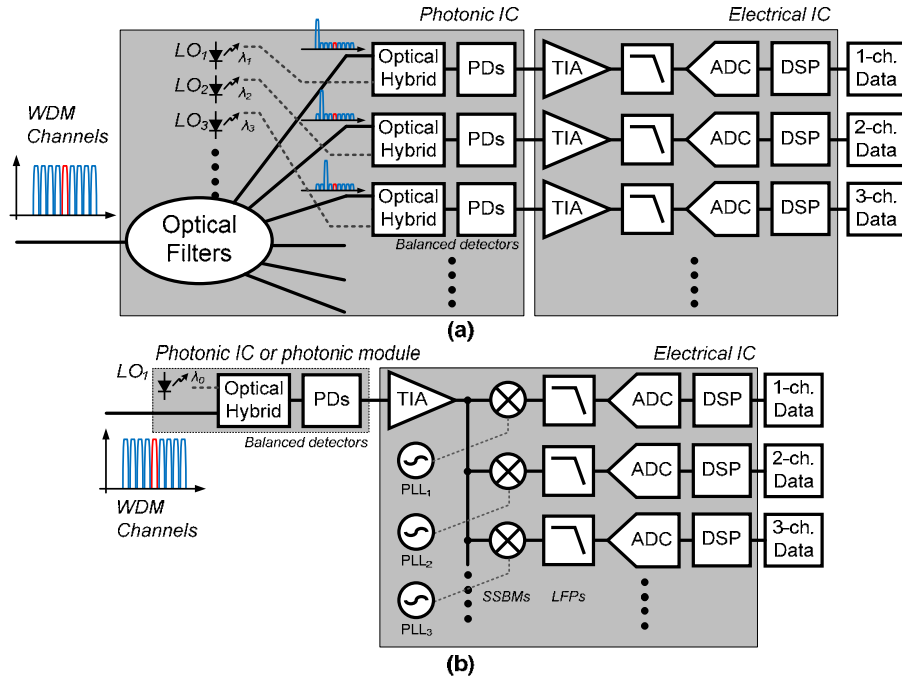


Fig. 1. Two different WDM receiver concepts: (a) conventional WDM receiver using optical filters, and (b) a new proposed WDM receiver.

signal-processors (DSPs), but this imposes a large power penalty and comes at the cost of reduced optical reach [7].

In this work, we propose and demonstrate a new coherent WDM receiver architecture (Fig. 1(b)) which can scale toward Tb/s operation while using only a pair (I and Q phases) of

optical detectors to recover multiple wavelength channels. The proposed receiver has a simple circuit configuration, can provide high spectral efficiency, and accommodates a flexible range of channel spacing and of data modulation formats. The complexity of the required PIC is greatly reduced, removing the optical filter and leaving only one set of balanced detectors and an LO laser. Most signal processing is instead performed in electrical integrated circuits (EICs). Sets of optical WDM channels are recovered in the EIC using single-sideband (SSB) mixers and their associated LOs as frequency down-converters. The EIC requires only a single broadband trans-impedance amplifier (TIA).

The channel capacity in the proposed receiver is ultimately limited by the bandwidth of the photodiodes (PDs) and of the de-multiplexing EIC. Very wide bandwidths are now feasible for these components. Uni-travelling carrier (UTC) PDs with 3-dB bandwidth $>300\text{GHz}$ [8] and high-speed InP hetero-junction bipolar transistors (HBTs) having power-gain cutoff frequencies $f_{\text{max}} >1\text{THz}$ [9] have both been reported. Even silicon-based transistors have attained $500\text{ GHz } f_{\text{max}}$ [10,11]. Amplifier EICs operating above 670GHz have been reported [12]. Given such components, the proposed receiver architecture can scale beyond 1Tb/s capacity using $>125\text{GHz}$ bandwidth PDs and EICs together with dual optical polarizations and 16-QAM modulation. Using 300 GHz photodiodes [8] and transistor amplifiers [12], a single EIC receiver could process 24 WDM channels at 25 GHz channel spacing. Further, in the proposed receiver, the optical channel wavelength allocation can be adjusted dynamically by tuning LO frequencies within the electrical frequency conversion circuits.

In this paper, an extension of [13], we first describe (section 2) the coherent multi-channel WDM receiver concept using cascaded optical and electrical down-conversions. We then describe (section 3) the component IC blocks of a two-channel ($\pm 25\text{GHz}$) implementation of the WDM receiver IC. Finally (section 4) we describe demonstrations of the two-channel receiver IC, including measurements of image rejection and of adjacent channel interference.

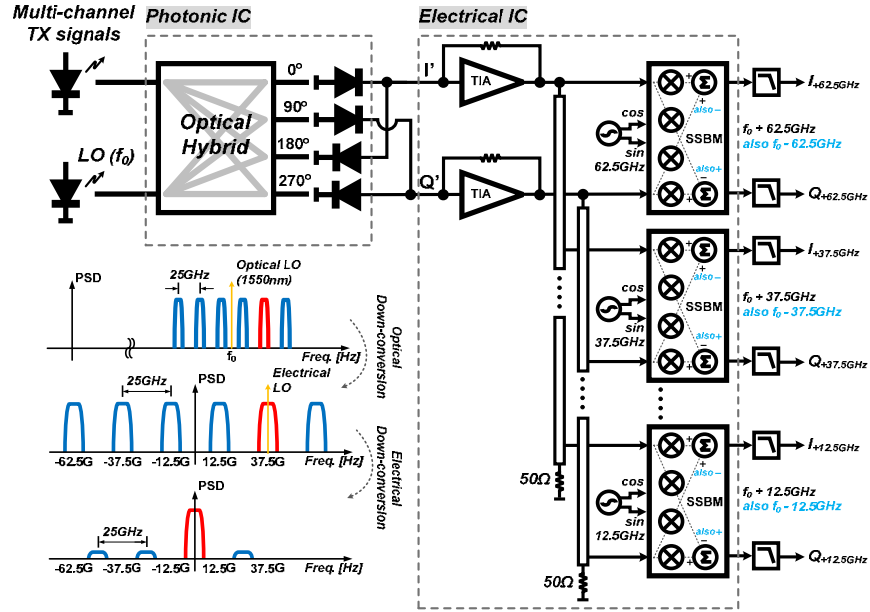


Fig. 2. A concept schematic diagram for a coherent single-chip multi-channel WDM receiver and its de-multiplexing flows for six modulated channels.

2. A single-chip multi-channel WDM receiver concept

Figure 2 shows a more detailed block diagram of the WDM receiver using, as an illustration, a six-channel configuration with 25GHz channel spacing. The receiver can de-multiplex these

six channels simultaneously using a single PIC with only a pair (I and Q) of detection channels and a single EIC. The PIC is a standard coherent balanced detector. The EIC includes a broadband TIA, clock and RF signal distribution networks, and broadband analog SSB mixers. Use of single-sideband (SSB) mixers permits the receiver to recover, without crosstalk, WDM channels lying both above and below the frequency of the optical LO. This SSB mixing therefore doubles number of the optical WDM channels which can be recovered within a given EIC and PD analog bandwidth. De-multiplexing of the six WDM carriers proceeds as follows:

- 1) An optical hybrid combines the six modulated WDM channels with a relatively strong optical LO (f_0) mixing these together on balanced photodiodes. In this optical down-conversion, the WDM channels become six electrical RF sub-carriers at 25 GHz spacing (± 12.5 GHz, ± 37.5 GHz, and ± 62.5 GHz).
- 2) Each RF sub-carrier is then down-converted to a baseband using a SSB mixer. This recovers both the I and Q components of the optical modulation. Independent SSB mixers independently recover the (± 12.5 GHz, ± 37.5 GHz, and ± 62.5 GHz) sub-carriers.
- 3) Low-pass filters in the I and Q outputs suppress interference from adjacent channels. Data can then be recovered through standard ADC and DSP.

Note that if the optical wavelength separations in the WDM transmitter are set by optical wavelength synthesis [14], then the WDM channel frequency separations are determined by the precision of the microwave synthesizers used to set the optical frequency offsets. In this case, the SSB mixers can use stable but asynchronous local oscillators with the resulting LO phase and frequency errors corrected by electrical differential phase-shift-keying demodulation [15].

3. Designs for two-channel (± 25 GHz) receiver IC

To demonstrate the proposed WDM receiver concept, a two-channel receiver IC, a key block of the WDM receiver, was designed using Teledyne Science Company's 500nm HBT process, using transistors with 300GHz f_T and f_{max} [16], and tested using two and three wavelength-modulated channels. Figure 3(a) shows the schematic of the 2-channel receiver EIC, while Fig. 3(b) shows a die photograph. The six-channel receiver of Fig. 2 was also designed and fabricated; to date, six-channel optical system experiments have not yet been completed, and we describe only results with the 2-channel unit.

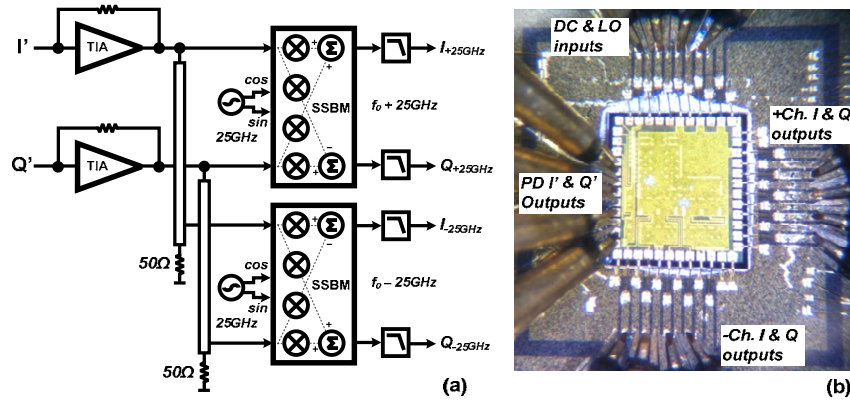


Fig. 3. (a) An EIC schematic for a two-channel (± 25 GHz) receiver IC, and (b) a photograph of the fabricated and mounted EIC on the test AIN board.

The PIC I' and Q' output signals are amplified with DC-107GHz broadband amplifiers [17] at the EIC inputs. In the present demonstration, an electrical LO is generated off-chip; internal to the EIC, polyphase filters and limiting amplifiers generate the quadrature LO

signals needed for the Weaver-configuration analog SSB mixers. RF signals within the EIC are routed using 50Ω transmission-lines and buffer amplifiers. The present ICs were designed without attention to DC power consumption; power consumption of future versions of the IC could be greatly decreased by minimizing the number of such internal 50Ω interconnects. The recovered I and Q components of each down-converted carrier are available at the EIC outputs; these I and Q signals are low pass filtered and amplified off-chip. Since the full amplitude and phase information of the input WDM carrier is preserved during down-conversion, the receiver is in principle compatible with any higher-order modulation formats (e.g. QPSK or 16-QAM). Using this receiver EIC, the two modulated channels with 50GHz channel spacing can be de-modulated simultaneously on $f_0 \pm 25\text{GHz}$ optical channels.

4. System demonstrations and experimental results

To demonstrate the WDM receiver system, using the two channel receiver IC (Fig. 3) we have measured image rejection for the two modulated carriers at $f_0 \pm 25\text{GHz}$, and thus $\pm 25\text{GHz}$ electrical sub-carriers, and have measured adjacent channel interference using three modulated carriers with channel spacing varying from 5GHz to 20GHz.

4.1 Image rejection experiment

To double the number of WDM channel processed, the SSB mixers were used in the receiver IC, independently recovering signals both below and above the optical LO frequency. Figure 4 shows a test configuration of the image rejection experiment. Three free-running distributed feedback (DFB) lasers, which have a narrow linewidth and low relative intensity noise (RIN), were used: L_1 as a transmitter carrier laser #1 at optical carrier frequency $f_0 + 25\text{GHz}$, L_2 as a transmitter carrier laser #2 at frequency $f_0 - 25\text{GHz}$, and L_3 as the LO laser at frequency f_0 . The carrier lasers L_1 and L_2 were modulated using 2.5Gb/s binary-phase-shift-keying (BPSK) data with two pseudo-random-binary-sequence (PRBS) pattern generators and Mach-Zehnder modulators (MZMs). PRBS of lengths $2^{31}-1$ and $2^{15}-1$ were applied to lasers L_1 and L_2 in this test. The modulated channels are combined in a 50%/50% optical directional coupler and coupled to the optical signal port of the receiver, with the LO laser L_3 connected to the receiver LO port.

In this experiment, we used a free-space 90° optical hybrid and balanced PDs contained in an Agilent optical modulation analyzer (OMA) N4391A. The balanced PDs have >33GHz 3-dB-bandwidth. The relative delays of the I'-channel and Q'-channel cables between the OMA and the two-channel receiver IC were carefully matched within 50ps by adjusting RF cable lengths and using phase shifters (PSs). This delay mismatch limited the bit rate to no more than 2.5Gb/s, but this mismatch issue can be solved by the hybrid integration of PIC and EIC. The EIC was contacted using multi-finger GGB RF probes. The two-channel receiver IC has I and Q outputs for both the $\pm 25\text{GHz}$ channels. One pair of $I_{\text{ch+}}$ and $Q_{\text{ch+}}$ outputs was low-pass filtered, amplified, and stored in an Agilent real-time oscilloscope (DSA-X 92004A). Frequency and phase errors were corrected by DSP (in this work, we used a simple phase error estimation technique using a Matlab code), thereby recovering the I-Q transmitted data

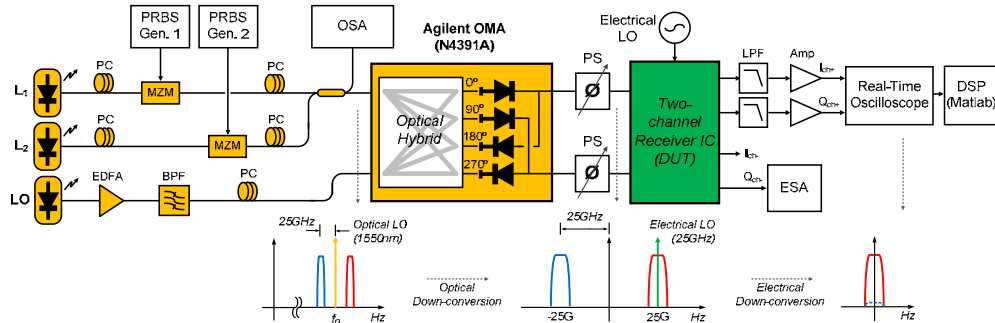


Fig. 4. Test setup for image rejection using two wavelength channels.

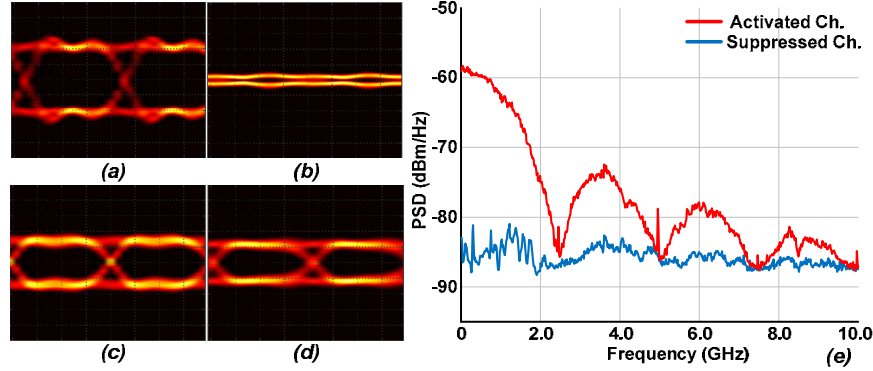


Fig. 5. Experimental results for image rejection measurement: (a)-(b) the eye diagrams for the activated (+) channel and the suppressed (-) channel with a single modulated carrier, (c)-(d) the eye diagrams for the (+) and (-) channels with two modulated carriers, and (e) the measured output spectra when the signal and the adjacent (crosstalk) channels are active. Crosstalk suppression is ~ 25 dB.

streams, as shown in Figs. 5(a)-5(d). The second pair of I_{ch} - and Q_{ch} - outputs was connected to an electrical spectrum analyzer (ESA) to monitor the suppression of adjacent-channel interference in the frequency domain. Figure 5(e) shows the spectra measured from the EIC output, comparing the cases when the lasers L_1 and L_2 are both active.

Figures 5(a) and 5(b) show the recovered data outputs on (+) and (-) channels using a single 2.5Gb/s BPSK modulated carrier (L_1 is on and L_2 is off) without the 50%/50% directional coupler. After the post signal processing, Fig. 5(a) shows fully activated (open) eye diagram on the (+) channel, and Fig. 5(b) shows suppressed (closed) eye diagram on the (-) channel. Figure 5(e) indicates that there is about 25dB (18:1 in voltage) image rejection ratio between the activated and suppressed channels. This is typical of that expected for well-designed SSB mixers. Regarding two 2.5Gb/s BPSK modulated carriers (L_1 is on and L_2 is on), both (+) and (-) channels show open eye diagrams, as shown in Figs. 5(c) and 5(d). The slightly degraded eye diagrams in this test are most likely because the input power to the two-channel receiver IC is 2:1 lower than that in the experiment involving only a single modulated carrier.

4.2 Adjacent channel interference experiment

To measure receiver crosstalk from adjacent channels and to determine the maximum spectral efficiency given the minimum channel grid spacing, three-channel experiments were performed using the test configuration shown in Fig. 6. Three DFB lasers and a Koshin (LS-601A) tunable laser, which also have a narrow linewidth and low RIN, were used: L_1 as a transmit carrier laser #1 at an optical frequency variable from $f_0 + 5$ GHz to $f_0 + 20$ GHz, L_2 as a fixed transmit carrier laser #2 at an optical frequency $f_0 + 25$ GHz, L_3 as a transmit carrier laser #3 at an optical frequency variable from $f_0 + 30$ GHz to $f_0 + 45$ GHz, and L_4 as a fixed LO laser at frequency f_0 . Again, three channels of 2.5Gb/s BPSK data were modulated on the carrier lasers of L_1 , L_2 and L_3 using differential outputs of a PRBS $2^{31}-1$ pattern generator and two MZMs as shown in Fig. 6. The two patterns were de-correlated using a path length difference of about one meter. The three modulated channels are combined using 50%/50% directional couplers and the power of each channel is equalized and monitored through an APEX high-resolution optical spectrum analyzer (OSA). Figure 7 shows the measured spectrum of the three optical modulated channels with channel grids of (a) 20GHz, (b) 10GHz and (c) 5GHz, the final case having no frequency guard band.

In this experiment, the qualities of the recovered data were measured and compared in Fig. 8 for the different channel spacing and differing combinations of input and output low-pass filter bandwidths. Here filter #1 is low pass filters (LPFs) located before the optical

modulators (MZMs) to suppress spectral side lobes in the transmitted optical spectrum, while filter2 is LPFs located at the two-channel receiver IC outputs to suppress adjacent channel interference. With 2.2GHz LPFs in the transmitter and 3GHz LPFs in the receiver, even with a 5GHz channel spacing, corresponding to no frequency guard band, a signal-to-noise including interference ratio (Q-factor), extracted from eye diagram outputs, of approximately 10:1 is measured. Note that $Q = 6$ corresponds to 10^{-9} bit error rate given Gaussian statistics.

As Fig. 8 demonstrates, the receiver IC operates with high signal/crosstalk ratios even when channels carrying 2.5Gsymbol/second modulation are spaced in frequency by only 5 GHz; the proposed WDM receiver system provides high spectral efficiency.

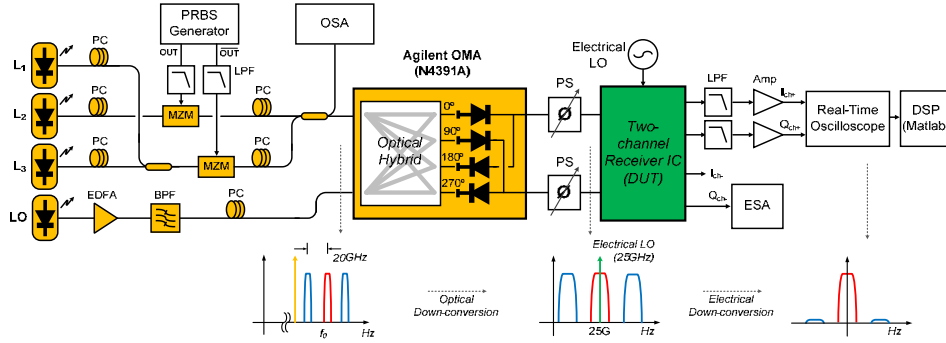


Fig. 6. Test setup for adjacent channel interference measurements using three wavelength channels.

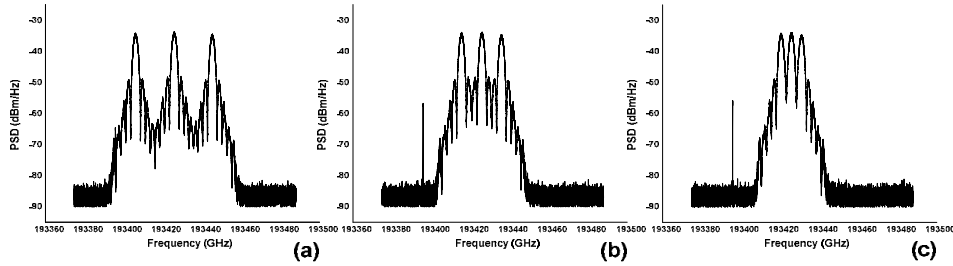


Fig. 7. Measured optical spectra for different channel spacing: (a) 20GHz, (b) 10GHz, and (c) 5GHz. The narrow band tone visible in (b) and (c) is from the LO laser.

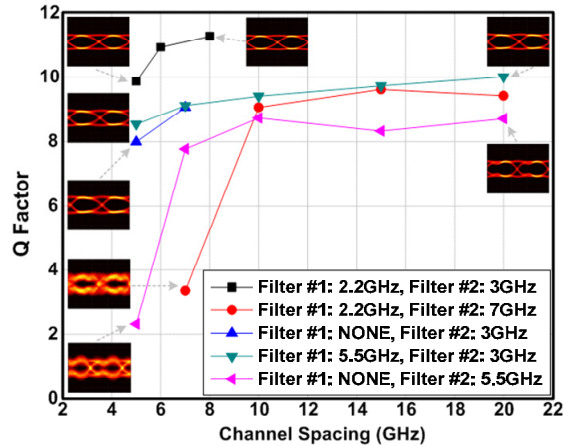


Fig. 8. Measured eye diagram qualities for the different channel spacing and filter combinations (filter #1 – before the optical modulators, and filter #2 – after the EIC).

5. Conclusion

We have demonstrated WDM receiver using cascaded optical and electrical down-conversion to recover multiple optical wavelength channels. Given the demonstrated bandwidths of modern photodiodes and EICs, the receiver can readily scale to a large number of WDM channels using only a single (I and Q) pair of optical coherent detection channels. Initial demonstrations indicate high image rejection and low adjacent channel interference.

Acknowledgments

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Fully integrated hybrid silicon free-space beam steering source with 32 channel phased array

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ABSTRACT

Free-space beam steering using optical phased arrays is a promising method for implementing free-space communication links and Light Detection and Ranging (LIDAR) without the sensitivity to inertial forces and long latencies which characterize moving parts. Implementing this approach on a silicon-based photonic integrated circuit adds the additional advantage of working with highly developed CMOS processing techniques. In this work we discuss our progress in the development of a fully integrated 32 channel PIC with a widely tunable diode laser, a waveguide phased array, an array of fast phase modulators, an array of hybrid III-V/silicon amplifiers, surface gratings, and a graded index lens (GRIN) feeding an array of photodiodes for feedback control. The PIC has been designed to provide beam steering across a $15^\circ \times 5^\circ$ field of view with $0.6^\circ \times 0.6^\circ$ beam width and background peaks suppressed 15 dB relative to the main lobe within the field of view for arbitrarily chosen beam directions. Fabrication follows the hybrid silicon process developed at UCSB with modifications to incorporate silicon diodes and a GRIN lens.

Keywords: silicon photonics, LIDAR, free-space communication, optical phased array, laser, tunable laser, hybrid silicon, integrated optics, beam steering, photonic integrated circuit

1. INTRODUCTION

Free-space beam steering has a wide range of applications. Of particular interest is light detecting and ranging (LIDAR) which collects high resolution three-dimensional images at high data acquisition rates. LIDAR can be used regardless of ambient light conditions and has better resolution than radar. It can even capture high resolution images beneath forest canopy and camouflage netting^[1]. Another application of interest is free-space point-to-point communication links where beam-steering maintains continuous data transmission by compensating for relative shifts in position between link points due to accidental (e.g. building sway) or purposeful (e.g. vehicle/satellite travel) movement. Additionally, one can select between several receiving points for selected bursts of data transmission.

Many implementations of free-space beam-steering require mechanically moving parts which are susceptible to mechanical wear and which typically suffer in performance due to vibrations and inertial forces.

1.1 Optical phased arrays and silicon photonics

Optical phased arrays offer an alternative method of beam-steering and shaping that requires no moving parts^[2], and have been used to demonstrate both LIDAR^[3] and free-space communication links^[4]. Typically these applications have been implemented by assembling individually packaged optical components into a larger system. However, there are several advantages to using an integrated approach where most optical components are combined within a single photonic integrated circuit (PIC)^{[5][6]}.

The integrated approach toward photonics reduces the overall size, weight, and cost of a device by removing packaging for individual components. It also removes much of the difficulty and cost of aligning each component with the others.

Additionally it is more tolerant to mechanical stresses from vibrations that might cause misalignment in assembled devices.

Silicon photonics provides a viable platform to realize integrated optical phased arrays while taking advantage of the CMOS processing facilities and knowledge that have accumulated over the past few decades. In recent years, optical phased arrays have been demonstrated using a silicon-on-insulator (SOI) platform with passive silicon waveguides and output gratings combined with resistive heaters for phase control^{[5][6][7]}, but this approach has demonstrated beam-steering using off-chip laser sources. While partial integration is an improvement, these devices still suffer from the additional packaging and aligning needs and the vibrational intolerance which come from separate components. Fiber-coupling to SOI adds the further disadvantage of a large difference in refractive index which introduces coupling losses. Additionally, propagation losses along different channels will inevitably be unequal due to processing variations, which will limit the accuracy of the optical phased array. Optical coupling and propagation losses reduce the efficiency of the device and limit the output power in the main beam lobe.

The hybrid silicon platform developed at UCSB^{[8][9]} offers a method well-suited for integrating an optical phased array with on-chip light amplification. III-V material is bonded to SOI wafers already patterned with passive waveguides, splitters, and output grating couplers. III-V devices are patterned and defined with lithography, giving nano-scale alignment. Light from the waveguides evanescently couples into the III-V quantum wells for light amplification and allows both amplifiers and lasers to be fully integrated with the passive devices. This report describes the design, fabrication, and demonstrated beam-steering of such a device.

2. CONCEPT

An optical phased array designed for two-dimensional beam-steering and shaping is typically formed by arranging emitter elements in a two-dimensional matrix. The far-field sum of the outputs can be shaped into a beam and steered to a desired angle by phase-tuning each element in the matrix. This method works well but has a fundamental problem with scalability. For an $N \times N$ matrix, N^2 phase controls are needed.

Alternatively, two-dimensional beam-steering can be achieved with a one-dimensional optical phased array using a surface grating emitter which acts as the second dimension of the optical phased array. In this configuration, each tooth of the grating scatters power from the optical mode with a phase delay dependent on the effective index of the mode. Emission from a single channel becomes a line in the far-field (perpendicular to the waveguide direction of propagation) with the emission angle determined by wavelength (λ), the waveguide effective index (n_{eff}), and the grating period (Λ) as shown in Eq. (1)

$$\sin(\theta) = \frac{\Lambda n_{\text{eff}} - \lambda}{\Lambda}. \quad (1)$$

Thus, by simply tuning the wavelength, the beam can be steered in one axis. The beam will be passively collimated in that axis to a degree dependent on the length of emission along the grating. By combining an array of surface grating emitters two-dimensional beam-steering can be achieved where the axis parallel to the waveguides (henceforth referred to as θ) is tuned with wavelength and the axis perpendicular to the waveguides (henceforth referred to as ψ) is tuned by phase-tuning the individual channels.

The simplest version of this configuration with N channels can be realized using a tunable laser coupled to a beam-splitter tree of $N-1$ splitters which separates the beam into N channels, a phase modulator for each channel, and a grating emitter for each channel. This can be achieved with an off-chip laser source and resist-heaters for tuning elements, and was demonstrated in Generation I^[6]. However, better functionality can be achieved by using a hybrid silicon platform to incorporate an on-chip laser, a pre-amplifier, and gain elements for each channel to compensate for channel-dependent losses and to increase the overall output of the device. Such a PIC would require $2N + 2$ controls as opposed to the N^2

controls required by the standard configuration. Tuning the θ axis with wavelength removes an entire dimension of control requirements. A CAD layout of a 32-channel design is shown in Figure 1.

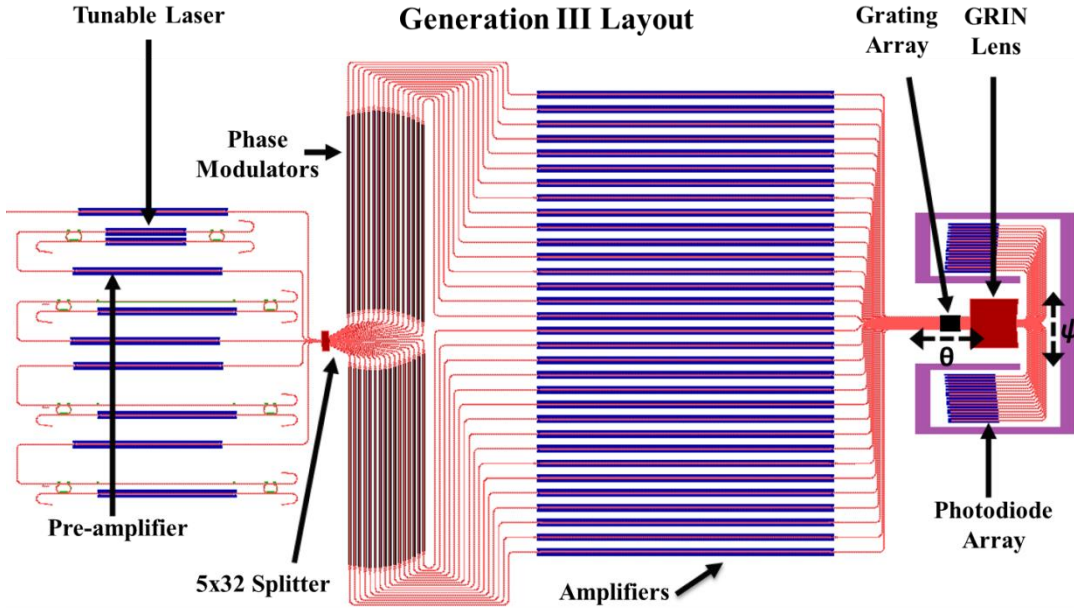


Figure 1. Layout of the 32-channel PIC. Redundant tunable laser sources are followed by semiconductor optical amplifier (SOA) pre-amplifiers. The beam is split into 32 channels which are individually phase tuned and amplified. The channels feed an array of surface grating for free-space emission. The angle of emission of the beam is determined by wavelength in the θ axis and by relative phase in the ψ axis. The remaining beam power is imaged into the far field with a Fourier lens feeding photodiode array for on-chip feedback.

3. COMPONENT DESIGN

3.1 Channel output spacing and count

The angular separation between the main lobe and the side lobes in the ψ axis is determined by the channel spacing d between output waveguides (center to center). Decreasing the channel spacing increases angular separation. Also, the peak power in the side lobes is a function of the ratio of output waveguide width to channel spacing, so an optimized system requires large output waveguides with slightly larger channel spacing. Practically, there must be a finite spacing between waveguides to prevent the modes from overlapping and causing crosstalk between channels. A final consideration is that increasing the total width of the array (i.e. the product of $(N-1) \cdot d$, where N is the number of channels and d is the channel spacing) decreases the width of the beam and increases the ratio of power in the main lobe to power in the side lobes. Plots of the calculated side lobe separation vs. channel spacing and beam width vs. array width are shown in Figure 2.

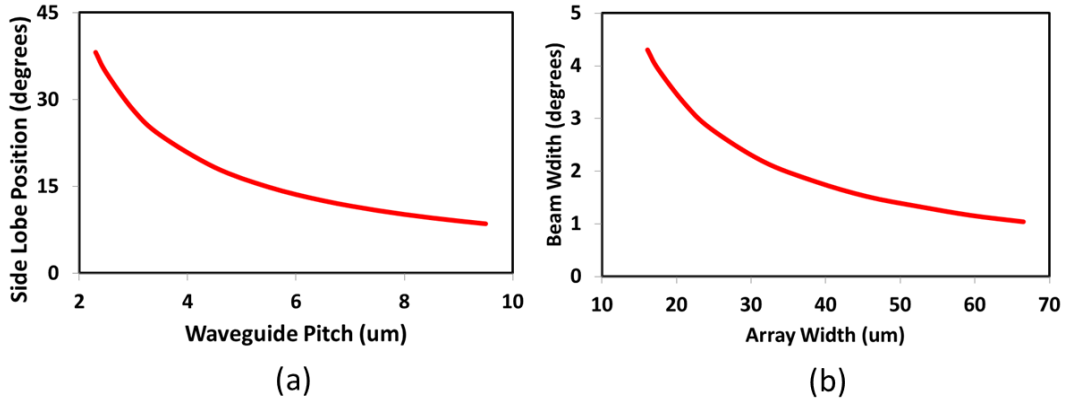


Figure 2. (a) Calculated far field separation between main lobe peak and side lobe base (i.e. where the side lobe rises above -10 dB relative to the main lobe peak) vs. waveguide pitch, and (b) calculated far field beam width vs. total array width.

3.2 Laser and amplifiers

The gain elements for the tunable laser and the SOAs were based on the design reported by Kurczveil et al.^[10] with an alteration of the width of the rib waveguide to 2.5 μm within the SOA gain regions so as to increase mode volume and maximum output power. The length of the channel amplifiers was chosen as 2.3 mm for high output powers, while the preamplifier length was chosen as 1 mm.

The tunable laser (Figure 3) was designed using two bus waveguides, each with a gain section, coupled together using two ring resonators as described in ^[11]. The rings are chosen of circumferences 400 μm and 420 μm respectively such that their respective transmission spectra overlap only once within the gain bandwidth of the device (Figure 4). The tunable laser had a narrow linewidth of less than 1 MHz over the tuning range. Typical linewidth and side mode suppression measurements are shown in Figure 5. Thermo-optic tuning of the ring spectra allowed the transmission peak to be tuned over 41 nm (Figure 6).

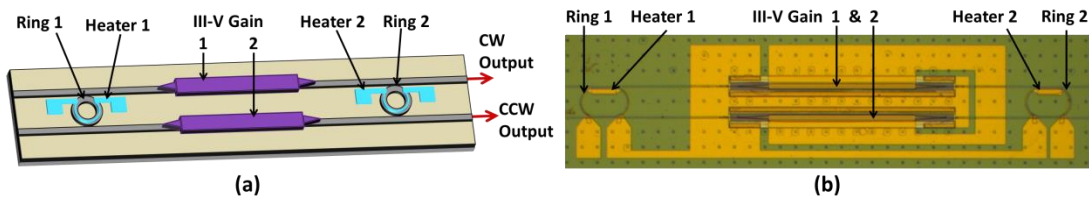


Figure 3. (a) Schematic and (b) photo of the hybrid silicon tunable laser developed for the scanner

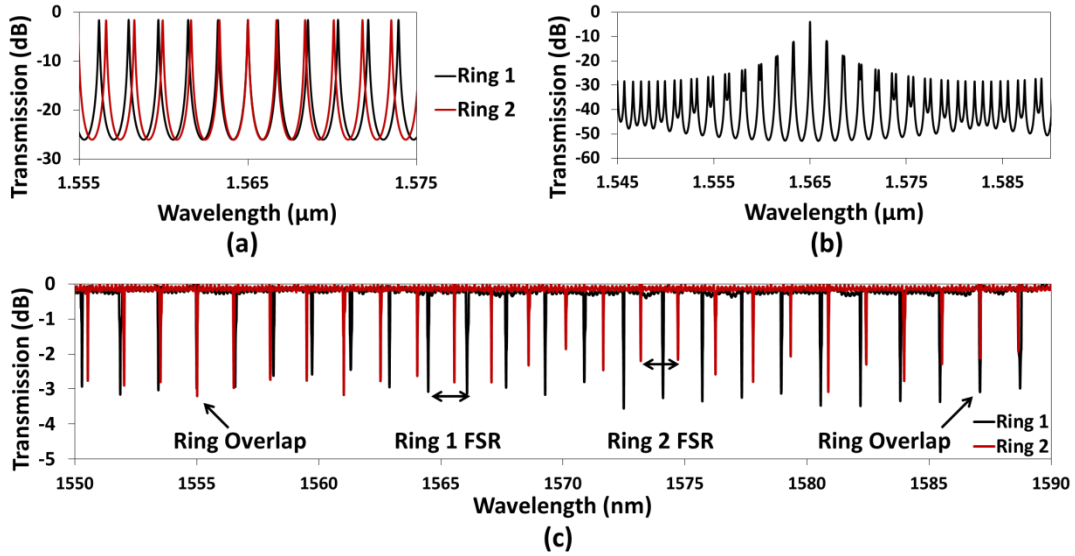


Figure 4. (a) Calculated transmission of the two rings, (b) calculated round-trip loss of the two rings, and (c) alignment of the FSR of the two measured rings showing the overlap of the FSR outside the gain of the hybrid silicon gain regions.

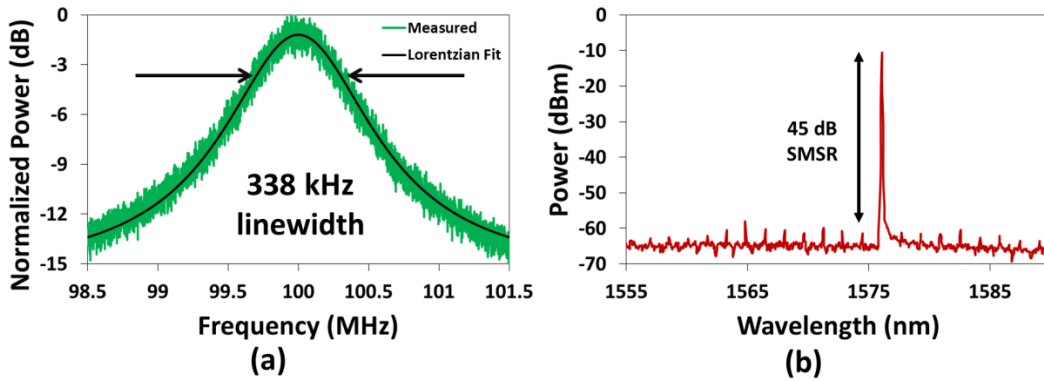


Figure 5. (a) Linewidth of the tunable laser and (b) side mode suppression of the other modes of the two cavities

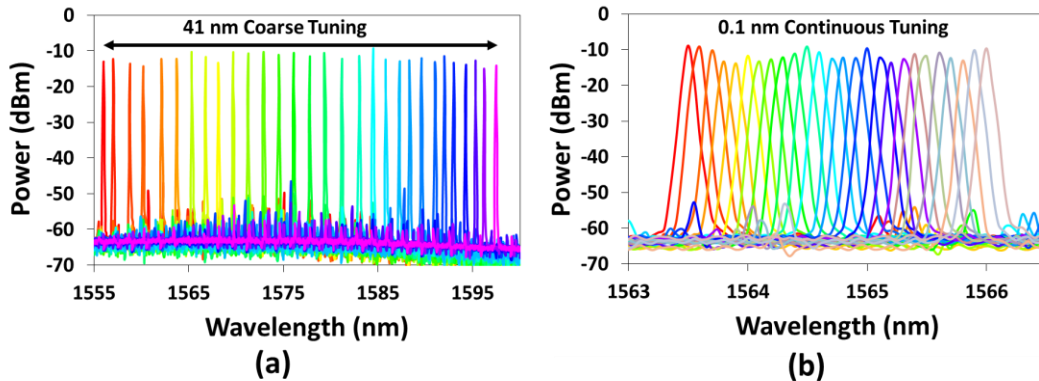


Figure 6. Superimposed spectra of tunable laser showing (a) coarse tuning over 41 nm and (b) 0.1 nm resolution fine tuning over 2.5 nm.

3.3 Phase modulators

The phase modulator was designed to tune phase thermo-optically by applying a forward bias to a $p-i-n$ diode overlapping the waveguide. Phase-dependent losses in the waveguide due to free-carrier absorption were made negligible by placing the n and p regions 11 μm apart.

Diode dopant profile after ion implantation and annealing was modeled using the Silvaco ATHENA software package, and the current-voltage characteristics and associated carrier densities within the waveguide were modeled using the Silvaco ATLAS software package. Carrier lifetimes within the waveguide were assumed to be 0.9 ns for this calculation in accordance with the data reported by Dimitropoulos et al.^[12]. Thermal tuning was predicted to be 57 mW/π using the relation given in Eq. (2)

$$P_{\pi} = \frac{\lambda \sigma w}{2t} \frac{dn}{dT}, \quad (2)$$

where λ is the wavelength, $\sigma = 1.35 \times 10^{-2} \text{W cm}^{-1} \text{K}^{-1}$ is the thermal conductivity of the buried oxide, $w = 10 \mu\text{m}$ is the effective width over which the heat is dissipated (approximated by the width of the intrinsic region), $t = 1 \mu\text{m}$ is the thickness of the buried oxide, and $dn/dT = 1.86 \times 10^{-4} \text{K}^{-1}$ is the thermo-optic coefficient of silicon.

The phase modulator was designed to be 2 mm long. A cross-section of the device and plots of phase shift and expected carrier density-induced loss vs. bias are shown in Figure 7.

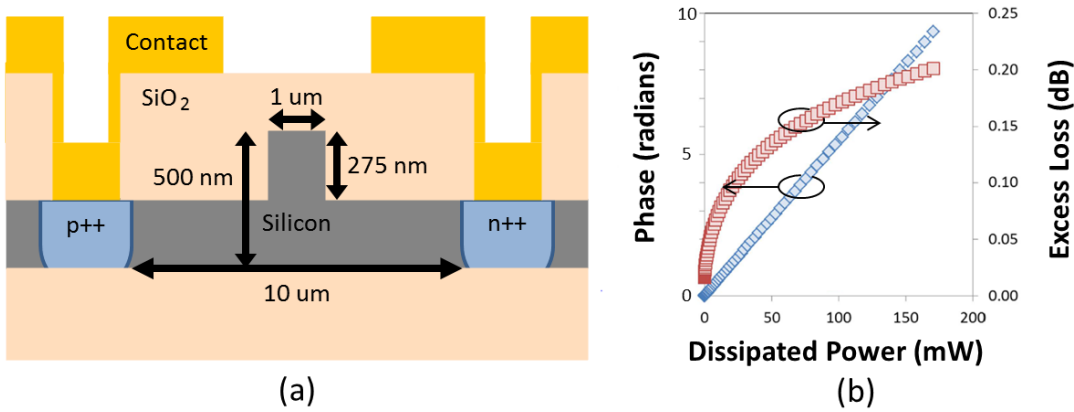


Figure 7. (a) Cross-section of the phase modulator profile, and (b) predicted thermo-optic tuning and free-carrier induced excess loss vs. thermal power.

4. FABRICATION

Device fabrication began with an SOI wafer with 500 nm top silicon and 1 μm buried oxide. Rib waveguides were lithographically patterned and etched to a depth of 275 nm. Phase modulator diodes were formed by implanting the silicon with boron and phosphorus dopants and then annealing for 10 minutes at 1050 $^{\circ}\text{C}$. Output surface gratings were patterned using e-beam lithography and then etched to a depth of 50 nm. III-V epitaxial material was wafer-bonded to the top silicon and then patterned and etched to form the laser and amplifier gain sections. Metal contacts were then deposited in an e-beam evaporation chamber. Buffer layers of SU8 and PECVD SiO_2 were used to prevent optical losses in the waveguide from metal traces.

5. GENERATION I^[6]

5.1 Generation I design

For simplicity, Generation I used an external laser capable of tuning from 1525 nm to 1605 nm. No gain elements were introduced on-chip, and active components were limited to resistive thermo-optic phase tuners overlaying the waveguides.

Specific goals for this system include a steering range of greater than 20° (ψ) \times 10° (θ), a full-width half-maximum (FWHM) less than 2° in both axes, and a side lobe suppression ratio (i.e. the ratio of the main lobe peak intensity to background peak intensity) of 10 dB within the 20° steering window. This translates into a matrix of 10 \times 5 resolvable spots in the far field.

To achieve the required 20° field of view, side lobes greater than 10 dB must fall outside that window even when tuning to the maximum angle (i.e. $\pm 10^\circ$). This requires that the channel spacing be no greater than 6.5 μm at a wavelength of 1550 nm. For this system we chose a channel separation of 3.5 μm which limits the significant side lobe suppression to beyond 23.7° from the center of the main lobe. For a far-field beam width of less than 2° the total array width must exceed 35 μm , thus for $d = 3.5 \mu\text{m}$ we chose $N = 16$. A 16-channel laser driver was purchased to interface with the device.

Surface gratings were chosen to have a pitch of 0.55 μm and a duty cycle of 20%.

The layout of the Generation I PIC is shown in Figure 8. Highlighted results are described below.

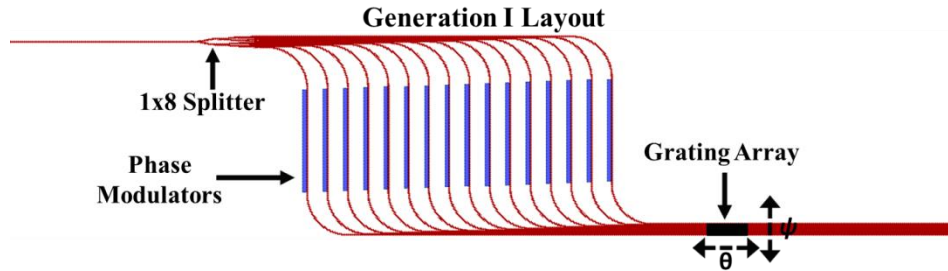


Figure 8. Layout of the Generation I device including 1x16 waveguide splitter, phase modulators, and grating array.

5.2 Generation I results

The output beam from the PIC was measured in the far field using an imaging lens system with an IR camera. A feedback algorithm adjusted the phase on each channel using the 16-channel laser driver, similar to the method described in [6].

Beam steering of $20^\circ \times 14^\circ$ was achieved. Profiles of the ψ axis normalized optical output power, both calculated and measured, are shown for four locations (Figure 9). Figure 10 contains plots of the beam profile for scanning across both dimensions, and 2D plots of the measured beam at the extents and center of the field of view are shown in Figure 11.

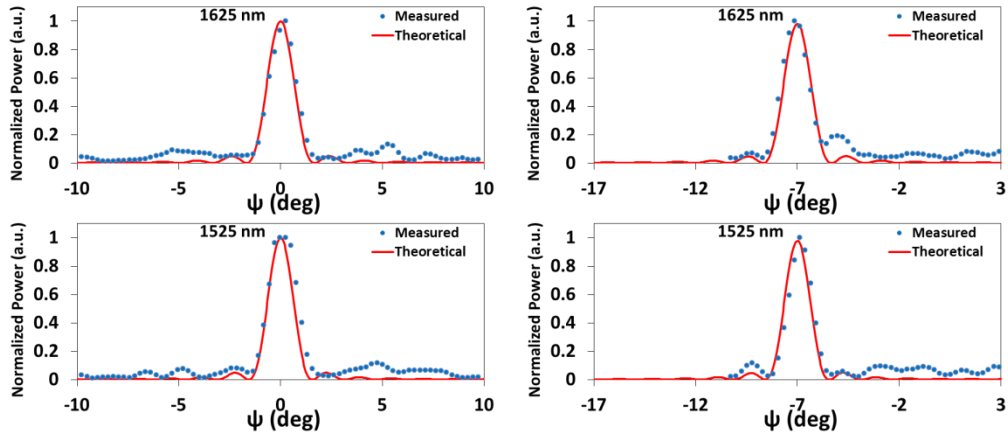


Figure 9. Plots of calculated and measured beam profiles in ψ with phase tuning to optimize side mode suppression at 0 and -7 degrees for 1525 nm and 1625 nm input wavelengths.

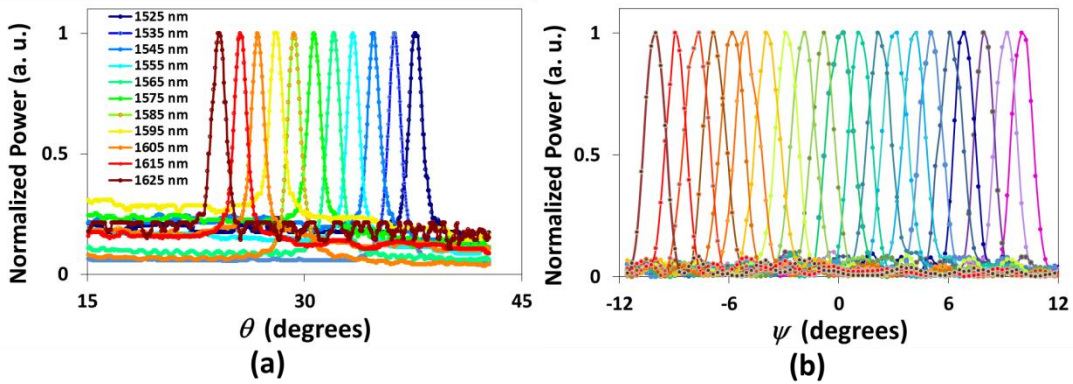


Figure 10. Normalized measured optical output power in the far-field (a) scanning wavelength and (b) phased array tuning.

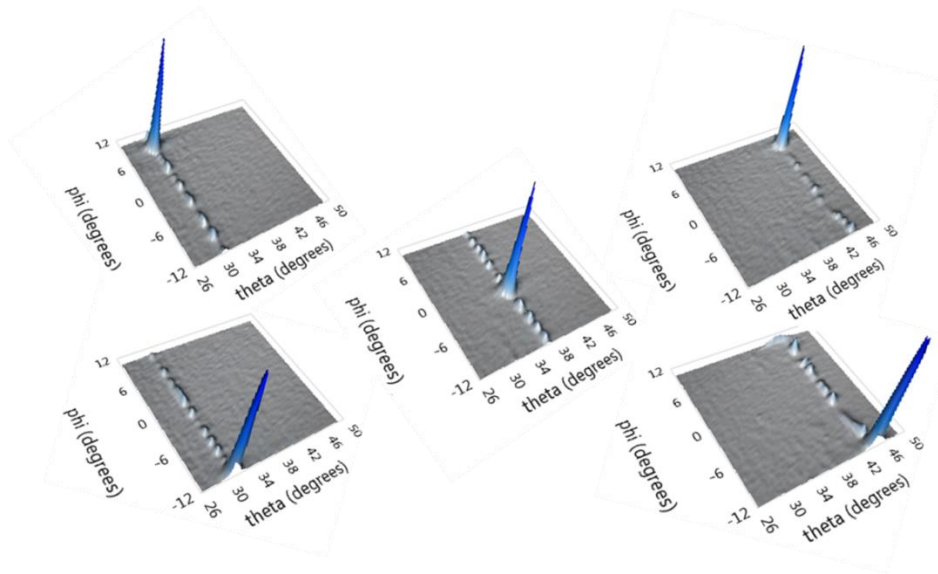


Figure 11. Plots of the measured beam profiles in the far field at the extents of the field of view. Secondary peaks are outside the field of view and not shown.

6. GENERATION II^{[13][14]}

6.1 Generation II design

The purpose of Generation II was to add on-chip laser and amplification sections. A reduction in the number of channels to $N = 8$ was required in order to drive channel amplifiers and phase modulators with the same 16-channel laser driver. To maintain a 2° beam width the channel separation was increased to $5.5 \mu\text{m}$ which limits the significant side lobe suppression to beyond 14.8° from the center of the main lobe and gives an expected field of view of greater than 12° in ψ . The on-chip laser described above was designed to have a 40 nm tuning range giving an expected field of view of 5.6° in θ .

Phase modulators for this generation used the *p-i-n* diode design described in Section 3.3 above.

The layout of the Generation II PIC is shown in Figure 12.

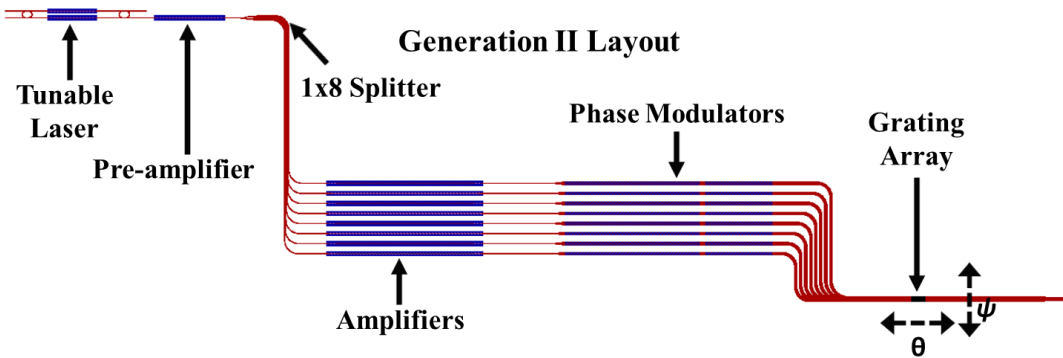


Figure 12. Layout of the Generation II device including tunable laser, pre-amplifier, 1x8 waveguide splitter, channel amplifiers, phase modulators, and grating array.

6.2 Generation II results

6.2.1 Tunable laser

The second generation chip had an eight channel emitter with an integrated tunable laser. The on-chip lasers were characterized and were found to typically have 5.5 mW output power, $< 340 \text{ kHz}$ linewidth, 45 dB side mode suppression, and 41 nm tuning range (1556 nm to 1597 nm), as described in Section 3.2 above. However, the particular laser integrated with the emitting array had faulty ring tuners, so only one axis of tuning for the integrated PIC is characterized below. The Generation III design has redundant on-chip lasers to avoid this problem.

6.2.2 Phase modulators

Phase tuner current-voltage characteristics were used to estimate the effective carrier lifetime, which was determined to be 1.9 ns instead of the predicted value of 0.9 ns . Calculations of the carrier densities suggested free-carrier absorption of 0.75 dB and free-carrier induced phase shift of -0.8 radians for 100 mW of dissipated power. The thermo-optic tuning efficiency including the negative effects from free carriers was measured on a Mach-Zehnder interferometer to be $97 \text{ mW}/\pi$. The measured result is shown in Figure 13 along with a fit curve using the carrier lifetimes derived from the current-voltage characteristic and the measured thermo-optic efficiency.

The silicon slab was etched down to the buried oxide between devices to reduce thermal crosstalk between channels. However, thermal isolation between the phase modulators and the SOAs was not sufficient to remove phase-dependent fluctuations in output power based on chip-scale heating.

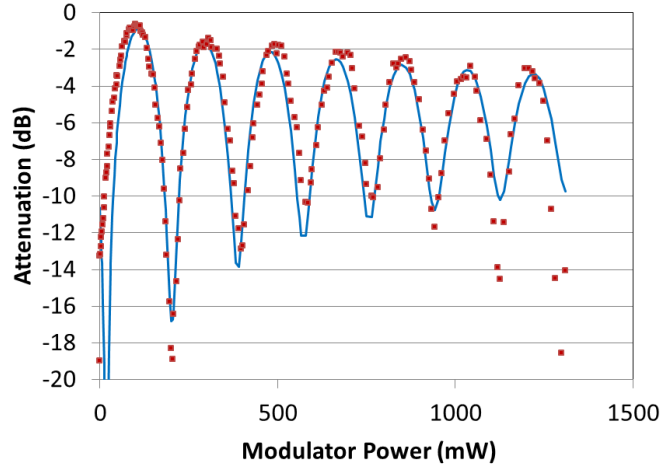


Figure 13. Thermo-optically tuned Mach-Zehnder interferometer transmission measurement and fit line. The fitted curve was calculated using the measured phase-tuning efficiency and the calculated attenuation from free-carrier absorption (deduced from the effective carrier lifetime).

6.3 Photonic Integrated circuit

Channel powers were equalized by emitting from one channel at a time and observing the intensity in the far field, then adjusting the SOA currents appropriately. One channel was found to be faulty in this device (channel 5) and was turned off for the remaining measurements – this limited the maximum possible background to 8.3 dB within the field of view. 7 dB background suppression was consistently measured with a beam width of 1.8° in the ψ axis and 0.6° in the θ axis.

Due to poor thermal isolation between the SOAs and phase modulators, SOA gain was highly dependent on the phase modulator settings. To reduce this effect and the overall temperature of the chip, phase modulator and SOA currents were cycled at 125 Hz, with a 20% duty cycle. The preamplifier was used to blank the beam for the first 800 μ s to avoid any contamination of the far-field signal while the phase modulators and SOAs were ramping up. During the profiling, the chip was mounted on a heat sink held at 18° C.

While holding the wavelength constant the beam was profiled and steered across the far field at 1° increments from -6° to $+6^\circ$ in the ψ axis. Wavelength tuning was not possible in this circuit due to faulty heater pads. However, with the 41 nm of tuning observed in a similar device on the chip, and with the measured wavelength steering of $0.14^\circ/\text{nm}$ for the surface gratings^[6], an expected 5.7° of tuning in θ axis is possible. A plot of measured and predicted beam cross-sections for each axis is shown in Figure 14, and plots of the beam steered to directions in the far field across a 12° range are shown in Figure 15.

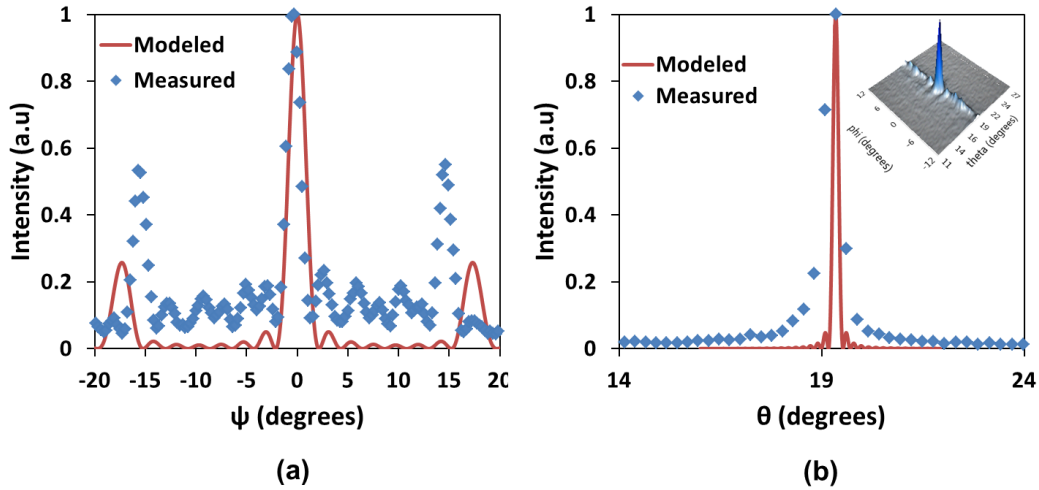


Figure 14. Measured and predicted beam cross-sections in (a) the phase-tuned ψ axis and (b) the wavelength-tuned θ axis. The inset shows the two dimensional profile of the beam.

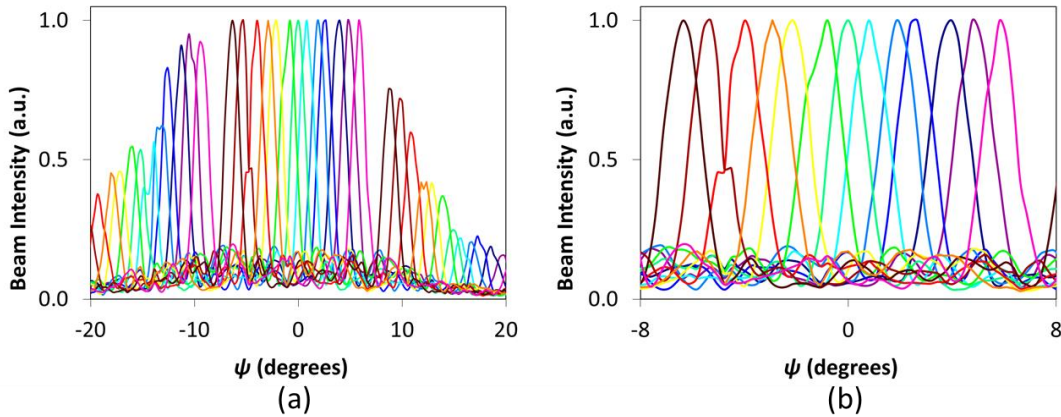


Figure 15. Measured beam profiles in the far field for the beam steered from -6° to $+6^\circ$ showing (a) both main and side lobes and (b) the aperture field of view.

As mentioned above, varying the phase modulator settings to change the output angle resulted in widespread chip heating. This affected the gain of the laser and amplifier elements and resulted in a non-uniform output beam power for disparate angles. However, it was found that these variations in beam output power could be completely compensated by adjusting the pre-amplifier pump current without altering the beam width or background suppression. Thus beam power was made flat as a function of steering angle.

The beam power was measured with a detector positioned in the far field and found to be $4.1 \mu\text{W}$. Side mode suppression and linewidth were measured by steering the beam to a fiber collimator connected to an APEX 2051A optical spectrum analyzer. Side mode suppression in the far field was 30 dB and linewidth was 36 MHz, both somewhat degraded from the standalone laser characteristics. This degradation is to be expected considering the many sources of feedback into the laser which come from the integrated device and is small enough as to not significantly affect the beam with respect to the target background suppression and beam width.

7. GENERATION III DESIGN

The Generation III design goals include > 20 dB background suppression, $< 1^{\circ} \times 1^{\circ}$ FWHM, and a $12^{\circ} \times 6^{\circ}$ steering window. This translates into an array of 12×6 resolvable spots. Tuning speeds higher than 4×10^6 /sec are also desired.

In addition to adjustments that have been made to the design of individual components such as phase modulators and gain elements, two additional components have been added to the PIC – A photonic crystal lens designed to convert the in-plane array output into the far field and a photodiode array were integrated for on-chip feedback. Figure 16 shows a block diagram of the 32 channel PIC.

Generation III chips are currently in fabrication and nearing completion with measured results pending.

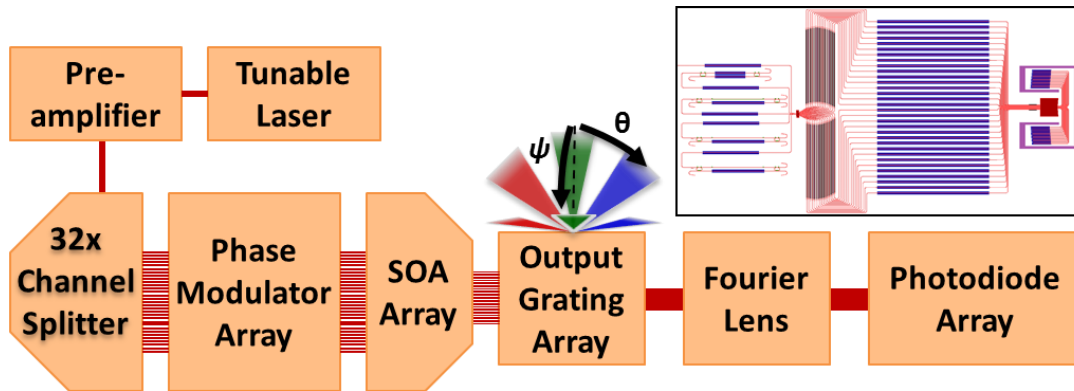


Figure 16. Generation III device configuration. The inset shows the CAD layout of the PIC.

7.1 Generation III channel output spacing and count

To decrease the beam width, the total width of the output array has been increased by changing the channel count to 32. Also, the channel spacing has been decreased in order to increase the angular separation of the side lobes.

Although the Generation I & II designs used uniform channel spacing, this is not necessarily the optimum geometry. Calculations were done using uniform, Gaussian, Lorentzian, and parabolic spacing. It was found that uniform and Gaussian spacing were the most promising geometries and devices with each were designed. They have respective total array widths of $126 \mu\text{m}$ and $144 \mu\text{m}$. The calculated far field beam is shown in Figure 17 for uniform output power and phase from each channel. Additional improvements can be made by varying the relative channel output powers and phases.

For the uniformly spaced channel device a star coupler was used to split the laser into the various channels with the intent that the central channels would receive more power relative to the outer channels. This should have a similar effect as the Gaussian spacing by concentrating more power toward the center of the output array. Adjustments to maximize the background suppression will be made with individual channel amplifiers.

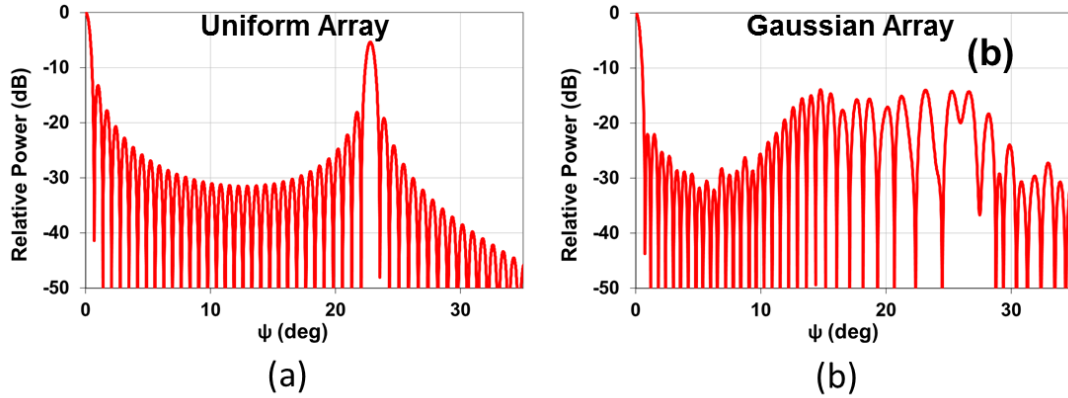


Figure 17. Calculated far field for (a) uniform and (b) Gaussian channel spacing using no relative phase or output power differences between channels.

7.2 Lasers, amplifiers and phase modulators

The gain elements used in this design were based on the same design as in Generation II but with shorter adiabatic tapers in the III-V. It was suspected that the longer tapers were not being pumped well and therefore generating excess loss.

To maximize yield, several lasers were coupled to the input of the PIC. One was chosen as the same design as in Phase I, and the rest were chosen with a similar design but with only one gain region of increased length. Also, a phase section using a resistive heater was added in place of the second gain region.

A pre-amplifier 1.5 mm in length was placed after each laser to maximize the input power before being split into channels. Each channel amplifier was chosen to be 3 mm in length to maximize the total output power.

7.3 Phase modulators

Phase modulators for this run were designed to employ electro-optic phase tuning in order to increase the tuning speed of the PIC. They were designed as *p-i-n* diodes similar to those in Generation II, but with the *p* and *n* regions closer together to decrease resistance. In this way less heat (which counteracts the electro-optic affect) is generated. The electro-optic tuning efficiency was measured on a Mach-Zehnder interferometer and found to be $14 \text{ mA}/\pi$. This falls within a low power regime where thermo-optic tuning is less present. The measured result is shown with a fit curve in Figure 18 along with the frequency response of the device. The device shows sufficient tuning speed for the proposed metrics with a 3 dB bandwidth greater than 50 MHz.

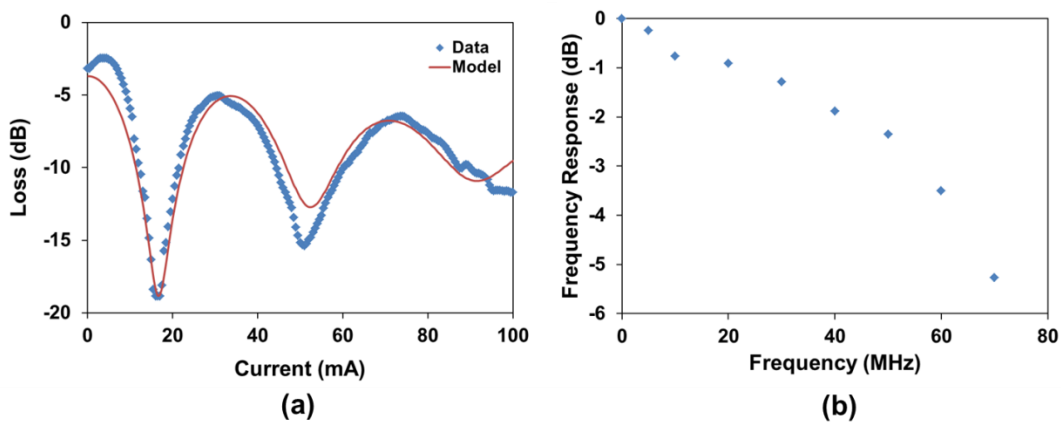


Figure 18. Output power relative to the loss of a straight waveguide (a) and frequency response (b) of a Mach-Zehnder modulator.

7.4 Lens and photodiode array

An on-chip feedback mechanism was designed using a 1D graded index (GRIN) lens to image the ψ axis far field onto a photodiode array positioned in the Fourier plane. The lens was made by varying the effective index across the top silicon layer of an SOI slab. Sub-wavelength circles with varied diameters were etched into the silicon and filled with SiO_2 . A parabolic index profile was designed by linearly varying the circle diameters (parabolically varying area) across the lens (Figure 19). A focal length of $473 \mu\text{m}$ is expected.

The waveguides feeding the photodiode array are located on the lens focal plane and span $64 \mu\text{m}$. There are 32 photodiodes giving 1.3° far field resolution and a total field of view of 41° .

Simulations of the electric-field profile and the expected power profiles at the output of the lens feeding the photodiode array are shown in Figure 20. The output powers incident on the photodiodes are calculated for several configurations of linear phase differences between adjacent channels of a uniformly spaced grating array.

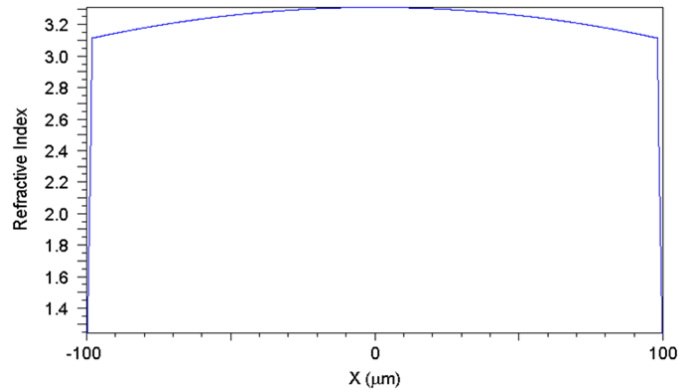


Figure 19. A plot of the calculated refractive index profile cross section for the GRIN lens.

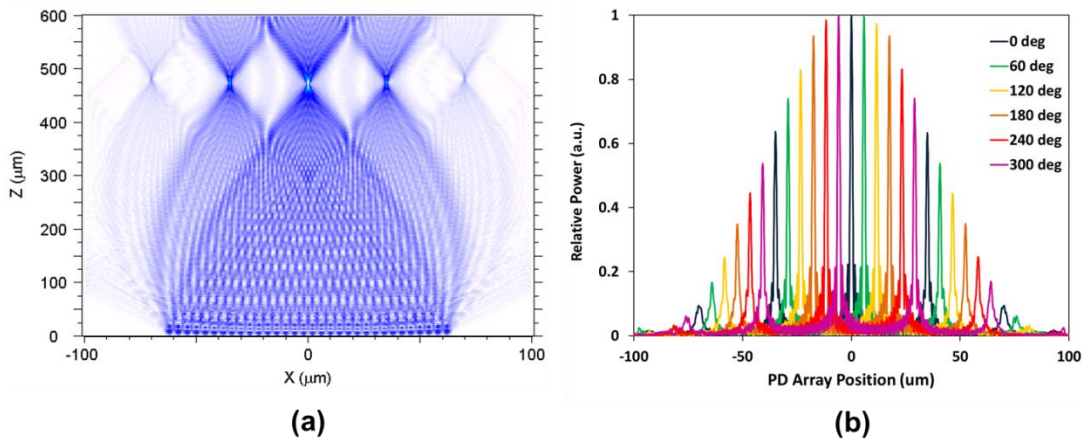


Figure 20. Simulated electric field profile for silicon GRIN lens (a) and calculated output powers from the lens for linear relative phase delays between adjacent channels.

7.5 Integrated 32 channel device

The layout of the full 32-channel device is shown in Figure 1. One of the larger challenges in driving this device is the difficulty in interfacing with the 100 different signals required. A driver board of significant complexity was designed, built, and programmed to supply current to the chip and receive communication from an external computer. As photonic integrated circuits grow in complexity, driving them and interfacing with them will be an increasingly difficult task.

8. CONCLUSION

A photonic integrated circuit fabricated on a hybrid silicon platform was demonstrated with free-space steering of a laser beam using an optical phased array integrated with a tunable laser. Phase controlled steering over 12° was achieved in ψ with a $1.8^\circ \times 0.6^\circ$ beam width, and the on-chip tunable laser was shown to having a tuning range providing 5.6° of steering in θ which results in a 7×9 resolvable spots in the far field with 7 dB background suppress.

A new photonic integrated circuit has been designed to achieve 12×6 resolvable spots with a beam width less than $1^\circ \times 1^\circ$ and rapid beam steering of steering 4×10^6 °/s in ψ .

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A Photonic Integrated Fractional Hilbert Transformer With Continuous Tunability

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Abstract: A continuously tunable fractional Hilbert transformer based on a photonic integrated chip in an InP-InGaAsP material system consisting of semiconductor optical amplifiers and current injection phase modulators is proposed and experimentally demonstrated.

OCIS codes: (250.5300) Photonic integrated circuits; (070.1170) Analog optical signal processing; (070.7145) Ultrafast processing

1. Introduction

The temporal fractional Hilbert transform (FHT) is a fundamental operator for signal processing that can find important applications, such as in communications systems [1] and digital image processing [2]. Compared with the conventional Hilbert transform (HT), the FHT permits an additional degree of freedom [3]. The FHT is usually implemented in the electrical domain using digital electronics, but with limited bandwidth and operating frequency. Due to the advantages of high speed and broad bandwidth offered by optics, the implementation of a microwave FHT using photonic techniques has been widely investigated recently [4-9]. These approaches can be classified into three categories. In the first category, an FHT was achieved based on a phase-shifted fiber Bragg grating (FBG) [4-6]. In [4], Asghari *et al.* proposed a uniform FBG with a single π phase shift in the middle of the grating to perform the HT. To obtain an FHT, Li *et al.* proposed to use the discrete layer peeling (DLP) method by which the FBG was directly designed based on the target response in the frequency domain corresponding to an FHT transmission function with a phase jump less or greater than π [5,6]. The major limitation of the FBG-based FHT is that the fractional order is not tunable. Once the FBG is fabricated, the order of the FHT is fixed. In the second category, an FHT was achieved in a photonic temporal pulse shaping (TPS) system. In [7], an FHT with tunable fractional order based on TPS was proposed and experimentally demonstrated. The fractional order of the proposed FHT was realized by applying a step function to a phase modulator to introduce a phase jump. Although a tunable fractional order was achieved, the system is complicated and costly due to the requirement of a high speed pattern generator to provide a fast step function. In the third category, an FHT was achieved by using a photonic microwave delay-line filter. A continuously tunable FHT can be implemented based on a multitap uniformly spaced or a nonuniformly spaced photonic microwave delay-line filter [8,9]. The multitap uniformly spaced filter should have negative coefficients which was realized based on polarization-modulation and polarization-modulation to intensity-modulation conversion in an optical polarizer [8]. The tunability of the fractional order was achieved by tuning the coefficient of the zero-th tap. Compared with the multitap uniformly spaced filter, a nonuniformly spaced delay-line filter is easier to implement and less costly since the negative coefficients can be equivalently realized through nonuniform sampling [9]. The FHTs in the three categories are implemented using discrete components with large size and poor stability.

In this paper, we propose a chip-scale tunable FHT in an InP-InGaAsP material system with semiconductor optical amplifiers (SOAs) and current injection phase modulators (PMs). The designed photonic integrated FHT employs a ring structure coupled with a bypass waveguide. The tunable coupling between the ring and the waveguide is realized by a multi-mode interference (MMI) Mach-Zehnder interferometer (MZI) coupler. Within the ring, there are two SOAs providing a peak gain of 9.6 dB per SOA to compensate for the MMI splitting loss and the insertion loss as a total of 3.6 dB. In addition, there is a current injection PM in the ring to achieve tunable working wavelength. The use of the device provides, for the first time, an FHT with both tunable fractional order and tunable operation wavelength in a single photonic integrated chip (PIC). The proposed FHT is fabricated and experimentally verified. The operation wavelength is tunable with a working bandwidth of 27.2 GHz, and the fractional order is also continuously tunable with a tunable range from 0 to 1.

2. Principle

The transfer function of an FHT with an order P is given as [2]

$$H_P(\omega) = \begin{cases} e^{-j\varphi}, & \omega \geq 0 \\ e^{j\varphi}, & \omega < 0 \end{cases} \quad (1)$$

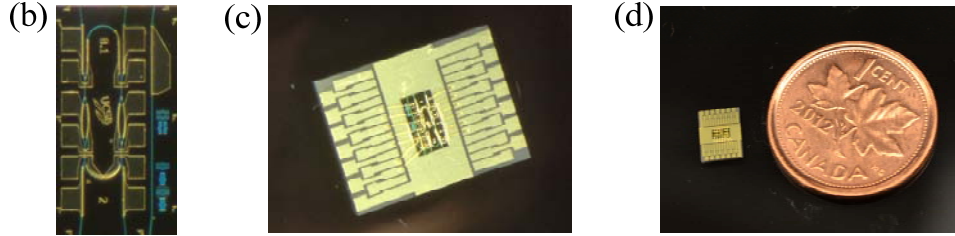
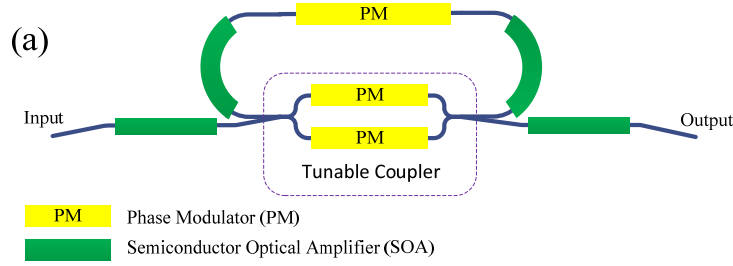


Fig. 1. (a) The schematic of the proposed on-chip FHT. (b) The fabricated on-chip FHT prototype (c) with wire bonding to a carrier and (d) its comparison to a Canadian penny

where $\varphi = P\pi/2$ and P is the fractional order. The FHT becomes a conventional HT when $P = 1$. For $P = 0$, we have $H_0(\omega) = 1$, which means that the signal at the output of the transformer is identical to the input signal. For $0 < P < 1$, the output is a weighted sum of the original signal and its conventional HT.

The FHT with tunable fractional order and central wavelength can be implemented based on a configuration shown in Fig. 1(a), which has a ring structure incorporating two active SOAs and a current injection PM. The frequency response of the ring in Fig. 1(a) can be considered as a periodical narrow-notch filter with its phase response determined by the coupling coefficient between the ring and the waveguide and its free spectral range (FSR) determined by the length of the ring. By locating the central frequency of the input signal at one of these notch filters, an FHT signal can be operated with its fractional order determined by the phase response of the notch filter. In our design, to achieve an FHT with a tunable fractional order and a tunable operating wavelength, the phase response of the notch filter is achieved by a tunable coupler between the ring and the waveguide, which is realized by the MMI MZI coupler in the configuration. By changing the injection current to the PMs in the tunable coupler, the coupling coefficient can be continuously tuned from 0% to 100%, which allows a continuously tunable fractional order from 0 to 1. In order to change the operating wavelength, the notch location of the FSR can be tuned by changing the injection current into the PM in the ring. In this way, an FHT with continuously tunable fractional order and operating wavelength can be achieved. To compensate for the propagation loss and the MMI splitting loss, there are two active SOAs in the ring, and two additional active SOAs at both input and output waveguides are designed to compensate for the fiber coupling losses.

3. Experiment

A prototype of the proposed FHT is fabricated in an InP-InGaAsP material system, as shown in Fig. 1(b), which is wire-bonded to a carrier for experimental demonstration as shown in Fig. 1(c). The chip size is 1 mm by 2 mm, and the comparison of its size with a Canadian penny is shown in Fig. 1(d). In the prototype, the length of the deeply etched waveguide ring is 3 mm. Two 400- μm SOAs with a confinement tuning layer offset quantum well (CTL-OQW) structure are fabricated in the ring to provide a peak gain of 9.6 dB per SOA. With 3 mm of ring length and 1.7 dBcm⁻¹ of passive waveguide loss, the total waveguide propagation loss is 1.6 dB. For a ring with 10% cross coupling and 0.5 dB MMI insertion loss, the couplers add about 2 dB of loss for a total round-trip loss of 3.6 dB, which is compensated for by the two 9.6 dB max gain SOAs. Two additional active SOAs are incorporated in both input and output waveguides to compensate for the fiber coupling losses. In addition, the waveguides are angled at 7° to minimize the reflections. Phase modulation in the ring and the tunable MMI MZI coupler is accomplished in forward bias via current injection and free carrier absorption through the carrier plasma effect. The PMs in the chip are fabricated with a standard length of 300 μm .

An experiment to validate the FHT is implemented. The FSR of the on-chip FHT is measured to be 27.2 GHz by an optical vector analyzer (OVA, Luna) as shown in Fig. 2(a). By changing the injection current to the PM in the ring, the notch location of the FSR is tuned and the FSR is slightly changed; the phase response corresponding to the

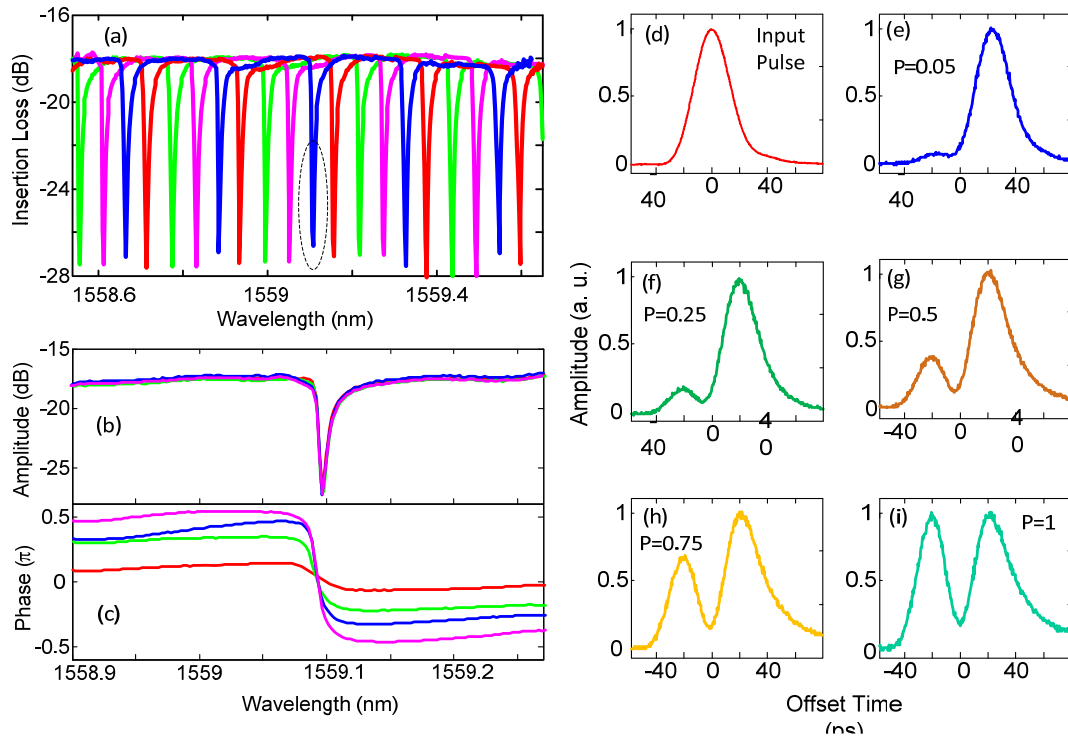


Fig. 2. (a) The spectral response of the proposed on-chip FHT at different injection current of the PM in the ring. (b) The spectral and phase responses of a selected notch at different coupling coefficient. (d) Input signal. FHT signal with a fractional order of 0.05 (e), 0.25 (f), 0.5 (g), 0.75 (h), and 1 (i).

fractional order of the FHT can also be tuned by changing the coupling coefficient, as shown in Fig. 2(b), which is achieved by changing the injection current to the PMs in the tunable MMI MZI coupler. To validate the operation of the FHT, a spectrally tailored Gaussian pulse train as shown in Fig. 2(d) generated by a mode-locked laser (MLL) source (IMRA Femtolite 780) with its central frequency at 1559.1 nm and a bandwidth of 0.2 nm is coupled into the FHT chip. By changing the coupling coefficient through controlling the injection current to the PMs in the tunable coupler, the input signal is fractionally Hilbert transformed with a tunable fractional order from 0.05 to 1, as shown in Fig. 2(e) (f) (g) (h) (i). The fractional order of the proposed FHT can be continuously tunable from 0 to 1.

4. Conclusion

We have proposed and experimentally demonstrated, for the first time to our knowledge, a photonic integrated FHT that provides both continuously tunable fractional order and tunable operation wavelength on a single chip. An FHT with a tunable fractional order from 0 to 1 and a tunable operation wavelength of 27.2 GHz was demonstrated.

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A Photonic Temporal Integrator With an Ultra-Long Integration Time Window Based on an InP-InGaAsP Integrated Ring Resonator

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Abstract—A photonic temporal integrator with an ultra-wide integration time window implemented based on a photonic integrated circuit (PIC) in an InP-InGaAsP material system consisting of semiconductor optical amplifiers (SOAs) and current-injection phase modulators (PMs) is proposed and experimentally demonstrated. The proposed photonic integrated integrator employs a ring structure coupled with two bypass waveguides. The tunable coupling between the ring and the waveguides is realized by a multi-mode interference (MMI) Mach-Zehnder interferometer coupler. Within the ring, two SOAs are incorporated to compensate for the insertion loss. In addition, there is a current injection PM in the ring for wavelength tuning. The use of the device provides a photonic temporal integrator with an ultra-wide integration time window and a tunable operation wavelength in a single PIC. The proposed integrator is fabricated and experimentally verified. The integration time window as wide as 6331 ps is achieved, which is an order of magnitude longer than that provided by the previously reported photonic integrators.

Index Terms—Analog optical signal processing, photonic integrated circuits (PICs), temporal integrator, ultrafast processing.

I. INTRODUCTION

A PHOTONIC temporal integrator, which performs the time integral of an input signal, is an important device for data processing [1], optical memory [2], and optical computing [3], [4]. A photonic temporal integrator, as a fundamental building block for all-optical signal processing, overcomes the speed limitation of its electronic counterparts. In the last few years, the implementation of a temporal integrator based on photonic techniques has been widely investigated, such as the implementation using a fiber Bragg grating (FBG) [5]–[9] or a microring resonator [10], [11]. In [5], Asghari and Azaña introduced a single uniform FBG incorporating phase shifts along its axial profile to realize an all-optical arbitrary-order temporal

integrator. By simply propagating an input optical waveform through the FBG, the cumulative time integral of the complex field envelope of the input waveform can be obtained. The proposed integrator was investigated numerically and optimized by maximizing its power efficiency [6], and a second-order complex-field temporal integrator was experimentally demonstrated with a single apodized uniform-period FBG [7], [8]. To compensate for the insertion loss in the FBG, Slavík *et al.* proposed an all-optical gain-assisted temporal integrator based on a superimposed FBG made in an Er-Yb co-doped optical fiber [9]. A photonic temporal integrator was experimentally demonstrated using the active resonant cavity in the superimposed FBG operating at the exact lasing threshold condition. In these approaches, although the main component is an FBG, the implementation of the system needs multiple discrete components, which makes the system bulky. In addition, the system cannot be reconfigured once the FBG is fabricated. To solve the problems, Ferrera *et al.* proposed an on-chip CMOS-compatible all-optical integrator [10]. The key component in the integrator is a passive micro-ring resonator. The 1st-order temporal integration of a complex-field optical waveform, with a time resolution of ~ 8 ps over an integration window exceeding 800 ps, was achieved. However, the throughput of the device was reduced by its very narrow resonance linewidth. The tradeoff between the integration bandwidth and overall power efficiency by performing all-optical integration in a micro ring resonator was explored [11]. An input to output power efficiency of 1.5% and an integration time window of ~ 12.5 ps was achieved.

Recently, we proposed a chip-scale photonic temporal integrator in an InP-InGaAsP material system with an ultra-high power efficiency by incorporating semiconductor optical amplifiers (SOAs) and current injection phase modulators (PMs) in a micro-ring resonator [12]. The photonic temporal integrator employs a ring structure coupled with two bypass waveguides. The coupling coefficients between the ring and waveguides are tunable, which is realized by a multi-mode interference (MMI) Mach-Zehnder interferometer (MZI) coupler. Within the ring, there are two SOAs providing a peak gain of 9.6 dB per SOA to compensate for a total insertion loss of 3.6 dB. In addition, there is a current injection PM in the ring for wavelength tuning. The use of the device provides, for the first time to the best of our knowledge, a photonic temporal integrator with both ultra-long integration time and tunable operation wavelength in a single photonic integrated circuit (PIC).

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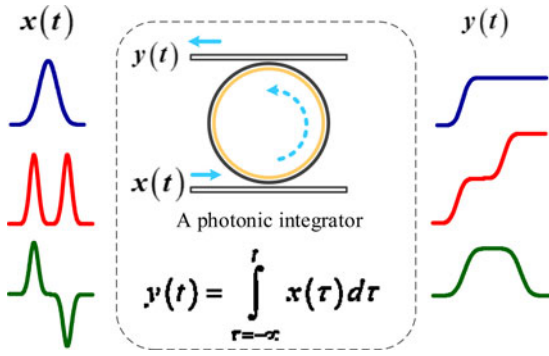


Fig. 1. The schematic diagram of a photonic temporal integrator based on a microring resonator.

The photonic temporal integrator proposed in [12] can be configured with a much larger integration time window for photonic temporal integration. In this paper, we provide a detailed theoretical study of the active temporal integrator reported in [12] and demonstrate the operation of the integrator with significantly improved performance. By optimizing the currents applied to the active components on the chip, the ring can be configured to work close to its lasing condition, at which, the integration time window can be significantly increased. In the experimental demonstration, the integration time window is improved from 198 to 6331 ps.

The paper is organized as follows. In Section II, the principle of the active temporal integrator is presented, with an emphasis on the configuration of the integrator to operate close to its lasing condition by tuning the injection currents to the SOAs on the chip to improve the integration time window. A simulation is then performed to study the integration time window for different Q -factors of the ring. In Section III, an experiment is performed. The temporal integration of a Gaussian shaped pulse, an in-phase doublet and an out-of-phase doublet pulse is demonstrated, with the integrated results measured and analyzed. The integration time window of the proposed integrator is measured to be 6331 ps. A conclusion is drawn in Section IV.

II. PRINCIPLE

Mathematically, a temporal integrator can be implemented using a linear time-invariant filter with a transfer function given by [11]

$$H(\omega) = \frac{1}{j(\omega - \omega_0)} \quad (1)$$

where $j = \sqrt{-1}$, ω is the angular optical frequency and ω_0 is the carrier frequency of the signal to be processed. A general approach to realizing a photonic integrator is to use an optical resonant cavity, for example, a Fabry-Pérot filter [9] or a ring resonator [10]–[12]. Fig. 1 shows a photonic temporal integrator based on a microring resonator. Three output temporal waveforms corresponding to three input waveforms of a Gaussian pulse, an in-phase doublet and an out-of-phase doublet are shown to demonstrate the integration operation. The detailed theoretical analysis of using a ring resonator to implement an

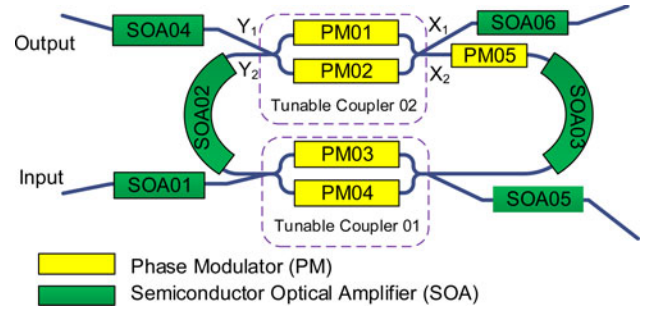


Fig. 2. The schematic of the proposed on-chip photonic temporal integrator based on a microring resonator.

optical integrator could be found in [13]. However, the integration time window of such an integrator is limited, and its operation wavelength is usually fixed. To implement a photonic integrator with an ultra-long integration time window and a tunable operation wavelength, we propose to use an active ring resonator incorporating SOAs and current injection PMs, as shown in Fig. 2.

The frequency response of the ring resonator in Fig. 2 consists of a series of narrow passbands with two neighboring passbands separated by a free spectral range (FSR) determined by the length of the ring [12]. By locating the central frequency of the input signal at the center of one of the narrow passband, the temporal integral of the input signal can be obtained at the output of the ring. In our design, to achieve temporal integration with an ultra-long integration time and a tunable working wavelength, two active SOAs (SOA02 and SOA03) and a current injection PM (PM05) are incorporated into the ring. By applying injection currents to the SOAs (SOA02 and SOA03), the insertion loss in the device can be totally compensated. By changing the injection current to the PM (PM05) in the ring resonator, the spectral response is laterally shifted, thus making the operating wavelength be tuned. In addition, the coupling between the ring and the bypass waveguides is achieved by two tunable couplers, with each having an MMI MZI structure consisting of one PM in each of the two arms (PM01 and PM02 for tunable coupler 01, and PM03 and PM04 for tunable coupler 02, as shown in Fig. 2). By changing the injection currents to the PMs in the tunable couplers, the coupling coefficients can be continuously tuned from 0% to 100%. To compensate for the fiber coupling losses, two other active SOAs (SOA01 and SOA04) are incorporated into the device at the input and output waveguides, respectively. In this way, a photonic temporal integrator with an ultra-high power efficiency and a continuously tunable operating wavelength can be achieved.

Theoretically, the transfer function of the proposed ring resonator with the output taken from the drop port shown in Fig. 2 is given by [14]

$$H(Z) = -\frac{\kappa_1 \kappa_2 \sqrt{\rho Z^{-1}}}{1 - t_1 t_2 \rho Z^{-1}} \quad (2)$$

where κ_1 and κ_2 are the field coupling coefficients of the two tunable couplers, t_1 and t_2 are the field transmission factors of

TABLE I
PARAMETERS FOR THE SIMULATION

Symbol	Description	Value
λ	Central wavelength	1558 nm
γ_1	Coupling coefficient of the input coupler	90% (0–100%)
γ_2	Coupling coefficient of the output coupler	90% (0–100%)
l	Length of the ring	3 mm
n	Refractive index of the waveguide	3.67
α	Waveguide loss	1.7 dB/cm
ρ	Insertion loss of the tunable coupler	2 dB
g	Gain of each SOA	0–9.6 dB

Coupler coefficients are tunable from 0% to 100%, which are considered as the coupling coefficient from X_2 to Y_2 as shown in Fig. 2.

the two tunable couplers, and ρ is the loss in the ring. If the insertion losses in the ring are completely compensated, the Q -factor of the ring is infinite, and the integration time is infinitely long. For real implementations, however, it is too difficult to achieve a complete compensation for the losses without reaching the lasing threshold ($t_1 t_2 \rho = 1$). Thus, we discuss the integration time window when the Q -factor of the ring is tuned by changing the injection currents to the SOAs on the chip, to achieve a large Q -factor while ensuring the ring is not lasing. The Q -factor of the ring is given by [15]

$$Q = \omega_r \frac{T_r}{\alpha L} = \omega_r N T_r \quad (3)$$

where ω_r is the resonant angular frequency of the ring resonator, T_r is the round trip time in the ring, α is the power attenuation coefficient, L is the optical length of the ring, and N is the number of round trips required to reduce the optical power to $1/e$. The integration time window is defined as the time duration for the output power to drop by 20% from its maximum value [10]. A simulation is performed to analyze the integration performance for the ring to be configured to operate far from the lasing condition to close to the lasing condition. In the simulation, the integration time window is calculated based on the output temporal waveform, which is obtained by an inverse Fourier transform of the product of the input Gaussian pulse spectrum and the transfer function of the ring resonator with different Q -factors. The parameters in the simulation are given in Table I. As shown in Fig. 3, the integration time window increases with the Q -factor. When the ring is approaching to the lasing threshold or the Q -factor is approaching to infinity, the integration time window is then approaching to infinity. However, for practical implementation, the ring resonator is very unstable when the gain is close to the lasing threshold, which prevents the proposed integrator from having an infinite integration time window.

III. EXPERIMENT

The proposed photonic temporal integrator is fabricated in an InP-InGaAsP material system by the UCSB nanofabrication facility, as shown in Fig. 4(a), which is wire-bonded to a carrier for experimental demonstration, as shown in Fig. 4(b). The chip size is 1 mm \times 2 mm, and the comparison of its size

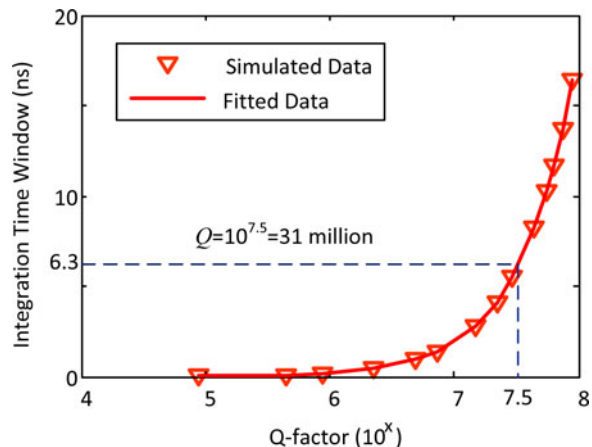


Fig. 3. Simulation results. The integration time window for different Q -factors of the ring.

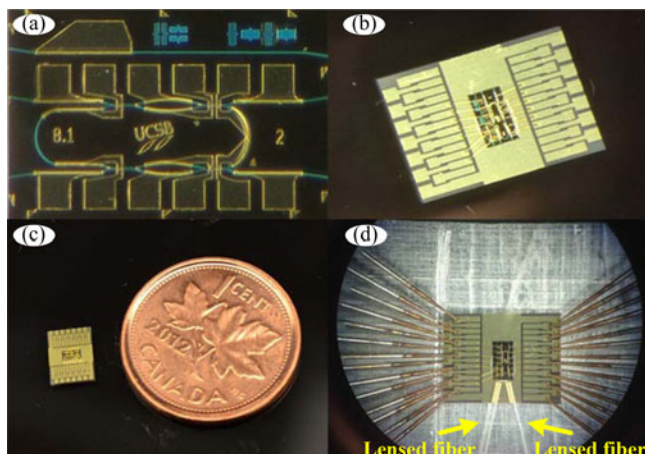


Fig. 4. (a) The fabricated on-chip photonic temporal integrator prototype. (b) Wire bonded to a carrier. (c) Comparison with a Canadian penny. (d) Experimental setup for optical coupling with two lensed fibers.

with a Canadian penny is shown in Fig. 4(c). In the prototype, the length of the deeply etched waveguide ring is 3 mm. Two 400- μ m SOAs (SOA02 and SOA03) with a confinement tuning layer offset quantum well [16] structure are fabricated in the ring to provide a peak gain of 9.6 dB per SOA. With 3 mm of ring length subtracting the length of the two SOAs (400 μ m each) and 1.7 cm^{-1} of passive waveguide loss, the total waveguide propagation loss is 1.6 dB. For a ring with a coupling coefficient of 90% and 0.5 dB MMI insertion loss, the couplers add about 2 dB of loss for a total round-trip loss of 3.6 dB, which is compensated for by the two SOAs. Two additional active SOAs (SOA01 and SAO04) are incorporated into the system at both the input and output waveguides to compensate for the fiber coupling losses, as shown in Fig. 4(a). In addition, the facets of the waveguides are angled at 7° to minimize the reflections. The phase modulation in the ring and the tuning of the MMI MZI coupler are accomplished by forward bias currents via current injection and free carrier absorption through the carrier

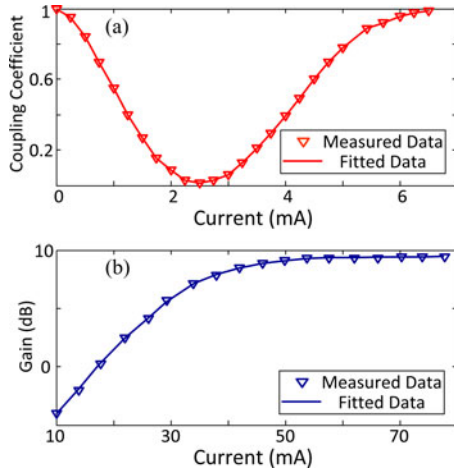


Fig. 5. (a) Tunable coupling coefficient of an MMI MZI coupler at different injection current of one PM on one of the two arms. (b) The gain profile of an SOA as a function of the injection current.

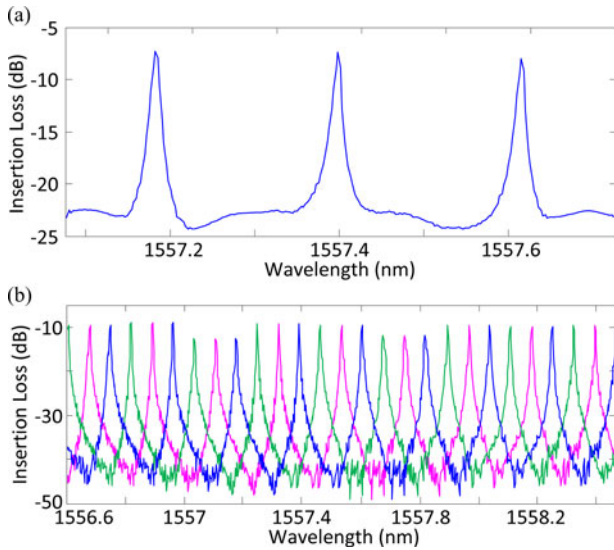


Fig. 6. The measured spectral response of the fabricated ring resonator. (a) The spectral response when no injection current is applied to the PM in the ring. (b) The spectral response of the integrator when the injection current to the PM in the ring is tuned at three different currents.

plasma effect in the PMs. The PMs (PM01-PM05) in the chip are fabricated with a standard length of 300 μm .

The coupling coefficients of the tunable couplers are measured at different injection currents to the PMs, which can be controlled from 0% to 100% when one of the PMs in each of the tunable couplers is injected with a current from 0 to 2.5 mA. Fig. 5(a) shows the measured coupling coefficient of tunable coupler 02 as a function of the injection current to PM02, from 0 to 6.5 mA. The large signal gain profile of an SOA is also measured. As can be seen the SOA has a maximum gain of 9.6 dB when the injection current is above 70 mA, as shown in Fig. 5(b). The FSR of the on-chip ring is measured to be 27.2 GHz as shown in Fig. 6(a). By changing the injection current to the PM (PM05) in the ring, the spectral response of the

TABLE II
THE INJECTION CURRENTS TO THE PMs AND SOAs

Components	Integrator	Lasing Condition
SOA01	50.000 mA/2.4992 V	N/A
SOA02	28.300 mA/2.1197 V	39.800 mA/2.3012 V
SOA03	34.202 mA/2.4209 V	34.202 mA/2.4209 V
SOA04	50.000 mA/2.4644 V	N/A
PM01	0	0
PM02	3.7867 mA/1.7758 V	3.7867 mA/1.7758 V
PM03	2.1291 mA/1.7361 V	2.1291 mA/1.7361 V
PM04	0	0

ring is laterally shifted, thus the peak location is also shifted, as shown in Fig. 6(b). In the experiment, the chip is working at 22 $^{\circ}\text{C}$ with a temperature controlling unit to maximize the stability of the ring resonator.

As discussed in Section II, the Q -factor is a critical parameter to the operation of the integrator. In the experiment, we also test the operation of the integrator when it is configured to operate close to the lasing threshold, with the injection currents to the PMs and the SOAs given in Table II. Under this condition of operation, three different input waveforms are generated and applied to the input of the integrator, to study the performance of the integration operation of the device.

A. Gaussian Pulse

We first test the integration of a Gaussian pulse by the photonic temporal integrator. The Gaussian pulse is generated by a mode locked laser source which is filtered by an optical band-pass filter (Finisar, WaveShaper 4000 S) with a bandwidth of 0.12 nm and a central wavelength at 1557.4 nm, as shown in Fig. 7(a), to make the Gaussian pulse have a temporal width of 54 ps centered at 1557.4 nm, which is then coupled into the photonic integrator by a lensed fiber. By configuring the photonic temporal integrator with the injection currents to the SOAs and PMs in the ring with the values given in Table II, a high Q -factor of 31 million is achieved and the ring is still under the lasing threshold. As shown in Fig. 7(b), the temporal integral of the input Gaussian pulse is realized. The integration window is measured to be 6331 ps.

B. In-Phase Doublet

We then test the integration of an in-phase doublet pulse by the proposed photonic temporal integrator. In the experiment, the in-phase doublet pulse is generated by launching a Gaussian pulse into an unbalanced MZI with a length difference between the two arms of 25 cm. As a result, two closely separated pulses, called an in-phase doublet, with a temporal separation of 1.14 ns, as shown in Fig. 8(a), are generated and then launched into the integrator. The waveform at the output of the integrator is shown in Fig. 8(b). As can be seen the integrator sums up the area of the in-phase doublet, giving two steps corresponding the area of the first pulse and the area of the first and the second pulses, as shown in Fig. 8(b).

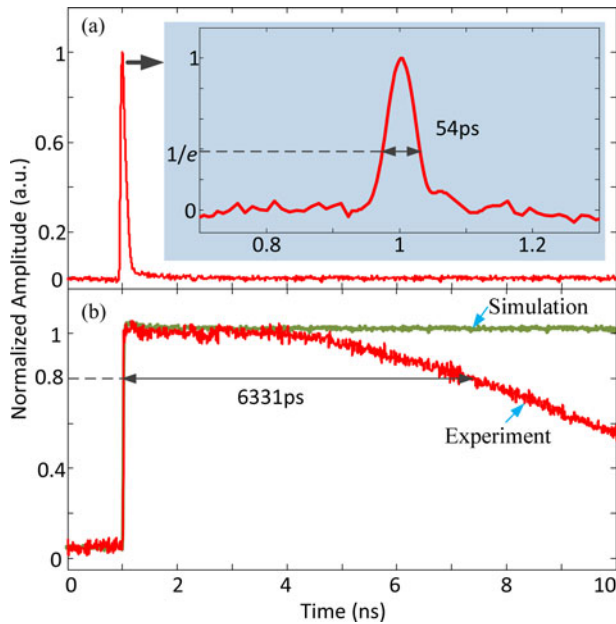


Fig. 7. The experimental results. (a) The input Gaussian pulse with a temporal width of 54 ps. (b) The integral of the Gaussian pulse with an integration time window of 6331 ps.

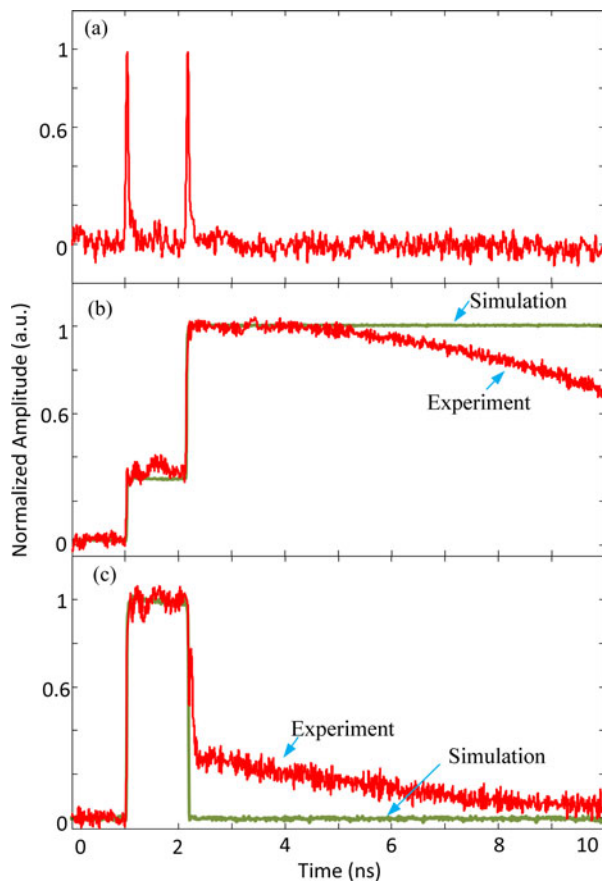


Fig. 8. The experimental results. (a) The input in-phase doublet pulse, (b) the integral of the in-phase doublet pulse, and (c) the integral of the out-of-phase doublet pulse.

C. Out-of-Phase Doublet

A photonic temporal integrator can be used as a memory device. The ability to reset the memory is a very important function. To validate the operation of the integrator as a memory unit, two closely separated pulses with a π phase shift (out-of-phase), called an out-of-phase doublet, generated by the same unbalanced MZI mentioned are coupled into the input port of the integrator. The π phase shift between the two pulses is introduced by the MZI by controlling the length difference between the two arms of the MZI. The waveform at the output of the integrator is shown in Fig. 8(c). As can be seen memory resetting function is performed by the integrator.

IV. DISCUSSION AND CONCLUSION

To utilize the proposed integrator as a processing unit in a large system, the power consumptions of the PMs and SOAs and the amplified spontaneous emission (ASE) noise from the SOAs should be considered. In the experiment, the total power consumption of the integrator is 401 mW including 248 mW consumed by the input/output SOAs, which can be avoided in a large system with all units fabricated on a single chip without fiber coupling loss between the units. In addition, a single SOA in a ring resonator is enough to compensate for the total loss. Therefore, a power consumption with a single SOA in a ring resonator and two PMs for tunable coupling would have a power consumption of 93 mW, which is much smaller than the power consumption of the single integrator demonstrated here. When the number of SOAs is reduced, the ASE noise will also be significantly reduced.

In summary, we have proposed and experimentally demonstrated a fully photonic integrated temporal integrator that provides an ultra-long integration time window and a continuously tunable working wavelength on a single PIC. A temporal integration window of 6331 ps with a bandwidth of 0.12 nm was obtained, which is far better than an electronic integrator. Compared with the previously reported photonic solutions, the proposed integrator provides an integration time window that is an order of magnitude longer. The temporal integration of different input waveforms was also investigated, which confirmed the effective operation of the proposed temporal integrator. This work represents an important step towards the realization of efficient optical signal-processing circuits capable of overcoming the limitation in the integration time window, bandwidth and power consumption imposed by electronics.

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1.5 Tbpsxm MMF transmission link with 1060nm VCSEL

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Abstract: 1060 nm VCSEL-based data transmission over 50m OM3 MMF at 30 Gbit/s is experimentally demonstrated. A highly-strained QW VCSEL with p-type modulation doping is used with 3.77 mA bias and 0.55 V data amplitude.

OCIS codes: (060.2330) Fiber optics communications; (060.4080) Modulation; (250.7270) Optoelectronics: vertical emitting lasers

1. Introduction

Vertical cavity surface emitting lasers (VCSELs) have long been recognized as key components for optical interconnects due to their small size, high speed and low power consumption. The most common operating wavelength for VCSELs used for data transmission, using multimode fibers (MMF), is 850 nm. Other VCSELs wavelength explored are 980 nm, 1010 nm, 1060 nm, 1090 nm and 1310 nm.

VCSELs operating in the wavelength region around 1060 nm are particularly attractive due to very high energy efficiency [1, 2] and good reliability [3]. An interesting feature of 1060 nm VCSELs is the possibility of emitting the light through the bottom of the VCSEL rather than through top as it is usually done. This offers significant benefits in terms of optical coupling, packaging and heat management, since the wirebonding can be placed opposite the optical aperture [4]. Compared to 850 nm interconnects, the 1060 nm wavelength region has the advantages lower fiber attenuation (1.5 dB/km compared to 3.5 dB/km @850 nm), and of high sensitivity indium-gallium-arsenide (InGaAs) photodiodes. Unfortunately, the most common multi-mode fibers OM3 and OM4 has higher modal dispersion at 1060 nm than at 850 nm; a factor that makes high-speed transmission challenging. Even so, in this paper we present the highest bit rate distance product ever achieved for 1060 nm MMF interconnects, namely 1.5 Tbpsxm achieved as 30 Gbps transmission over 50 m of OM3 multimode fiber. This result is realized with a bottom-emitting 1060 nm VCSEL using only 3.77 mA bias and 0.55 V peak-to-peak data amplitude.

2. 1060 nm VCSEL design

The employed light source is a bottom emitting, highly-strained 1060 nm QW VCSEL with p-type modulation doping. Fig. 1 shows its schematic diagram. The VCSEL is grown on a semi-insulating GaAs substrate using molecular beam epitaxy (MBE). The bottom mirror consists of GaAs/AlAs and Si doped GaAs. The top mirror consists of GaAs/AlGaAs. The active region is surrounded by an asymmetric $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ separate confinement heterostructure (SCH) that is parabolically graded down to GaAs spacers. Three 8 nm thick highly-strained $\text{In}_{0.3}\text{Ga}_{0.7}\text{As}$ quantum wells (QWs) are separated by 8 nm GaAs barriers. Growth is stopped halfway into the barrier

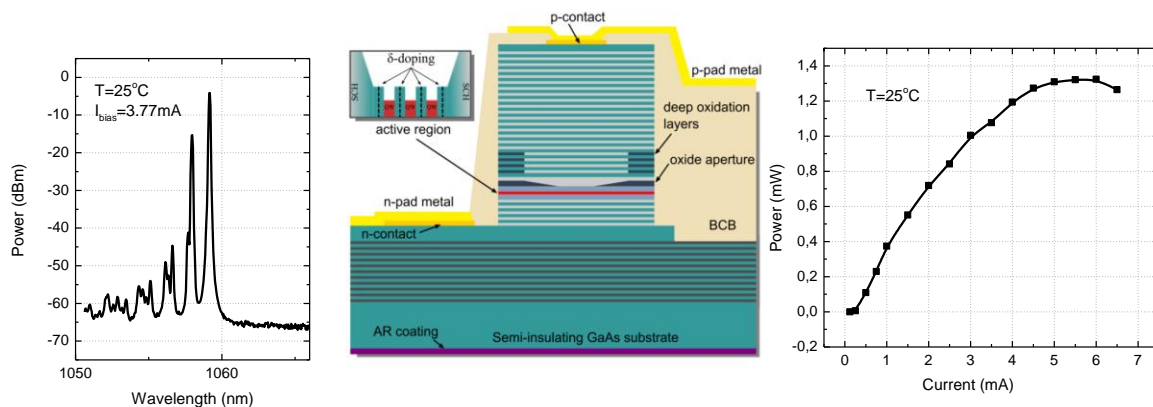


Fig. 1 Optical spectrum; VCSEL structure [1]; Power versus current curve.

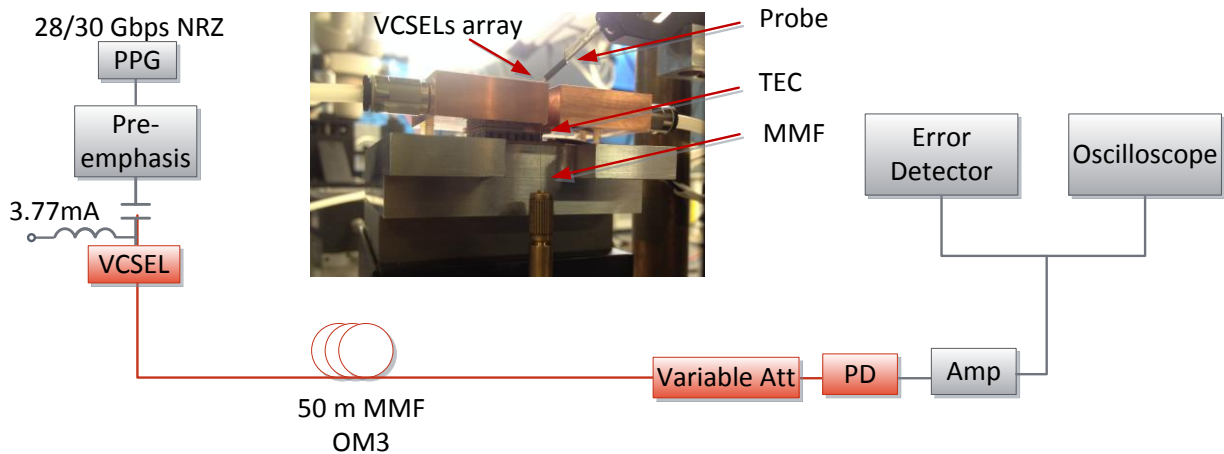


Fig. 2 Experimental setup for high speed transmission with 1060 nm VCSEL.

and the surface is δ -doped with carbon using a carbon tetrabromide (CBr₄) precursor. The high differential gain of the 1060 nm laser comes at the price of increasing the nonlinear gain compression. Modulation p-type doping was used suppress nonlinear gain compression which resulted in increasing the K-factor compared to stained QWs alone. Fig. 1 shows the power versus current curve measured at T=25°C for the VCSEL used in the transmission experiment. A very low threshold current of 0.15mA is observed. The corresponding optical spectrum measured at a bias current of 3.77mA is presented in Fig.1 as an inset. Further details of the VCSEL design can be found in [1].

3. Experimental setup

Fig. 2 shows the setup used in the transmission experiment. Electrical pseudo-random binary (PRBS $2^{15}-1$) data signals at 28 Gbps (0.682 V peak-peak) or 30 Gbps (0.548 V peak-to-peak) generated by a pulse pattern generator (PPG) is combined with a 3.77 mA bias current in a bias-Tee and applied to the VCSEL using a 40 GHz electrical probe. The temperature is stabilized at 25°C using a temperature controller. The modulation format used is non-return-to-zero (NRZ) using 1 post/1 pre-cursor pre-emphasis configuration as shown in Fig. 3. Fiber launch power is 0.7 dBm and the attenuation of the 50 m fiber link is 0.9 dB. The light from the VCSEL is coupled into a 50 m OM3 compliant multimode 50 μ m core diameter fiber. The optical signal is received by a commercially available photodiode with a wavelength range of 900-1350 nm and a 30 GHz 3-dB bandwidth, amplified to 1 V peak-to-peak and analyzed in real time by an error detector.

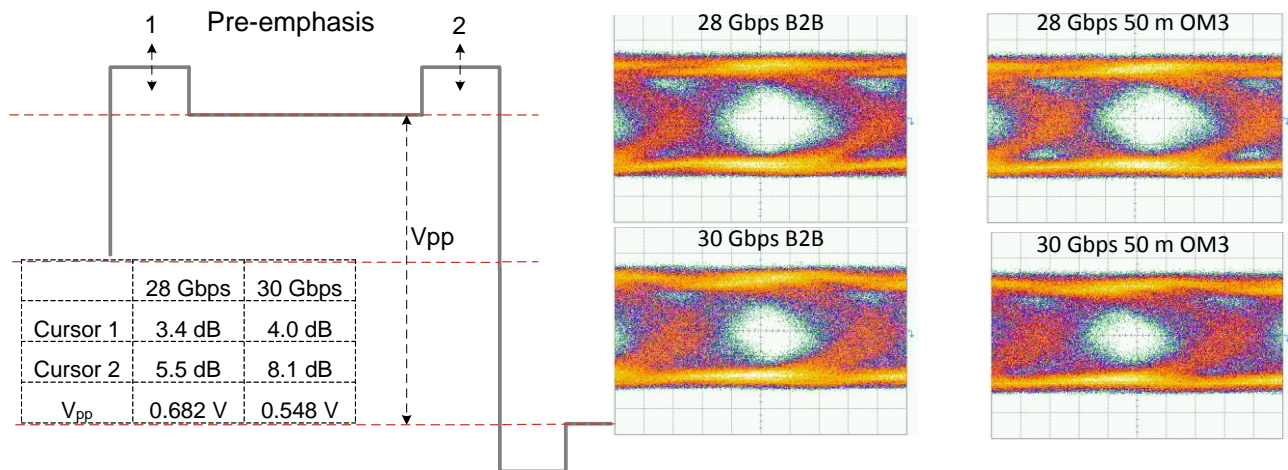


Fig. 3 Pre-emphasis module settings; Eye diagrams for B2B and transmission over 50 m OM3 MMF at 28 Gbps and 30 Gbps.

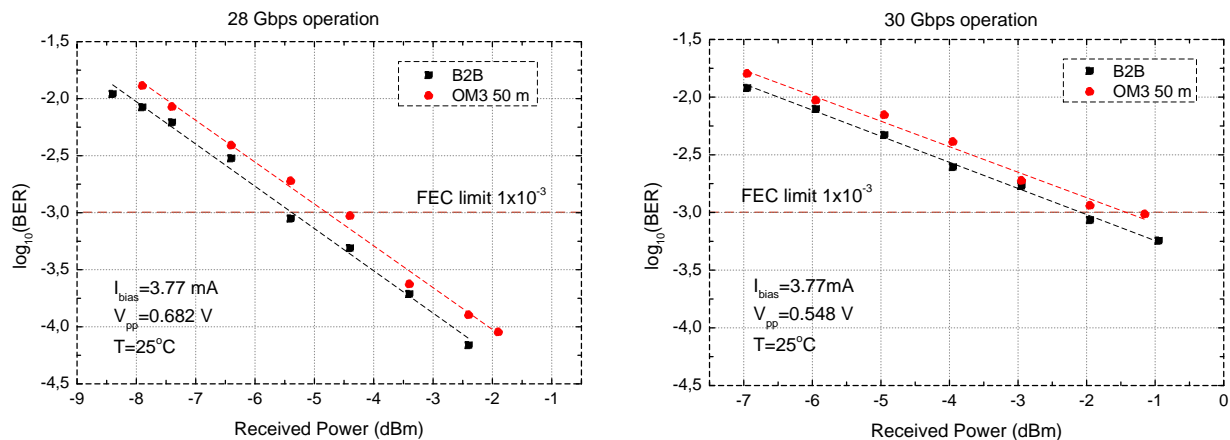


Fig. 4. Bit error rate curves for B2B and Transmission at 28Gbps and 30 Gbps with 1060 nm VCSEL.

4. Results and Discussions

Fig. 3 shows the measured eye diagrams and Fig. 4 bit error ratio (BER) as a function of the received optical power back-to-back (B2B) and after 50 m MMF transmission for the two considered bit rates. Receiver sensitivity at the 7%-overhead forward error correction (FEC) limit of 1×10^{-3} for B2B is -5.4 dBm at 28 Gbps and -2.05 dBm at 30 Gbps. In both cases a penalty of 0.8 dB is observed after fiber transmission. The optimal setting of pre-emphasis improved the transmission BER by 1 order of magnitude allowing all BER curves to be below the FEC threshold.

The advantage of 1060 nm VCSELs for interconnect links include the ability to balance energy efficiency and reliability. Our reported results has encouraging prospects too in relation to bottom emitting devices for packaging and heat management when incorporating these light sources into modules for interconnects and short range links.

5. Conclusions

A high speed 30 Gbps transmission employing 1060 nm bottom-emitting VCSEL has been demonstrated with transmission over 50 m of OM3 MMF resulting in a bit rate-distance product of 1.5 Tbpsxm. In this reported experiment, the achieved energy efficiency is high due to the use of only with 3.77 mA bias and 0.55 V peak-to-peak data amplitude.

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30 Gbps Bottom-Emitting 1060 nm VCSEL

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Abstract 1060 nm VCSEL-based data transmission over 50 m OM3 MMF at 30 Gbit/s is experimentally demonstrated. A highly-strained bottom-emitting QW VCSEL with p-type modulation doping is used with 3.77 mA bias and 0.55 V data amplitude.

Introduction

Vertical cavity surface emitting lasers (VCSELs) have long been recognized as key components for optical interconnects due to their small size, high speed and low power consumption. The most common operating wavelength for VCSELs used for data transmission, using multimode fibers (MMF), is 850 nm. Other VCSELs wavelengths explored are 980 nm, 1010 nm, 1060 nm, 1090 nm and 1310 nm. Moving to higher wavelengths allows taking advantage of e.g. lower fiber attenuation.

VCSELs operating in the wavelength region around 1060 nm are particularly attractive due to very high energy efficiency^{1,2} and good reliability³. An interesting feature of the presented 1060 nm VCSEL is the possibility of emitting the light through the bottom of the VCSEL rather than through top as it is usually done⁴. This offers significant benefits in terms of optical coupling, packaging and heat management, since the wirebonding can be placed opposite the optical aperture⁵. As previously mentioned, the 1060 nm wavelength region has the advantage over 850 nm region in terms of lower fiber attenuation (1.5 dB/km@1060 nm compared to 3.5 dB/km @850 nm), lower power consumption (threshold currents below 1 mA) and of existence of high

sensitivity indium-gallium-arsenide (InGaAs) photodiodes. Unfortunately, the most common multi-mode fibers OM3 and OM4 have higher modal dispersion at 1060 nm than at 850 nm; a factor that makes high-speed transmission challenging. Even so, in this paper we present the FEC-conformed performance over 50 m of OM3 multimode fiber.

A transmission over 200 m OM3 MMF has been recently reported using a top emitting 1060 nm VCSEL operating at 25 Gbaud⁴. In this contribution we present a 30 Gbps transmission over 50 m of OM3 MMF. This result is realized with a bottom-emitting 1060 nm VCSEL using only 3.77 mA bias and 0.55 V peak-to-peak data amplitude.

1060 nm VCSEL design

The employed light source is a bottom emitting, highly-strained 1060 nm QW VCSEL with p-type modulation doping. It has previously been presented and described in the referenced work¹. Fig. 1 shows the schematic diagram of the device.

The VCSEL is grown on a semi-insulating GaAs substrate using molecular beam epitaxy (MBE). The bottom mirror consists of GaAs/AlAs and Si doped GaAs. The top mirror consists of GaAs/AlGaAs. The active region is surrounded by an asymmetric $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ separate

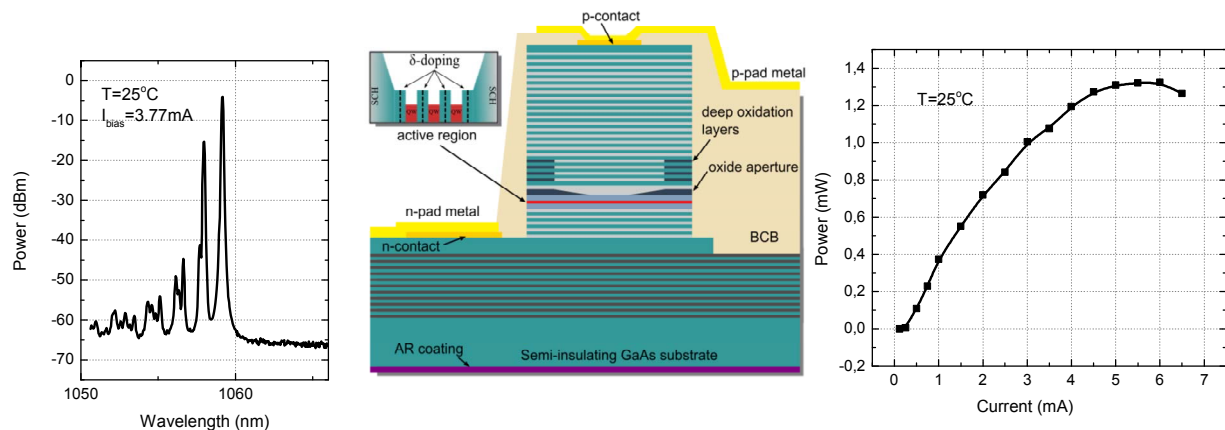


Fig. 1: Optical spectrum; VCSEL structure¹; Power versus current curve.

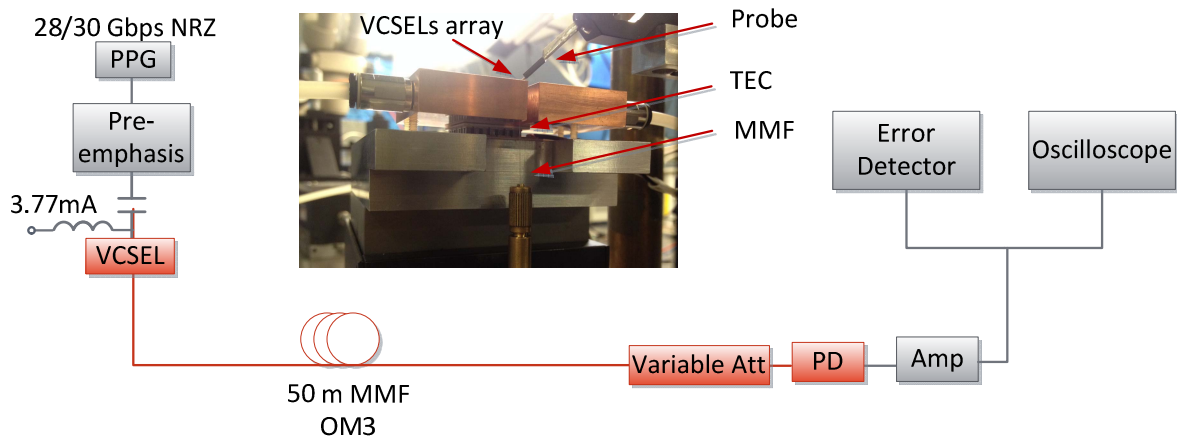


Fig. 2: Experimental setup for high speed transmission with 1060 nm VCSEL.

confinement heterostructure (SCH) that is parabolically graded down to GaAs spacers. Three 8 nm thick highly-strained $\text{In}_{0.3}\text{Ga}_{0.7}\text{As}$ quantum wells (QWs) are separated by 8 nm GaAs barriers. Growth is stopped halfway into the barrier and the surface is δ -doped with carbon using a carbon tetrabromide (CBr_4) precursor. The high differential gain of the 1060 nm laser comes at the price of increasing the nonlinear gain compression. Modulation p-type doping was used to suppress nonlinear gain compression which resulted in increasing the K-factor compared to stained QWs alone.

Fig. 1 shows the power versus current curve measured at $T=25^\circ\text{C}$ for the VCSEL used in the transmission experiment. A very low threshold current of 0.15 mA is observed. The corresponding optical spectrum measured at a bias current of 3.77 mA is presented in an inset of Fig.1. Further information on the presented 1060 nm VCSEL design are described in referenced work¹ and the details on analogous device design at 980 nm is presented in the Chapter 7 of 'VCSELS'⁶.

Experimental setup

Fig. 2 shows the setup used in the transmission experiment. Electrical pseudo-random binary (PRBS $2^{15}-1$) data signals at 28 Gbps (0.682 V peak-peak) or 30 Gbps (0.548 V peak-to-peak) generated by a pulse pattern generator (PPG) is combined with a 3.77 mA bias current in a bias-Tee and applied to the VCSEL using a 40 GHz electrical probe. The temperature is stabilized at 25°C using a temperature controller. The modulation format used is non-return-to-zero (NRZ). In the transmitter the 1 post/1 pre-cursor pre-emphasis configuration is used, as shown in Fig. 3. The pre-emphasis parameters (Cursor 1, 2 and V_{pp} in inset Table in Fig. 3) are optimized for the transmission scenario and the same settings are used for measuring the B2B case. The light from the VCSEL is coupled into a 50 m OM3 compliant multimode 50 μm core diameter fiber. Fiber launch power is 0.7 dBm and the attenuation of the used 50 m fiber link is 0.9 dB. The optical signal is received by a VI Systems photodiode with a wavelength range of 900-1350 nm and a 30 GHz 3-dB bandwidth. The

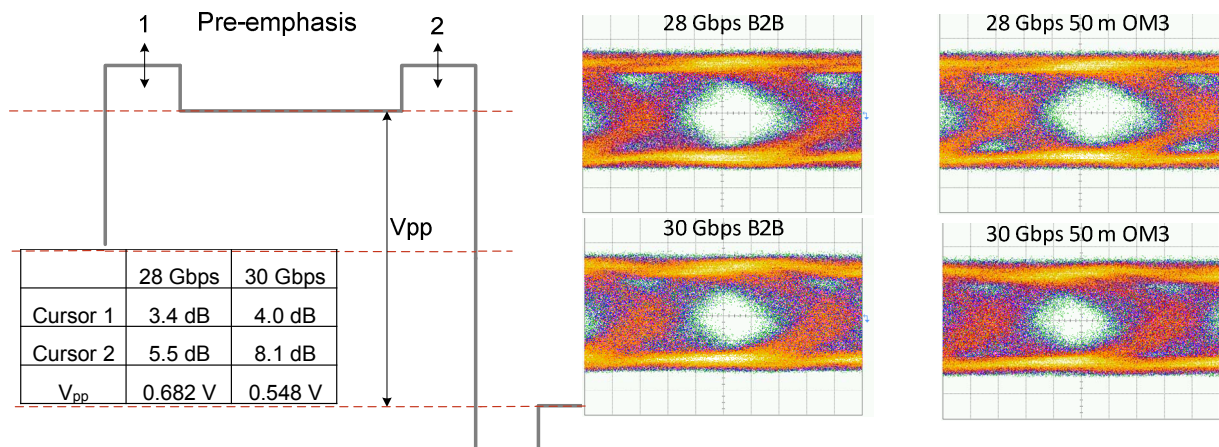


Fig. 3: Pre-emphasis module settings; Eye diagrams for B2B and transmission over 50 m OM3 MMF at 28 Gbps and 30 Gbps.

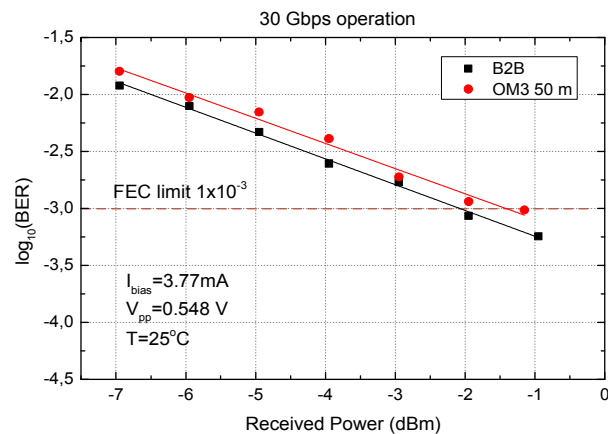
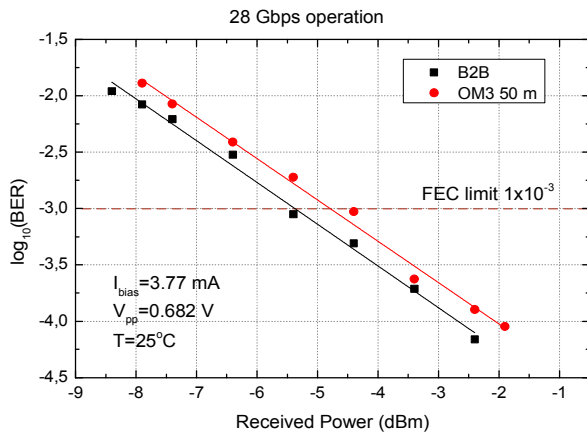


Fig. 4: Bit error rate curves for B2B and Transmission at 28 Gbps and 30 Gbps with 1060 nm VCSEL.

received signal is then amplified to 1 V peak-to-peak and analyzed in real time by an error detector.

Results and Discussions

Fig. 3 shows the measured eye diagrams and Fig. 4 bit error ratio (BER) as a function of the received optical power back-to-back (B2B) and after 50 m MMF transmission for the two considered bit rates. Receiver sensitivity at the 7%-overhead forward error correction (FEC) limit of 1×10^{-3} for B2B is -5.4 dBm at 28 Gbps and -2.05 dBm at 30 Gbps. In both cases a penalty of 0.8 dB is observed after fiber transmission.

The optimal setting of pre-emphasis (Fig. 3) improves the transmission BER by 1 order of magnitude allowing BER to be below the FEC limit.

Further work on pre-emphasis is required to maximize the achievable distance. Moreover, the transmission reach can be increased by employing OM4 MMF or fibers designed and optimized for 1060 nm range. The 1060 nm VCSEL is proven to be a potential candidate for the optical interconnects which use the benefits of direct intensity modulation and direct detection. The advantage of 1060 nm VCSELs for interconnect links include the ability to balance energy efficiency and reliability.

Conclusions

A high speed 28 Gbps and 30 Gbps transmission employing 1060 nm bottom-emitting VCSEL has been demonstrated with transmission over 50 m of OM3 MMF resulting in a bit rate-distance product of 1.5 Tbpsxm. In the reported experiment, the bias of only 3.77 mA and 0.55 V peak-to-peak data amplitude

confirms energy efficiency of the VCSEL based system. The optimized pre-emphasis module at the transmitter allows a FEC-conformed BER values to be achieved.

Our reported results have encouraging prospects in relation to bottom emitting devices for packaging and heat management when incorporating these light sources into modules for interconnects and short range links.

Acknowledgements

We would like to acknowledge VI Systems Germany for supporting this work with the VIS Photoreceiver.

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Polarization degenerate micropillars fabricated by designing elliptical oxide apertures

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A method for fabrication of polarization degenerate oxide apertured micropillar cavities is demonstrated. Micropillars are etched such that the size and shape of the oxide front is controlled. The polarization splitting in the circular micropillar cavities due to the native and strain induced birefringence can be compensated by elongating the oxide front in the [110] direction, thereby reducing stress in this direction. By using this technique, we fabricate a polarization degenerate cavity with a quality factor of 1.7×10^4 and a mode volume of $2.7 \mu\text{m}^3$, enabling a calculated maximum Purcell factor of 11. © 2014 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4872003>]

Quantum dots (QDs) in micropillar cavities form an interesting platform for cavity quantum electrodynamics experiments in the solid state.¹ For example, the coupling between the spin in a singly charged QD and the polarization of a photon in the Purcell regime holds promise for applications in hybrid quantum information processing.² For this purpose oxide apertured micropillars are attractive as they combine simple fabrication of voltage contacts, excellent mode-matching with external fields, and access to the Purcell regime.^{3,4}

An important challenge, however, is to obtain polarization degenerate cavity modes. This is an important condition in order to prepare entanglement between an electron spin and the polarization of a photon,⁵ which is essential for schemes as described in Ref. 2. Several post-processing techniques have been demonstrated to tune the polarization properties. These techniques rely on the application of strain mechanically⁶ or on the optical application of surface defects.^{7,8} It is more desirable to obtain close-to polarization degenerate cavities after the wet oxidation processing step and thereby minimize the need of further tuning.

In this paper, we demonstrate that, by systematically varying the shape of the etched micropillar, the shape of the oxide aperture can be controlled, thereby controlling the spectral properties. Two arrays of micropillars of which the diameter and ellipticity are systematically varied are fabricated and the optical modes are characterized at 9.0 K. Micropillars with circular oxide fronts exhibit optical modes with a large circular symmetry, but due to birefringence the fundamental mode is polarization non-degenerate. However, for elliptical oxide fronts that are elongated in the [110] direction, the native birefringence is compensated for by strain-induced birefringence and polarization degenerate fundamental modes are obtained.

The samples used in this study are grown by molecular beam epitaxy on a GaAs [100] substrate. First, a planar distributed Bragg reflector (DBR) cavity is grown which consists of a spacing layer and 26 pairs of GaAs/Al_{0.90}Ga_{0.10}As layers in the top mirror and 29 pairs in the bottom mirror. The

spacing layer consists of a λ GaAs layer, containing a layer of InAs self-assembled QDs in the center,⁹ and a $\frac{3}{4}\lambda$ Al_xGa_{1-x}As aperture region. The oxidation aperture consists of a 10 nm AlAs layer embedded between 95 nm Al_{0.83}Ga_{0.17}As and 66 nm Al_{0.75}Ga_{0.25}As layers, providing a linearly tapered oxidation upon the wet oxidation. Micropillars are etched such that they are connected to the bulk region via three bridges, to provide global electrical contacts, as shown in Fig. 1(a).

This geometry was found to be an optimum as for two bridges the oxide front is found to be more elliptically shaped, while for more than three bridges the bridges are too thin and the risk increases that the electrical conductance to the micropillar center is insufficient.¹⁰ This geometry, together with the etching process, is however expected to induce in-plane anisotropic strain, which needs to be compensated for together with the native birefringence, that can be present even in perfectly circular mesas.

Figures 1(b) and 1(c) schematically show that the micropillar diameter d in the $[1\bar{1}0]$ direction and diameter $d + \Delta$ in

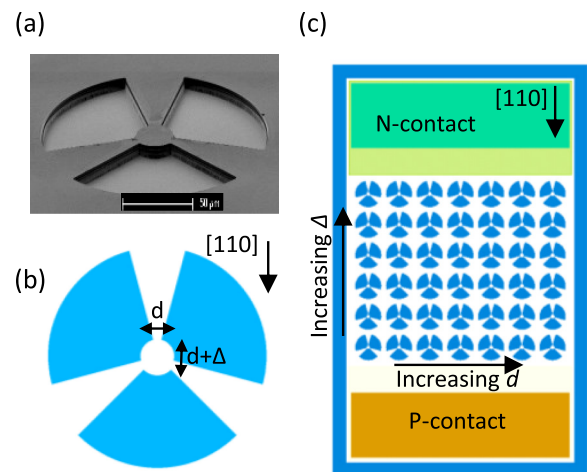


FIG. 1. (a) SEM image of a micropillar. (b) The micropillars have diameter d and are elongated in the [110] direction by an amount $+\Delta$. (c) Systematic variations of d and Δ are applied over an array.

the [110] direction are systematically varied in a 6×7 array, with $d = [29, 30, 30.5, 31, 31.5, 32, 33] \mu\text{m}$ and $\Delta = [0, 0.5, 1.0, 1.5, 2.0, 2.5] \mu\text{m}$. Then a wet thermal oxidation procedure to form an oxide aperture is applied.¹¹ Finally, electrical contacts to the p- and n-doped GaAs surrounding the QDs are fabricated.

To characterize the optical properties of the confined optical modes, standard microphotoluminescence techniques are used. The sample is held in a cryostat at 9.0 K and pumped using an 852 nm laser diode to excite QD emission. We characterize the anisotropy of every micropillar in two different ways. First of all, we measure the polarization-splitting of the fundamental mode to characterize the birefringence. Second, we measure the wavelength differences between the first-order transverse modes and the fundamental mode. This transverse mode splitting is linked to the optical confinement, which can be different in the two directions.

Finally, in order to get an indication of the shape of the buried oxide aperture layer, which determines the optical confinement, a spatial reflection scan is performed at room temperature. For this, a laser with a wavelength $\lambda = 1064 \text{ nm}$ located outside of the DBR stopband is used, such that the reflectance depends on interfering reflections from the top and bottom DBR mirrors. This interference is a function of the optical length of the spacing layer and therefore the reflectance depends on the buried oxide thickness.¹² The front of the oxide is clearly visible as a ring with a lower reflectivity.

Figure 2 shows a micropillar that was elongated slightly, by $0.5 \mu\text{m}$, in the [110] direction. Due to a faster wet oxidation rate in this direction this results in a nearly circular oxidation front as shown in Fig. 2(c). The circular symmetry is apparent as well in the spatial profiles of the confined modes in Fig. 2(b), where the incoherent sum of the two first higher-order Hermite-Gaussian modes resemble a Laguerre-Gaussian transverse mode profile. In Fig. 2(a), however, a clear frequency splitting between two linear orthogonal

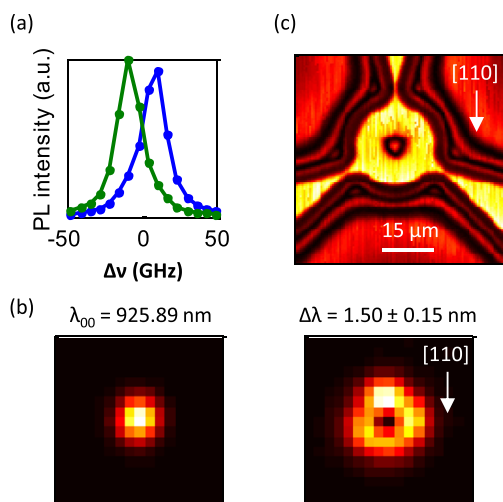


FIG. 2. (a) PL from the fundamental Ψ_{00} mode at two orthogonal polarizations. (b) Spatial PL scans at the wavelength of the fundamental mode and a wavelength interval overlapping with both first-order modes. Wavelengths are selected using a spectrometer. (c) Spatial reflectivity scan of a focused $\lambda = 1064 \text{ nm}$ laser spot indicates the circular oxide front.

polarization modes of the fundamental mode is visible due to birefringence.

Figure 3 shows an even more elliptical micropillar, elongated in the [110] direction by $2 \mu\text{m}$. This elongated shape is now also visible in the shape of the buried oxide aperture in Fig. 3(c). In Fig. 3(b), clear Hermite-Gaussian modes are identified that now possess a great difference between the modesplittings $\Delta\lambda_{10(01)} = \lambda_{00} - \lambda_{10(01)}$, owing to a difference in the amount of optical confinement in orthogonal directions. We define $\Delta\lambda_{10}$ to be in the [110] direction. The polarization splitting of the fundamental mode however is about 1 GHz, less than 6% of the FWHM, indicating the birefringence has been strongly reduced.

Figure 4 shows the result of a systematic characterization of two arrays of which array 2 is oxidized slightly further. Figure 4(a) shows the modesplittings between the fundamental and first order modes, averaged over the two linear polarizations. Clearly, the average modesplitting decreases as the size of the micropillar is increased, as expected. Figure 4(b) shows the ratio $\Delta\lambda_{01}/\Delta\lambda_{10}$ between the modesplittings in two directions. An increasing ratio $\Delta\lambda_{01}/\Delta\lambda_{10}$ corresponds to less optical confinement in the [110] direction with respect to the $[\bar{1}\bar{1}0]$ direction which arises from a more elongated oxide front. This correlates with increasing Δ . Figure 4(c) displays the polarization splitting $\Delta\nu$ of the fundamental Ψ_{00} mode. A clear relation is visible between $\Delta\lambda_{01}/\Delta\lambda_{10}$ and $\Delta\nu$.

We qualitatively explain our findings by a modification of the birefringence under the influence of uniaxial strain in the [110] direction.⁸ Even for the almost circular apertures that remain after oxidation, some uniaxial strain is expected as the oxide layer is more extended in the [110] direction. This can be the result of an anisotropy of the oxidation rate in combination with the location of the three bridges. When the oxide front is more elongated, however, we expect the strain to be reduced such that the birefringence can be fully compensated for.

An important figure of merit of microcavities is the Purcell factor. For the cavity shown in Fig. 3, we find a

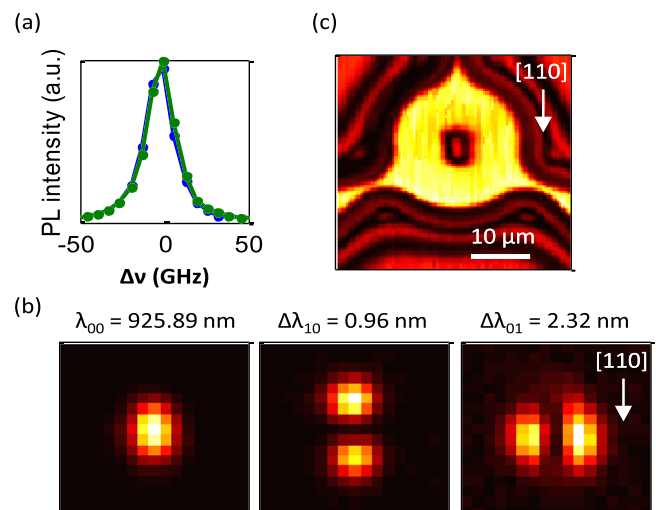


FIG. 3. (a) PL from a polarization degenerate Ψ_{00} cavity mode. (b) Spatial PL scans of the fundamental Ψ_{00} and the first-order Ψ_{10} and Ψ_{01} modes. (c) Spatial $\lambda = 1064 \text{ nm}$ reflectivity scan that indicates the oxide front is elongated in the [110] direction.

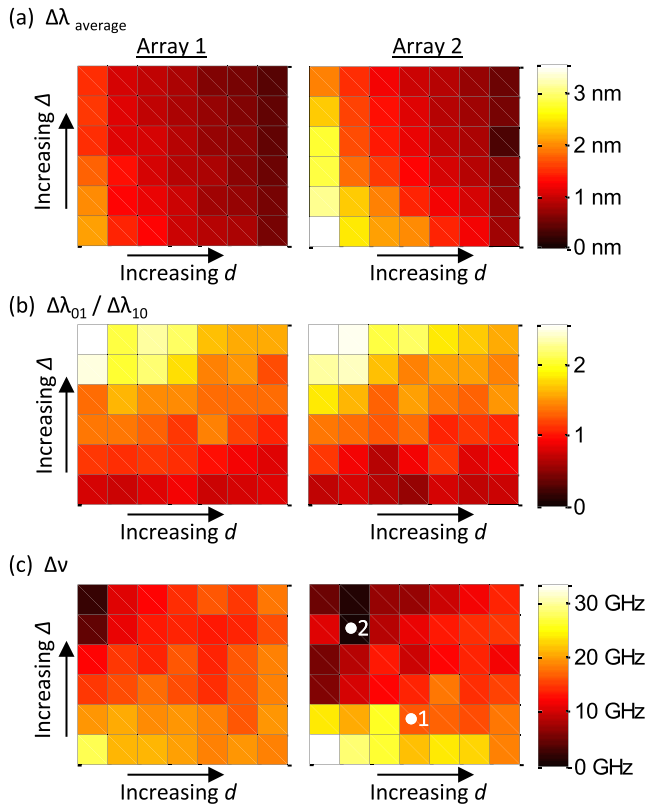


FIG. 4. Colormaps indicate from two arrays: (a) the average modesplittings $\Delta\lambda_{\text{average}}$ between the first order Ψ_{10}/Ψ_{01} modes and the fundamental Ψ_{00} mode, (b) the ratio $\Delta\lambda_{01}/\Delta\lambda_{10}$ of the modesplittings between the Ψ_{01}/Ψ_{10} and the Ψ_{00} modes, and (c) the polarization splitting $\Delta\nu$ of the Ψ_{00} mode. Array 2 exhibits a larger average modesplitting and thus has oxidized slightly further. The dots 1 and 2 denote the cavities displayed in Figs. 2 and 3, respectively.

Q -factor of $Q \approx 1.7 \times 10^4$ and by following methods described in Ref. 13 we predict that a maximum Purcell factor of 11 can be achieved.

We would like to remark that shape birefringence due to anisotropic confinement is small (<1 GHz) in our micropillars and a paraxial (and scalar) description practically suffices. The polarization/vector correction to the scalar wave equation, as calculated from perturbation theory,^{14,15} predicts that the shape-induced birefringence of the fundamental mode is a factor $(\Delta\lambda_{01} + \Delta\lambda_{10})/(2\lambda_{00})$ smaller than the

shape-induced confinement splitting $(\Delta\lambda_{01} - \Delta\lambda_{10})$, which results in a value of 0.84 GHz for the numbers mentioned in Fig. 3.

In conclusion, we have shown it is possible to control the shape of the oxide aperture by the shape of the micropillar. By applying systematic variations in the etched shapes, the strain-induced birefringence is varied and polarization degenerate cavities are obtained. This is an appealing approach towards fabrication of polarization degenerate microcavities with minimal post-processing tuning techniques required.

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Formation of InGaAs fins by atomic layer epitaxy on InP sidewalls

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We describe a fabrication process which forms InGaAs fins with sub 10 nm thickness and 180 nm height. The process flow requires no semiconductor dry-etch, thereby avoiding surface damage arising from such processes. Instead, InGaAs fins are formed using nanometer controlled atomic layer epitaxial growth, using tertiarybutylarsine, upon InP sidewall which are eventually selectively etched. Such fins can serve as channels of field effect transistors, allowing excellent electrostatics and with potentially high operating current per fin.

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1. Introduction

As the gate length of field effect transistors (FETs) in VLSI is reduced, the channel thickness must be proportionally reduced to maintain strong electrostatic control of the channel potential by the gate and thereby suppress short-channel effects.¹⁾ Even for finFETs,²⁾ whose electrostatics are superior to those of planar FETs, for low drain-induced barrier lowering (DIBL) and steep subthreshold characteristics the fin thickness must be at most half the channel length.¹⁾ Thus for a 22 nm gate length, the fin must be less than 11 nm thick. State of the art finFETs have been fabricated using dry-etch processes, exhibiting excellent off-state performance, but greater than 50 mV/V DIBL was observed for a device with 60 nm gate length and 30 nm fin thickness.²⁾

To further reduce the gate length, to 11 nm or less, the finFET body thickness must be reduced to a few nanometers, hence nanometer control of this dimension is essential. Isotropic wet-etching cannot produce highly anisotropic structures such as fins. Even with highly directional dry-etching, if the fin height exceeds the fin thickness by a large ratio, then small deviations from vertical in the etched edge sidewall profile will lead to large fractional variations with height in the fin thickness; a 10 nm tall fin with 3 degree variation from vertical in sidewall slope would show 1.0 nm thickness variation between base and top. Particularly with III-V semiconductors, dry-etch processes also produce significant surface damage. Nanometer-thick fins can also be defined using facet-selective etches,³⁾ while nanowire FETs can be formed using selective chemical etches to remove sacrificial semiconductor layers grown between planes of semiconductor channel material.⁴⁾

Here we report fabrication of sub-10 nm-thick channels by atomic layer epitaxial (ALE) growth on a template whose vertical sidewalls are in turn defined by a facet-selective etch. The fins are subsequently released by removing the growth template with selective chemical etches.

ALE provides nanometer control of the thickness of grown layers.^{5,6)} It is conformal, and hence can grow nanometer thick channel layers on a sidewall of a ridge. Ide⁷⁾ has reported ALE growth of InGaAs on the sidewalls of GaAs grooves, while Usui⁸⁾ demonstrated sidewall growth by ALE of InGaP on various GaAs facets.

In contrast to previous work using arsine as the group V-precursor,⁹⁾ here we report ALE of InGaAs using tertiary-butylarsine (TBAs). We also report a process flow to fabricate InGaAs fins using ALE growth on the (0 $\bar{1}$ 1) sidewall of patterned InP ridges or fins.¹⁰⁾ The group-III precursors were trimethylindium (TMI) and trimethylgallium (TMGa) and all experiments were conducted at a reactor pressure of 30 Torr in a horizontal Thomas Swan 2-in. MOCVD reactor.

2. Process flow and InGaAs ALE calibration

Figure 1 outlines the process flow and in this section we will describe this process in detail.

The process starts by formation of a ridged InP template upon which the InGaAs fins are grown. After growth by MOCVD on a semi-insulating InP substrate of a InP buffer layer, a 20-nm-thick InGaAs etch-stop layer and a 180 nm InP template layer were then grown. The wafer is then coated by a plasma enhanced chemical vapor deposition (PECVD) SiN_x 100-nm-thick hard-mask layer. Lines of 200 nm width and 200 nm spacing, oriented in the [011] direction, are then defined in the SiN_x by Ebeam lithography with subsequent dry etching of the SiN_x using CHF₃. The InP layer is then wet-etched in 3 : 1 H₃PO₄ : HCl with weight assays of 85.3 and 37.5% respectively, to form the growth template. This etch is facet-selective, and reveals the (0 $\bar{1}$ 1) sidewall surface. Figure 2(a) shows the fin template profile; there is only minor etch undercut at the InP/SiN_x interface, as also shown previously.¹¹⁾ Initial experiments using photoresist (SPR955-CM series) as the etch mask failed due to poor resist adhesion, while a PECVD-deposited SiO₂ hard mask showed >100 nm lateral undercutting of the InP during the H₃PO₄ : HCl etch [Fig. 2(b)].¹²⁾

After forming the ridged InP growth template using a SiN_x hard mask, the InGaAs channel layers were then grown by ALE onto (0 $\bar{1}$ 1) sidewalls of the InP template. As shown in the gas injection scheme, Fig. 3, in each ALE growth cycle, TMGa and TMI were first injected simultaneously, followed by a H₂ purge, the injection of TBA, and a second H₂ purge. As the cycle times were varied to characterize the ALE growth, equal times were maintained for these four steps. The ALE growth cycles were controlled by mass flow controllers (MFCs) rather than by pneumatic valves.

The InGaAs ALE growth was first calibrated by characterizing InGaAs layers grown on (100) InP substrates using X-

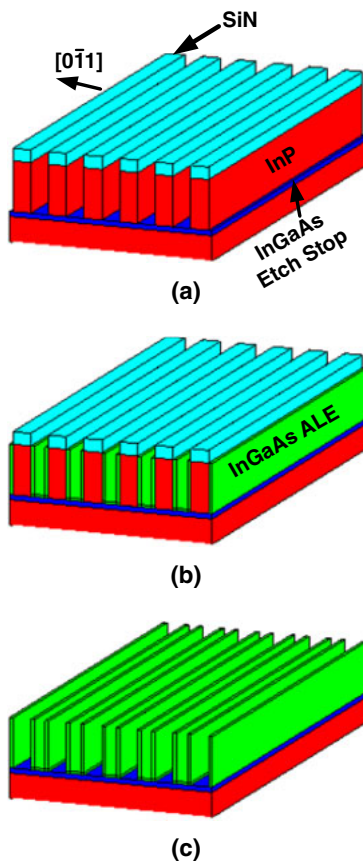


Fig. 1. (Color online) Process flow to form array of fins using InGaAs ALE. (a) Fin template formation. (b) InGaAs Channel growth by ALE. (c) Fin release.

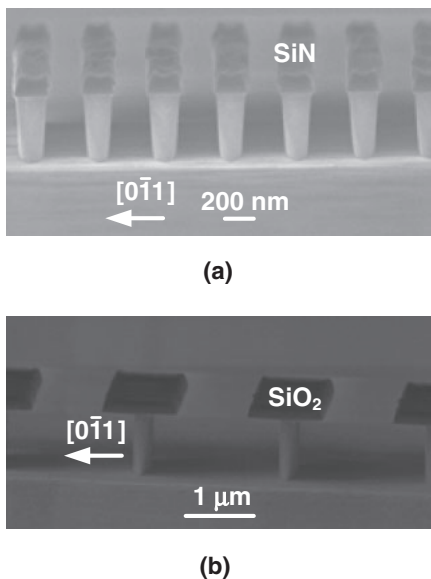


Fig. 2. SEM images of (a) ridged InP growth template formed using SiN_x as the hard mask for the H₃PO₄ : HCl facet-selective wet etch, and (b) a similar InP template wherein SiO₂ was used as the hard mask for the H₃PO₄ : HCl etch. With SiN_x, much smaller etch undercut is observed at the mask/InP interface.

ray diffraction (XRD) with a coupled scan ($\omega-2\theta$) of the incident angle (ω) and the diffracted angle (2θ). The InGaAs layer thickness and composition were extracted by numerical fitting to the width and location of the Bragg diffraction peak.

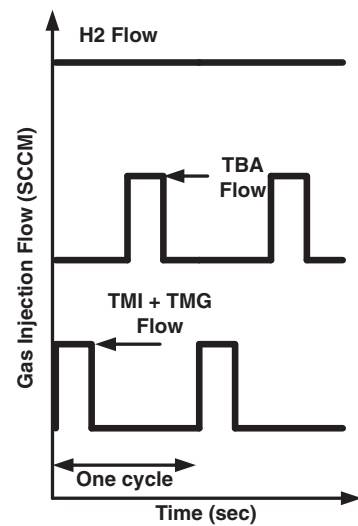


Fig. 3. Gas injection scheme.

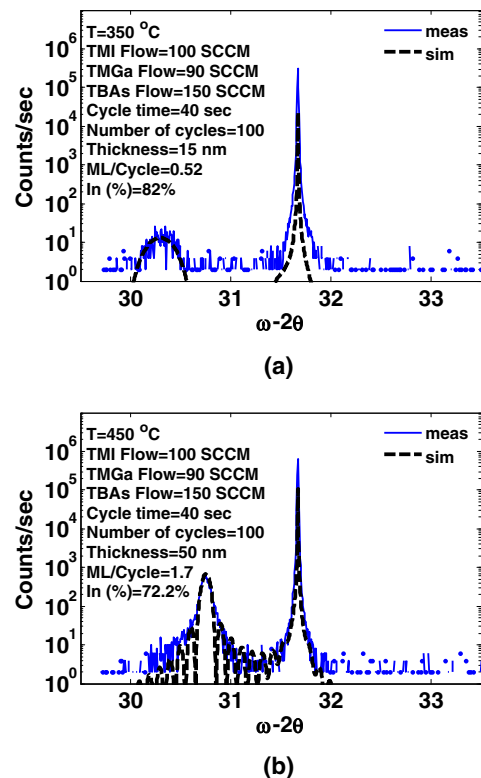


Fig. 4. (Color online) XRD data for 100 cycles of ALE InGaAs grown on a (100) InP substrate at 350 °C (a) and 450 °C (b).

ALE growth temperature is determined largely by the decomposition temperatures of the metalorganic (MO) sources.⁶⁾ TMI and TBAs begin to decompose below 300 °C, while TMGa decomposes above 400 °C.¹³⁾ Growth characterization started with 100 cycles of ALE growth of InGaAs on a (100) InP substrate at 350 °C. Each growth cycle was 40 s duration and the TMGa, TMI, and TBAs flows were 90, 100, and 150 sccm respectively. Give the low 350 °C growth temperature, the TMGa does not fully decompose, and a 15-nm-thick indium-rich layer, In_{0.82}Ga_{0.18}As, was grown [Fig. 4(a)]. Increasing the growth temperature to 450 °C, with the same MO flow rates and the

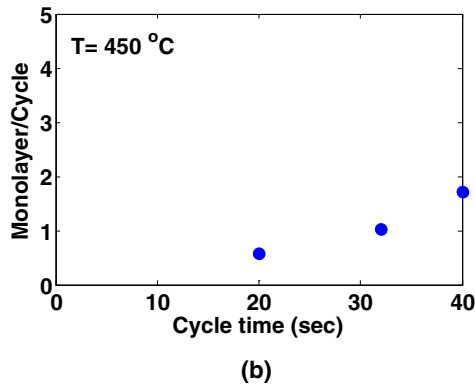
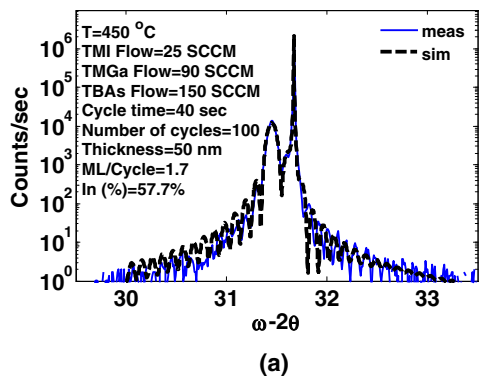


Fig. 5. (Color online) XRD of lattice-matched InGaAs grown by ALE (a) and monolayers of growth per cycle vs cycle time (b). Both experiments were done on a (100) InP substrate with TMI, TMGa, and TBAs fluxes of 25, 90, and 150 sccm.

same cycle times, results in more complete TMGa decomposition. The 450 °C growth produced a thicker and less indium-rich layer, 50 nm $\text{In}_{0.72}\text{Ga}_{0.28}\text{As}$, as measured by XRD [Fig. 4(b)].

Adjusting the TMI and TMGa flow rates to 25 and 90 sccm, respectively, then resulted in the ALE growth, after 100 cycles, of 50 nm $\text{In}_{0.57}\text{Ga}_{0.43}\text{As}$ [Fig. 5(a)], a composition close to being lattice-matched to InP. The 50 nm (100) layer corresponds to 1.7 monolayer per cycle (ML/cycle), where one InGaAs monolayer equals to 0.29 nm. This growth rate, above one ML/cycle, indicates that the growth was not self-limiting as in a classic ALE process, most likely related to the relatively high growth temperature at which TBAs and TMI completely decompose.¹³ The growth sequences above are nevertheless sufficiently well-controlled to grow layers of a few nm thickness. The relationship between cycle time and growth rate was then investigated. Growths were performed on a (100) InP substrate, at 450 °C with TMI, TMGa, and TBAs fluxes of 25, 90, and 150 sccm. As illustrated in Fig. 5(b) the number of InGaAs monolayers deposited per cycle monotonically increased with cycle time, indicating that the growth was not self-limiting as we mentioned above.

Given that the InGaAs fins are grown on the (0 $\bar{1}$ 1) sidewalls of the InP template, ALE growth of InGaAs on (110) InP was then characterized. Growth was performed at 450 °C, with TMI, TMGa, and TBAs fluxes of 25, 80, and 150 sccm, and with a 40 s cycle time. 60 cycles ALE growth produced 20 nm $\text{In}_{0.48}\text{Ga}_{0.52}\text{As}$ layer as measured by XRD (Fig. 6). In the (110) orientation, one monolayer is 0.21 nm,

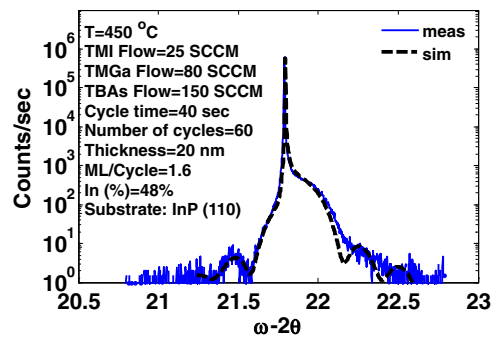


Fig. 6. (Color online) XRD of lattice-matched InGaAs grown by ALE on (110) InP substrates with TMI, TMGa, and TBAs fluxes of 25, 80, and 150 sccm.

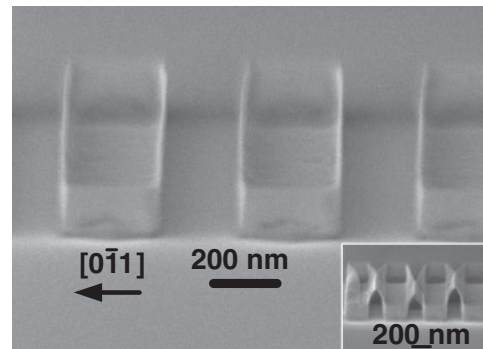


Fig. 7. SEM image of fins of <10 nm width and 180 nm height. When fins are fabricated at spacing less than 200 nm, the fins bend and stick together during drying (inset).

hence the observed growth rate corresponds to 1.6 ML/cycle. On this sample, ~ 0.3 nm average roughness (R_a) and ~ 0.3 nm root mean square roughness (R_q) were measured by atomic force microscopy, and an electron mobility of $3300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and electron concentration of $1.19 \times 10^{15} \text{ cm}^{-3}$ were extracted from Hall measurement.

For all subsequent experiments, involving InGaAs ALE on the (0 $\bar{1}$ 1) sidewalls of InP fins, growth was performed at 450 °C, with TMI, TMGa, and TBAs fluxes of 25, 80, and 150 sccm. With ALE growth on planar (110) and (100) InP wafers characterized, samples were then prepared for the ALE growth of InGaAs onto the (0 $\bar{1}$ 1) sidewalls of InP ridged growth templates. InP ridged growth templates were first prepared as described above [Fig. 1(a)], oxidized by UV ozone, etched in dilute HCl and then the InGaAs was grown on the InP template sidewalls [Fig. 1(b)]. The SiN_x hard mask was then stripped and the InGaAs fins were released [Fig. 1(c)] by a selectively etching away the InP template layer in 3 : 1 H_3PO_4 : HCl, thereby leaving free-standing InGaAs fins.

3. Results and discussion

Figure 7 shows a typical structure, showing InGaAs fins of ~ 10 nm width and 180 nm height, at 200 nm spacing, grown with 20 cycles ALE. When the wafer is rinsed and dried after H_3PO_4 : HCl etching, the fins are exposed to large forces arising from surface tension. With 10 nm width and 180 nm height, these forces cause the fins to bend and stick together if their spacing is less than 200 nm (Fig. 7 inset). It is possible that this bending might be avoided by drying the

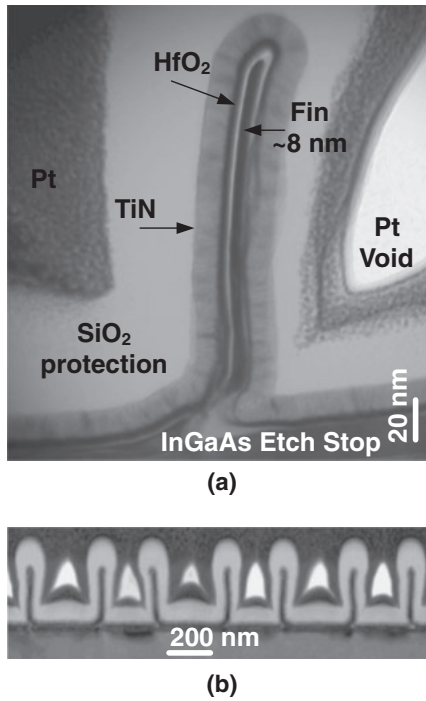


Fig. 8. TEM images of (a) 8 nm width fins of 180 nm height coated with HfO₂ gate dielectric and TiN gate metal and (b) fin array at 200 nm pitch.

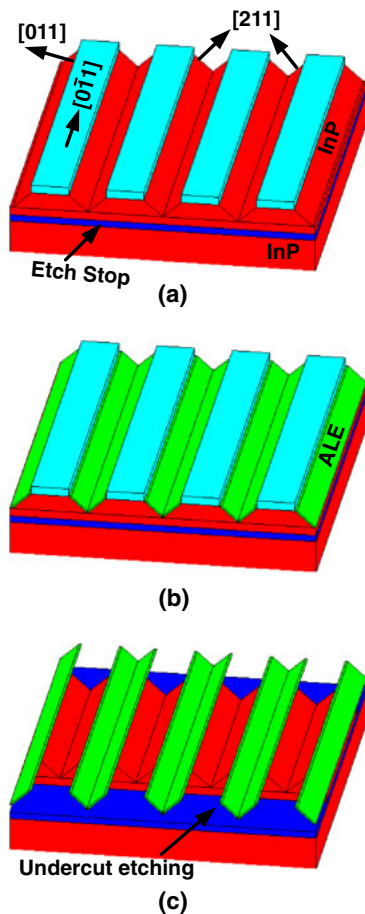


Fig. 9. (Color online) Fabrication sequence for fabrication of (211) InGaAs fins. The SiN_x mask is (a) oriented in the [011] and the InP template layer etched in H₃PO₄ : HCl, InGaAs is grown by ALE (b) on the resulting (211) InP surfaces and (c) the InP template is partially removed, liberating the fins.

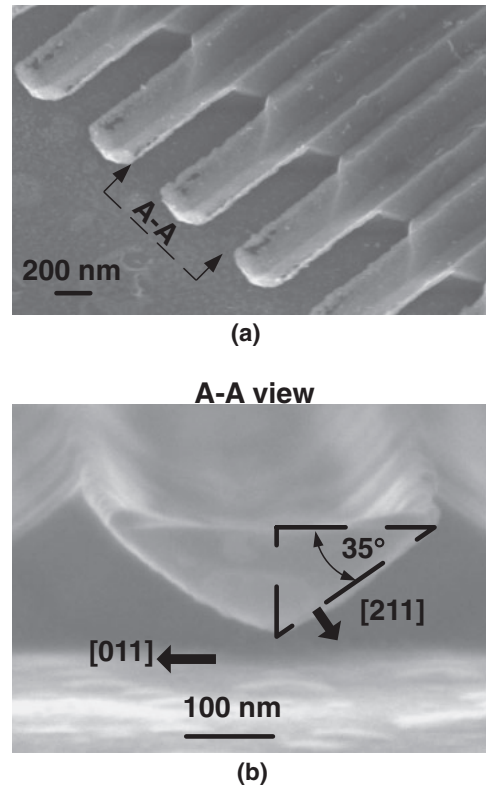


Fig. 10. SEM image of 30 nm wide ALE channel on top of [211] InP grooves (a). A side view (b) shows 35° between the [211] InGaAs ALE channel and [011].

samples in CO₂ at the critical point,¹⁴ as has been reported in the fabrication of MEMS structures.

Bending can also be avoided by first providing mechanical support before releasing the InGaAs fins from the InP support layer. This support can be provided by selective-area MOCVD growth of N⁺ InGaAs source and drain regions contacting the InGaAs fin.¹⁰ Fins fabricated in this fashion are shown in Fig. 8; these are surrounded by 4 nm HfO₂ gate dielectric and 10 nm TiN gate metal, both deposited by atomic layer deposition (ALD) as part of a full finFET process.¹⁰ Support by the N⁺ regrowth prevents the fins from bending and adhering even when fabricated at 200 nm pitch [Fig. 8(b)].

In order to explore the robustness of the process flow to manufacture channels upon different facets than (011) InP, ALE growth on other InP sidewalls was also investigated. If the SiN_x mask lines are oriented in the [011] direction (Fig. 9), then the H₃PO₄ : HCl facet-selective etch forms grooves in the InP with inclined (211) sidewalls.¹⁵ 60 cycles of InGaAs was then grown by ALE upon these InP surfaces, using the growth conditions of Fig. 6. In this process, to retain mechanical support of the InGaAs fins, the InP growth template is not removed over the full length of the InGaAs regrowth (Fig. 9). Where the InP is removed, the InGaAs is a free-standing, cantilevered membrane. Figure 10(a) shows a SEM image from above, of the free-standing (211) InGaAs fins, while Fig. 10(b) shows an end-view. While not of immediate interest for finFet applications, the results illustrate the versatility of the investigated fabrication procedure.

4. Summary

In summary, InGaAs fins of <10 nm width and 180 nm height were fabricated using atomic layer epitaxy on the sidewalls of InP growth template layers. A full nm finFET fabrication process is in development.

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