# Vertical-cavity surface-emitting lasers with lateral carrier confinement

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A novel method to reduce threshold currents in vertical-cavity surface-emitting lasers (VCSELs) is proposed. By using selective quantum well intermixing, lateral heterobarriers are created that prevent carriers from diffusing away from the optical modes. Our devices show 40% reduction of threshold currents with the implementation of lateral carrier confinement.

*Introduction:* Optics is a viable solution to address the limitations of copper-based electronics in short-distance interconnects [1]. In these compact systems, devices must meet the stringent requirements imposed by the power budget and the thermal restriction. Recently, VCSELs have received considerable interest for board and chip level interconnects owing to their small footprints, ease of fabrication in arrays, and high-speed operation at low power dissipation. Smaller VCSELs are even more favourable in terms of speed and power consumption. However, as the dimension of VCSELs scales down, threshold currents do not scale accordingly owing to optical diffraction loss [2], current spreading [3], and carrier diffusion [4]. Optical diffraction loss can be reduced using tapered oxide aperture [2], and current spreading can be eliminated by placing the aperture close to the active region. Once carriers enter the quantum wells (QWs), the large lateral concentration gradient drives carriers to diffuse outwards and, consequently, a significant portion of the current does not provide useful gain to the optical modes and is dissipated as heat. To alleviate the problem, carriers must be confined laterally inside the QWs. In this Letter, we report a new VCSEL-compatible quantum well intermixing (QWI) process to achieve lateral carrier confinement. Using a sacrificial silicon-doped InGaP layer, we were able to selectively intermix InGaAs QWs for 980 nm VCSELs and our smallest 1 µm diameter device shows 40% reduction of threshold with the implementation of lateral carrier confinement.

*Device structure and fabrication:* The sample was grown on an *n*-type GaAs (100) substrate by molecular beam epitaxy (MBE). The bottom mirror consists of a 19-period silicon-doped GaAs/AlGaAs distributed Bragg reflector (DBR), followed by a 113 nm $Al_{0.3}Ga_{0.7}As$ separate confinement heterostructure (SCH). The active region consists of three InGaAs/GaAs QWs. On top of the QWs is a 36 nm $Al_{0.3}Ga_{0.7}As$ SCH, followed by a 50 nm GaAs layer for aluminum-free regrowth. A 300 nm sacrificial InGaP layer was then grown for intermixing purpose with the top 200 nm heavily doped with silicon to enhance QWI [5].

The intermixing process began by depositing and patterning $SiO_2$ on top of the sample and then subjecting the sample to reactive ion etch (RIE) with $CF_4/O_2$ gases to fluorinate the surface. It was then capped with another layer of $SiO_2$ and annealed at 850°C for 8 min using rapid thermal annealing (RTA). During the RTA, gallium atoms outdiffused into the $SiO_2$ and left vacancies at the surfaces in direct contact with $SiO_2$. Sequentially, these vacancies diffused down into the QWs and promoted the intermixing process [6]. On the other hand, fluorine bound with gallium and indium atoms to create gallium and indium fluorides during the RIE step on the surfaces without $SiO_2$, and these fluorides were reported to be thermally stable [7]. Because vacancies were not created, the intermixing process was suppressed. After RTA, the $SiO_2$ and InGaP layers were stripped off using buffered HF and diluted HCl, respectively, and the sample was loaded into MBE for regrowth.

A 10 nm GaAs layer was grown on top of the regrowth layer, followed by a 60 nm $Al_{0.8}Ga_{0.2}As$ and a 10 nm AlAs to form the tapered oxide aperture. The top mirror consists of a 32-period carbon-doped GaAs/AlGaAs DBR, followed by a highly doped *p*-contact layer. The device fabrication began by etching cylindrical mesas and forming the aperture using wet oxidation. Ti/Pt/Au and AuGe/Ni/Au were evaporated for *p*- and *n*-contacts, respectively. Finally, an antireflection coating was deposited to reduce the backside reflection.

*Results and discussion:* Fig. 1 shows the secondary ion mass spectrometry (SIMS) results for the non-intermixed and the intermixed areas on a test sample. In Fig. 1*a*, three indium peaks corresponding to three InGaAs QWs are clearly seen, which indicates that surface fluorination did help to preserve the layer structure during the RTA. The only noticeable difference from the as-grown sample (not shown) is that silicon atoms on the top 200 nm InGaP layer diffuse towards the active region. On the other hand, the indium profile of the QWs is completely washed out for the intermixed areas, as shown in Fig. 1*b*. Aluminum also diffused into the QWs, which is necessary to get enough bandgap shift for effective carrier confinement. Silicon atoms also diffused into the QWs at the non-intermixed areas and will introduce free carrier absorption loss, as will be seen in the device results.

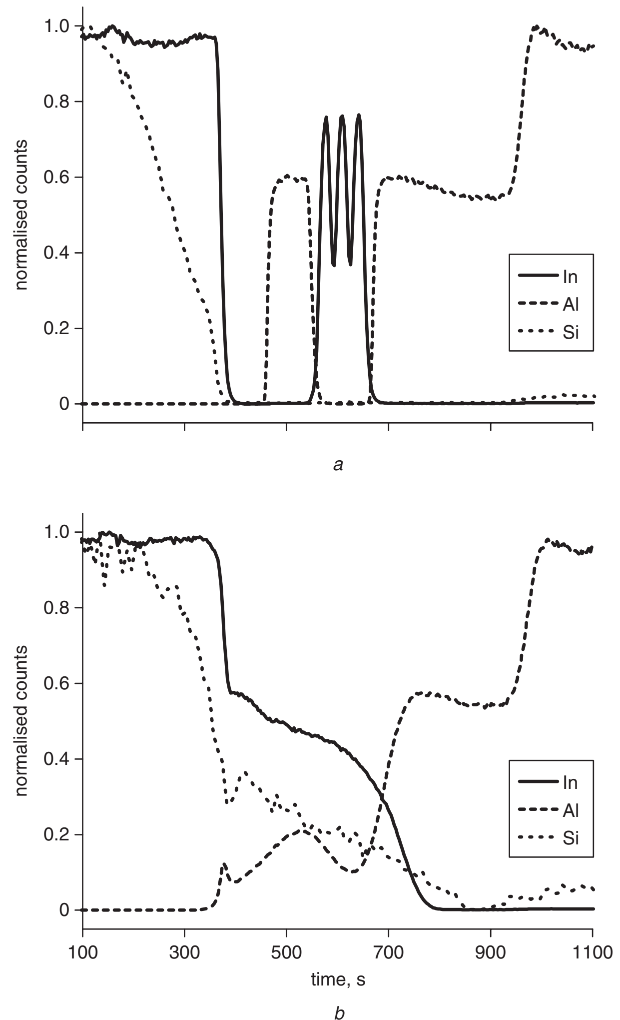


**Fig. 1** *SIMS results showing aluminum, indium and silicon profiles*

*a* On non-intermixed area
*b* On intermixed area

Fig. 2 shows the threshold currents and differential quantum efficiencies for intermixed and non-intermixed VCSELs. There is significant scatter in the data owing to the roughness of the *p*-DBR regrowth interface, causing random amounts of loss for each device. However, the general trend is obvious. The devices where QWs have been selectively intermixed clearly show reduced threshold currents compared with the samples where QWs have not been intermixed. The reason that the VCSELs show higher thresholds overall can be explained by extra added loss at the regrowth interface since the differential quantum efficiencies are also statistically lower, as seen in Fig. 2*b*. For those that have been selectively intermixed, differential quantum efficiencies drop slightly for devices smaller than 4 µm. This indicates a size-dependent loss mechanism that is only present for the intermixed devices. Most likely, this loss comes from silicon diffusion into the QWs during the intermixing process and is more severe for smaller devices. To get a better measure of the amount of intermixing, the thresholds are fitted to a model to estimate the barrier height. The data lies partially on the 200 meV barrier curve for larger devices and partially on the 100 meV curve for smaller devices. Owing to the

size-dependent loss, the barrier is more likely to be closer to 200 meV, which is enough to provide lateral carrier confinement in VCSELs.

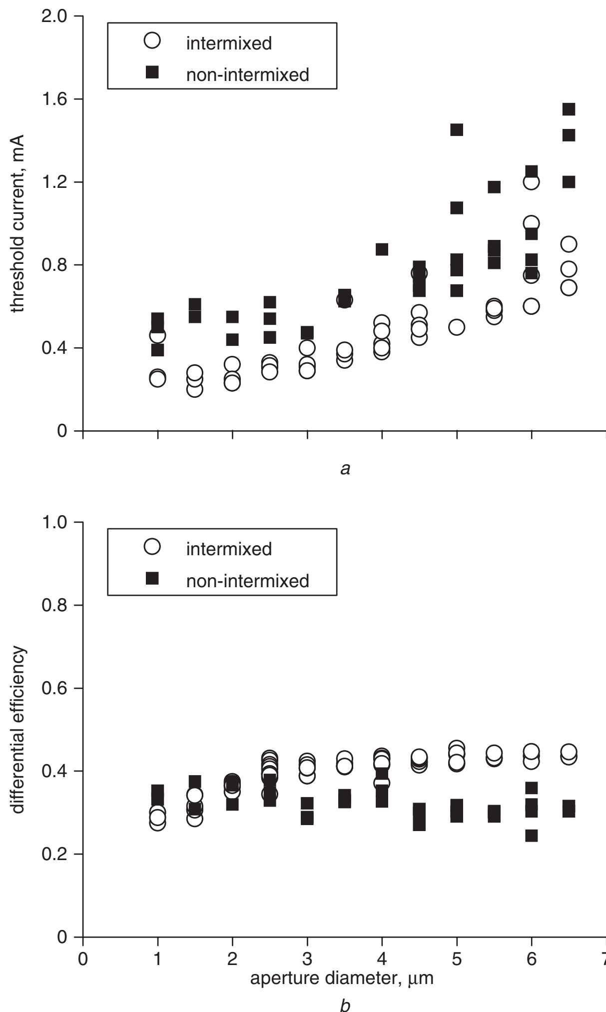


**Fig. 2** *Threshold currents for different diameter devices, and differential quantum efficiencies for different diameter devices*

*a* Threshold currents
*b* Differential quantum efficiencies

*Conclusions:* We have developed a new VCSEL-compatible QWI process to achieve lateral carrier confinement in VCSELs and our results show that threshold currents are indeed reduced with lateral carrier confinement.

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