An 8 × 8 InP Monolithic Tunable Optical Router (MOTOR) Packet Forwarding Chip

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***Abstract*—In this paper, we demonstrate single-channel operation of the first InP monolithic tunable optical router (MOTOR) chip designed to function as the packet forwarding engine of an all-optical router. The device has eight-input and eight-output ports and is capable of 40-Gb/s operation per port with bit-error rates below 1E-9. MOTOR integrates eight wavelength-tunable differential Mach–Zehnder semiconductor optical amplifier (SOA) wavelength converters with preamplifiers and a passive 8 × 8 arrayed-waveguide grating router. Each wavelength converter employs a widely tunable sampled-grating distributed Bragg reflector (DBR) laser for efficient wavelength switching across the C band and other functions required for 40-Gb/s wavelength conversion. Active and passive regions of the chip are defined through a robust quantum well intermixing process to optimize the gain in the wavelength converters and minimize the propagation losses in passive sections of the chip. The device is one of the most complex photonic integrated circuits (PICs) reported to date, with dimensions of 4.25 mm × 14.5 mm and more than 200 functional elements integrated on-chip. We demonstrate single-channel wavelength conversion and channel switching with this device using $2^{31} - 1$ pseudorandom bit sequence (PRBS) data at 40 Gb/s. A power penalty as low as 4.5 dB was achieved with less than 2-W drive power per channel.**

***Index Terms*—Arrayed-waveguide grating router (AWGR), photonic integrated circuits (PIC), quantum-well intermixing (QWI), wavelength converter.**

I. Introduction

ADVANCED photonic integrated circuits (PICs) in InP are a critical technology to manage the increasing bandwidth demands and core functions of next-generation optical networks [1]–[4]. The integration of many of the discrete functions required in optical networks into a single device provides a reduction in system footprint and optical losses due to the elimination of fiber coupling junctions between components, and an increase in overall reliability. Many key network components such as transceivers [5], wavelength converters [6]–[9], optical cross connects [10], add-drop multiplexers [11], and channel selectors [12] have already been realized in InP via monolithic integration. While the potential benefits of creating larger, higher functionality PICs have long been suggested, there are still very few demonstrations of PICs with more than 50 integrated components [2], [13].

Large scale integration in silicon-based integrated circuits has led to exponential growth in that industry and tremendous performance gains with a reduction in costs to the consumer. Robust design and manufacturing techniques that will enable high-yield production of large scale PICs are thus required to realize similar performance and cost improvements in the photonics industry [3]. Such efforts have been underway for several years, and the benefits of large scale integration are now being seen commercially with the recent report by Infinera of plans to deploy a 400-Gb/s PIC transmitter with more than 300 optical functions in live networks [14].

All-optical routing is a potential avenue in which large scale PICs could play a revolutionary role [15]. By moving the functions of dynamic wavelength conversion and routing to the optical layer, it may be possible to ease the increasing power consumption demands associated with scaling electronic-based routers to higher data rates [16]. For instance, discrete all-optical wavelength converters have been reported that entirely eliminate the need for power-hungry optical-to-electrical (O/E) and electrical-to-optical (E/O) data conversion [6]–[9]. While these demonstrations of wavelength conversion without O/E/O conversions are promising, the realization of a competitive all-optical alternative to electronic routers is still limited by challenges associated with optical buffering [17].

In [18], a label-switched all-optical router (LASOR) with the ability to process 40-Gb/s packets was proposed. This router architecture (Fig. 1) enables synchronization and buffering of input packets in the optical domain, and provides a means to write the input data onto a new wavelength for wavelength-selective routing. While each functional block of the router could be realized with a discrete PIC, the performance of this system in terms of reliability, optical coupling losses, and overall footprint can be significantly improved via large scale monolithic integration.

In this work, we combine the wavelength conversion and passive routing elements of LASOR shown in Fig. 1 into a single InP chip to demonstrate a monolithic tunable optical router (MOTOR) that serves as the packet-forwarding engine of an all-optical router [Fig. 2(a)]. The eight-channel InP/InGaAsP device operates at 40-Gb/s line rate per port giving a total potential data capacity of 640 Gb/s and integrates an array of eight tunable all-optical wavelength converters with a passive 8 × 8 arrayed-waveguide grating router (AWGR).

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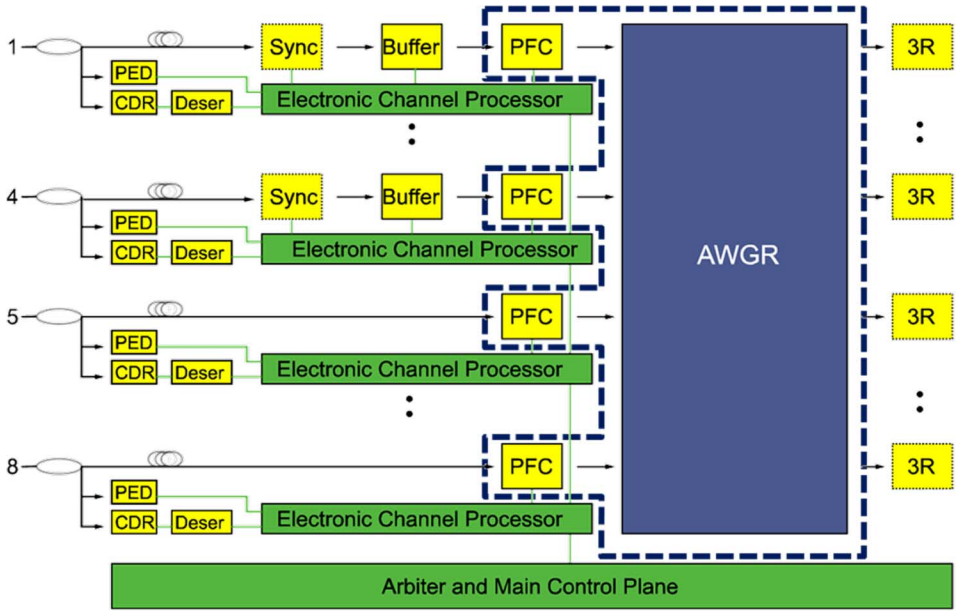

Fig. 1. Overall LASOR architecture. Key to abbreviations: PED = payload envelope detection; CDR = clock data recovery; Deser = deserializer; Sync = synchronizer; WC = wavelength converter; AWGR = arrayed-waveguide grating router; 3R = retiming, reshaping, and reamplification. The dotted region represents the elements integrated in the MOTOR chip.

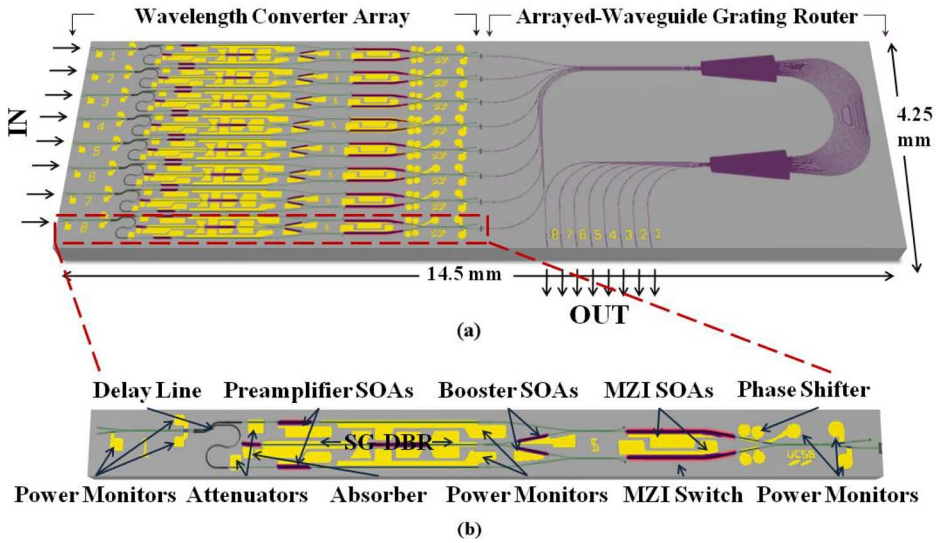

Fig. 2. (a) Schematic of overall MOTOR chip. (b) Expanded view of a single-input wavelength converter showing several key device elements.

The device represents one of the most complex InP PICs ever reported with more than 200 integrated functional elements on a single chip.

II. Device Design and Operation

A. Wavelength Converter Array

The active core of the MOTOR chip contains an array of eight wavelength converters. The technology used to implement these wavelength converters must provide: 1) error-free high-speed operation at 40 Gb/s; 2) wide tunability across the C band; 3) a small footprint; and 4) low power consumption (i.e., no O/E/O conversions). Two popular monolithic approaches to achieve these goals with 40-Gb/s data rates involve carrier-modulation effects in nonlinear semiconductor optical amplifiers (SOAs) [6], [7] or field-modulation effects with a photodiode and a modulator [9]. While each approach has inherent advantages, the design and fabrication of field-modulation-based wavelength converters tends to be more complex than that of carrier-modulation-based devices because they require integrated resistors and more complex modulator structures [9]. In order to target high device yields, we use the simpler carrier-modulation approach in the MOTOR chip.

Because our wavelength converter design exploits nonlinear SOA within a Mach–Zehnder interferometer (MZI) as in [7], both cross-phase and cross-gain modulation effects are present. However, cross-phase modulation in the MZI is the method used to shape the output pulses from the device. A detailed view of a

single-input MOTOR port is shown in Fig. 2(b). The input data signal to the chip depletes the carriers in a nonlinear SOA and changes the phase in one branch of an MZI. This phase change modulates the MZI and carves out the input data pattern onto a continuous wave (CW) source operating at the new wavelength. The overall speed of these devices is inherently limited by the carrier lifetime in the SOAs, so a differential delay line at the front end of the chip is included [7]. By time delaying the input data signal on one side of the MZI, it is possible to overcome the limitation of carrier recovery lifetime so that modulation of the MZI is governed by carrier depletion effects. The time delay is accomplished using an on-chip differential delay line before the inputs to the MZI. After the input data signal is split using a 50/50 multimode interferometer (MMI) splitter, the signals are sent to opposite branches of the MZI. The path length for one branch is increased relative to the other using a compact, tight bend radius waveguide section that adds about 11 ps of propagation delay. This delay time was chosen to simultaneously minimize the overall power penalty associated with wavelength conversion while keeping the delay line length as small as possible to minimize device footprint [19]. In general, improved performance can be achieved if the input power levels to each side of the MZI are slightly imbalanced [7], [20]. Because the path length of the inputs to the MZI differ (and hence the propagation losses differ), and because the observed splitting ratio of the fabricated MMI is sensitive to lithographic resolution, variable optical attenuators (VOAs) are included on each input line to the MZI to control the relative power levels in each branch.

The wide tunability of the wavelength converter is accomplished by incorporating a sampled-grating distributed Bragg reflector (SG-DBR) laser as the on-chip CW source. The laser consists of five sections: a 550-μm active gain section, a 470-μm front, a 910-μm back tuning mirror, a short 100-μm phase tuning pad, and a 175-μm active absorber. About 40 nm of tuning is possible through the Vernier effect [21]. By biasing both the front and back mirrors during operation, it is possible to precisely tune to any of the allowed output wavelengths of the AWGR across the C band.

The MOTOR chip also integrates SOAs with three different functions. First, 285-μm booster SOAs are used to amplify the SG-DBR output power after it is split by a 50/50 MMI splitter and before it is input into each branch of the MZI. Because the SG-DBR output power is already high, the booster SOAs are saturated but provide enough gain to overcome the halving in power from the MMI splitter. Second, nonlinear SOAs are required in the Mach–Zehnder for cross-phase and cross-gain modulation. These SOAs are >1000 μm in length in order to reduce the carrier recovery time, which tends to decrease with increasing SOA length [20]. Finally, 300-μm linear preamplifier SOAs are inserted before the input to the MZI to amplify the input data signal. It is crucial that these SOAs provide an optimal combination of high gain (to ensure that the input pulses have enough power to deplete the carriers in the MZI SOAs) and high saturation power (to avoid pattern dependent distortions that arise if the preamplifier SOAs are operated in the nonlinear regime).

One important consideration with this approach to wavelength conversion is the possibility of wavelength blocking.

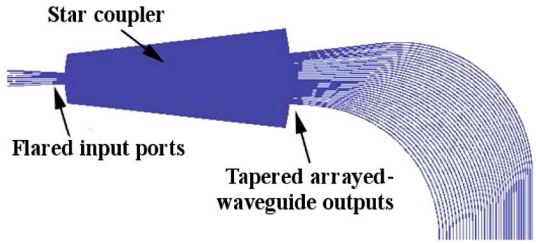

Fig. 3. Schematic view of the AWGR illustrating the flared input and tapered output waveguides.

Unlike the field-modulated wavelength converters of [9], it is not possible to convert back to the input wavelength with the differential MZI SOA wavelength converter because the input data signal exits the device from the same port as the converted signal. In a routing application, this means that the input frequency comb must be different than the output frequency comb and either a high- or low-pass filter would be required at the output to remove the original frequencies.

B. Arrayed-Waveguide Grating Router

The output of the wavelength converter is connected to an AWGR, which passively routes the wavelength converted signal based on the new wavelength of the data (as set by the SG-DBR). Our design employs an 8×8 configuration with 200-GHz channel spacing (to give a reasonable AWGR size), a center wavelength of 1550 nm, and a periodic output frequency response. The major source of loss in an AWGR is from imperfect coupling between the waveguides and the star couplers (or free propagation regions) [22]. To reduce these losses and improve coupling, our design employs flared and tapered waveguides at the star couplers (Fig. 3). The flares and tapers are 100 μm long in order to minimize the excitation of higher order modes. The 2.2-μm waveguide inputs to the star couplers are flared to 8.0 μm and are spaced by 1.0 μm. The 34 arrayed waveguides at the output of the star couplers taper from 8.25 to 2.2 μm and are spaced by only 0.8 μm. The overall size of the AWGR (not including the waveguides to the input star coupler and the waveguides from the output star coupler) is 2.84 mm $\times$ 2.60 mm.

III. Integration Platform

The integration platform used for the MOTOR chip should provide several key features: 1) high-gain regions for the SG-DBR laser and SOAs; 2) low-saturation-power (i.e., nonlinear) SOAs in the MZI; 3) high-saturation-power (i.e., linear) SOAs for preamplifiers; 4) efficient phase modulator regions for the MZI; and 5) low-loss waveguides for the AWGR and passive sections of the wavelength converters. Additionally, the integration platform should minimize the number of required regrowths and limit the overall fabrication complexity in order to maximize device yield. To meet these demands, we use an impurity-free quantum-well intermixing (QWI) process and a single, blanket p-type cladding regrowth.

The initial base epitaxial layer structure [Fig. 4(a)] is grown by MOCVD on a sulfur-doped InP substrate. It is composed of ten 6.5-nm InGaAsP quantum wells under $+0.9\%$ compressive strain and eleven 8.0-nm InGaAsP barriers under -0.2% tensile

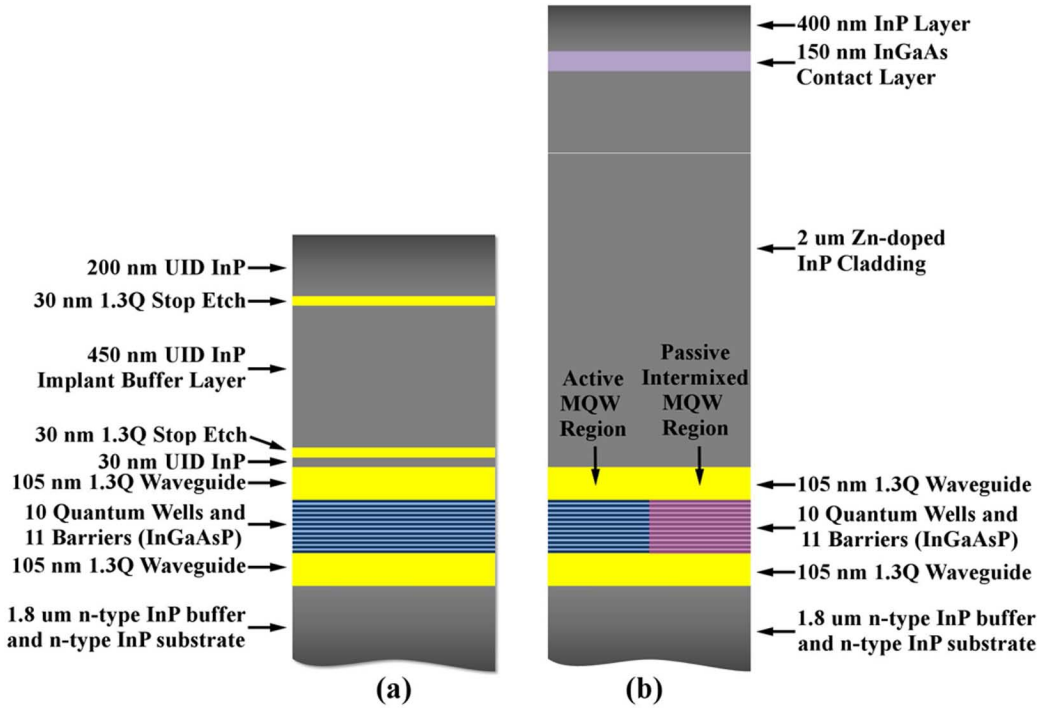

Fig. 4. (a) Initial base epitaxial growth structure. (b) Final growth structure showing both an as-grown active MQW region and an intermixed passive MQW region.

strain ($\lambda_{\mathrm{PL}} = 1545$ nm). The multiple quantum well (MQW) stack is sandwiched by a 105-nm quaternary waveguide ($\lambda_{\mathrm{PL}} = 1300$ nm) on both sides to maximize the modal overlap in the MQWs, resulting in a $\sim$13% optical confinement factor. The increased optical confinement provides high-gain regions for the booster SOAs and the gain section of the SG-DBR and low-saturation power regions for the nonlinear MZI SOAs. However, the decrease in saturation power due to high optical confinement limits the maximum possible unsaturated gain from the preamplifier SOAs. The base growth also incorporates an undoped InP buffer layer above the waveguide for QWI [23]. Passive device regions are defined by selectively implanting phosphorous into the undoped buffer layer above these regions. The implant creates point defects which are then diffused through the waveguide region using a rapid thermal anneal process in N_2 at 675 °C. These vacancies and interstitials allow diffusion of the group V elements across the metastable well and barrier boundaries to reshape the compositional profile of the MQW region and blue shift the band edge from an as-grown λ_{PL} of 1545 to 1420 nm. Because the passive regions still contain quantum wells, it is possible to realize more efficient phase shifters in the MZI region than would be available with only bulk waveguide. MQWs provide a greater refractive index change for a given injected current density than bulk material because of the step-like density of states of a 2-D system [24]. In practical terms, this means that less current (and hence a lower drive power) is required to tune the phase of the MZI to a normally closed (noninverting) or open (inverting) state.

Following QWI, the implant buffer layer is removed across most of the sample by wet etching. In the passive regions of the differential delay line and the AWGR, however, the buffer layer is not removed in order to provide an undoped setback

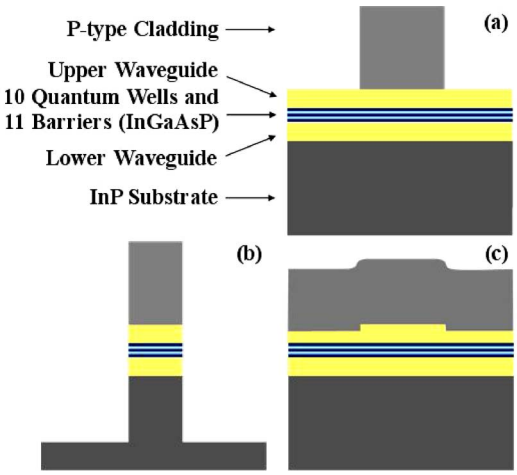

Fig. 5. Waveguide architectures used in the MOTOR chip: (a) surface ridge waveguide; (b) deeply etched waveguide; and (c) buried rib waveguide.

layer between the waveguide and the subsequent cladding. As described in [25], this helps to reduce optical loss from free carrier absorption due to the Zn dopant used in the cladding layer. The epitaxial structure is completed by a simple, blanket p-type regrowth [Fig. 4(b)]. A 150-nm heavily Zn-doped InGaAs layer is included in the regrowth for Ohmic p-type contacts. Using a single regrowth step reduces fabrication complexity and should have a positive impact on device yield. However, the Zn doping profile with this approach must be optimized to provide efficient active diode performance without detrimentally increasing passive propagation losses from free carrier absorption [26]. To address this inherent tradeoff, our cladding regrowth starts with a thin undoped InP layer followed by growth with Zn doping.

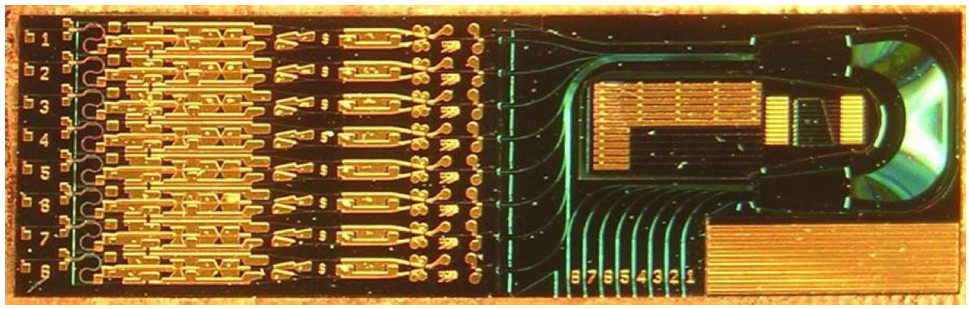

Fig. 6. Photograph of fabricated MOTOR chip. The chip is soldered to a large copper block and electrodes are directly probed. Miscellaneous test structures are contained in the center of the AWGR region, but these components are not used during the operation of the device.

Due to the elevated growth temperature, some Zn diffuses toward the waveguide, creating the desired p-i-n junctions of the device. The thickness of this undoped regrowth layer (typically ∼30–50 nm) is calibrated to ensure that the Zn doping concentrations within the waveguide are as low as possible. To reduce the loss further, additional pre- and postgrowth techniques are employed. Prior to growth as mentioned above, the undoped QWI buffer layer is left in the delay line and AWGR region to push the Zn away from the waveguide. After growth, a proton implant is utilized to passivate some of the activated Zn atoms above the waveguide, thus reducing passive losses to a more manageable level of about 1.9 cm^{-1} for a surface ridge waveguide.

Three different ridge waveguide architectures are used in MOTOR (Fig. 5). A surface ridge that stops at the top of the waveguide layer is utilized for all active components and most passive regions of the wavelength converters. This design offers a simple fabrication approach through a combination of dry and selective wet etching. Although the selective nature of the wet etch provides precise control of the etch depth, its crystallographic nature leads to detrimental undercutting of waveguides with an angle greater than about 15° off $[\bar{1}\,10]$ toward the $[110]$ direction. The device also employs a high-contrast, deeply etched waveguide region for the compact differential delay line in the wavelength converter. This region is partially defined during the dry etch step of the surface ridge waveguide to eliminate misalignment between the two sections. It is then protected with a resist mask during the wet etch of the surface ridge. An SiO_2 liftoff process is subsequently used to open the delay line region and a second dry etch through the waveguide is performed. Last, a buried rib waveguide is created in the AWGR region by dry etching through the implant buffer layer and 70 nm of the upper waveguide prior to the cladding regrowth, which consequently buries the structure. Because no selective wet etch is used, this approach can provide waveguides in the AWGR region that can be bent a full 180° to achieve a more compact structure.

IV. Experimental Setup

The fabricated MOTOR chip (shown in Fig. 6) was soldered to a copper block for testing. Because this is not an ideal heat sinking configuration, the device was maintained at 16 °C during operation using a thermoelectric cooler (TEC) to reduce thermionic emission of carriers from the MQW region of the device. Wire bonding was not practical given the size of the device so all electrodes were directly probed. Light was coupled to and from the chip using lensed fiber. The response of the AWGR was characterized using on-chip sources (i.e., MZI SOAs and the SG-DBR) and coupling the output from each port to an optical spectrum analyzer (OSA). Wavelength conversion and routing functions of the MOTOR chip were tested under single-channel operation with pseudorandom bit sequence (PRBS) $2^{31} - 1$ RZ data at 40 Gb/s. The input data signal is generated with a modulated external cavity tunable laser source, amplified with an erbium-doped fiber amplifier (EDFA) and filtered with a 5-nm filter. Because the device employs compressively strained MQWs, it is TE-polarization sensitive and a polarization controller is used to rotate the input signal to a TE orientation. Although the AWGR provides on-chip filtering at most wavelengths, the fiber-coupled output signal from the device is also filtered with an external 5-nm filter for cases in which the wavelength of the original input signal might correspond to an allowed output wavelength of the AWGR. The output was then transmitted to a preamplified receiver. Bit error rate (BER) measurements were made using a 40-Gb/s SHF BERT. A schematic of the test setup is shown in Fig. 7. Back-to-back BER measurements were made using all test elements in this setup with the MOTOR chip removed.

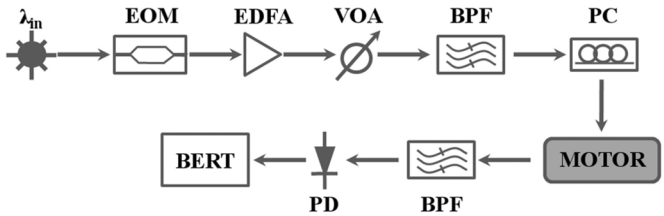

Fig. 7. Schematic of test setup. Key to abbreviations: EOM = electro-optic modulator; EDFA = erbium-doped fiber amplifier; VOA = variable optical attenuator; BPF = band-pass filter; PC = polarization controller; PD = photodiode; BERT = bit error rate tester.

V. Arrayed-Waveguide Grating Router Results

The performance of the AWGR was first characterized by forward biasing the MZI SOAs on a single-input wavelength converter to generate amplified spontaneous emission (ASE) and the spectral response from each egress port was measured. Fig. 8(a) shows a well-defined free spectral range (FSR) of approximately 11.1 nm from the AWGR and a single-channel crosstalk between −15.8 and −20.9 dB across all output ports (measured at the center wavelength of the ASE peak). Next, the pair of MZI SOAs in each input wavelength converter were

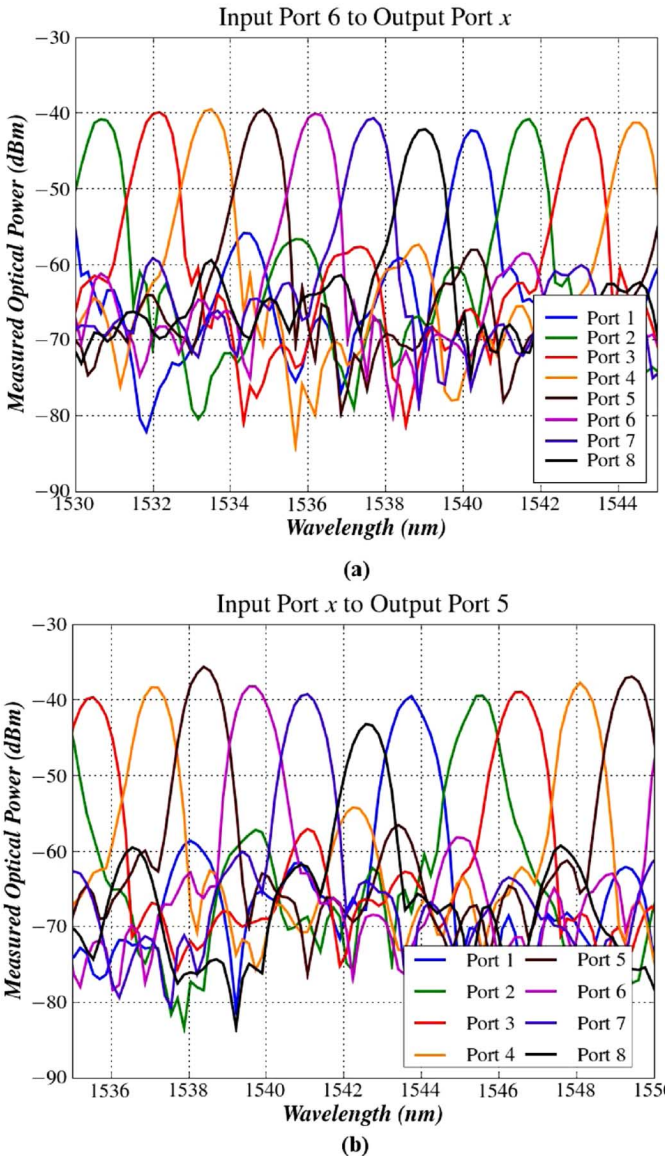

Fig. 8. Output ASE response of the integrated AWGR: (a) measured optical output from all output ports using input wavelength converter #3; (b) measured optical output from output port #2 using each input wavelength converter.

biased pair-by-pair at a constant bias level and the resulting spectra were measured from a single-output port [Fig. 8(b)]. Although some difference in power level is expected between center and outer ports of an AWGR, this figure illustrates that the performance of each input port varies, likely due to fabrication variations across the device. In general, all but one input port show crosstalk values in excess of −15.6 dB. Input port #8 only demonstrates a crosstalk of −12.3 dB, most likely due to a waveguide imperfection within this port. This will translate into a reduction in performance for port #8 relative to the other input wavelength converters.

To verify the performance of the device in terms of tunability, the SG-DBR was used in conjunction with the booster SOAs, which were forward biased to provide gain to the CW signal from the SG-DBR. Because the MZI SOAs are in the path between the SG-DBR and the AWGR, they were also biased in order to allow the signal to propagate without being absorbed.

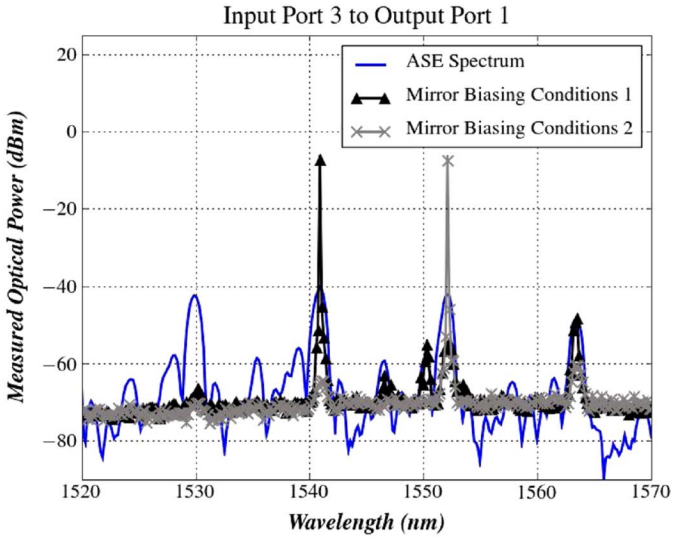

Fig. 9. Lasing spectra for different biasing conditions using the SG-DBR of input wavelength converter #3 superimposed on the ASE spectrum generated by forward biasing just the MZI SOA pair in that channel, all measured from output port #1.

By changing the biasing conditions on the front and back mirrors of the SG-DBR, the laser can be tuned to any of the allowed output wavelengths of a given port in order to achieve full channel switching. Fig. 9 shows the resulting spectra for two different mirror biasing conditions from a single-input wavelength converter to a single output. In this configuration, we measured output powers approaching −5 dBm.

Given the current architecture of our device, it is not possible to directly measure the insertion loss of the AWGR without cleaving it from the wavelength converter array. To make a reasonable estimate of the total throughput loss between the wavelength converters and the output, we measured the total power (including ASE) directly at the exit of the wavelength converter in an integrated power monitor diode with the SG-DBR, booster SOAs, and MZI SOAs forward biased at typical operating conditions. (We estimated the quantum efficiency of this power monitor by measuring the absorbed power in this pad when coupling a CW signal backward through the device from the exit of the AWGR into the wavelength converters and then comparing it to the power measured in the long MZI SOAs which should absorb all the incoming light.) The total power out of the AWGR was coupled into an output fiber and measured in an OSA. Assuming 4–5 dB of coupling loss to the fiber, the total power loss through the AWGR was estimated to be ∼8–10 dB. It is important to note that this loss also includes the loss associated with transitioning from the surface ridge waveguide of the wavelength converter to the buried rib waveguide of the AWGR, which could not be measured directly.

To improve overall device performance, the total loss in the AWGR region should be reduced. The higher than desired loss in our structure is likely due to two main factors. First, because the input and output lines and the arrayed waveguides are defined with the buried rib structure which etches into the waveguide layer, sidewall roughness created during the dry etch can result in high scattering losses. This would especially affect the input and output waveguides to and from the star couplers,

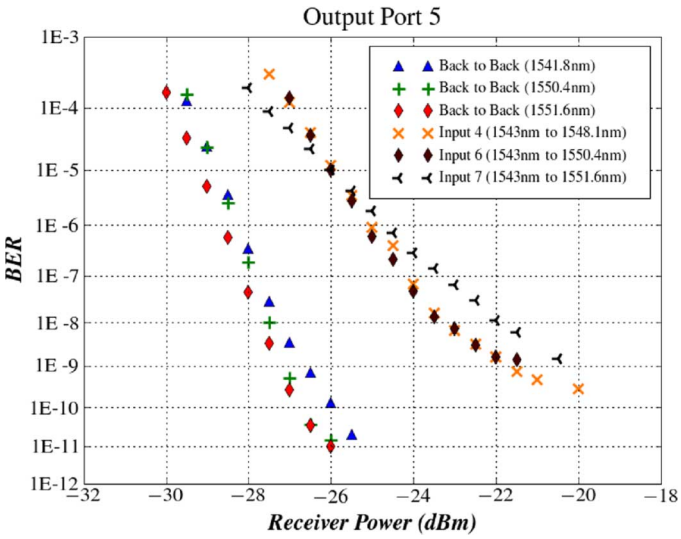

Fig. 10. BER measurements for several input wavelength converters at 40 Gb/s monitored from a constant output port. Back-to-back BER measurements are also included for the converted wavelengths.

which range in length from 6 to 10 mm. A future, more compact AWGR design similar to that of [27] could reduce these passive losses and increase the overall output power from the router. The design of [27] is also promising because it would eliminate the separate dry etch step currently used for the AWGR, thus reducing fabrication complexity. A second contribution to our AWGR loss is the coupling loss between the star couplers and the arrayed waveguide. Our lithographic capabilities should allow us to bring the waveguides separation down from their current value of 0.8 to about 0.5 μm in a future design to help reduce these coupling losses.

VI. Wavelength Converter and Routing Results and Discussion

Once the tuning characteristics of the SG-DBR are known, 40-Gb/s wavelength conversion and channel switching in the RZ data format can be achieved. Typical bias levels used for wavelength conversion are given in Table I. Figs. 10 and 11 show BER results and the associated eye diagrams for wavelength conversion from multiple-input channels through a constant output port, respectively. Eye diagrams are not shown for three of the eight wavelength converters. Although the diode yield was close to 100%, two channels did not function because of a random ridge defect in the MZI region. The other missing channel was damaged during testing. However, since the working channels have an identical structure, there are no inherent wavelength converter design issues and all channels are expected to work with an improved fabrication yield. Next, we measured the BER for wavelength conversion through different output ports using a constant input channel (Fig. 12). Open eye diagrams were also obtained for all eight output ports using a single-input channel (Fig. 13).

These results demonstrate the tunable routing ability of the MOTOR chip, as the input data to one input port can be directed to different output ports by simply changing the SG-DBR mirror biasing conditions. Figs. 10 and 12 also demonstrate that BERs

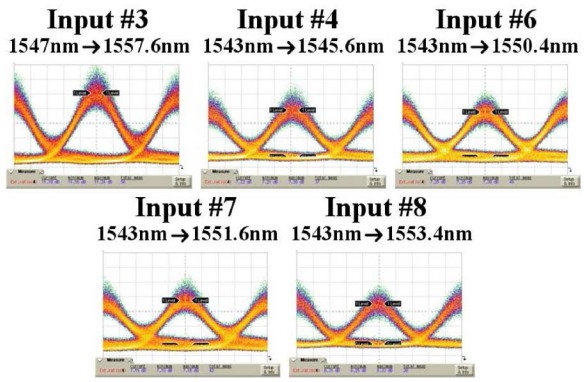

Fig. 11. Open eyes diagrams for several input wavelength converters at 40 Gb/s from a constant output port.

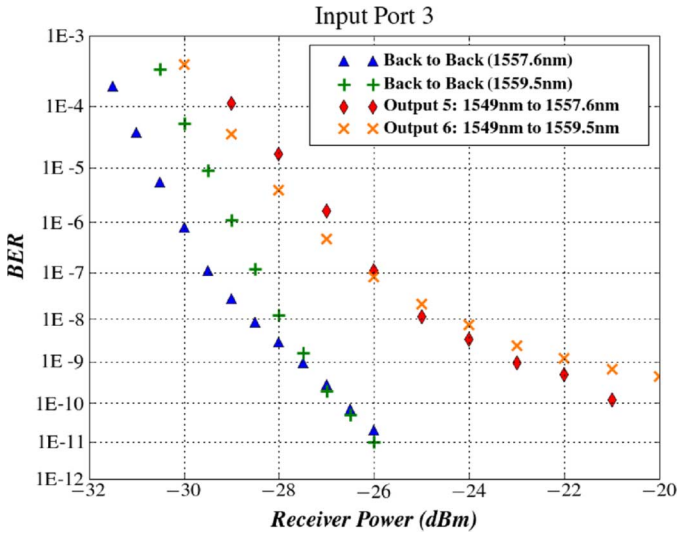

Fig. 12. BER measurements for a single-input wavelength converter at 40 Gb/s monitored from different output ports. Back-to-back BER measurements are also included for the converted wavelengths.

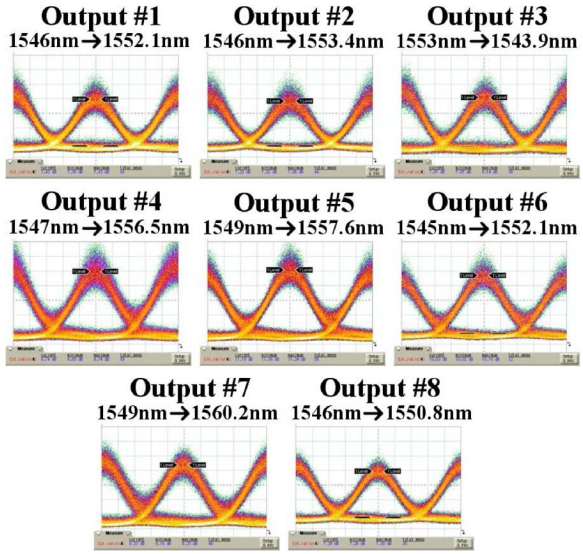

Fig. 13. Open eyes diagrams for a single-input wavelength converter at 40 Gb/s from all eight output ports.

below 1E-9 are possible for the combined wavelength conversion and routing process. The measured power penalties at this

TABLE I
WAVELENGTH CONVERTER TYPICAL BIASES

Component	*Bias (mA)*
Preamplifer SOAs	110-140
Booster SOAs	30-60
MZI SOAs	210-290
MZI Phase Modulator	0-5
SG-DBR Gain	100-110
SG-DBR Front Mirror	0-25
SG-DBR Back Mirror	0-25

BER range from approximately 4.5 to 7.0 dB (depending on the input port).

The noise floor and high-power penalty seen in these results are likely attributable to two main factors. First, the tested MOTOR chip was not antireflective (AR) coated. Additionally, given the high power of the SG-DBR, other minor reflections may exist in the device during operation. These reflections within the chip might occur at the transitions between the three different waveguide architectures. In future MOTOR designs, optimized AR coatings are planned to address this reflection issue.

Second, we measured a clear pattern dependence during wavelength conversion due to saturation in the preamplifier SOAs made from the centered MQW band edge. In order to provide enough gain to the input signal to deplete the MZI SOAs of carriers and modulate the MZI, the preamplifier SOAs had to operate in the nonlinear gain regime. This resulted in pattern distortion effects and an increased BER. In order to overcome these limitations, a more complex preamplifier structure will be required. One possible approach to increase the saturation power of the preamplifiers would involve combining the short centered MQW SOA in our device with a second MQW SOA section regrown some distance above the center of the waveguide as in [28]. This method has demonstrated SOAs with gains as high as 15 dB and output saturation powers of $>$19 dBm, but the additional regrowth could have a negative impact on device yield.

The results reported here apply only to single-channel operation. Moving to multiple-channel operation will not only require more elaborate biasing and fiber coupling schemes, but will also increase the expected power penalty for the combined process of wavelength conversion and switching. One key reason for this is expected to be the increased heating in the device with all diodes biased. This increased heating can lead to signal degradation and reduced output power due to thermal crosstalk effects in both the wavelength converters and the AWGR. Efficient heat sinking will therefore be vital to overall performance.

VII. POWER CONSUMPTION CONSIDERATIONS

The wavelength conversion and switching functions of the MOTOR chip come at a relatively low cost in terms of power consumption. Under normal operating conditions, the single-channel drive power is less than 2 W, giving an overall expected drive power of less than 16 W for eight-channel operation. However, additional power is necessary for TEC cooling. In our current testing configuration, the TEC requires $\sim$0.5 W to maintain a single channel at the 16 °C temperature used during testing. In a real application, the chip would be packaged with more efficient heat sinking (i.e., flip-chip bonding) with all channels operating simultaneously. The operating temperature would also likely be higher to match that of other system elements. Therefore, although the results reported here are promising, further work to characterize TEC demands under these conditions is needed before accurate comparisons with electronic router components can be drawn.

VIII. CONCLUSION

We report the demonstration of the first InP 8×8 MOTOR capable of 40-Gb/s operation per port with BERs below 1E-9. The device represents one of the most densely integrated InP chips ever reported, with more than 200 integrated functions and power penalty as low as 4.5 dB at 40 Gb/s. Under normal operating conditions, the per channel power consumption is less than 2 W. Improved power penalty is expected with future designs employing AR coatings and optimized preamplifier SOAs.

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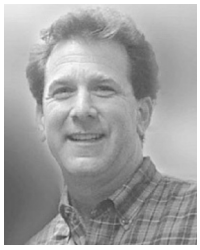

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