An 8x8 Monolithic Tunable Optical Router (MOTOR) Chip in InP

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Abstract: We demonstrate 10 Gbps error free operation through multiple ports of an InP monolithic tunable optical router consisting of eight input wavelength converters and an 8x8 passive arrayed-waveguide grating router.

1. Introduction

All-optical routing technologies are an attractive alternative to traditional electronic-based routing because of the potential to reduce power dissipation and the number of OEO interfaces [1]. Full on-chip switching functions can be realized by integrating wavelength converters and passive routers. This level of integration has the potential to reduce: (1) the overall device footprint; (2) discrete component-to-component coupling losses; and (3) packaging costs. Such benefits have been realized previously with the development of monolithically integrated all-optical wavelength converters [2,3].

We demonstrate the first reported 8x8 monolithic tunable optical router (MOTOR) in InP. Each MOTOR input port consists of a wavelength converter (WC) that is tunable across the C-band. The output of each wavelength converter is connected to the input of a passive 8x8 arrayed-waveguide grating router (AWGR) that performs channel switching to a certain output port based on the input wavelength. This switch requires the dense integration of more than 200 functional building blocks, including sampled-grating DBR (SG-DBR) lasers, multiple semiconductor optical amplifiers (SOAs), phase modulators, and an AWGR, representing one of the most complex InP photonic integrated circuits reported to date.

2. Device Design and Integration

As shown in Figure 1, the MOTOR chip consists of an array of eight widely-tunable WCs and an AWGR, resulting in an overall device footprint of 14.5 mm x 4.25 mm. Wavelength conversion is achieved through cross phase modulation effects in an SOA-based, differential Mach-Zehnder interferometer (MZI) [4]. 10 Gbps wavelength conversion in the NRZ format is accomplished by sending data into one branch of the MZI, with the input to the other branch turned off (i.e., the preamplifier SOA on this branch is not biased). The new wavelength of the converted data, which is set by the CW signal from an SG-DBR, determines the subsequent routing in the AWGR as explained in [5].

(a) (b)

Figure 1: (a) Schematic overview of MOTOR architecture; (b) Photograph of fabricated device (area in the center of the AWGR consists of test structures that are not involved in device operation).

To realize the MOTOR chip, a platform consisting of multiple quantum wells (MQW) centered in the device waveguide was selected. Because of the high overlap of the optical mode with the MQW region, high gain regions that are ideal for the SG-DBR laser and the MZI SOAs can be achieved. However, the increase in gain comes at the expense of saturation power. While this is ideal to increase the nonlinear response of the MZI SOAs, the reduced

saturation power is problematic for the input preamplifier SOAs, whose length and overall gain are thus limited. For active/passive definition, quantum well intermixing was used to shift the as-grown MQW bandedge from 1545nm to 1420nm in all passive sections as described in [6]. The wavelength converters employ a surface ridge architecture, where a combination of dry and selective wet etching was used to etch ridges down to the top of the waveguide. An integrated delay line at the WC input [4] was fabricated exclusively by dry etching. To minimize the loss in the AWGR region, a buried rib waveguide structure was utilized. The loss in this region was further reduced by leaving an undoped implantation buffer layer (used in intermixing, but typically removed immediately thereafter) above the etched rib to create a setback from the Zn doped cladding as described in [7]. The advantage of this method is that it reduces optical loss in the AWGR region without the need of a special UID regrowth to bury the rib and separate the optical mode from Zn dopant atoms. As a result, the MOTOR chip required only a single, low-risk, blanket, p-type cladding regrowth. Minimizing the number and complexity of regrowth steps is essential to increase component yield.

3. Device Results

The MOTOR chip was tested using PRBS 2^{31}-1 data streams at 10 Gbps. Only a single channel was tested at a given time. However, the single-channel crosstalk of the AWGR was measured to be 16 dB or greater (depending on the output port). The chip was soldered directly to a copper submount for efficient heat sinking. The submount was held at a temperature of 16°C for all experiments. The size of the chip prohibited sensible wire-bonding, so the metal pads were each directly probed.

Figure 2 shows wavelength converted eyes for six of the eight input ports. Although the individual SOAs worked on Inputs #1 and #5, these devices had a random material defect in the ridge near the MZI that prevented them from functioning as WCs. Figure 3 shows wavelength converted eyes out of every output port using a single input channel.

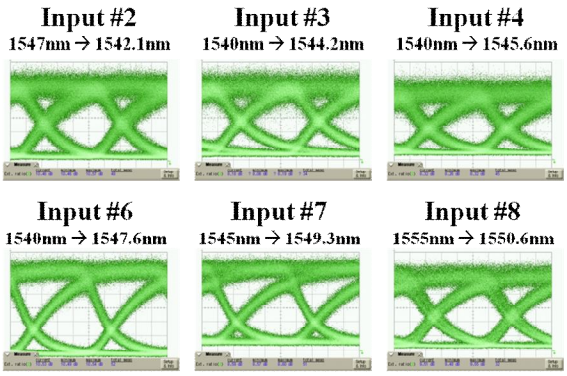

Figure 2: 10 Gbps eyes for the six working input channels measured out of output port #3.

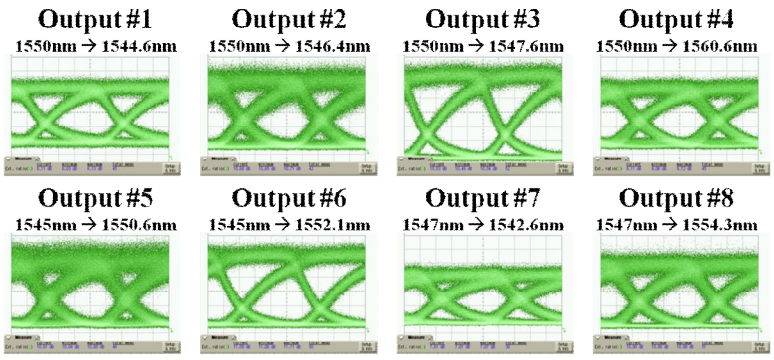

Figure 3: 10 Gbps eyes using input channel #6 measured out of every output port.

Finally, BER measurements were performed in order to determine the power penalty associated with 10 Gbps operation. Figure 4 shows BER curves for converted data along with back-to-back measurements for two of the six working input channels. The power penalty associated with the conversion at a BER of 10^{-9} ranges from 3.2 to 4.4 dB. One factor that contributes to this power penalty is the lack of antireflective (AR) coatings on the chip. Additionally, the preamplifiers have a low saturation power due to the centered MQW design, and this causes pattern dependence at longer pattern lengths. By employing an AR coating and an improved preamplifier design as in [8], this power penalty could be reduced.

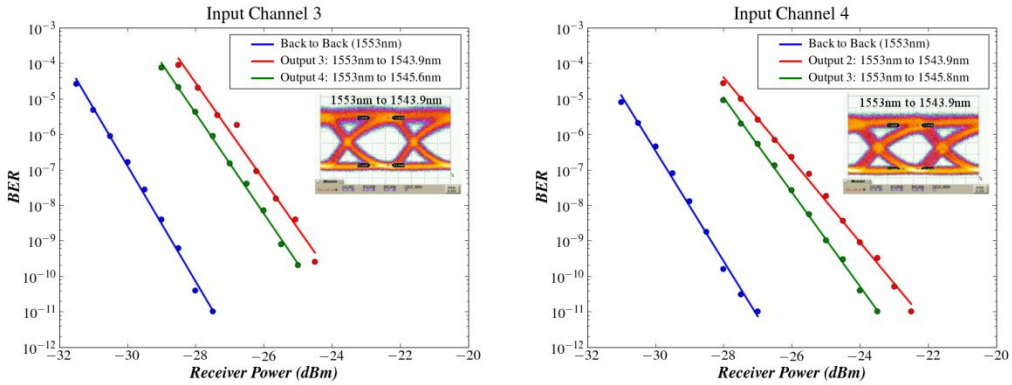

Figure 4: BER measurements for input channels 3 and 4. BERs are measured from two different output ports for each input port. Power penalties at a BER of 10^{-9} range from 3.2 to 4.4 dB.

4. Conclusions

Using a QWI platform with several ridge architectures, we have demonstrated a monolithic tunable optical router (MOTOR) in InP, consisting of eight input wavelength converters a passive AWGR. We have demonstrated error-free operation at 10 Gbps using six of the eight input channels and every output channel with a power penalty of 3.2 to 4.4 dB.

5. Acknowledgements

This work was supported by the DARPA MTO DOD-N Program under the LASOR Project (W911NF-04-9-0001). A portion of this work was done in the UCSB nanofabrication facility, part of the NSF funded NNIN network.

6. Reference

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