Large-Scale Photonic Integration for Advanced All-Optical Routing Functions

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Abstract: We review the first InP monolithic tunable optical router chip, consisting of eight wavelength converters and an 8x8 AWGR. The device integrates more than 200 functional elements and operates at 40 Gbps per port.

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1. Introduction

Large-scale photonic integrated circuits (LS-PICs) could have a transformative influence on future-generation optical networks [1]. In general, photonic integration promises improved performance and reliability over discrete component systems because it can lead to a reduction in device footprint and the elimination of many component-to-component fiber links. Recent advances in InP-based epitaxial growth and fabrication technologies have improved component yield, such that densely-integrated multi-channel devices can now be demonstrated in single-chip form. LS-PICs can process data completely in the optical domain, thus eliminating the need for successive optical-to-electrical and electrical-to-optical conversions, common in today's electronic routers. This translates into potential energy savings through reduced power consumption.

As part of the DARPA/MTO and Army DOD-N LASOR program [ref], we have previously demonstrated several important single-channel PIC devices [2]. Recently, we have extended our integration technologies to realize the first 8-channel monolithic tunable optical router (MOTOR) chip operating at 40 Gbps per port. This multi-channel LS-PIC integrates an array of 8 tunable wavelength converters (WC) with a passive 8x8 arrayed-waveguide grating router (AWGR) and functions as a wavelength-based switching element. The MOTOR chip has a very high level of integration with more than 200 functional elements on chip.

2. Device Design and Integration Strategy

The fabricated MOTOR chip is shown in Fig. 1a. Each input port (see Fig. 1b) consists of a wavelength converter (WC) that incorporates a widely-tunable sampled-grating DBR (SG-DBR) laser. The CW-output from the laser is

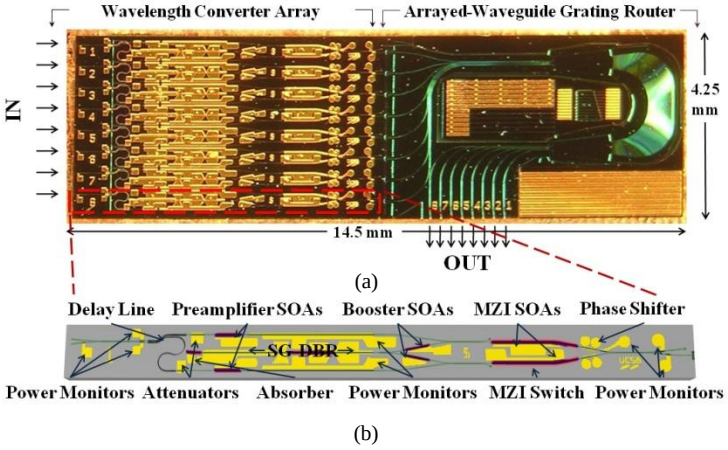


Figure 1. (a) Microscope image of fabricated MOTOR chip; (b) close-up schematic of the wavelength converter design.

modulated by an input data signal using cross-phase and cross-gain modulation effects in nonlinear semiconductor optical amplifiers (SOAs) within a Mach-Zehnder interferometer (MZI) [3]. In order to overcome the limits of carrier-recovery in these SOAs and achieve 40 Gbps operation, the input data signal in each port is split 50/50 and input into different branches of the MZI with a relative time delay. This delay is accomplished on chip through a compact, low-loss delay line. (The device can also operate at 10 Gbps line rates by bypassing the delay line and injecting the input data signal into only one branch of the MZI.) Additionally, the device incorporates two linear preamplifier SOAs before the MZI to amplify the input data signal. The original and converted data are both passed to one input of an 8x8 AWGR, which passively routes the converted signal to a desired output port based upon its new wavelength. The input and output frequency combs of the device are placed in different wavelength ranges so that a high- or low-pass filter can be placed at the output to remove the original input data signal.

To realize all of these components simultaneously, we developed an integration strategy that uses quantum-well intermixing and a single p-type cladding regrowth. The chip also has 3 waveguide architectures in different regions of the chip to optimize the optical properties of the various components. These include a surface ridge waveguide in the wavelength converter section, a high-contrast deeply etched waveguide in the delay line for compactness, and a buried rib waveguide in the AWGR region. More detail regarding this integration strategy is provided elsewhere [4]. The fabricated chip was then soldered to a copper mount and held at 16°C during operation.

3. AWGR Characterization

The performance of the AWGR was characterized using on-chip amplified spontaneous emission (ASE) generated by forward biasing the MZI SOAs of an input port and fiber coupling the output of all ports (one-by-one) to an optical spectrum analyzer (OSA) (Fig. 2a). A free spectral range (FSR) of approximately 11.1 nm and a single-channel crosstalk between -15.8 to -20.9 dB across all output ports were measured. Next, the MZI SOAs of each WC were biased and the resulting spectrum was measured from a single output port (Fig. 2b). With this measurement we see some variation in crosstalk performance between WCs, likely due to fabrication variations across the device. Lastly, Fig. 2c shows that the by changing the biasing conditions on the mirror diodes of the SG-DBR, the laser can be tuned to any of the allowed output wavelengths of a given port. A simple tuning map can made in order to achieve full channel switching from any input port to any output port.

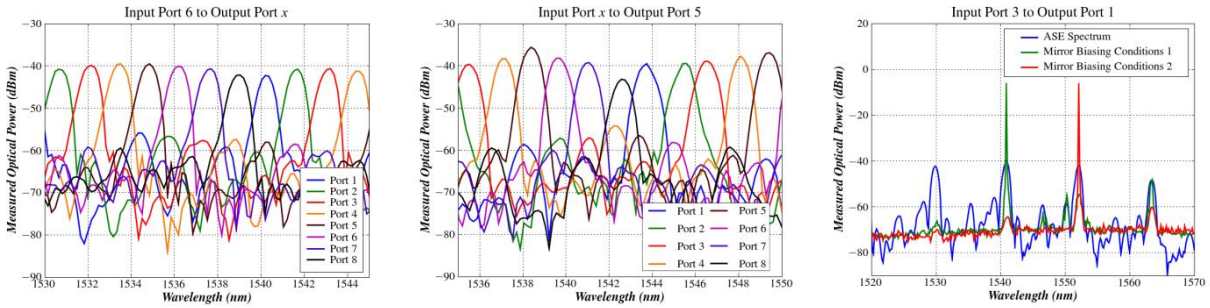


Figure 2: Output response of the AWGR: (a) measured response from input WC port #3 from each output port; (b) measured optical output from output port #5 from each input WC port; and (c) lasing spectra at different mirror biasing conditions with the SG-DBR of input WC port #3. The ASE spectrum for that channel is superimposed.

4. Wavelength Conversion and Routing Demonstration

Single-channel wavelength conversion and routing were tested under various conditions. In each case, a PRBS data was generated off-chip and amplified with an erbium doped fiber amplifier (EDFA). It was then transmitted through an optical attenuator to control the input power level, a 5-nm filter, and a polarizer to align the polarization state to TE before the signal was coupled into the chip. The fiber-coupled output was also filtered with a 5-nm passband (to ensure the original input signal was removed) and was transmitted to a preamplified receiver. Bit-error-rates (BER) were then determined using a SHF BERT.

First, 10 Gbps operation of the device was examined by inputting a PRBS 2^{31}-1 NRZ signal into only one branch of the MZI (Fig. 3) [5]. At a BER of 10^{-9} a power penalty as low as 1.3 dB was measured. Eye diagrams of the converted signal show open eyes with extinctions up to 8.79 dB. There is some distortion in the eye that can most likely be attributed to saturation in the input preamplifier SOA.

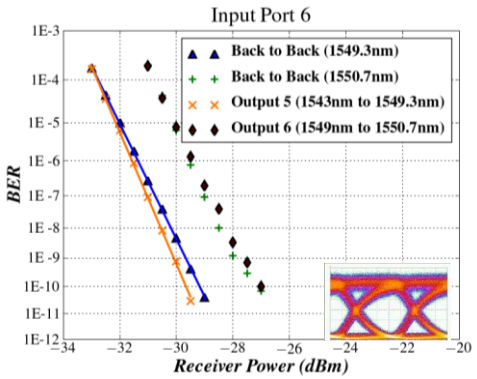
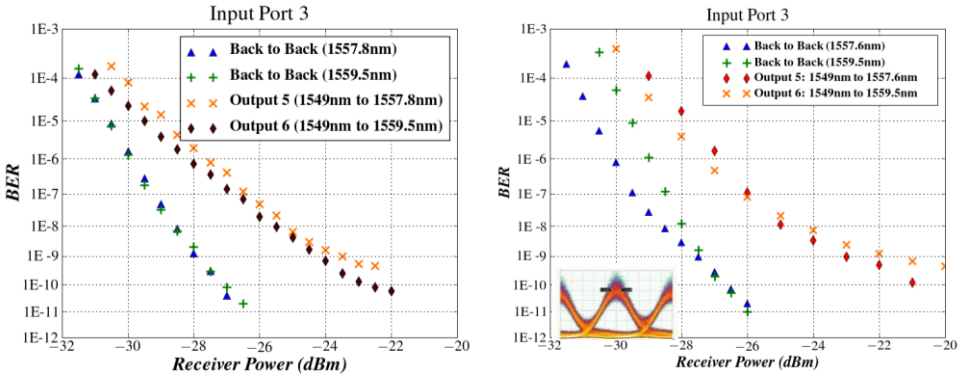


Figure 3. 10 Gbps BER measurements from multiple output ports using input WC #6.

Next, the device was tested using the differential delay approach with 40 Gbps PRBS 2^7-1 RZ data [6]. Fig. 4a shows the BER for a single input channel while monitoring a constant output port. In this configuration, power penalties as low as 3.5 dB at a BER of 10^{-9} were measured. When the pattern length was increased to 2^{31}-1 bits, there was a noticeable increase in power penalty (to 4.5 to 7 dB depending on the input/output port combination). We also saw the emergence of a noise floor at low BERs. Subsequent investigation revealed that in order to achieve sufficient input signal power to deplete the carriers in the MZI SOAs and modulate the SG-DBR signal, the preamplifier SOAs had to be operated beyond the 1-dB output saturation point. This is likely the main factor leading to the pattern length dependent power penalty. Additionally, however, it is noted that the facets of the device were not AR coated, so internal reflections could be contributing to the degradation in performance.



(a) (b)

Figure 4. 40 Gbps BER measurements for input port #3 with (a) 2^7-1 PRBS and (b) 2^{31}-1 PRBS input data signals.

5. Acknowledgements

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6. References

[1] R. Nagarajan *et al.*, "Large-scale photonic integrated circuits for long-haul transmission and switching," *J. Opt. Netw.*, vol. 6, pp. 102-111, Feb. 2007.

[2] M. L. Mašanović *et al.*, "Advanced photonic integrated technologies for optical routing and switching," presented at SPIE Photonics West Conference, Proc. SPIE 7219, 72190I, Jan. 2009 (*invited)*.

[3] V. Lal *et al.*, "Monolithic Wavelength Converters for High-Speed Packet-Switched Optical Networks," *IEEE J. Sel. Topics Quantum Electron.*,vol. 13, pp. 47-57, Jan./Feb. 2007.

[4] S. C. Nicholes , M. L. Mašanović, B. Jevremović, E. Lively, L. A. Coldren, and D. J. Blumenthal, "An 8x8 InP Monolithic Tunable Optical Router (MOTOR) Packet Forwarding Chip," *J. of Lightwave Tech.*, vol. 28, pp. 641-650, Feb 2010.

[5] S. C. Nicholes, M. L. Mašanović, E. Lively, L. A. Coldren, and D. J. Blumenthal, "An 8x8 Monolithic Tunable Optical Router (MOTOR) Chip in InP," presented at IPNRA Conference, paper no. IMB1, July 2009.

[6] S. C. Nicholes, M. L. Mašanović, B. Jevremović, E. Lively, L. A. Coldren, and D. J. Blumenthal, "The World's First InP 8x8 Monolithic Tunable Optical Router (MOTOR) Operating at 40 Gbps Line Rate per Port," presented at postdeadline session of OFC Conference, paper no. PDPB1, Mar. 2009.