## **On-Chip VCSEL Interconnects Enabled by 3-D Interposer-Based Integration and Polarization Modulation**

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Invited Paper

**Abstract:** Optical interconnects are required for a continued scaling of a version of Moore's Law. VCSELs remain the most efficient sources to integrate, and these can be compatibly integrated with emerging 3-D integration technology using active interposers. Polarization-modulation can double the bisection bandwidth available together with coarse WDM and other modulation techniques.

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## 1. Introduction

Within the past decade there has been a tremendous amount of progress on Si-photonics as well as Sisystem-in-a-package technology[1,2]. Perhaps we now see some convergence between these two. Not too long ago, a main selling point for Si-photonics was being able to put all of the photonics and electronics on a single chip. Today, the emergence of 2.5-D as well as 3-D integration—the concept of placing numerous chiplets on a common interposer as shown in Fig.1—is beginning to change this perspective[1-3]. In fact, even before this, the simple issue of incompatibility of the photonics with the electronics, either in size, in manufacture, in performance, or in operation, has led to a similar desire to have separate chips, stacked on top of or beside of each other, very closely together. This change in perspective has also re-opened the issue of having different materials platforms for the different chiplets.



Figure 1: Schematic view of the interposer concept. [1]

In this paper, we will review the performance of state-of-the-art laser sources as candidates for integration with interposers and conclude that VCSELs are still the leading practical choice. We specifically will not consider schemes for coupling light from external sources, or sources that do not emit sufficient well-directed powers. VCSELs can operate over temperature ranges exceeding 60 °C and maximum temperatures over 120 °C with useful output powers. Over such temperature ranges, ~ 30 course WDM channels are

possible with data rates ~40 Gb/s using simple direct modulation of the laser drive currents with some of the lowest total power dissipations, including the bias and modulation drive powers. For such WDM over this temperature range, multiple VCSEL chiplets would be involved with wavelengths extending from 850nm to the 1060nm range. This enables relatively simple muxing and demuxing at both ends of the optical links.

Secondly, we will discuss in more detail our more recent results with polarization modulation [4]. Prior work has demonstrated [5-7] that it is possible to control the polarization by means of asymmetric current injection (ACI) in the active region of the VCSEL. Since this technique relies on current induced anisotropies in the VCSEL, the polarization can be controlled at ultrahigh speeds. Most prior work obtained with ACI has been limited ~50kHz [8] due to the dominant thermal polarization switching. However, in our recent report electrically controlled polarization modulation speeds of over 4Gb/s were shown, and those VCSELs had ultralow threshold currents (~150-300 $\mu$ A) as well as very good differential quantum efficiencies. This is still the fastest reported direct modulation of the polarization of

a VCSEL. With this technique we now demonstrate that the data rate obtained with other modulation techniques can be doubled by modulating different data on each polarization and simple polarization filtering at the receiver.

## 2. Polarization VCSEL Results

The VCSELs used for polarization-modulation experiment consisted of MBE grown, strained InGaAs/GaAs quantum well devices, optimized for lasing at 980nm, with a bottom emitting architecture. A dual intracavity structure is used to maximize the effect of asymmetric current injection. A schematic of the device architecture is shown in Fig. 2. Two sets of P and N contacts are fabricated, such that the current P1N1 flows perpendicular to P2N2, to maximize the current asymmetry. Orientation of these contacts are along <110> and  $<1\overline{10}>$  crystalline planes, to maximize the anisotropy.



Fig. 2: (a) Biasing scheme for the two contacts of a VCSEL: P1N1 is modulated with Data 1, and P2N2 is modulated with Data 2, (b) Optical response at the output of the VCSEL: X polarization only (top) and the difference between Y and X polarization (bottom)

The LI curve on a typical chip had a threshold current of 0.3 mA and an output power of 0.6 mW at 2 mA with 4 spontaneous flips in polarization in between—the polarization was opposite for application of the current to the opposite set of terminals. The polarization contrast ratios exceeded 14dB by changing the directionality of the current flow. The experimental setup to exploit this to modulate the polarization of the VCSEL is shown in Fig. 2(a). Both P contacts of this multimode VCSEL are biased at a common DC current via bias-T. One set of data is applied across P1-N, while a second data-stream is applied to P2-N. The output of the VCSEL is passed through a polarizer, focused on to a multimode fiber and detected with a high speed detector. Fig. 2(b) shows the polarization resolved time domain response obtained on an oscilloscope. For this particular case, the signal on P1-N1 (data 1) modulates both X and Y polarizations, while the signal on P2-N2 (data 2) modulates only the X polarization. Therefore, by simply subtracting the output of X-polarization ( $P_x$ ) from that of Y-polarization ( $P_y$ ), the two data-streams are completely recovered. Thus, we demonstrate for the first time, that a VCSEL can support simultaneous, independent modulation on two different linear polarized modes—effectively doubling the maximum possible data-rate from the VCSEL. It is expected that the polarization switching speed can be further improved with this technique, by reducing the parasitic capacitance.

## References

- [1] S. Cheramy, et al, Chip Scale Review, 18 (3) May/June, 2014.
- [2] M. Heck , et al, IEEE JSTQE, 19 ( 4) 6100117, July/August 2013.
- [3] <u>www.luxtera.com</u>
- [4] A. Barve, A. Mehta, A. Husain, L. Coldren, Optical Interconnects Conf., TuC5, Coronado Bay, CA, May, 2014.
- [5] L. M. Augustin, et al, *IEEE Photon. Technol. Lett.*, **16** (3), 708 (2004)
- [6] Y. Zheng et al, IEEE Photon. Technol. Lett., 23 (5), 305 (2011)
- [7] Y. Sato et al, IEEE Photon. Technol. Lett., 20 (17), 1446 (2008)
- [8] M.P. Tan et al, IEEE Photon. Technol. Lett., 24 (9), 745 (2012)