Phase-Locked Coherent Optical Interconnects for Data Links

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In large-scale digital systems, propagation delay and power consumption of the interconnects are vastly larger than that of the transistors themselves [1,2]. Reduced power consumption, and increased capacity is required for interconnects, whether on-chip, between circuit boards, or within large data centers. Here we will consider coherent optical interconnects for high-capacity, sub-km links within data centers. At the other extreme of interconnect length, we will also briefly consider alternative approaches for reduced $CV^2/2$ switching energy of VLSI interconnects.

Within data centers, optical links can readily provide >> 100 Gb/s capacity using wavelength-division and polarization multiplexing. Coherent links [3] offer more complex constellations, increased spectral efficiency, and greater capacity. Most long-haul coherent links [3] use free-running local oscillator (LO) lasers; the receiver uses digital signal processing (DSP) to both equalize dispersion and correct LO phase fluctuations. In few-km links, dispersion need not be compensated; if the LO laser is then phase-locked to the received signal, DSP can then be eliminated to greatly reduce receiver cost and DC power.

In phase-locked [4,5] coherent receivers, the LO laser phase is locked to the received signal. In optical PLLs (OPLLs) [6,7,8], wide ~1GHz loop bandwidths are necessary to suppress the LO laser's phase noise, and, as noted by Coldren [6,7,8] photonic integration (PIC) is required to provide the needed small component propagation delays. Because the signal and LO lasers may be initially offset by 5-50GHz, broadband (DC~50GHz) phase-frequency [9] difference detectors force the loop to lock. By these techniques we have demonstrated 35Gb/s coherent phase-locked BPSK receivers [6] (fig. 1a).

Used in WDM transmitters, OPLLs can further improve spectral efficiency. Using broadband digital *SSB* mixing [9], the OPLL forces a frequency offset of controlled sign between the reference and slave lasers, generating optical frequency offsets, and WDM channel separations, at the ~1 ppm. precision of a microwave synthesizer (fig. 1b). This is *optical frequency synthesis*. Cascading such offset OPLLs, precise WDM combs can be generated.

In coherent receivers, WDM signals can be demultiplexed electrically [10] (fig. 2), replacing many WDM receivers with one PIC and one electrical IC. WDM signals at 25GHz separation become electrical subcarriers at 25GHz separation, and are downconverted to DC. There are large potential power-savings; initial demonstrations [10] used several-Watt ICs, but power can be saved using CMOS time-domain mixers [11] and charge-steering logic [12]. Today's ICs support 600 GHz bandwidths [13], hence one such electrical IC might recover 48 WDM channels at 25 GHz channel spacing.

On-chip interconnect $CV_{DD}^2/2$ dissipation is a central barrier to improved digital systems [1,2]. Though tunnel FETs offer reduced V_{DD} , projected I_{on} is small [14], hence logic will be slow. Alternatives to the widely-studied tunnel FET thus warrant greater consideration. By operating finFETs near threshold (fig. 3) for low V_{DD} and then increasing the fin height-spacing ratio [15,16] to offset the loss in on-current arising from the low V_{DD}, low $CV_{DD}^2/2$ dissipation, and moderately high drive current per unit IC area, hence low gate delay, can be obtained simultaneously. At the expense of two supplies and three PMOS thresholds, $CV_{DD}^2/2$ dissipation can also be reduced using circuit techniques with low-static-dissipation interconnect buffers with voltage gain (fig. 4). Here long interconnects are driven by gates with a low V_{DD}, producing a 200 mV swing. The interconnect receivers must have shifted V_{th} to maintain low I_{off} , hence have low I_{on}. Buffer gate delay is minimized by using only short interconnects (<1 μm) between the line receivers and normal 500-mV-V_{DD} logic stages.

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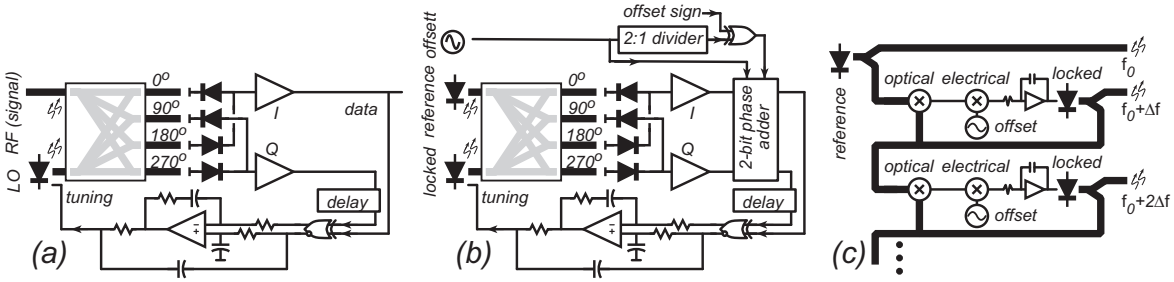

Figure 1: Phase-locked optical components: coherent BPSK optical receiver (a), optical frequency synthesizer (b), and precision generation, by optical frequency synthesis, of wavelength channel spacings within WDM (c).

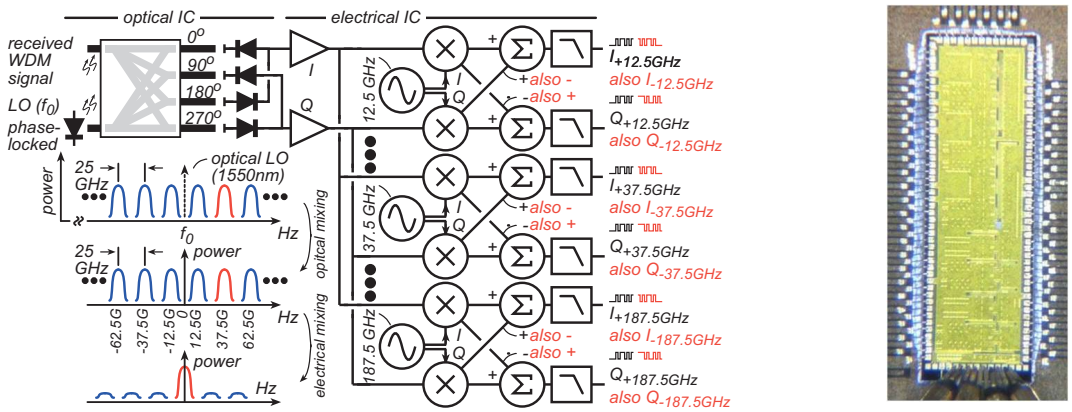

Figure 2: Receiver for demodulation of optical wavelength-division-multiplexing demodulation in the electrical domain; block diagram (left) and die photograph of prototype six-channel receiver (right).

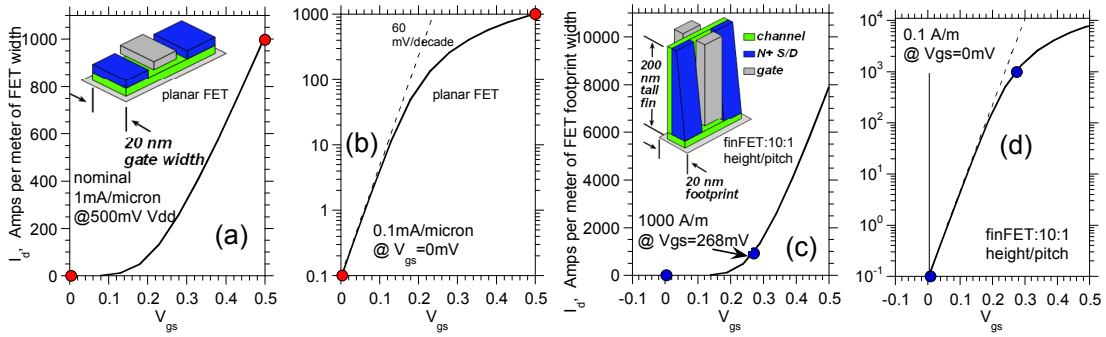

Figure 3: Simulated (a,b) characteristics of a planar ballistic FET with I_{on}=1000A/m and I_{off}=0.1A/m for a 500 mV supply. With a 10:1 height/pitch ratio, the same on- and off-current per unit *footprint width* (c,d) can obtained with a 268 mV supply

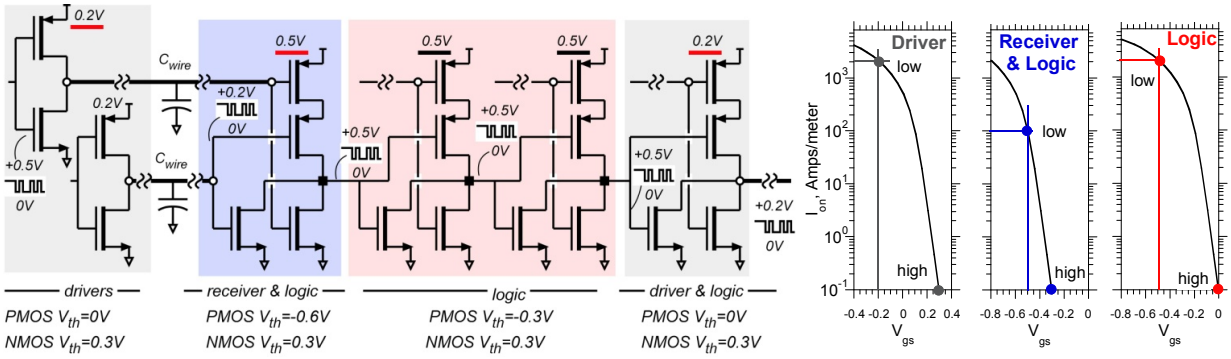

Figure 4: Voltage-gain buffering for reduced interconnect $CV^2/2$ dissipation. Long interconnects are driven by gates with a low V_{DD}, producing a 200 mV swing. Interconnect receivers have shifted V_{th} to maintain low I_{off}, hence have low I_{on}. Gate delay is minimized by using only short interconnects between the line receivers and 500-mV-V_{DD} logic stages.