Highly Integrated Homodyne Receiver for Short-reach Coherent Communication

Mingzhi Lu¹, Hyun-Chul Park¹, Eli Bloch², Leif A. Johansson¹, Mark J. Rodwell¹, and Larry A. Coldren^{1,3}

¹Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA, 93106, USA. (Currently with Infinera Corp., Sunnyvale, CA) ²Department of Electrical Engineering, Technion – Israel Institute of Technology, Haifa 32000, Israel. ³Department of Materials, University of California, Santa Barbara, CA, 93106, USA.

lumz85@gmail.com

(Invited)

Abstract: A highly integrated homodyne receiver has been demonstrated within a footprint of 1 cm². The receiver successfully receives 40 Gbit/s BPSK and error free is achieved up to 35 Gbit/s. Theoretical analysis has been also carried out showing the feasibility of integrated 16 QAM homodyne coherent receivers.

OCIS codes: (250.5300) Photonic integrated circuits; (060.2840) Heterodyne; Optical phase-locked loop; optical frequency synthesis

1. Introduction

Recently, a resurgence of effort is being devoted to the research of coherent optic fiber communications, because its advantages of higher sensitivity, better noise tolerance, and more importantly, its compatibility with complex modulation format, such as QPSK, 16 QAM. Based on advanced digital signal processor (DSP) technology, DP QPSK coherent links have been deployed widely, and 16 QAM links also start to be applied to metro or even long haul applications. Modern DSP-based intradyne receivers solve most of the problems in coherent communication systems, but it also gives rise to a very high power consumption (roughly 1 W/Gbps or higher) and high cost, both of which limit its application within long-haul or long-distance metro links. In order to solve the high-cost and high power consumption problems that intradyne receiver inherently have, optical phase-locked loop (OPLL) based homodyne receivers become an alternative [1].

Although research in 1980s and 1990s indicates the difficulties of the implementation of OPLL-based homodyne receiver, especially its stringent limit on linewidth and physical loop delay [3], photonic and electronic integration technology have solved this problem to a great extent [1,2]. By integrating all the optical components on the same chip and combing with the ASIC, the system size decreases dramatically and the physical loop delay reach the order of sub-ns [1,2,4]. Therefore the stringent limit on laser linewidth It not only makes homodyne receiver practically feasible, but also make it excel intradyne receiver in many aspects, including power consumption, size, and baud rate.

2. Experimental demonstrations

In this work, a highly integrated Costas loop is proposed and demonstrated. By photonic and electronic integration, the whole receiver is realized within a footprint of 10 mm \times 10 mm area, and 120 ps loop delay is achieved. The architecture of the Costas loop is shown in Fig. 1. The receiver consists of three main parts: a photonic integrated circuit (PIC), and an electronic integrated circuit (EIC) and a hybrid loop filter (Fig. 1) [1].

The incoming signal and the LO are mixed in the optical 90 degree hybrid, and I/Q signals are then generated on four photodetectors. The I/Q signals are then mixed at the XOR gate on the EIC, and therefore the data-OPLL cross-talk is eliminated by the phase doubling. The XOR gate together with the delay line works as a quadric-correlator frequency detector, and the XOR itself also acts as a phase detector. The phase/frequency error signals are then fed back to the laser phase tuning section through the loop filter, as shown in Fig. 1.



Fig. 1. Homodyne receiver architecture.

Fig. 2. Measured BER of the homodyne receiver.

On the PIC, a widely tunable sampled-grating DBR (SG-DBR) laser, a directional-coupler-based 90 degree hybrid, four uni-travelling-carrier (UTC) photodetectors and microstrip transmission lines are integrated monolithically [5].

The PIC, EIC, and loop filter are connected together using wirebonds. A BPSK transmitter is built using commercial components for the testing purpose. 2^{31} -1 PRBS data is applied to the transmitting laser using the NRZ BPSK format. A VOA and an EDFA are used to control the OSNR of the received signal. The BPSK signal is coupled into the PIC through a lensed fiber, and the power of the SG-DBR laser is coupled out through another lensed fiber, and beat with the transmitting laser on a high-speed photodetector for the monitoring purpose. Bit error rates (BERs) are also measured [1].

We successfully locked the optical phase of the SG-DBR laser to the phase of the transmitting laser. The beating spectrum measured by the ESA showed 1.1 GHz closed-loop bandwidth. BER is also measured with various OSNR of the input signal. Error free (BER $< 10^{-12}$) is achieved with a data rate up to 35 Gbit/s. Both measured BER and the theoretical BER are plotted in Fig. 4. The power consumption of the system is around 3 Watt, not including the TEC cooling. [1]

3. Theoretical analysis for 16 QAM receiver [6]



Fig. 3. Noise analysis model for PLL.

In the previous experiment, the LO laser linewidth has a seemingly large spectral linewidth of >10 MHz. However, no linewidth-related performance degradation is observed. It is because that the noise suppression bandwidth the homodyne receiver, the closed loop bandwidth, is large enough to suppress most of the phase noise from the local oscillator [1,3].

An OPLL model is shown in Fig. 3, where noise are introduced from two locations, ϕ_{N_0} from the input of the phase detector, and ϕ_{PN} from the output of the CCO. The summed effects of ASE noise, shot noise, the thermal noise and RIN are represented by ϕ_{N_0} , and the laser phase noise is ϕ_{PN} . The system performance can be expressed in the following equation.

$$\left(\phi_{N_0}+\phi_{in}-\phi_{out}\right)\cdot K_{pd}\cdot F_{LF}(s)\cdot \frac{\kappa_{CO}(s)}{s}+\phi_{PN}=\phi_{out},$$

where $K_{pd} \cdot F_{LF}(s) \cdot \frac{K_{CO}(s)}{s}$ indicates the open loop response of the homodyne receiver. Within the loop bandwidth, the LO phase noise is suppressed by the closed-loop response function, while on the other hand ASE noise, thermal noise, laser RIN and shot noise are passed through within the loop bandwidth. As for laser phase noise modeling,

both ASE noise and 1/f carrier-injection noise are considered. Parameters used in this calculation are listed in Table 1.

Using the parameters listed in Table 1, the phase noise spectrum of the OPLL can be obtained and therefore the laser residue phase error variance can be obtained. Based on the residue phase noise and the other white noises, the Q-factor of receiver can be obtained. The detailed derivation can be found in [6]. By utilizing this receiver as a 16 QAM receiver, the BER is calculated (Fig. 4). As we can see, with a 1 GHz loop natural bandwidth, the receiver can work in an error-free (BER<1e-12) condition with no digital signal processing. When the loop bandwidth is 2-3 GHz, the receiver performance is optimized. When the assumed loop bandwidth reaches 10 GHz, the low SNR performance is degraded due to the high ASE noise level. It is worth mentioning that the calculation is based on the summed laser linewidth of 3 MHz, which is higher than most of the published 16 QAM receiver work.

Parameter	Value
Summed laser linewidth $(\Delta \nu)$	3 MHz
Reference laser power on each photodetector (P_{sig})	1.25 mW
LO laser power on each photodetector (P_{LO})	1.25 mW
Photodetector responsitivity (\Re)	0.8 A/W
Photodetector load resistor (R)	50Ω
Photodetector bandwidth (Δf)	25 GHz
Data symbol rate $(R_s = \Delta f)$	25 Gbaud/s
Imperfect power balance of the balanced photodetector (η)	95 %
LO laser RIN (RIN)	-140 dBc/Hz
OPLL loop type and order	Second order type II
OPLL damping factor (ζ)	0.7
TIA noise figure (F)	20 dB
Reference bandwidth for OSNR (B_{ref})	0.1 nm



Table 1. Parameters used in calculation.

Fig. 4. Calculated BER of the 16 QAM receiver with various loop bandwidth.

4. Conclusion

A 40GB/s OPLL-based homodyne receiver has been demonstrated with very low power consumption and good overall performance. Utilizing the same OPLL model, the feasibility of a 16 QAM receiver is theoretically proved, and with a 1 GHz loop bandwidth error-free reception can be achieved with a 3 MHz linewidth laser as local oscillator. It provides a good solution for relatively short distance, cost effective, efficient coherent communication.

Acknowledgement

This work is mainly supported by DARPA PICO project. A portion of this work was done in the UCSB nanofabrication facility, part of the National Science Foundation (NSF) funded NNIN network. The EIC is fabricated at Teledyne Scientific and Imaging Company.

Reference:

- Mingzhi Lu, Hyun-chul Park, Eli Bloch, Abirami Sivananthan, John S. Parker, Zach Griffith, Leif A. Johansson, Mark, J. W. Rodwell, and Larry A. Coldren, "An Integrated 40 Gbit/s Optical Costas Receiver," Journal of Lightwave Technology, Vol. 31, Iss. 13, pp. 2244–2253 (2013).
- [2] M. Lu, H. Park, E. Bloch, A. Sivananthan, A. Bhardwaj, Z. Griffith, L. A. Johansson, M.J. Rodwell, and L.A. Coldren, "Highly integrated optical heterodyne phase-locked loop with phase/frequency detection," Opt. Express 20, 9736-9741 (2012).
- [3] L. Kazovsky, "Decision-driven phase-locked loop for optical homodyne receivers: Performance analysis and laser linewidth requirements," Lightwave Technology, Journal of, vol. 3, no. 6, pp. 1238-1247 (1985).
- [4] S. Ristic, A. Bhardwaj, M. Rodwell, L. Coldren, and L. Johansson, "An optical phase-locked loop photonic integrated circuit," Lightwave Technology, Journal of, vol. 28, no. 4, pp. 526-538 (2010).
- [5] M. Lu, H. Park, E. Bloch, A. Sivananthan, J. S. Parker, L. A. Johansson, M. J. W. Rodwell, and L. A. Coldren, "Monolithic Integration of a High-speed Widely-tunable Optical Coherent Receiver," Photonics Technology Letters, Vol. 25, No. 11 (2013).
- [6] M. Lu, "Integrated Optical Phase-locked Loops", Ph.D. dissertatioin, University of California, Santa Barbara (2013).