Integrated Optical Phase-Locked Loop

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Abstract: We demonstrate the first integrated optical phase-lock loop (OPLL) photonic IC, containing two SG-DBR lasers with >5 THz tuning range, a balanced detector pair and output modulators. A proof-of-concept homodyne OPLL demonstration has been performed.

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1. Introduction

Optical phase-locked loops (OPLLs) are routinely constructed using low-linewidth solid state or external cavity lasers. They are more challenging to build using wide linewidth semiconductor lasers due to the required short feedback delay. Past semiconductor laser OPLL demonstrations have typically used miniature bulk optics to meet these latency requirements [1,2]. In this paper, we demonstrate for the first time, an integrated optical phase-lock loop photonic integrated circuit in which all required optical components are integrated, including lasers, waveguides, couplers and photodetectors, as well as optical modulators. This eliminates the latency and instability from free-space or fiber optical paths to allow a very fast and robust OPLL.

Moreover, the OPLL photonic IC is built using widely-tunable lasers with over 5 THz wavelength range. This is key to several applications. First, it allows the development of homodyne coherent receivers in the form of Costa's loop, without the requirement for complex, power hungry DSP electronics to manage laser phase noise. The relative simplicity of the Costa's loop will also allow scaling to high data rates, >100Gbps. Second, an OPLL with 5 THz wavelength tuning range will allow coherent beam forming for sub-mm resolution LIDAR applications. Third, together with a THz photodetector, it will allow optical heterodyne signal generation with a DC to 5 THz frequency range with maintained coherence. Applying optical phase or amplitude modulation to one optical line will now generate a coherent phase or amplitude modulated THz signal. This is the target application for this paper. The photonic integrated circuit is described in section 2 and a proof-of-concept homodyne OPLL demonstration is described in section 3.

2. Optical Phase Lock Loop Photonic Integrated Circuit

A diagram of the PIC is shown in Fig. 1, and the corresponding SEM image is shown in Fig. 2, left. The PIC epitaxial structure has been grown on an S-doped InP substrate by MOCVD. The integration platform used here is often referred to as "Offset Quantum Well Platform" and has been described in more detail in [3] and references therein. In this platform, the light is guided by a 300 nm 1.4Q surface-ridge-waveguide core layer, which forms a basis for "passive" components: waveguides, Multimode Interference Splitters/Couples (MMIs), and Franz-Keldysh modulators. Above this layer, the epitaxial material structure contains a 119-nm Multiple-Quantum-Well Region (MQW) region that forms a basis for "active" components: gain sections in SGDBR lasers, SOAs, as well as photodetectors. The "active" MQW region is defined by wet etching, as the very first processing step, followed by grating patterning/etching, waveguide p-cladding re-growth, and the rest of the steps, main of which are: surface-ridge wet etching, top N-contact wet etching and deposition, BCB patterning for modulators and detectors, P-metal pads, P-metal via etching, P-metal deposition, wafer thinning, and back-side N-metal deposition.

Light from each of the two SGDBR lasers is first divided by a 90-µm-long 1 X 2 MMI splitter into two equal-power components, and all four components are amplified by four 400-µm-long SOAs. One of these two components from either laser is used for the feedback loop, and the other is used for the PIC output. The half-power component from either laser that is used in the feedback loop first enters a 340-µm-long 2 X 2 MMI coupler (with tuning pads), which is, in turn, followed by a balanced receiver, containing two 250-µm-long phase modulators. These phase modulators are followed by a pair of 50-µm-long active photodetectors that can be used as a balanced receiver. The residual light that is not absorbed in the photodetectors will additionally be absorbed in 200-µm-long curved (7˚) active sections with grounded pads. The P-metal electrodes for both types of detectors are supported by

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BCB and are connected to 100 µm X 100 µm RF pads, which are laid out in a G-S-G-S-G-S-G configuration (150 µm pitch) on either side of the PIC for direct probing.

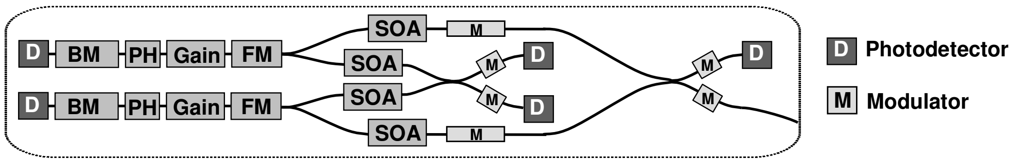

Fig.1. Functional schematic of chip.

Each of the other two half-power components from the 1 X 2 MMI splitter (directed toward the output) is first passed through a 400-µm-long phase modulator before entering a 340-µm-long 2 X 2 MMI coupler (with tuning pads). These two modulators connect to the same RF pads as the photodetectors mentioned above. Following the 2 X 2 MMI coupler, light passes through a 250-µm-long additional amplitude modulators in each branch that can be used for electronic monitoring of the PIC's output. Similar to the feedback loop, one of the modulators is followed by a photodetector (also for electronic monitoring of the output), while the other is followed by a 7° curved output waveguide with AR coated facet. The back sides of the SG-DBR lasers are also AR coated. The output modulators connect to RF pads that are identical to those in the feedback loop. Total length of the PIC is about 6.6 mm and its width is about 450 µm.

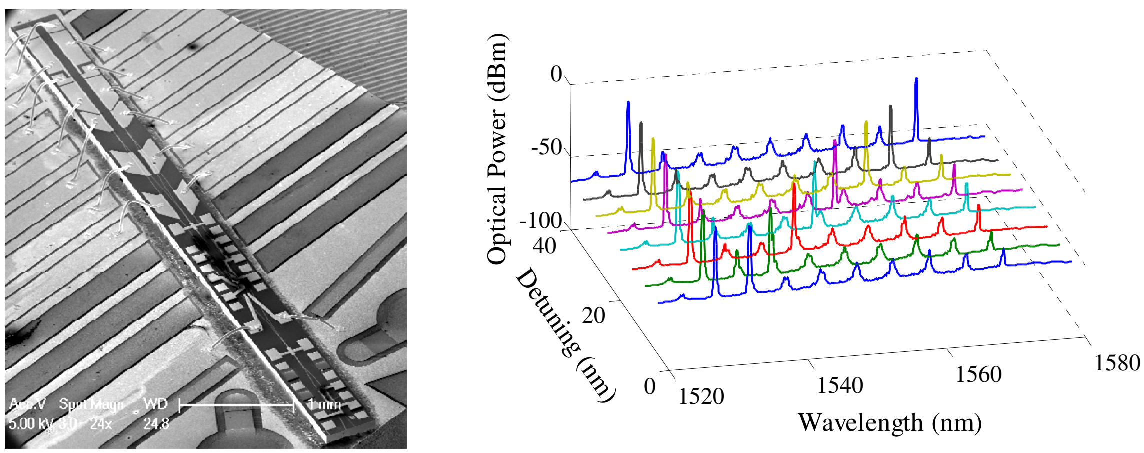

Fig.2. Left) SEM of Integrated OPLL PIC. Right) Output spectra from heterodyne optical source.

The SG-DBR lasers have more than 40nm wavelength quasi-continuous tuning range. By keeping one laser at fixed frequency and tuning the second laser, a heterodyne optical output signal is generated from the photonic IC where the heterodyne difference frequency can be selected over the full 0 to 5 THz frequency range, corresponding to the 40nm tuning range. This is illustrated by Fig. 2, right, where a series of optical spectra are captured to illustrate the output frequency range.

3. Proof-of-Concept OPLL Demonstration

A simplified schematic of the proof-of-concept OPLL arrangement is shown in Fig. 3, left. One of the integrated photodetectors is used to detect the beat signal between the two SG-DBR lasers. The detected photocurrent is then used to generate the wavelength tuning current applied to the phase section of one of the SG-DBR lasers, now acting as a current-controlled oscillator. A FET-transistor is required to translate the reverse biased detector current, to a forward biased phase section injection current. The detector load is tailored to generate a second order loop transfer function with lag compensation. In addition, the phase section is terminated by an inductor to compensate for the 3-dB bandwidth of the FM response of the SG-DBR laser (around 100MHz). The resulting loop bandwidth is around 300MHz. The free-running heterodyne beat signal is shown in Fig. 3, center, on a linear amplitude scale. The FWHM of the beat signal is around 300 MHz. However, it has been shown that the linewidth of SG-DBR lasers is dominated by low-frequency jitter [4], and as such, the phase noise can be well suppressed by a 300MHz loop bandwidth, as evidenced by the results below.

By splitting off part of the output of each laser before heterodyne detection, the phase and amplitude of each locked laser can be individually controlled. The two laser signals are then combined a second time, but now the heterodyne beat signal will carry any applied phase or amplitude modulation. In other words, this source has the potential to translate optical vector modulation to modulation on a coherent mmW or THz beat signal. For this homodyne OPLL demonstration, an applied phase modulation will directly result in a change in output amplitude due to coherent combination with the second laser output. This is illustrated by Fig. 3, right, where relatively pure phase modulation is applied by injecting a current into the phase modulator, resulting in a change in detected photocurrent in the on-chip monitor photodiode. This confirms successful optical phase locking of the two lasers. The finite extinction is a result of imbalanced detected power from the two lasers. In contrast, changing the modulator phase when the OPLL is unlocked, results only in the observation of residual amplitude modulation of the phase modulator, as also seen in Fig. 3, right.

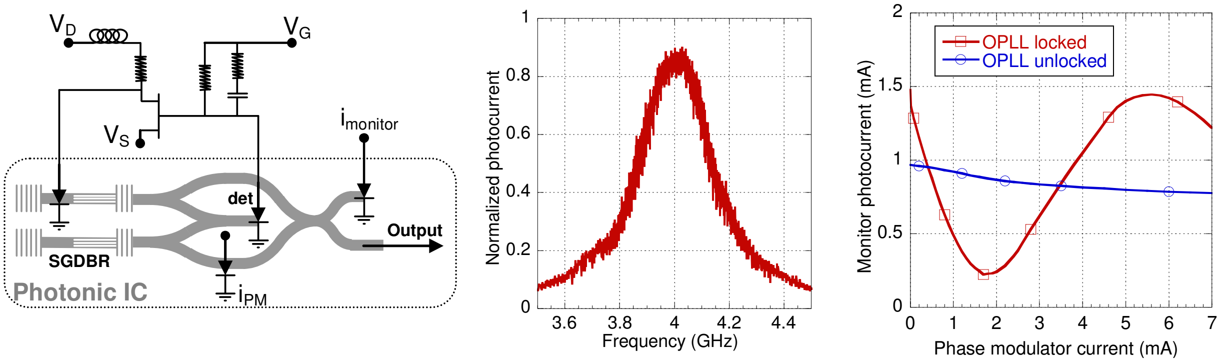

Fig.3. Left) Schematic of proof-of-concept OPLL demo. Center) Free-running laser heterodyne signal. Right) Interference between two locked lasers

4. Conclusion

In this paper we have demonstrated a monolithically integrated optical phase-locked loop photonic circuit in which all required optical components are integrated, including lasers, waveguides, couplers and photodetectors. This device includes widely tunable lasers with 5 THz tuning range and a capacity to apply modulation to a single optical line, translating optical vector modulation to a optical heterodyne signal. A simple proof-of-concept homodyne OPLL demonstration has been performed, confirming the suitability of SG-DBR lasers as a VCO laser in an OPLL. Future mmW heterodyne OPLL versions will fully utilize balanced detection, already in place on the photonic IC and integrated feedback electronics to increase the loop bandwidth and reduce laser amplitude noise fed back into the loop, for lower resulting phase noise.

Acknowledgements

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