

Research in Optoelectronics (A)

Reprints published in 2011

by

Professor Larry A. Coldren

and Collaborators

Published as

Technical Report # ECE 12-01

of

The Department of Electrical & Computer Engineering

The University of California

Santa Barbara, CA 93106

Phone: (805) 893-4486

Fax: (805) 893-4500

E-mail: coldren@ece.ucsb.edu

<http://www.ece.ucsb.edu/Faculty/Coldren/>

Introduction:

The 2011 volume of Research in Optoelectronics (A) includes articles on which Professor Coldren led or collaborated with others on semiconductor device and fabrication research. Any journal or conference publication in which Prof. Coldren was named as a co-author is included. Most of the work originated from proposals generated within Coldren's group. As in recent years the work has a focus on III-V compound semiconductor materials as well as the design and creation of photonic devices using these materials—mostly diode lasers and photonic integrated circuits (PICs). The work spans efforts from basic materials and processing technology, through device physics, design, and formation, to their characterization within systems environments.

The work on **I. Photonic Integrated Circuits** (PICs) is further broken down into the sub-categories: *IA. Tutorials and Reviews*; *IB. Ring Lasers and Filters*; *IC. Coherent Receivers with Phase-locked Tunable LOs*; *ID. Coherent RF Receiver using Tracking Modulators*; and *IE. Coherent Beam Sweeping*. Coherent photonics is a pervasive theme, and much of the work on ring lasers and filters was also directed at Microwave Photonics applications. A second major area, also directed at coherent and/or microwave photonics applications, was in **II. Fabrication and Component Development**. A third area, which unlike the first two, relies upon a significant Molecular Beam Epitaxial (MBE) growth effort, is **III. Vertical-Cavity Surface-Emitting Lasers (VCSELs)**. Finally, we continued to support the MOCVD activity, which now also involves a strong effort by Prof. J. E. Bowers: **IV. MOCVD Growth**. In nearly every project the work requires efforts in materials research, device physics, device design, process development, device fabrication, and device characterization. Most students are deeply involved in several, if not all, of these efforts, so our graduates tend to be known for their “bandwidth.”

The work was performed with funding from several grants from industry and government, some gift funds from industry, and support from the Kavli Endowed Chair in Optoelectronics and Sensors. Several projects were funded by the MTO Office of DARPA and the industries involved included Rockwell-Collins, JDSU, Corning, Teledyne, Telcordia, Ziva, and Freedom Photonics.

The first group of reprints (*IA.*) includes six INVITED papers, the first a magazine article, the next two major journal papers, the following two conference papers, and the last a PLENARY presentation, for which the presentation slides are included. All also center about the photonic integration technology we have originated, although the first article also mentions our second major device activity on VCSELs. The third paper features work led by Prof. Blumenthal's group on photonic switching and networking that was strongly supported by Coldren's group.

A good summary of both the growing demand for communication bandwidth and the development of Photonic ICs is contained in the last set of slides in Section *IA* as presented in a Plenary Talk at the Asia Communications and Photonics (ACP) Conference. The ultimate focus of this presentation, as it has been within Coldren's research group for this year, is on the use of integration for coherent communication and

sensing chips. These make use of the full vector field of the lightwaves rather than just the optical intensity to transmit and receive information, thereby greatly increasing the spectral efficiency. Much of this work has been in collaboration with Professor Rodwell’s group. Optical phase locked loops (OPLLs) enable Hertz level relative frequency stability, rapid tunability over many GHz, and linewidths as low as the reference source (<100kHz).

The Second group of six papers (*IB.*) summarizes work on *Ring Lasers and Filters*. The filter work aims to demonstrate programmable multi-section infinite-impulse response (IIR) analog filters with relatively high dynamic range using semiconductor optical amplifiers (SOAs) as the internal variable-gain element. This has required special design of the SOAs to prevent premature saturation as well as novel filter design to optimally place these elements within the ring resonators. Record Spur-Free Dynamic Range (SFDR) has been demonstrated in filters having high programmability of the filter center frequency, bandwidth, and shape. The Introduction of the 2010 Reprint Book illustrated a couple of designs. This work was funded under the DARPA PhASER program.

The ring laser work also used single or coupled ring resonators, but explored them with SOA gains exceeding the lasing threshold. Some of the work focused on mode-locking many adjacent ring modes of the ring lasers to provide multi-GHz repetition-rate pulse trains. The cover shows a photo of such a device. One important application, outlined in the ACP slides, is to phase lock one of the lines of the mode-locked lasers to a stable reference source, and then to phase lock a widely-tunable laser (e.g., SGDBR) to any of the other lines to translate the same stability to the tunable laser across a wide range of wavelengths. See slides labeled “Optical waveform synthesis LIDAR transmitter” and “Tuning across the comb.” The latest results for the mode-locked ring lasers are also shown there in the next slide—“Broadband comb generation.” The first slide is repeated here for clarity. The formal publications will appear in 2012. This work is being funded under the DARPA CIPHER program, Rockwell-Collins, and some other industrial partners.

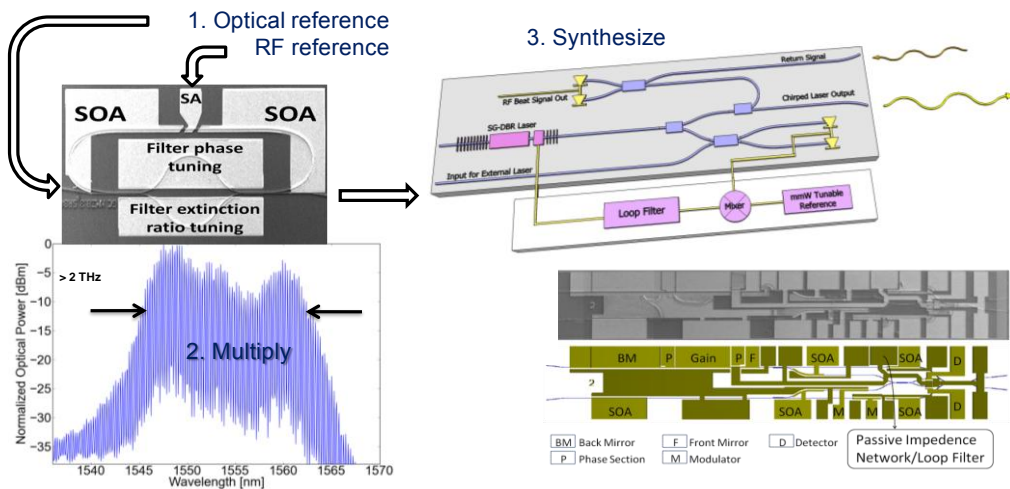


Fig. 1. Schematic of synthesized optical source for sensor and communication applications. Optical reference fixes a line of the mode-locked laser to which the SGDBR widely-tunable laser is locked with a mmW source offset. Tunable laser acquires properties of reference and can coherently move across its entire tuning spectrum by moving from line to line.

Integrated *Coherent Receivers with Phase-Locked Tunable LOs (IC.)*, as outlined in the ACP talk slides of Section *IA*, resulted in one publication in 2011. As mentioned above this work is in collaboration with Prof. Rodwell and is funded by the DARPA CIPhER program as well as several companies. The project not only involves the design and fabrication of a complex PIC that contains the tunable Local Oscillator (LO), a novel optical hybrid, and at least four high-bandwidth photodiodes, it also involves the hybrid integration of this PIC with a custom EIC and a feedback loop filter designed by Prof. Rodwell's group. Fig. 2 shows a schematic taken from the ACP talk. Thus, it is quite an accomplishment to now know that this all is finally beginning to work. We expect to see numerous publications to follow in 2012.

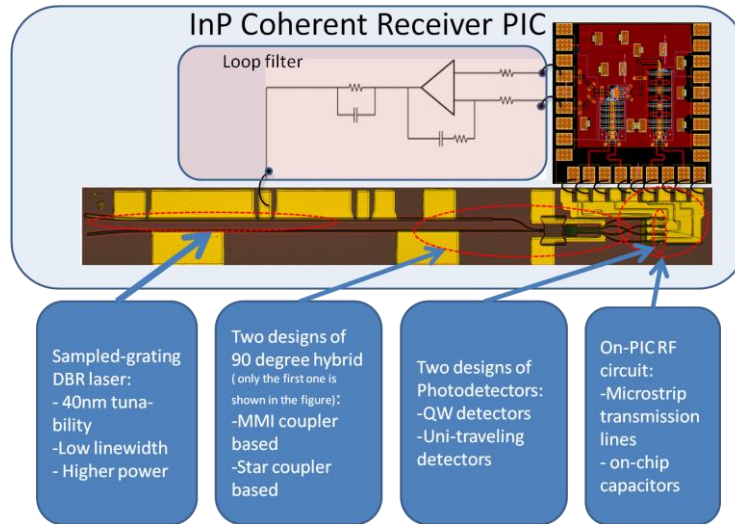


Fig. 2. *Integrated Optical Phase-Locked Loop (OPLL) showing feedback to tuning element of widely-tunable SGDBR laser (LO in receiver) via Costa's loop EIC and loop filter on a common carrier.*

Besides the lattice filter effort described in Section *IB.*, another RF photonics effort has been funded by the DARPA PHORFRONT program led by Prof. Bowers to integrate *Coherent RF Receivers using Tracking Modulators (ID.)*. This year the results are all on the collaboration with Profs. Li and Herczfeld, of Dartmouth and Drexel, respectively. The papers give results on their concept of an attenuated counter-propagating OPLL, in which the tracking modulator has resistive traveling-wave electrodes that are fed from the end where the lightwave exits. The idea, which provides an effectively shorter modulator at higher frequencies, was successfully demonstrated.

In the *Coherent Beam Sweeping (IE.)* section, initial results are given for a new project funded via the DARPA SWEEPER program, which is in collaboration with Prof. Bowers. The aim of the project is to generate narrow, agile beams than can be swept in two dimensions up to a total of 45 degrees in both dimensions. As indicated in Fig. 3, our concept is to use a single-chip emitter with an array of waveguides that are fed coherently each having surface-emitting gratings in some emission region. To deflect the beam in the axial (along the propagation), or φ , direction, the wavelength is changed; to deflect the beam in the lateral (perpendicular to guides), or θ , direction, the phases of the waveguides must be adjusted—like a typical phased-array. Thus, for an $n \times n$ array, one

needs to adjust $n + 1$ controls— n phases and 1 wavelength. Side-lobes can also be controlled by shaping the near-field with a pre-amplifier SOA array. Finally, in order to monitor what is being emitted without a detector above the chip, an on-chip photodetector array has also been included. Both near-field and far-field detector array versions are being explored. In the Coldren group a monolithic InP chip approach is being investigated; in the Bowers group a hybrid InP/Si approach is being used.

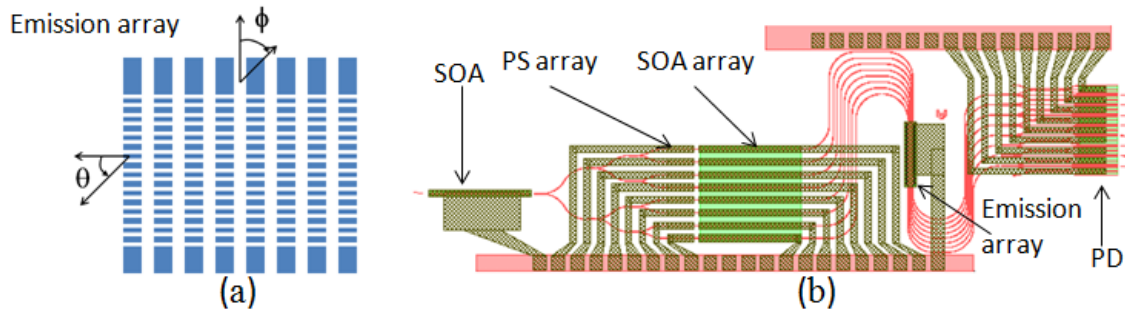


Fig. 3. Coherent beam sweeping chip. (a) 8-waveguide array with surface-emitting gratings; (b) integrated InP chip including all elements except tunable laser.

The publications in Section **II. Fabrication and Component Development**, include five papers on techniques developed to either fabricate somewhat generic components or even more generic techniques to create a variety of components. Most of the work involves variations on dry-etching technology. The first and third papers are specifically looking at etching narrow trenches with a high-aspect ratio; the second focusses on obtaining vertical etch walls where a second wall is not necessarily very close (Fig. 4 shows SEMs); the fourth again considers narrow trenches, but this time using the reduction in etch rate in a trench—the so-called lag effect—to advantage to create directional couplers. The fifth paper uses dry etching with a single holographically-defined lithography to create smooth-walled Si nanowires. As shown in Fig. 4, very good control of feature size and aspect ratio are possible with modern ICP tools. Support for these efforts was provided by DARPA and UCSB sources.

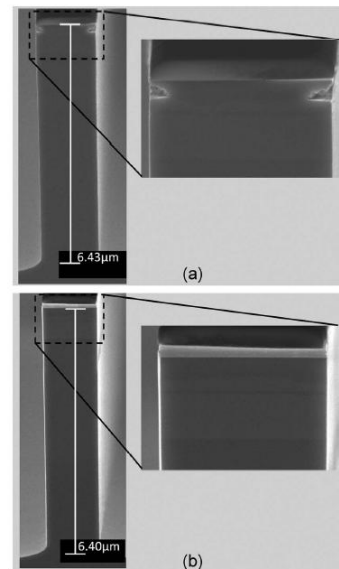


Fig. 4. $\text{Cl}_2/\text{H}_2/\text{Ar}$ ICP etching with (a) and without (b) H_2 flood at initial ignition.

Section **III. Vertical-Cavity Surface-Emitting Lasers (VCSELs)**, includes six publications describing recent advances on novel high-speed and three-terminal VCSELs. Results on polarization modulation and stabilization as well as a novel carrier separation-modulation scheme are reported. Both were introduced in the 2010 Reprints edition. However, more detailed design, modeling and experimental results are contained in this volume. For example, it was found that the polarization selectivity has a definite crystallographic preference. The last paper was an invited presentation given at the

Global COE International Symposium held in honor of the retirement of Prof. Iga as President of the Tokyo Institute of Technology. Support for these efforts has been coming from DARPA, NSF, and an STTR with Ziva Corp.

The last couple of papers in Section **IV. MOCVD Growth**, summarize recent work primarily directed by Prof. Bowers on epitaxial lateral overgrowth of InP on Si. Prof. Coldren's group continues to be active in MOCVD growth, but only on InP at this point.

Professor Coldren's Group



Back Row: Weihua Guo, John Parker, Rob Guzzon, Milan Mashanovitch

Middle Row: Mingzhi Lu, Abi Sivananthan, Leif Johansson, Chad Althouse, Erik Norberg

Front Row: Libby McCollum, Pietro Binetti, Professor Larry Coldren, Chin-Han Lin, Yan Zheng

Professor Coldren's Group

I. Researchers

| | |
|--------------|---|
| A. Bhardwaj | Visiting Scientist, UCSB, now at JDSU |
| P. Binetti | Postdoctoral Scholar, UCSB |
| W. Guo, | Assistant Project Scientist, UCSB |
| Y. Hung | Visiting Student from National Taiwan University of Science and Technology, UCSB |
| L. Johansson | Associate Research Engineer, UCSB |
| M. Masanovic | Project Scientist, UCSB |
| S. Ristic | Postdoctoral Scholar, UCSB |

II. Students

| | |
|-------------------|---|
| C. Althouse | Ph.D. Program |
| C. Chen | Ph.D. Program, now at NTT |
| M. Dummer | Ph.D. Program, now at Vixar Inc. |
| R. Guzzon | Ph.D. Program, now at Aurrion |
| U. Krishnamachari | Ph.D. Program, now at Binoptics Corporation |
| C. Lin | Ph.D. Program |
| M. Lu | Ph.D. Program |
| S. Nicholes | Ph.D. Program, now at Micron Technology |
| E. Norberg | Ph.D. Program, now at Aurrion |
| J. Parker | Ph.D. Program |
| A. Sivananthan | Ph.D. Program |
| A. Tauke-Pedrotti | Ph.D. Program, now at Sandia National Labs |
| Y. Zheng | Ph.D. Program |

III. Staff

| | |
|-------------|--|
| D. Cohen | Principal Development Engineer, reports to Prof Nakamura |
| L. McCollum | Center Assistant, OTC |

Collaborators

I. *Faculty*

| | |
|---------------|--|
| D. Blumenthal | UCSB |
| J. Bowers | UCSB |
| S. DenBaars | UCSB |
| P. Herczfeld | Drexel University |
| S. Lee | National Taiwan University of Science and Technology |
| Y. Li | University of Massachusetts at Dartmouth |
| N. McKeown | Stanford University |
| P. Petroff | UCSB |
| M. Rodwell | UCSB |

II. *Researchers*

| | |
|---------------|--|
| H. Ambrosius | Director of Clean Room, Optoelectronics Devices Group, Eindhoven University of Technology |
| J. Barton | Assistant Project Scientist, UCSB (Blumenthal) |
| N. Beheshti | Ericsson Research Lab |
| E. Bloch | Research Scientist, Technion Israel University of Technology and UCSB (Rodwell) |
| E. Burmeister | Ciena |
| J. Doylend | Postdoctoral Scholar, UCSB (Bowers) |
| G. Epps | Cisco Systems |
| A. Fang | Aurrion |
| Y. Ganjali | Faculty Member, University of Toronto |
| M. Gross | Ziva Corporation |
| M. Heck | Postdoctoral Scholar, UCSB (Bowers) |
| B. Kim | Aurrion |
| J. Klamkin | MIT Lincoln Labs |
| B. Koch | Intel |
| V. Lal | Infinera |

| | |
|--------------|--|
| P. Mages | Project Scientist, UCSB (Bowers) |
| J. Peters | Senior Development Engineer, UCSB (Bowers) |
| H. Poulsen | Research Scientist, UCSB (Blumenthal) |
| A. Ramaswamy | Aurrion |
| B. Stamenic | Senior Development Engineer, UCSB (Blumenthal) |
| M. Sysak | Intel |
| B. Thibeault | Project Scientist, UCSB (Rodwell) |
| R. Wang | Researcher, University of Massachusetts at Dartmouth |

III. Collaborating Students

| | |
|---------------|---|
| J. Bovington | UCSB, Bowers |
| J. Garcia | UCSB, Blumenthal |
| B. Jevremovic | UCSB, Blumenthal |
| S. Jin | University of Massachusetts at Dartmouth (Li) |
| N. Julian | UCSB, Bowers |
| E. Lively | UCSB, Blumenthal |
| J. Mack | UCSB, Blumenthal |
| K. Nguyen | UCSB, Blumenthal |
| H. Park | UCSB, Gossard |
| C. Zhang | UCSB, Bowers |

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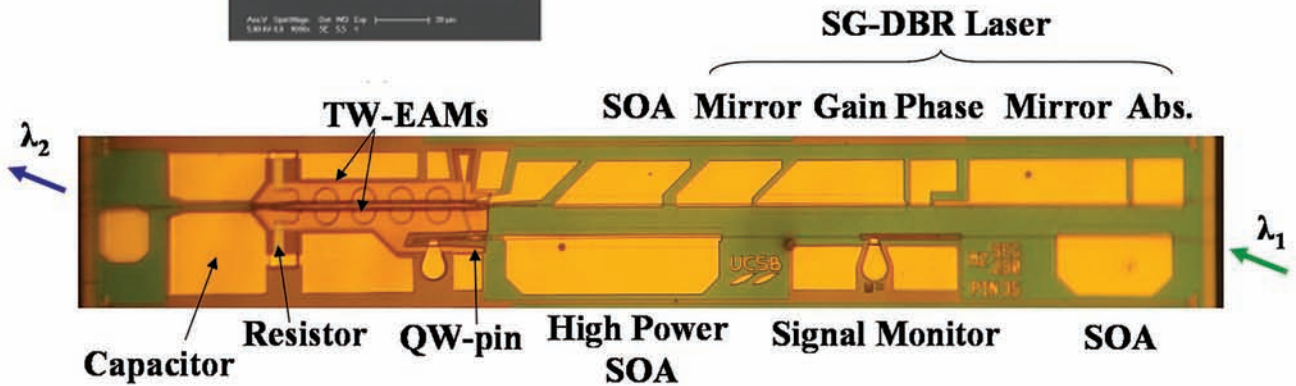
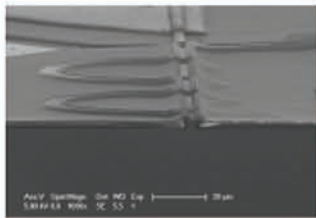
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I. Photonic Integrated Circuits

A. Tutorials and Reviews

Semiconductor Laser Advances: The Middle Years



Semiconductor Laser Advances: The Middle Years

Applications that stimulated advances 20 years ago are now the latest rage!

By Larry A. Coldren, UCSB

Introduction

As we celebrate the 50th anniversary of the Laser and roughly the 40th anniversary of the semiconductor laser, I am reminded of some important developments that occurred about 20 years ago that really revolutionized the field and have had a lasting effect on many of the semiconductor lasers that impact our lives today. The developments are in two widely separated segments of semiconductor laser technology—widely-tunable lasers and vertical-cavity surface-emitting lasers (VCSELs). Indeed, both are very important today; the first in dense wavelength-division-multiplexed (WDM) fiber communication and fiber sensor technology, and the second in data communications, computer mice, and other emerging consumer applications. Both are also loosely connected because both rely upon sophisticated and novel Distributed Bragg Reflector (DBR) mirrors.

In both cases the desirability of such devices and some basic concepts had been put forth by the late 1980s, but the viability of such devices was unclear. *Some breakthroughs were needed.* In the case of the widely-tunable laser, work on coherent communication during the 1980s had defined a need for a tunable local oscillator (LO) in the coherent heterodyne receivers that could tune across the fiber C-band of some 40 nm, much like the LO of a car radio receiver that tunes across the entire FM band. A single universal transmitter laser that could be set to any wavelength was also desired. Bulky, expensive external-cavity lasers existed that could do this, but there were no monolithically integrated semiconductor lasers that might have the kind of cost and reliability desired. In the case of VCSELs, again the arguments had been made that such devices would be very desirable, if they could be practically manufactured [1]. However, after a significant multi-year effort by Prof. Iga and his elite group at the Tokyo Institute of Technology (TIT), the results were still somewhat marginal, and the structure also appeared to be rather complex. CW operation finally came in 1988 [2], but the practicality of the device was still in question. I was lucky enough to find myself in a position to make contributions to both of these opportunities beginning in the late 1980s.

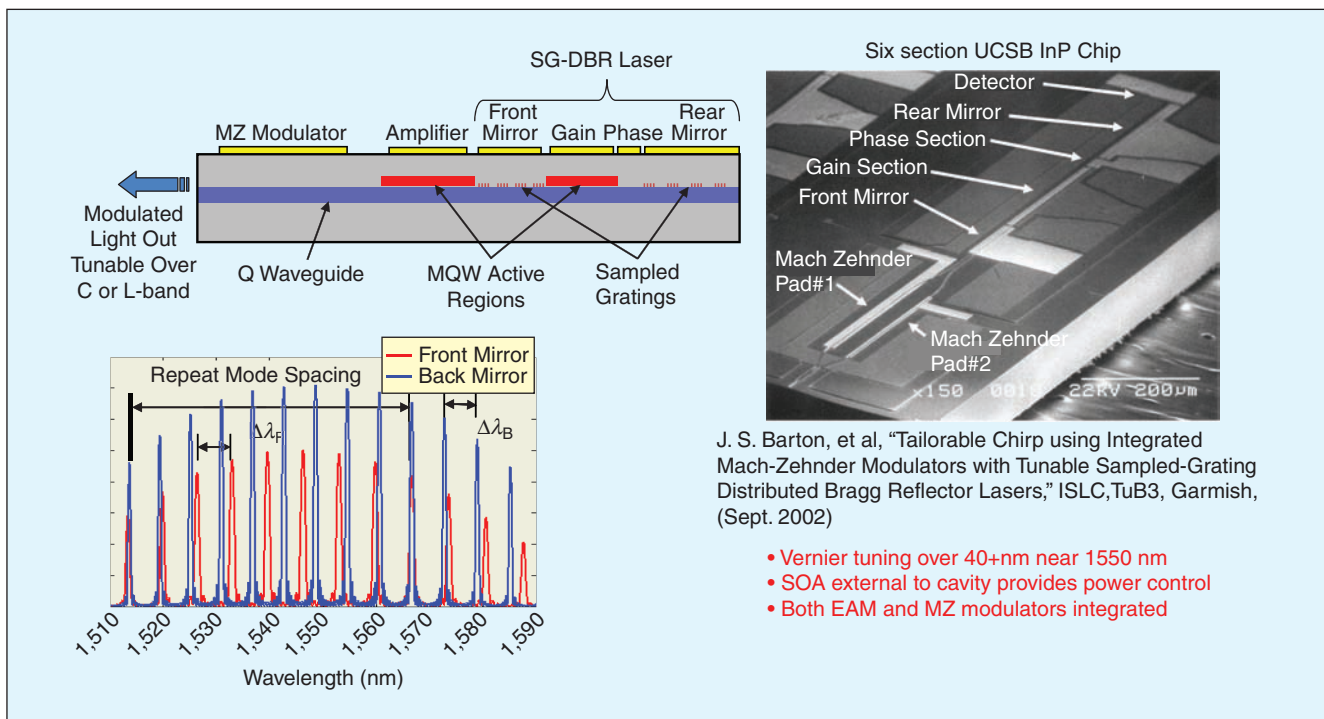
Widely-Tunable Lasers

My efforts on monolithic tunable diode lasers actually began at Bell Labs in the late 1970s with efforts on monolithic coupled-cavity lasers in the then new InGaAsP/InP materials system [3]. After going to UCSB in 1984, my work continued on tunable 2-section coupled-cavity lasers, but it was soon realized that these had some significant limitations.

Three-section tunable DBRs had also appeared in the 1980s [4, 5], but these also had their limitations. The coupled-cavity lasers had trouble with spurious mode suppression and reproducibility, and the 3-section DBR was practically limited to < 10 nm of tuning in the 1550 nm range, much less than the ~ 40 nm that was desired for the coherent as well as the emerging WDM applications.

The first breakthrough idea involved a combination of some concepts from both the coupled-cavity and 3-section DBR lasers. It was to be a *4-section multi-element mirror laser*. It enabled full wavelength coverage over > 40 nm in multiple wavelength bands within a single monolithic chip. Like the coupled-cavity laser, it used the vernier effect; in this case using differently spaced reflection maxima from the two mirrors rather than the two differently spaced Fabry-Perot mode spacings of the coupled cavities. But similar to a standard DBR laser, it also used an intra-cavity tuning electrode to line up a cavity mode with the single net reflection maximum resulting from the product of the two mirror spectra. (See Fig. 1) A patent was filed in 1988 and issued in 1990 [6], and this later became the key element in the Intellectual Property of a company to be formed nearly a decade later—Agility Communications.

Before Agility was formed in 1998 to commercialize the multi-element mirror widely-tunable laser technology, quite a bit of additional R & D was done on the preferred embodiment, the Sampled-Grating-DBR or SGDBR laser at UCSB [7, 8]. During the 1990s, many other monolithic widely-tunable laser designs also evolved. For example, there were variants on the SGDBR that used chirped grating bursts rather than uniform sampled grating bursts [9]; there were relatively complex vertically-coupled laser structures that used the wide tuning feature of a grating-assisted co-directionally coupled filter within their cavities [10]; and there were even VCSELs with electrostatically moveable mirrors mounted on microscopic cantilevers [11]. Although many of these were also the subject of startup companies, most of this technology is no longer in production today. More recently another variant on the SGDBR, the so-called DSDBR has been developed and is now being mass produced in similar quantities to the SGDBR [12]. It uses a similar concept for the back mirror, but a multiply-contacted grating array for the front mirror. Together these two account for the majority of all of the dense WDM lasers being sold today. The SGDBR is currently being manufactured by JDSU which acquired Agility in 2005.



J. S. Barton, et al, "Tailorable Chirp using Integrated Mach-Zehnder Modulators with Tunable Sampled-Grating Distributed Bragg Reflector Lasers," ISLC, TuB3, Garmish, (Sept. 2002)

- Vernier tuning over 40+nm near 1550 nm
- SOA external to cavity provides power control
- Both EAM and MZ modulators integrated

During the 1990s, work on the SGDBRs at UCSB, as well as some of the work on other monolithic tunable lasers elsewhere, began to spawn larger Photonic Integrated Circuits (PICs) as it became obvious that the same fabrication steps required to make the laser could also form other components outside of the cavity at the same time. Thus, these lasers integrated with modulators, amplifiers, and monitoring detectors were soon demonstrated [8, 13]. In fact, the very first Agility products had integrated Semiconductor Optical Amplifiers (SOAs) or Electro-Absorption Modulators (EAMs) as well as back-side monitoring detectors integrated with the SGDBRs. Today JDSU manufactures an integrated Mach-Zehnder Modulator (MZM) with the SGDBR.

The InP-based PIC work at UCSB has continued to evolve in recent years with improvements in the capabilities of the integration platform and the design of the components. For example, a robust impurity-free, quantum-well intermixing technology for the InGaAsP/InP system has been found to be invaluable in providing multiple active and passive waveguide sections from a single initial epitaxial layer growth [14]. Integrated widely-tunable transmitters operating up to data rates of 40 Gb/s have been demonstrated in a variety of designs and technologies. (See Fig. 2) Wavelength converters using both integrated SOA-PIN receivers directly driving the modulator of a widely-tunable transmitter [15, 16]—the so-called separate absorption and modulation (SAM) design—and designs using cross phase modulation in SOAs within the MZM modulator of a widely-tunable transmitter [17]—the so-called combined absorption and modulation (CAM) design—have been demonstrated up to 40 Gb/s. Using eight of these integrated with an Arrayed Waveguide Grating Router (AWGR) on a single chip, we have more recently demonstrated a

MONolithic Tunable Optical Router (MOTOR) PIC, which functions as an 8×8 crossbar switch [18]. Current work is focused on coherent transmitters and receivers that incorporate SGDBRs (e.g. Fig. 3)—sort of ironic that some 20 years later we are finally focusing on the primary application that spawned the invention!

VCSELS

Going back to the mid-1980s again, the other half of our research at UCSB was focused on reflective surface-normal modulators for optical interconnects within and between computers. To support the modulator work we had developed a Molecular Beam Epitaxy (MBE) effort focused on the GaAlAs/GaAs materials. The modulator work evolved toward resonant-cavity designs with multi-layer DBR mirror stacks and multiple-quantum-well (MQW) active regions in the cavities. In order to improve their efficiency, modeling indicated that the quantum-wells should be placed only at the peaks of the electric field standing wave of the resonant cavity. This was true whether one considered the index shift or absorption from the quantum wells. We realized very quickly that this enhancement would also be true for VCSELS, and proposed devices designed with quantum-well gain regions placed only at the standing-wave peaks in order to get up to 2x the modal gain as compared to the same amount of gain material distributed uniformly along the standing wave. [It's really just the maximum value of $\cos^2 x$ compared to its average.] (See Fig. 4) This concept was first published at CLEO in 1988 [19], but surprisingly the VCSEL veterans didn't get very excited about this key advance. Of course, a factor of *two* in modal gain for the same current and active volume is *huge*. This completely changes

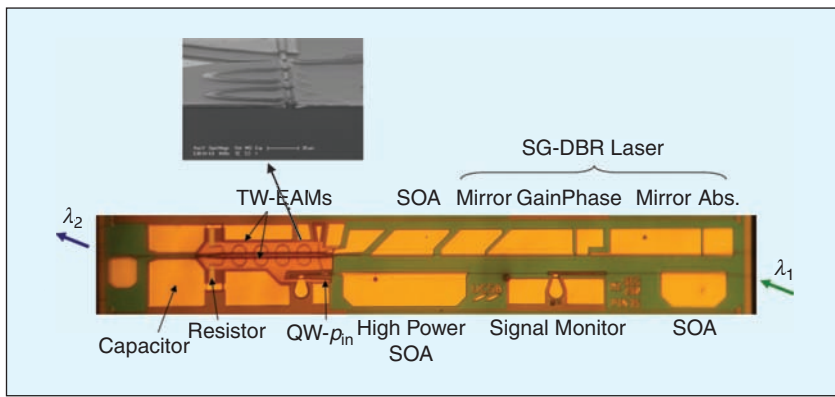


Figure 2. Transceiver/wavelength-converter: 2-stage-SOA-PIN Receiver and SGDBR-TW/EAM Transmitter.

the design possibilities, for example, enabling cavities to have twice the loss and still lase.

There was one believer, but he wasn't a VCSEL guy, he was another modulator guy—Jack Jewell. He also knew something we did not—that multi-layer mirror stacks could be made with >99% reflectivity. Thus, only one set of quantum wells at one standing wave peak would be necessary to make a viable VCSEL, while we thought that ~98% was about as high as could be expected for a vertical mirror stack. So, our modeling showed that we would need at least three or four periods of gain, which made the problem considerably harder. So, we at UCSB tried to make this multiple-periodic-

gain laser, while Jack put together a single period device at Bell Labs with the help of multiple collaborators. We both also had to develop bandgap engineered mirrors to reduce the voltage drops caused by the discontinuities between the high and low Al-containing layers.

By the time it was realized that high-reflectivity mirrors could be formed, more than a year had gone by, and Jewell, et al beat us into print by a few months with the first cw electrically-pumped, low-threshold “microlaser” that used a thin active region (1–3 QWs) on a single standing wave peak [20]. (However, in our defense it might be mentioned that our first publication reported considerably better results [21].) Our UCSB group went on from there to generate a few years of leading results in VCSEL efficiency, output power, and temperature stability [22]. Essentially *all* commercial VCSELs from that time through the present have included the design features developed jointly with Jewell—that is, an all-epitaxially grown cavity, a thin active region placed at a single standing wave maximum, high-reflectivity (>99%) mirrors, and graded interfaces between layers within the cavity. In recognition of these contributions we jointly received the 2009 Aron Kressel Award.

Since the early 1990s, our UCSB VCSEL efforts have continued to focus on high efficiency, all-epitaxial designs.

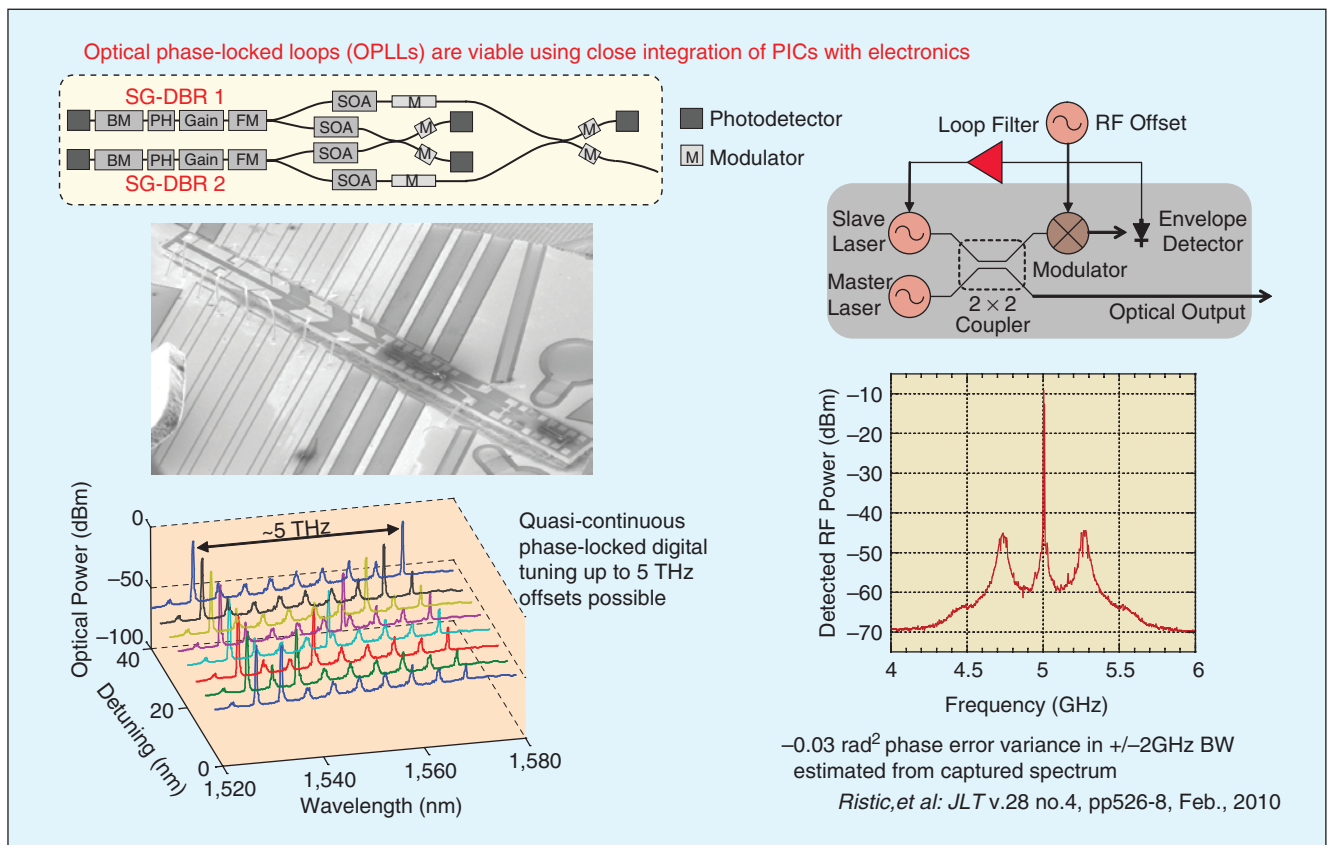


Figure 3. Optical Phase Locked Loops: Offset Locking Two SGDBRs.

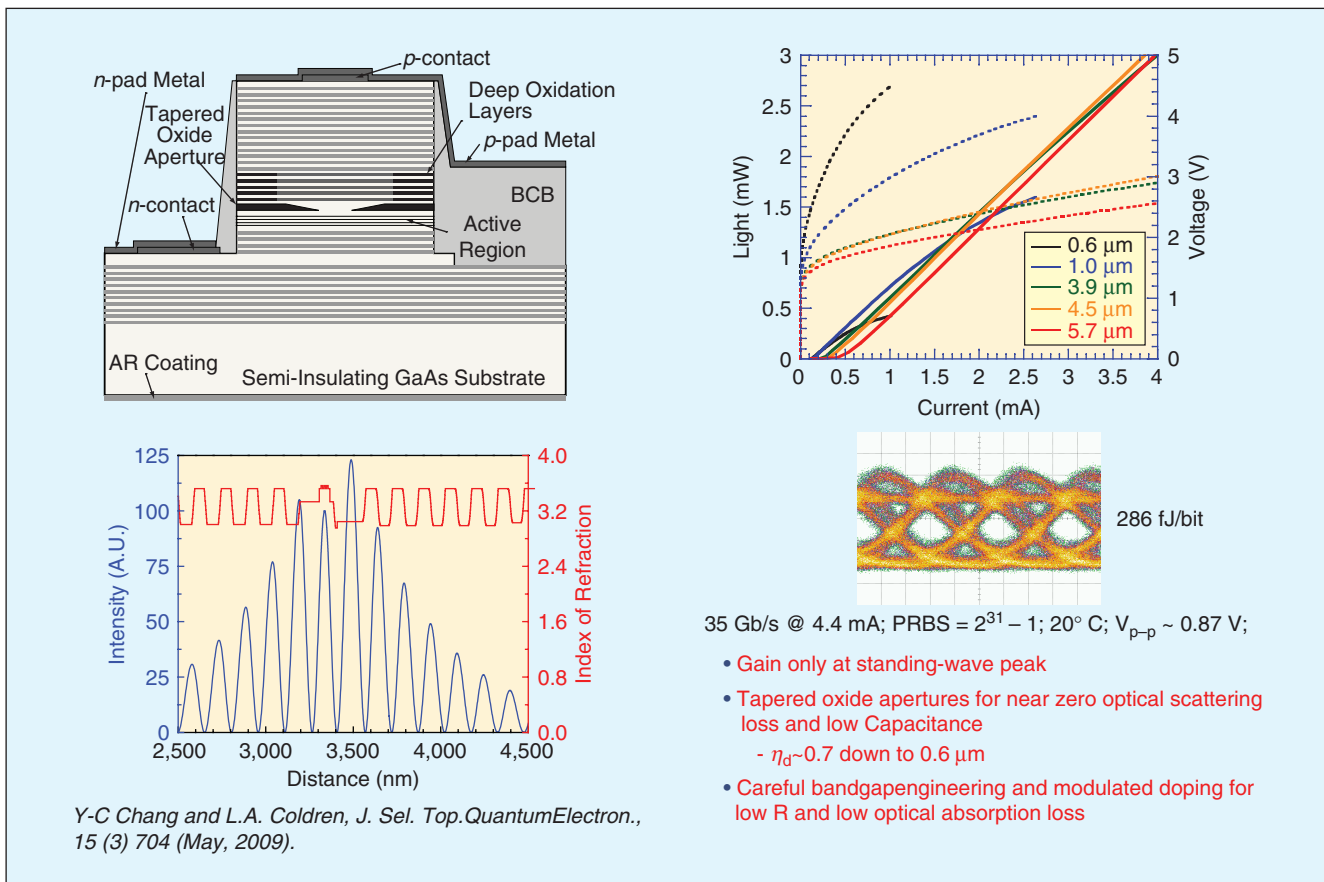


Figure 4. VCSEL Advances.

This has required the use of strained quantum-well active regions, which results in a wavelength in the ~ 980 nm range in the GaAs system. Unfortunately, for a number of practical reasons at the time, a data-link standard ~ 850 nm was established in the 1990s for VCSELs, so the more efficient devices that we pursued were not widely developed commercially. Even the companies that Jack Jewell and I co-founded, which initially worked on our original designs at 980 nm, eventually switched away from this wavelength for market reasons. (At UCSB we did demonstrate strained 850 nm AlInGaAs quantum-well VCSELs, with good properties, but our GaAs-based efforts continued to focus at 980 nm because of the numerous benefits associated with the longer wavelength [23].)

Another key contribution made by our UCSB group in the 1990s, which has enabled the record power efficiencies and bit rates/mW that have been demonstrated, was the virtual elimination of optical scattering loss by the incorporation of an intra-cavity lens-like aperture. This invention also provides a Gaussian cavity mode for low diffraction loss output beams as well as enabling the cavity volume to be reduced (for higher bandwidth) without requiring added threshold current density [24].

More recently there has been renewed interest in high-efficiency devices, so our long term pursuit of the longer-wavelength, strained-active-region VCSELs on GaAs is beginning to be more appreciated. VCSELs are now being used in high-

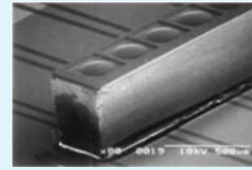
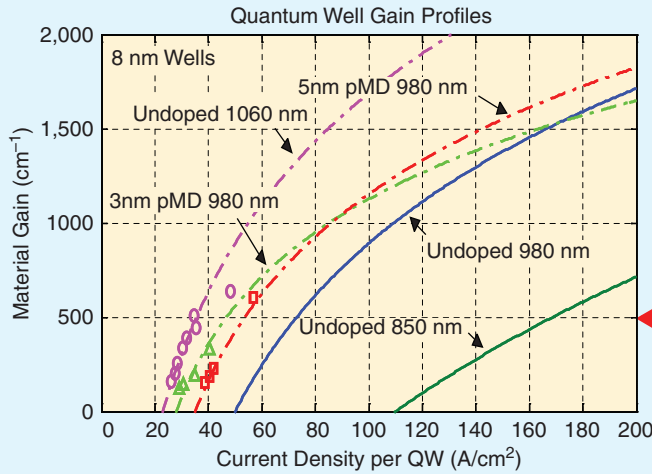
density arrays for optical interconnects in data centers and between and within high-performance computers. Again, we see the motivation that drove some key advances 20 years ago becoming a key driver today. In fact, compressively-strained active regions provide more than improved efficiency, which occurs because of their lower transparency current and higher differential gain. Importantly, these active regions also appear to have higher reliability [25], they operate better at higher temperatures [26], they provide a higher intrinsic modulation bandwidth, and the longer wavelengths they emit can penetrate the GaAs substrate enabling flip-chip mounting and easier coupling optics. (See Fig. 5) Today, several companies are pursuing VCSELs with highly strained quantum-well active regions having wavelengths even longer than 980 nm—1060 nm appears to be the new choice [23]. Again, the primary driver is computer interconnects with high efficiency and high reliability.

Larry A. Coldren is the Fred Kavli Professor of Optoelectronics and Sensors and Acting Richard A. Ahlhl Dean of Engineering at the University of California, Santa Barbara, CA. He received the Ph.D. degree in Electrical Engineering from Stanford University in 1972. After 13 years in the research area at Bell Laboratories, he joined UC-Santa Barbara in 1984 where he now holds appointments in Materials and Electrical & Computer Engineering. In 1990 he co-founded Optical Concepts, later acquired as Gore Photonics, to develop novel VCSEL

- Higher-intrinsic modulation bandwidth @ lower current density

$$f_M = \left[\frac{v_{ga} a}{qV_p} \eta_i (I - I_{th}) \right]^{1/2}; \quad a \propto dg/dJ$$

- Lower threshold and better efficiency
- Improved reliability and high temperature performance
- Transparent substrate (flip-chip/backside optics/simple contacts, etc.)
- Lower fiber loss and material dispersion



For 500 cm⁻¹:

- InGaAs QWs @ 1060 nm require ~ 21% of the current vsGaAs
- InGaAs QWs @ 980 nm require ~ 43% of the current Versus GaAs

L.Coldren, et al, *Photon. Soc. Sum. Top., Playa Del Carmen, pap TuD2.1, July, 2010.*

Figure 5. The case for 980-1100 nm (strain/GaAs).



Figure 6. Student Testing Photonic IC.

technology; and in 1998 he co-founded Agility Communications, later acquired by JDSU, to develop widely-tunable integrated transmitters.

At Bell Labs, Coldren initially worked on waveguided surface-acoustic-wave signal processing devices and coupled-resonator filters. He later developed tunable coupled-cavity lasers using novel reactive-ion etching (RIE) technology that he created for the then new InP-based materials. At UCSB he continued work on multiple-section tunable lasers, in 1988 inventing the widely-tunable multi-element mirror concept, which is now used in some JDSU products. Near this same time period he also made seminal contributions to efficient vertical-cavity surface-emitting laser (VCSEL) designs that continue to be implemented in practical devices to this day. More recently, Prof. Coldren's group has developed high-performance InP-based photonic integrated circuits (PICs) as well as high-speed VCSELs, and they continue to advance the underlying materials growth and fabrication technologies.

Professor Coldren has authored or co-authored over a thousand journal and conference papers, 7 book chapters, 1 textbook, and has been issued 63 patents. He has presented dozens of invited and plenary talks at major conferences, he is a Fellow of the IEEE, OSA, and IEE, a recipient of the 2004 John Tyndall and 2009 Aron Kressel Awards, and a member of the National Academy of Engineering.

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High Performance InP-Based Photonic ICs—A Tutorial

Larry A. Coldren, *Fellow, IEEE, Fellow, OSA*, Steven C. Nicholes, Leif Johansson, *Member, IEEE*, Sasa Ristic, *Member, IEEE*, Robert S. Guzzon, Erik J. Norberg, and Uppiliappan Krishnamachari

(Invited Tutorial)

Abstract—The performance of relatively complex photonic integrated circuits (PICs) is now reaching such high levels that the long sought goal of realizing low-cost, -size, -weight, and -power chips to replace hybrid solutions seems to have been achieved for some applications. This tutorial traces some of the evolution of this technology that has led to an array of high-functionality InP-based PICs useful in optical sensing and communication applications. Examples of recent high-performance PICs that have arisen out of these developments are presented.

Fundamental to much of this work was the development of integration strategies to compatibly combine a variety of components in a relatively simple fabrication process. For the UCSB work, this was initially based upon the creation of a single-chip widely tunable semiconductor laser that required the integration of gain, reflector, phase-tuning and absorber sections. As it provided most of the elements needed for many more complex PICs, their creation followed somewhat naturally by adding more of these same elements outside of the laser cavity using the same processing steps. Of course, additional elements were needed for some of the PICs to be discussed, but in most cases, these have been added without adding significant processing complexity. Generally, the integration philosophy has been to avoid patterned epitaxial growths, to use post-growth processing, such as quantum-well intermixing to provide multiple bandgaps, rather than multiple epitaxial regrowths, and to focus on processes that could be performed with vendor growth and implant facilities so that only basic clean room processing facilities are required.

Index Terms—Photonic integrated circuits (PIC), quantum-well intermixing (QWI), tunable lasers, wavelength converters.

I. INTRODUCTION

HIGH-PERFORMANCE large-scale photonic integrated circuits (PICs) in InP have recently been created for transmitter, receiver, wavelength-conversion, and

Manuscript received July 16, 2010; revised October 24, 2010; accepted December 09, 2010. Date of publication January 06, 2011; date of current version February 07, 2011. This work was supported by the DARPA MTO under various contracts. Device fabrication was done in the UCSB nanofabrication facility, part of the NSF funded NNIN network.

L. A. Coldren is with the Department of Electrical and Computer Engineering and the Department of Materials, University of California, Santa Barbara, CA 93106 USA (e-mail: coldren@engineering.ucsb.edu).

S. C. Nicholes was with the Department of Materials, University of California, Santa Barbara, CA 93106 USA. He is now with Aurion Photonics, Santa Barbara, CA 93117 USA.

L. Johansson, S. Ristic, R. S. Guzzon, E. J. Norberg, and U. Krishnamachari are with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106 USA.

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Digital Object Identifier 10.1109/JLT.2010.2100807

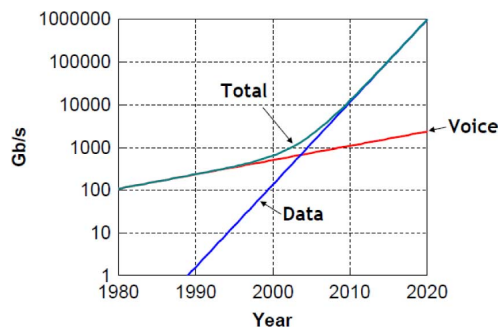


Fig. 1. Network traffic growth.

packet-switching applications [1]–[7]. Applications in coherent transmitters and receivers as well as in signal-processing circuits are also being explored [8]–[11]. Integration provides a reduction in system footprint, inter-element coupling losses, packaging cost, and usually power dissipation, as a single cooler can be used for multiple functions. Although yield issues must be addressed, reliability appears to improve once such issues are, because reliability is often related to packaging or other external factors once the inherent semiconductor failure mechanisms are satisfied [1], [2].

Other motivations for photonic integration include the desire to eliminate or reduce the number of expensive and power-consuming optical-to-electronic-to-optical (OEO) conversions by performing some of processing in the optical domain. The simplest example might be optical amplification; more complex examples include tunable transceivers and wavelength converters [4]–[6], [12], [13] and all-optical switching and routing chips [3], [14].

In order to justify the cost of designing the chip and refining the fabrication technology for a single unique PIC, however, one must assume some significant volume for the chip that is being produced. Otherwise, the cost might be difficult to recover. This can be somewhat ameliorated by chip designs that use exactly the same process, so that multiple chips can be placed on the same wafer, and produced simultaneously. In practice it seems that both issues are important to address. That is, generic design rules should be developed that can be used for a wide variety of PICs, and reasonable production volumes need to be identified. Production volumes might also be increased by trying to define a few general purpose PICs that can be used in a number of applications by a wide number of users.

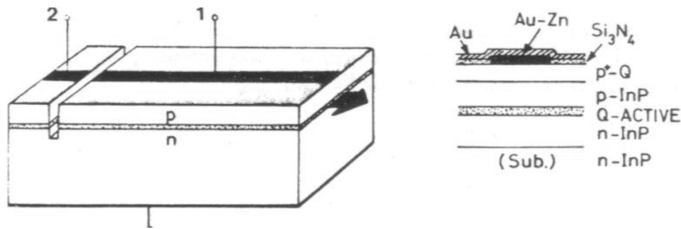


Fig. 2. Two-section etched-groove laser formed by RIE.

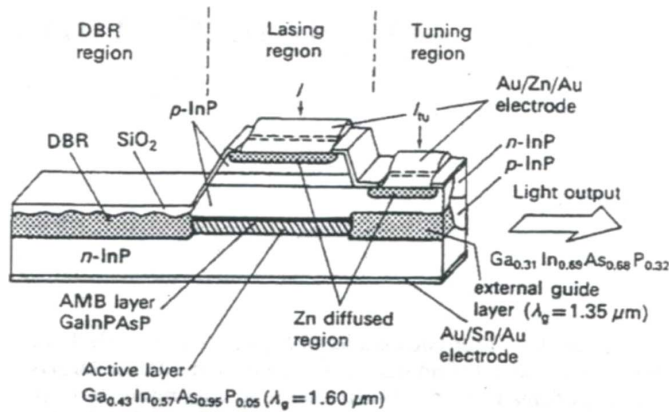


Fig. 3. Tunable DBR laser that also employed vertical coupling.

The demand for PICs has been aided by the significant increase in network traffic in recent years as indicated by Fig. 1. The bandwidth on the optical fiber network is now growing by two orders of magnitude per decade due to the tremendous increase in data transmission. Some years ago, when efforts on photonic integration began, network traffic was only growing by a factor of ~ 2.2 in each decade.

II. EARLY WORK

Work on the InGaAsP/InP materials system was still developing in the early 1980s when some of the first efforts to monolithically integrate multiple elements together appeared. Fig. 2 illustrates an early tunable two-section laser effort that used an etched groove as a partially transmissive mirror between the sections [15]. Such etched grooves provide a very compact mirror, but due to difficulty in reproducibly fabricating them, they were replaced by gratings for most applications. Recently, however, more work is reappearing on etched grooves using improved etching technology [16].

Fig. 3 shows some of the first integration of active and passive sections using distributed Bragg reflectors (DBRs) in the InP system [17]. Multiple-regrowths were employed, and tunable single-frequency lasers were demonstrated, although with a very modest amount of tuning. The DBR work continued as an integration platform, but most of the work with grating devices began to focus on distributed feedback (DFB) lasers in which the grating is formed along the active region.

Fig. 4 shows an electroabsorption-modulated laser (EML), first produced in the mid 1980s, but similar to those in production today [18]. It indicates the use of the preferred single-frequency DFB laser together with the integrated EA-modulator that uses the absorption shift of the bandedge with a reverse

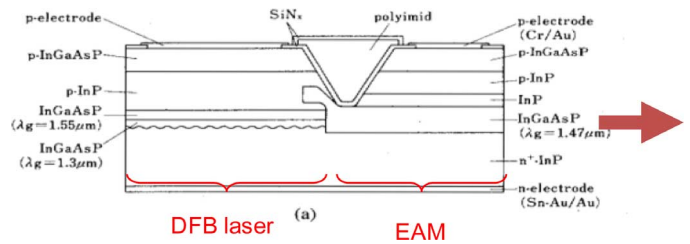


Fig. 4. Early EML using DFB butt-jointed to EAM.

bias. It also uses a butt-joint regrowth step to form the modulator next to the laser. Such EMLs are also formed by numerous other active-passive integration technologies [19], [20].

Coherent technology was being widely explored in the 1980s because of its promise of increased transmission distance that should result from improved receiver sensitivity [21]. Er-doped fiber amplifiers (EDFAs) [22] had not been developed, and wavelength division multiplexing (WDM) was not very cost competitive because of the cost of WDM repeaters. These involved de-multiplexing and converting all of the wavelengths into the electrical domain, amplifying, demultiplexing again to a lower data rate, regenerating, multiplexing up to the higher data rate, modulating the information back onto different optical wavelengths, and multiplexing these back into the fiber again. Indeed, a complex and costly system that didn't compete well with simply increasing the data rate or even adding more fiber.

Thus, coherent approaches, which promised to perhaps double the repeater separation were very interesting, and they also offered the possibility of placing the WDM channels closer together, because the channel filtering would be done by a fixed IF filter in the RF-domain after heterodyne down-conversion by tuning the optical Local Oscillator (LO), much as in a radio.

However, making an optical heterodyne receiver was quickly found to be very difficult to make stable using bulk components. But, if the components could be integrated on a single chip, perhaps many of the difficult issues would be solved. Thus, some efforts were initiated to explore this possibility. Fig. 5 illustrates the most successful of these [23]. It includes all of the optical components of a coherent receiver, including an integrated LO laser, a 3 dB coupler, and a balanced detector pair.

Although the results from the chip of Fig. 5 were not extremely impressive, it did set a milestone on what could be accomplished by using photonic integration. Unfortunately, the work on PICs for coherent did not progress too much further than this, first because of an economic slow-down in the 1990 timeframe, and then second, because of the appearance of the EDFA and improved optical multiplexers. These two technologies enabled practical WDM systems to expand to many wavelengths without the need to de-multiplex down to individual channels for electronic regeneration every 30 km or so. Thus, by the mid 1990's dense WDM was being rapidly deployed [24] and work on coherent was being terminated.

Both the coherent work and that on WDM identified a need for tunable lasers. For coherent, one desired local oscillators that could tune across the desired optical wavelength range of the receiver [25]. For WDM, universal sources [26] that could

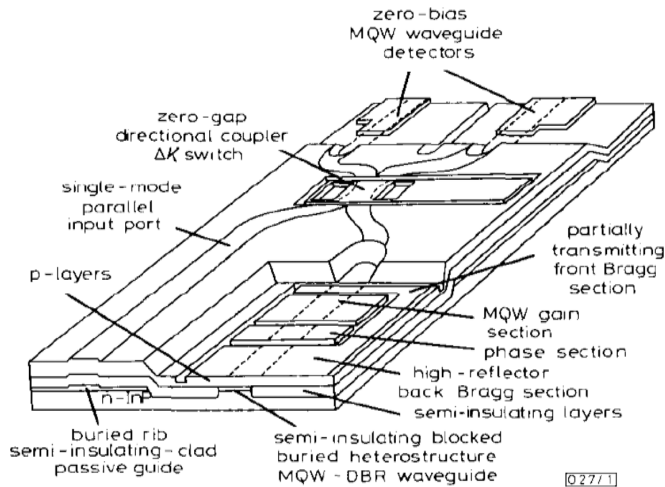


Fig. 5. Integrated coherent receiver chip.

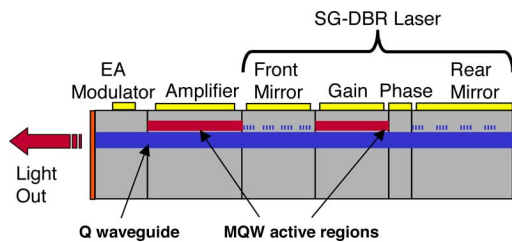


Fig. 6. Schematic of SG-DBR laser integrated with a semiconductor-optical-amplifier (SOA) and EAM.

output any channel wavelength across the C-band—the central band of the EDFA used by fiber optic networks—were desired. Thus, so-called ‘widely-tunable’ lasers were desired—ones that could tune across 40 nm or more near 1550 nm. Such lasers were also desired in various sensing applications where the resolution was proportional to the wavelength span [27].

Therefore, beginning in the 1980s and throughout the 1990s there was a lot of work on tunable lasers that continues even to this day [28]. The widely-tunable lasers became especially popular during the ‘telecom bubble times’ near the turn of the century. Many companies were formed, and some were successfully acquired, but only a few of the original technologies continue to be produced today. One of these, the sampled-grating DBR (SG-DBR) laser [29], as depicted in Fig. 6, is still at the heart of some products of the JDS-Uniphase Corporation [30].

This single-chip widely-tunable SG-DBR laser, which contains gain, phase-tuning, absorber and mirror sections, integrates many of the basic building blocks needed in many more complex PICs. It utilizes two multielement (sampled) Distributed Bragg Reflector (DBR) mirrors to provide two differently spaced multi-peaked reflectors, so that only one peak from each mirror can line up for a particular current injection. As the currents into the mirrors are varied, different combinations of individual mirror peaks (typically spaced by 6 or 7 nm) can be brought into alignment to extend the tuning range over a number of (~ 7) bands.

In fact, since this laser was invented at UCSB [31], it became the starting point for much of the InP-based PIC work that has

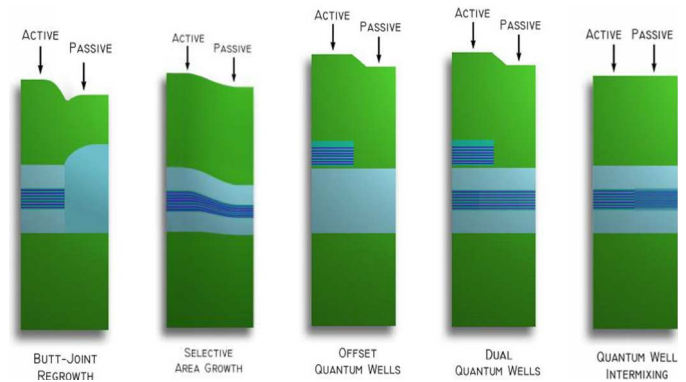


Fig. 7. Active-passive waveguide integration approaches.

been carried out at UCSB over the past two decades. As illustrated in Fig. 6, an amplifier and electro-absorption modulator can be added external to the laser cavity by simply adding another gain section and passive section (same as phase-tuning section) along the same waveguide during the same fabrication process. For the EAM, the terminal is reverse biased to provide a reduction in the bandgap, and thus add absorption, whereas for the phase-tuning section, the terminal is forward biased to inject carriers into the waveguide, thereby reducing the index of refraction to tune to laser wavelength to smaller values.

Of course, additional elements are needed for some of the PICs to be discussed, but in most cases, these can be added without adding significant processing complexity. Generally, the integration philosophy at UCSB has been to avoid patterned epitaxial growths, to use post-growth processing, such as quantum-well intermixing to provide multiple bandgaps, rather than multiple epitaxial regrowths, and to focus on processes that could be performed with vendor growth and implant facilities so that only basic clean room processing facilities are required.

III. BASIC INTEGRATION TECHNOLOGY

A. Active-Passive Axial Waveguide Integration

Fig. 7 illustrates five different approaches to integrate regions with different absorption/gain properties together along a single waveguide. As these have been discussed previously in some detail [32], [75], we here will only focus on the right-most three that have been the object of most of our work. All of these can be formed with a single ‘blanket’ regrowth of semiconductor cladding, which does not involve any foreign masking material on the wafer surface to define the epitaxial growth dynamics as do the two left-most approaches. In fact, we have been successful in having these blanket regrowth steps done by multiple vendors with minimal development effort.

Although we have previously [4] also included some discussion of the active-passive platforms that do not require even this type of simple regrowth, we have dropped the explicit discussion of approaches such as the vertical active-passive twin guide [33] here because of the large transition distances that are involved, and the resulting incompatibility with multiple active-passive interfaces desired in a high-functionality PIC. Single-material waveguide PICs are also similarly not considered because of the extreme limitations on their performance

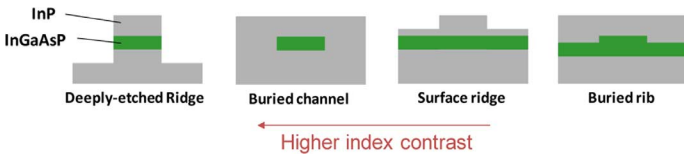


Fig. 8. Lateral waveguide choices.

and functionality. To summarize, the issues with regrowth that these approaches sought to avoid are avoided with our unpatterned blanket regrowth approach without making most of the compromises.

However, although it requires a patterned regrowth, it should be pointed out that the butt-joint approach does provide the maximum flexibility in choosing the properties of the two waveguide sections, as the properties of one can be almost totally divorced from the other, aside from the need to be nominally latticed-matched to InP. Thus, this approach is often used when no compromise in waveguide properties can be tolerated. Nevertheless, there is a price to pay in fabrication complexity, compatibility with other structures across a large PIC, and ultimately design flexibility and yield in using such patterned-growth processes.

The ‘offset quantum-well’ configuration and its close cousin, the ‘dual-quantum-well’ active-passive geometry are both fabricated by an unpatterned regrowth of the upper cladding on a base wafer, which has had regions of the MQW-active region formed on top of a common waveguide removed where passive waveguides are to be formed. The dual-quantum-well approach has been used to enhance the performance of modulator sections placed in the ‘passive’ regions [34].

The ‘quantum-well-intermixed’ (QWI) active-passive configuration [32], [75] is similarly fabricated with an unpatterned cladding regrowth, but in this case the common waveguide contains the MQW-active region, and the bandgap of the MQW region has been selectively increased by a patterned implant and one or more annealing steps to selectively intermix the quantum-well barriers and wells in regions that are to become passive, or perhaps modulator sections, if the shift is not as large. Shifts saturate ~ 100 nm in the 1550 nm InGaAsP materials and are easily controlled. Intermediate shifts, as for modulators, require careful calibration. The intermixing must also be done in the absence of other rapidly diffusing species in the wafer, such as zinc. Thus, as will be detailed in Section IV.D, QWI must be completed before a zinc-doped p-cladding is regrown.

In all cases the interfaces between the active and passive regions are slanted with respect to the axes of the waveguides that will be eventually formed to prevent reflections back along the waveguide.

B. Lateral Waveguide Choices & Mode Transformers

In order to complete the waveguides after their active-passive nature is decided along a particular length, some lateral waveguiding geometry must be defined. Fig. 8 illustrates four possibilities.

As indicated, they are arranged from the strongest waveguiding on the left to the weakest on the right. Correspondingly, the waveguide loss tends to go in the opposite direction, with the higher-contrast guides having the higher losses, assuming

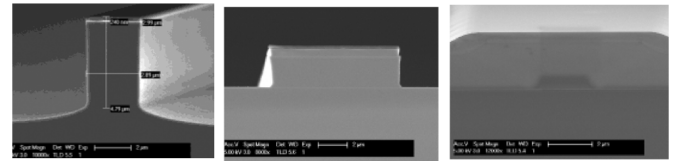


Fig. 9. SEMs of deeply-etched ridge, surface-ridge, and buried-rib waveguides. Deep ridge is formed by ICP dry etching; surface-ridge by HCl wet etching; and buried-rib by dry etching followed by regrowth.

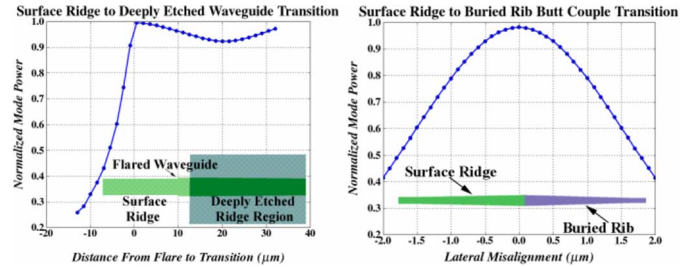


Fig. 10. Lateral waveguide transitions. Relative power coupled versus distance from flare (surface-ridge/deep-ridge—left), or versus lateral misalignment (surface-ridge/buried-rib—right).

similar surface roughness. This is also related to the fact that the stronger (higher-index-contrast) waveguides need to be smaller for single-mode operation.

The deeply-etched ridge and surface-ridge types can be formed after epitaxial growth, whereas both the buried channel and buried rib must be defined prior to epitaxial regrowth. Dependent upon the type of active-passive technology used, this may require a special regrowth. Fig. 9 shows SEM cross sections of all but the buried channel type.

The surface-ridge waveguide has been a relatively popular choice in the InGaAsP/InP system, both because of its ease of fabrication and the fact that crystallographic wet etches can be used to provide very smooth side walls along some directions in InP. For example, an InGaAs contact layer can serve as a mask for a strong HCl etch, which provides very smooth side walls for InP-clad waveguides aligned with the $\langle 011 \rangle$ direction, and it will stop-etch on a quaternary waveguide layer [35]. However, this technique is not useful for waveguide orientations more than a few degrees off of the $\langle 011 \rangle$ direction.

For the deeply-etched ridge as well as most of the other waveguide types, dry-etching is generally used. Better pattern transfer is possible, and orientation dependencies are not as severe.

A major issue to be addressed if two or more of the different lateral guides are to be used on the same PIC is transitioning between them along some waveguide path. Fig. 10 gives simulated data and schematics for waveguide transitions between surface-ridge to deep-ridge and surface-ridge to buried rib guides [14]. As illustrated, in the first case the surface ridge flares and tapers before the deep ridge section [36]. In the second case, the surface ridge flares and butt couples to a tapering rib section.

The other significant type of mode transformation that must be considered is that in coupling the PIC to a fiber. In this case the general problem is transforming the mode from an elliptical shape to a round one as well as increasing its diameter. We will

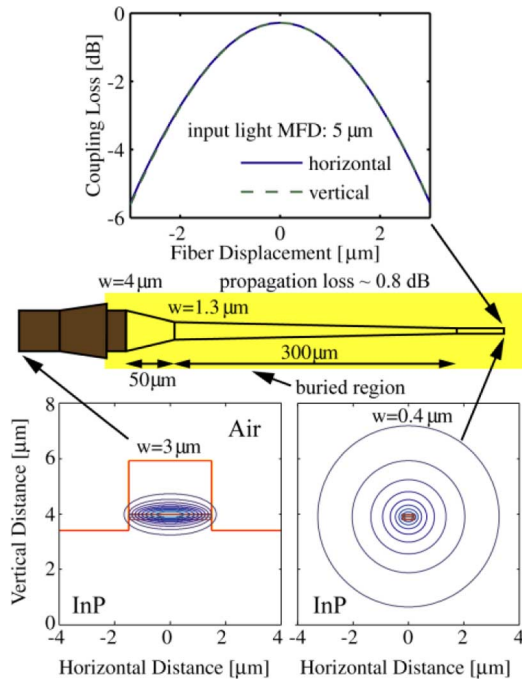


Fig. 11. Compatible mode transformer design. Top—coupling vs lateral fiber displacement; middle—topview illustrating lateral taper; bottom-left—initial waveguide and mode cross section; bottom-right—final waveguide and mode cross section. The detailed material layer structure for these simulations will be given in Fig. 27.

not consider butt-coupling to a fiber because that would require too much mode expansion, but if the mode can be transitioned to a circular cross section and increased in diameter by two or three times, we have found that the coupling loss to simple lensed fibers can be reduced from the typical ~ 5 dB to <1 dB.

Fig. 11 shows schematics of waveguide tapers as well as the theoretical mode shapes and resulting coupling losses for one mode transformer concept that can be incorporated into our blanket regrowth platform.

C. Other Waveguide Elements

Waveguide couplers and splitters are other important elements in Photonic ICs. Multimode interference couplers have become the most popular way to make 1×2 and 2×2 splitters because the waveguides are separated at the inputs and outputs and critical “Y-junctions” are avoided. Fig. 12 illustrates a design example for a 2×2 coupler.

However, such standard MMI designs can become relatively large, and if one desires a more compact design, it is possible to collapse the structure by reducing the width and waveguide spacing, in effect approaching a zero-gap directional coupler. Fig. 13 illustrates a 3 dB coupler in which the coupling length is only 45 μm [37].

Another interesting and useful coupler is one with variable coupling. In order to obtain a very large range of coupling values, one approach is to use a miniature Mach-Zehnder modulator as the variable coupler [38]. Fig. 14 illustrates this. Here two 3 dB MMI 2×2 couplers are separated by intermediate phase modulated delay lines. When the phase of the delay lines is adjusted, the output power alternates between the two output waveguides. As can be observed nearly full extinction is

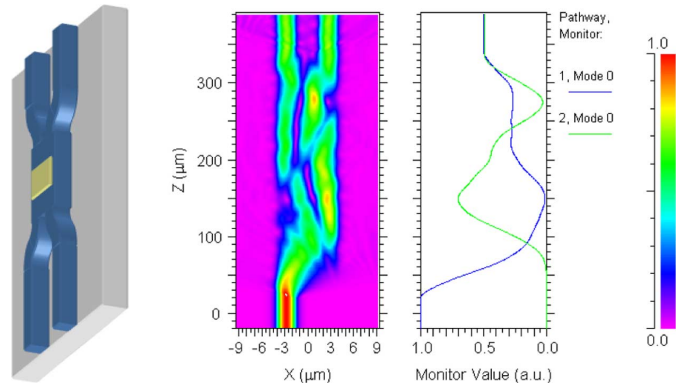


Fig. 12. 2×2 MMI design example. Schematic on the left; intensity distribution in center (keyed at far right); and plots of net power that would be transmitted if the MMI were terminated at the indicated length. Illustrated finally is a single input being split equally to the two outputs.

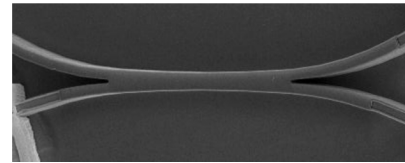


Fig. 13. SEM of compact 3 dB MMI coupler design. Waveguide width is 2 μm and coupling length is 45 μm .

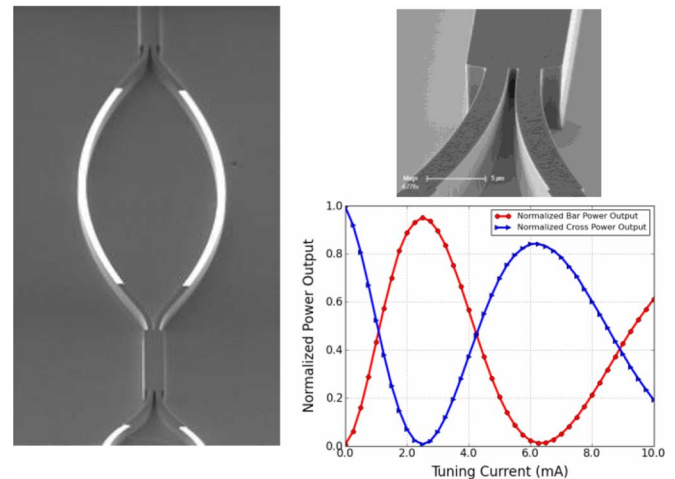


Fig. 14. SEM of variable directional coupler; blow-up of input to MMI; plots of relative output power to the two output ports.

possible on either output. Such couplers are especially useful in filter design [39].

A Star coupler may be viewed as simply using a free-space region to enable one of several input guides to equally illuminate a number of output waveguides [40]. It can also be analyzed via the multimode interference technique. Fig. 15 illustrates a STAR coupler with 8 input and 34 output waveguides. This figure also shows a second device called an arrayed waveguide grating router (AWGR) [41], [76]. It is formed by placing a mirror-image STAR coupler at the opposite ends of the output waveguides of a first STAR coupler once the intermediate waveguide lengths have been adjusted to vary linearly across the array. With such a design the device becomes dispersive in wavelength and can function as a wavelength multiplexer or

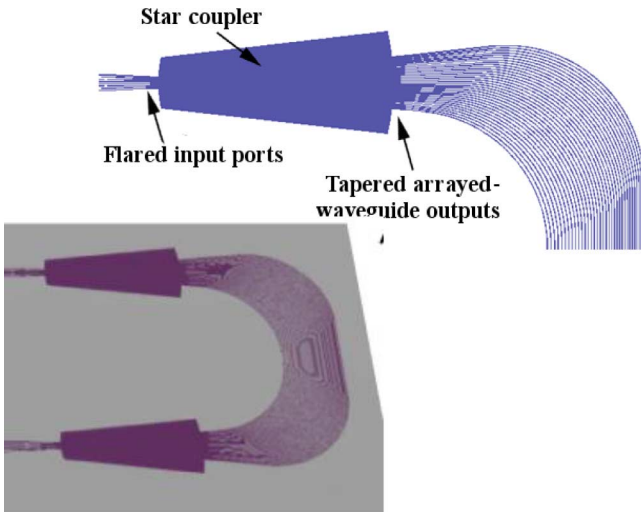


Fig. 15. 8 × 34 STAR coupler (top) and 8 × 8 AWGR (bottom).

de-multiplexer in a WDM system [42], [43], and with multiple inputs such AWGRs can also serve as a wavelength-controlled switching fabric, since the wavelength at the input determines to which output the power will be switched. In a later section an array of wavelength converters integrated with an AWGR on a single chip to demonstrate this kind of switching architecture will be described.

IV. TOWARD MORE COMPLEX PICS

A. Motivation

As indicated in Section II, by the mid 1990s EDFAs and improvements in wavelength multiplexers were enabling the rapid expansion of WDM technology. Dozens of wavelengths could be sent over hundreds of kilometers at 2.5 Gb/s per channel without the need to demux down to single channels and regenerate in the electrical domain at lower data rates. This expensive OEO every 30 km or so could be avoided. Tunable lasers were on all of the roadmaps, because universal sources were needed, and other applications were being proposed. Wavelengths on fiber became channels between nodes.

One problem that quickly arose was that as some wavelengths on some fibers became fully utilized, it was desired to change the information to another wavelength, but this meant OEO, because there was no other way to do this. So researchers began to look at means to do ‘wavelength conversion’ without the need to convert every bit of information into an electrical bit at some lower data rate and then convert it back up to the optical domain at a different wavelength again. Thus, research on optical wavelength conversion also began in the mid 1990s [44].

At about the same time, it was realized that if one could change the wavelength of the optical data, one could also use a passive device, such as the newly devised AWGR to physically switch the data from one port to another, or from one fiber to another. Thus, still another set of ideas were generated in this direction [45].

At UCSB, as we were doing leading research on widely-tunable lasers necessary for useful wavelength converters and such

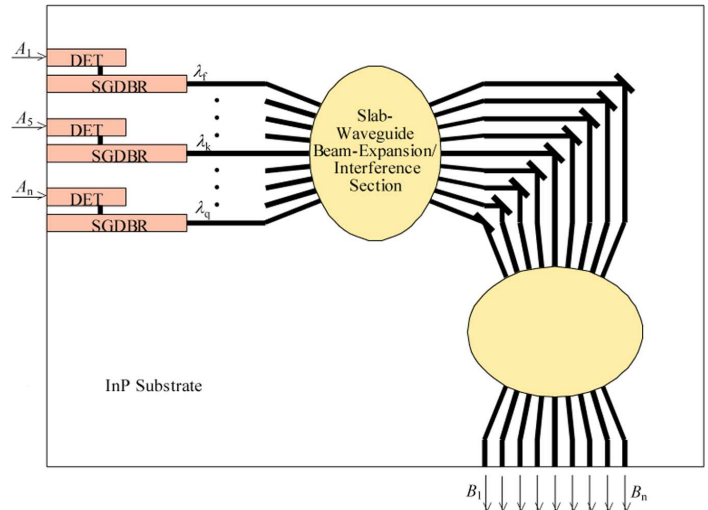


Fig. 16. Crossbar switch using an array of wavelength converters as the active switching elements feeding an AWGR, which acts as the passive switching fabric.

crossbar switches, we quickly got involved in these new directions, and proposed research on a monolithically integrated space switch based upon integrating an array of wavelength converters with an AWGR. Fig. 16 is taken from the original proposal to AFOSR in 1995 [46]. Significant features included novel wavelength converters consisting of SGDBRs directly-modulated by integrated photodiodes and a compact AWGR using corner reflectors in the waveguide array.

The chip illustrated in Fig. 16 set about a number of years of research at UCSB. Most work on wavelength conversion at that time was using isolated SOAs [47], which consumed a lot of power and the results were not very impressive. These did not seem suitable for integration. This was the main reason we decided to go the route of integrating a detector that could directly drive the gain region of the laser. Our initial proposal included ideas about using avalanche photodetectors (APDs) for gain in the detector or ‘gain levered’ active regions in the SGDBR. Soon we realized that SOA preamplifiers as well as SOA post-amplifiers, as illustrated in Fig. 17, could be made to be fairly efficient, so these were also included in our designs [48], [77].

As the research continued over several years the desired data rate for such wavelength converters and crossbar switches increased to 10 Gb/s, and then even to 40 Gb/s. Thus, the directly-driven approach of Fig. 17, was clearly inappropriate. It also tends to distort the signals, so external modulation approaches were soon found to be necessary. In fact, the work with a photocurrent-driven Mach–Zehnder modulator integrated with an SGDBR was published in the same time period [50] as the work in Fig. 17, as were the efforts to integrate nonlinear SOAs in the arms of Mach–Zehnder modulators with direct optical injection into them [51].

Whether to use photodetectors driving modulators or directly inject the input optical signal into SOAs, which are within a modulator configuration for wavelength conversion still remains a topic of research [52]. The PD-modulator approach appears to require less real estate and power, and no filters are required to remove the input signal, but the nonlinear SOA approach is

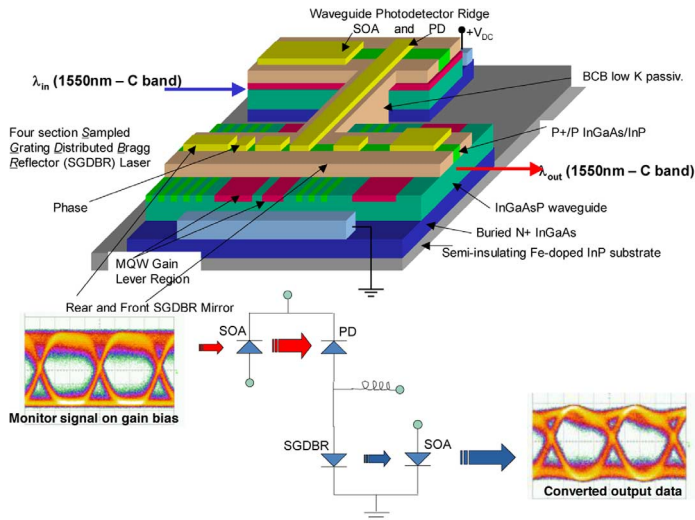


Fig. 17. Directly-driven SOA-PD/SGDBR-SOA wavelength converter. Schematic and equivalent circuit, including eye patterns from input and output data at 2.5 Gb/s [49].

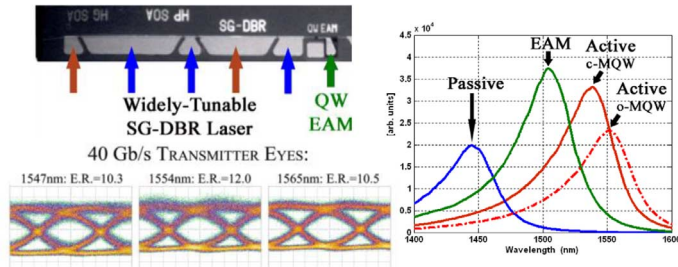


Fig. 18. QWI-based widely-tunable 40 Gb/s transmitter [52].

somewhat simpler to fabricate and may have higher yield in arrays.

B. Transmitters, Wavelength Converters, and Other Mostly-Serial Integration Efforts

Three more recent high-performance PIC efforts centered around SGDBR widely-tunable lasers will be briefly reviewed in this section. Then recent results with lattice filter PICs will be introduced. The first laser-based result illustrates the use of a quantum-well intermixing (QWI) integration platform for a 40 Gb/s SGDBR-EAM transmitter, while the second two use the dual-quantum-well platform to demonstrate wavelength conversion at rates up to 40 Gb/s using direct photocurrent drive of either traveling wave EA or Mach-Zehnder modulators.

Fig. 18 gives results for the QWI-based 40 Gb/s SGDBR/EAM transmitter [53]. As indicated by the photoluminescence plots, the initial unshifted PL peak at 1540 nm is shifted by about 35 nm for the EAM and by about 95 nm for the other ‘passive’ regions of the device, which also include the tuning sections of the SGDBR. This dual shift is accomplished by two annealing steps; the second is performed after removing the implanted material that supplies the diffusing vacancies from above the modulator region. (The ‘o-MQW’ photodetector region is not used in this device.)

For the 175 μm long EAM of the test device, the 3 dB bandwidth was 32 GHz, and the modulation efficiency was about

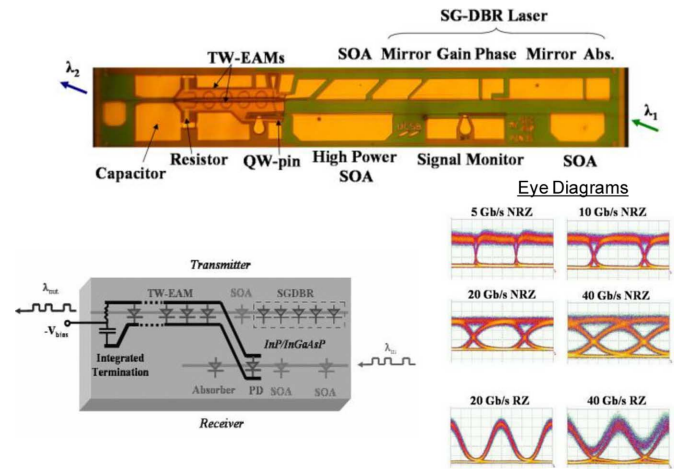


Fig. 19. Widely tunable, traveling-wave PD-EAM wavelength converter transparent to data format and bit rate. Photo, equivalent circuit, and eye diagrams from 5 to 40 Gb/s [12].

20 dB/V over the 1536–1560 nm range, provided the DC bias was properly adjusted at each wavelength. The rf modulation was fixed at 2.5 V peak-peak for all wavelengths, and this provided >10 dB extinction (E.R.) for the 40 Gb/s eyes shown from 1547 to 1565 nm.

Fig. 19 illustrates an integrated optical wavelength converter that can also function as a transceiver, if the receive and transmit stages are operated independently. It integrates an all-photonic SOA-PIN receiver with an SGDBR-traveling-wave-EAM modulator [12]. The by-pass capacitor and termination resistor are also integrated, so it can be operated without any external rf connections.

The all-photonic receiver includes a two-stage SOA preamplifier that incorporates both high-gain and high saturation power stages prior to a high-saturation power PIN photodiode. A signal monitoring port is also available. For wavelength-converter operation as depicted, a transmission line directly connects the photodiode to the velocity-matched traveling-wave EAM stage.

For the device characterized in Fig. 19, less than 2 dB of power penalty was observed across a wavelength span of 1548 to 1560 nm for all data rates and either RZ or NRZ modulation. A termination resistance $\sim 25 \Omega$ led to about 1 dB of peaking in the optical-to-optical response in the 10 GHz range and a 3 dB bandwidth ~ 30 GHz. Input levels were ~ -4.5 dBm, and the output power varied from -6.0 to -4.0 dBm across the wavelength range, so the device had near zero optical conversion loss. Extinction ratios were in the 7–8 dB range. Overall power dissipation was ~ 1 –1.5 Watt range, dependent upon the tuning current to the SGDBR mirrors at these conditions.

The second photocurrent-driven wavelength converter example is shown in Fig. 20. In this case a series-push-pull configured Mach-Zehnder (MZ) modulator follows the SGDBR in the transmitter section [13].

Use of the Mach-Zehnder modulator enables better chirp management compared to the EAM designs. A negatively chirped output can compensate for some of the natural fiber dispersion and extend the transmission distance. Transmission

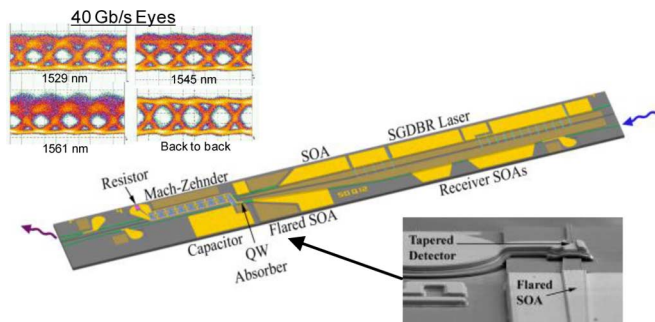


Fig. 20. Widely tunable PD-MZ wavelength converter. Eyes from 1529 to 1561 nm, schematic, and SEM of flared high-saturation power SOA-PD region [13].

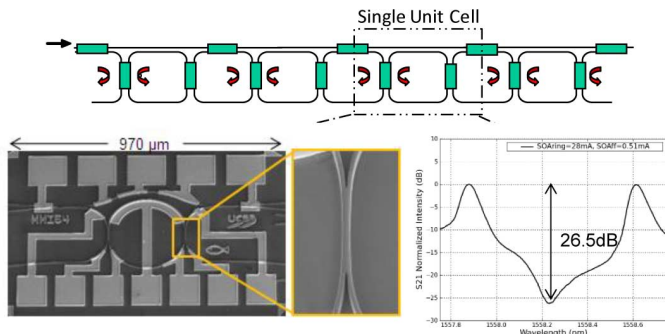


Fig. 21. Programmable lattice filter schematic and SEM of fabricated unit cell with expanded view of compressed MMI coupler. Data illustrates one of many possible filter responses from a single stage [55].

up to 60 km was demonstrated with 2 dB power penalty at 10 Gb/s.

For the reported results, a termination resistor of 25 Ω was used, and less than 2 dB of power penalty was observed over the wavelength range. The output levels were ~ -7 dBm for inputs ~ -4 dBm.

The remaining example of a PIC that employs mostly serial integration is the programmable lattice filter element shown in Fig. 21. In this case no lasers are present, but it is desired to rapidly tune and reconfigure the characteristics of complex optical filters, so the filter does include a number of SOAs, phase shifters, and couplers, which in some cases may be variable couplers.

Such filters may be interesting for adaptive dispersion control or equalization, but they appear to attract most interest as agile pre-filters for signal-processing applications. Fig. 21 shows a possible serial lattice configuration as well as an SEM of one unit cell of the proposed lattice filter [37]. The experimental result superimposes a zero resulting from the Mach-Zehnder response of the upper and lower branches with two adjacent poles of the ring resonator within the lower branch.

The filter passband is tunable over >100 GHz, and more recent examples have illustrated flat-topped bandpass characteristics, which result from coupling several stages together, programmable both in bandwidth and center frequency [54].

C. Multichannel PICs and Other Mostly Parallel Integration Efforts

The work emphasizing the parallel integration of a number of channels appeared in the mid 1990s with the emergence of

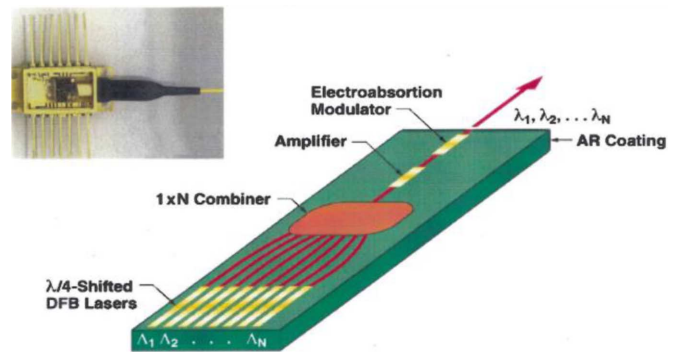


Fig. 22. Wavelength selectable laser employing quarter-wave shifted DFBs and a 1/N combiner together with an SOA and an EAM [55].

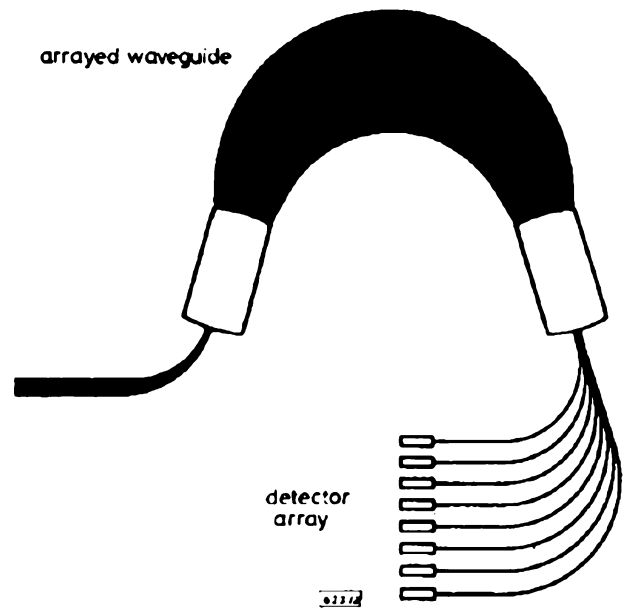


Fig. 23. 8-channel receiver incorporating AWGR and PIN detector array with 2 nm channel spacing [42].

WDM. Fig. 22 shows a wavelength selectable laser [55], and Fig. 23 shows a multi-wavelength receiver [42]. The wavelength selectable laser, which employed a simple Star coupler with a 1/N splitting loss, later evolved into a multi-channel transmitter by incorporating an EAM with each laser together with a low-loss multiplexer such as an AWGR.

The wavelength selectable laser in the form shown competed with widely-tunable lasers, such as the SGDBR, by also using heating and cooling of the substrate to thermally tune the wavelength of the laser array to cover the wavelength ranges over the gaps between the room temperature values of the array, $\Lambda_1, \Lambda_2, \dots, \Lambda_N$. Thus, eight or ten DFB lasers arrayed in this way might be able to cover over a 100 WDM channels using this approach. Such lasers are still being used in WDM systems today [56].

Figs. 24 and 25 illustrate commercial PIC designs of Infinera that have been available in their products for several years. Shown are the PICs contained in their ten-channel 10 Gb/s transmitter and receiver modules, respectively [57]. As can be seen the transmitter PICs consist of a parallel array of ten DFB laser-based transmitter elements that feed an AWG multiplexer.

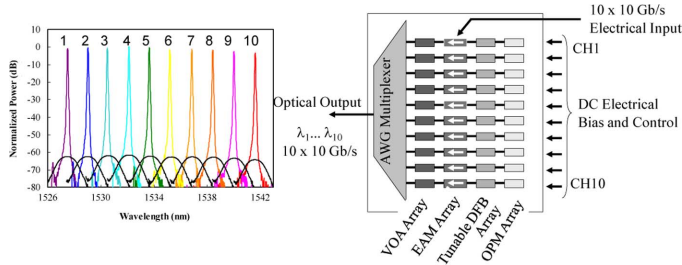


Fig. 24. Schematic and output spectra of Infinera 10×10 Gb/s transmitter PIC.

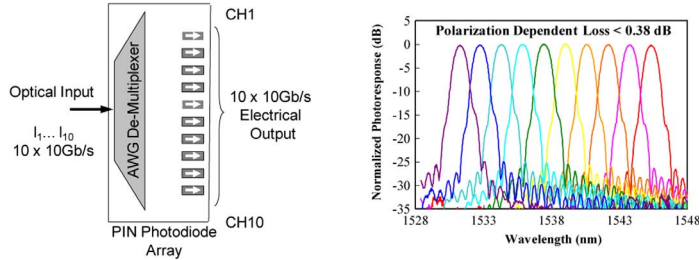


Fig. 25. Schematic and superimposed response of the ten photodetectors as an input signal is swept across the wavelength band for the Infinera 10×10 Gb/s receiver PIC.

Each transmitter element contains a DFB laser that can be tuned by a small amount, an EA-modulator, a variable optical attenuator (VOA) to adjust the output power level, and an optical power monitor (OPM) behind the DFB.

Infinera has also demonstrated analogous 40×40 Gb/s research results [58], and more recently, ten-channel polarization-multiplexed differential-quaternary-phase-shift-keying (PM-DQPSK) transmitter and receiver PICs operating at 400 Gb/s for coherent communications [59]. These latter results will be reviewed in Section V below on Coherent PICs.

D. Serial/Parallel Integration—The MOTOR Chip

Some researchers and analysts have viewed the world of photonic integration as a complex plane with two axes: one labeled serial integration, the other parallel integration. Thus, one might choose to try to locate any particular PIC as some point in this plane, dependent upon how much serial versus parallel integration technology it contained. For example, the transmitter PICs of Figs. 6 and 18 might be considered entirely serial, the wavelength converters of Figs. 19 and 20 mostly serial with just a little parallel (a transmitter and receiver in parallel), and the transmitter and receiver PICs of Figs. 23 and 24 as mostly parallel with a little bit of serial.

Now more controversially, some have even argued that serial is more interesting than parallel integration. After all, parallel is just putting a lot of the same thing side by side, and this is what one always does when using semiconductor planar-processing technology. Needless to say this latter statement is a little naïve, because in mostly parallel PICs the parallel channels are not quite the same, they all have to work, and they ultimately are all coupled together in some way. Nevertheless, we are amongst those who argue that serial integration is more interesting and sophisticated than parallel, mostly because we have tended to do more of it.

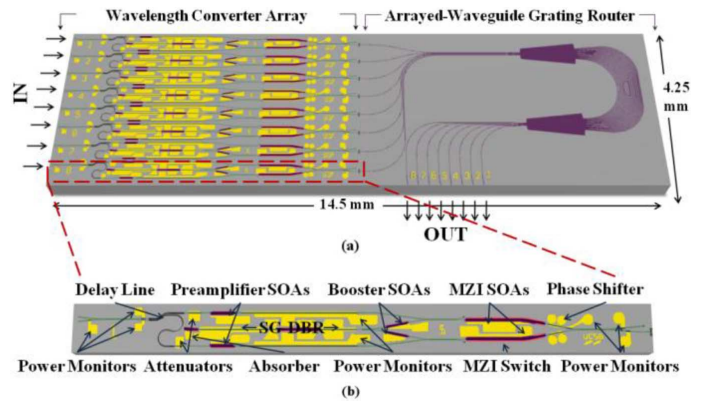


Fig. 26. Wavelength switched 8×8 crossbar switch/router: (a) MOTOR chip and (b) element of the wavelength converter array with various components labeled.

In what follows we present a compromise position, a device that has a large amount of serial integration but a healthy amount of parallel integration as well. The MONolithic Tunable Optical Router (MOTOR) chip basically has the same architecture as the crossbar chip proposed in Fig. 16, but it is much more sophisticated, it was actually fabricated, and it works at 40 Gb/s [7], [14].

Fig. 26 illustrates both the MOTOR chip and the wavelength converter elements, which in this case are nonlinear-SOA-based wavelength converters. Although not included here, these can include packet header rewrite modulators in each—hence, the designation as a router. Again, an SGDBR laser within each wavelength converter provides the wide tunability of the outputs. The particular SOA-based wavelength converter employed uses a differential modulation technique specific to a ‘return-to-zero’ (RZ) modulation format. That is, the input signal is split, and while one half is used to unbalance the MZ-modulator to allow light from the SGDBR to be emitted, the other is delayed a bit, and then used to rebalance the modulator to turn off the light in order to generate a pulse. The input light changes the index of refraction of the modulator arms by saturating the SOAs, thereby reducing their carrier densities, and increasing the indexes of refraction in these regions.

As illustrated in Fig. 26 the MOTOR chip employed an 8×8 AWGR, as also shown in Fig. 15 above, with 8 wavelength converters receiving 8 inputs and 8 outputs transmitted from the AWGR. The channel spacing was 200 GHz in the 1550 nm range. The AWGR employed waveguide tapers into and out of the Star couplers to reduce coupling losses.

A QWI integration platform was chosen to provide active and passive regions throughout the device. Fig. 27 gives the details of the layer structures following the first and second epitaxial growth steps.

There are actually two different types of ‘passive’ regions where the quantum-wells are intermixed. Both are formed at the same time. For the first, the unintentionally doped (UID) InP implant buffer layer remains (as shown) to separate the optical mode from the p-type doping in the upper cladding in order to minimize optical losses; for the second, this implant buffer layer is removed so that p-n junctions are formed for the modulator

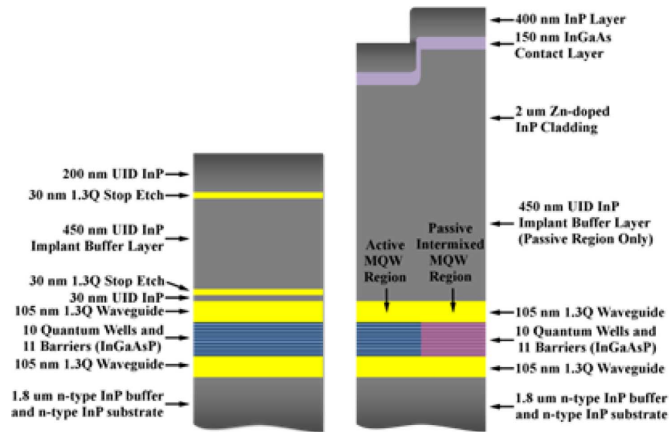


Fig. 27. (a) Initial base epitaxial growth structure. (b) Final growth structure showing both an as-grown active MQW region and an intermixed passive MQW region wherein the implant buffer remains.

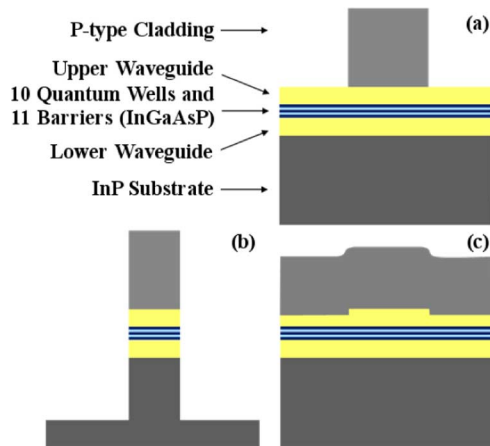


Fig. 28. Waveguide architectures used in the MOTOR chip: (a) surface ridge waveguide; (b) deeply etched waveguide; and (c) buried rib waveguide.

and phase-shift sections. The active sections include all of the SOAs, the absorbers, and the gain regions of the SGDBRs.

As illustrated in Fig. 28, three different lateral waveguiding structures are incorporated within the MOTOR chip. For most of the wavelength converters, including the SGDBRs, the surface-ridge structure is used; for the short 11 ps “S-shaped” differential delay a deeply-etched waveguide was used to enable the sharp bends required; and for the AWGR, a buried-rib waveguide was employed to minimize losses. Importantly, all are formed with only a single ‘blanket’ regrowth step. The UID implant buffer was left on for both the deeply etched and buried-rib regions to further reduce optical losses.

Chlorine-ICP dry etching is used to form the deeply-etched waveguide after regrowth, and methane-hydrogen-RIE is used for the slight etch into the quaternary waveguide for the buried-rib waveguide prior to regrowth. The surface ridge is formed by a combination of an initial ICP etch followed by an HCl-based “clean-up” etch to expose the smooth crystallographic ridge sidewalls as well as stop-etch on the quaternary waveguide.

An example of the MOTOR chip’s operation is shown in Fig. 29. In this case random RZ data at 40 Gb/s is injected into

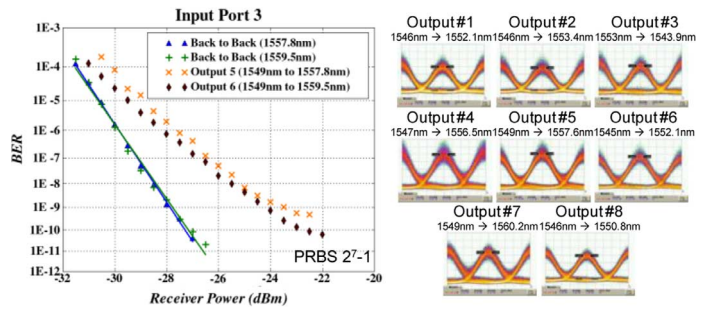


Fig. 29. MOTOR chip BER and output eyes for switching from input port 3 to any output port at 40 Gb/s RZ.

port 3, and this wavelength converter is then sequentially adjusted to translate the data to various wavelengths so that it exits the device at each of its eight output ports.

The bit-error-rate (BER) illustrates some slight pattern dependence that appears to be related to some saturation of the SOA preamplifiers. In other efforts, higher saturation power SOAs have been used [60], and this probably would address this issue. Also no anti-reflection coatings were applied to this device and this might have contributed to some pattern effects. The power penalty was <4 dB @ a BER of 10^{-9} for this case.

Under nominal bias conditions the MOTOR chip consumed about 2 W per channel. The signal insertion loss through the device was ~ 10 dB, the majority of which were due to waveguide transition and AWGR losses. Both of these numbers could be improved with further optimization using results that have been previously demonstrated. For example, at least 2 dB is attributed to each of the Star couplers in the AWGR. Crosstalk values between channels were generally better than -15 dB with the exception of one input port, which appeared to suffer from some defects that lowered its level to about -13 dB.

V. BACK TO THE FUTURE—COHERENT PICs

A. Motivation

Referring back to Fig. 1, it may be apparent that meeting future demand for bandwidth is going to be a continuing challenge. Introductions of new and expanded services, such as HD-TV, Youtube, Facebook, programmed stock trading, and soon 3D-TV, have continued to maintain the extreme 100x increase/decade slope. Fig. 30 overlays some data for fiber capacity on this total demand curve for both research and commercial fiber links [61]. The straight lines indicate trends for commercial systems, which show that the tremendous growth in bandwidth, due to WDM adoption in the 1995–2002 timeframe, has now saturated due to a limitation in the number of practical WDM channels as well as the data rate in each.

To increase fiber capacity further we are now looking to improve the spectral efficiency (SE)—the net bits/s of data rate per Hz of bandwidth, or more simply the channel rate/channel spacing. This is being done with advanced modulation formats and coherent detection—really a step toward making optical communication closer to rf. Fig. 31 gives a set of tables that summarize the system evolution over the past few decades as

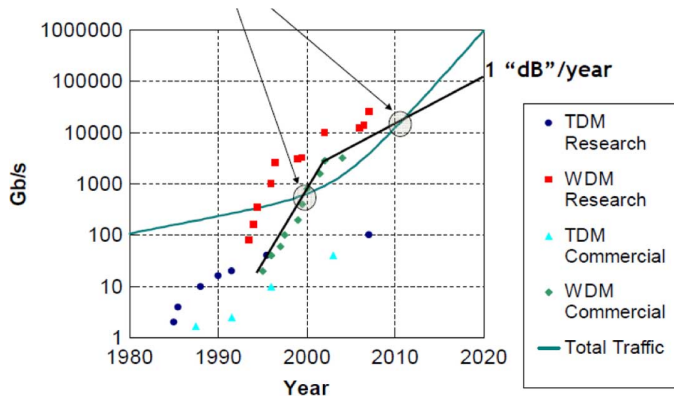


Fig. 30. Growth of research and commercial fiber link capacity data over the total network demand.

| 1990s | 2000 | 2010 | 2020 |
|--------------------------|----------------------|-----------------------|-----------------------|
| 2.5-10 Gb/s channel rate | 10 Gb/s channel rate | 100 Gb/s channel rate | 1 Tb/s ! channel rate |
| 8, 16, 40 Channels | 100 Channels | 100 channels | 100 Channels |
| 20-160 Gb/s Capacity | 1 Tb/s Capacity | 10 Tb/s Capacity | 100 Tb/s Capacity |
| SE = .025-.05 | SE = 0.2 | SE = 2.0 | SE = 20 ! |
| History | History | Planned | Needed |

$SE = \text{Spectral Efficiency} = \text{Channel Rate} / \text{Channel Spacing}$

Fig. 31. System evolution, past and future.

well as what a simple extrapolation might predict for the next [61].

As might be immediately obvious, even with an extrapolation of the current rapid growth in fiber capacity, it does not meet the network demand by 2020, even if doubled or tripled by using the fiber S and L bands in addition to the standard C-band which is plotted in Fig. 30. Even worse, calculations show that we will never be able to reach $SE = 20$ due to limitations in fiber dynamic range because of its limited power handling capacity [62], [78]. An $SE \sim 10$ seems more realistic for transmission distances $\sim 100\text{--}500$ km, typical of WDM systems.

Having set these goals, it should be realized that even reaching $SE = 2$ is nontrivial. Fig. 32 shows a bidirectional link that provides $SE = 2$ by using quaternary phase-shift keying (QPSK) [63]. By adding dual polarization multiplexing (PM-QPSK) this can be doubled to $SE = 4$, but this also doubles the number of components as well as requiring polarization splitters and combiners. The transmitters use a nested pair of Mach-Zehnder modulators (MZMs) following the laser source with one of the outputs delayed by 90 degrees before recombining with the other. The receivers split the signal, and after a 90 degree delay in one leg, combine both with the local oscillator laser in 2×2 couplers which illuminate balanced photodetector pairs. One pair provides the in-phase (I) output and the other the quadrature-phase (Q) output.

B. Recent Telecom Experiments

Infinera has demonstrated the integration of ten QPSK 40 Gb/s transmitters consisting of DFB lasers followed by a

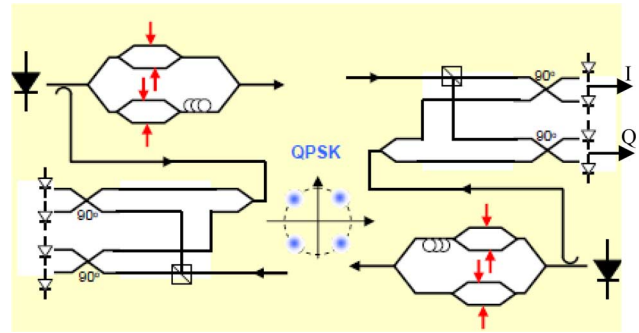


Fig. 32. Bidirectional QPSK link schematic showing transmitter and receiver circuits involved. I and Q outputs available from center of balanced detectors. The QPSK 4-phase constellation is also indicated over the complex plane.

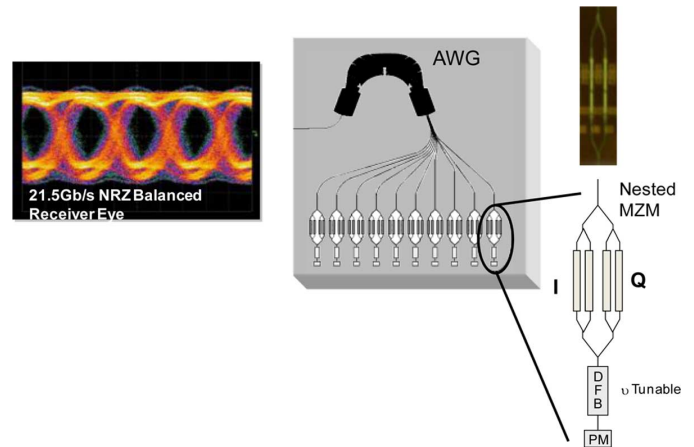


Fig. 33. Infinera 10-channel QPSK transmitter PIC providing 400 Gb/s output together with received eye from one of the two I/Q channels.

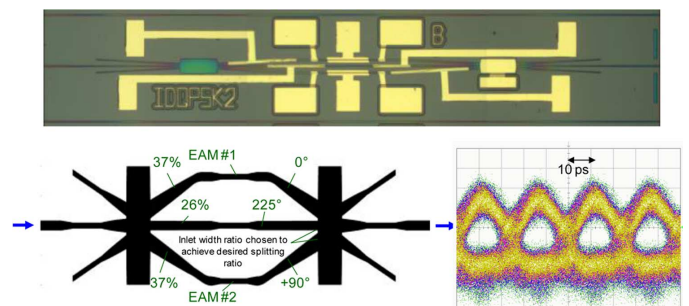


Fig. 34. Bell labs DQPSK modulator photo, schematic, and receiver output.

nested MZM pair together with an AWG multiplexer. Fig. 33 gives a schematic of their chip along with an eye diagram of one of the two received I/Q outputs [59].

Doerr, *et al.*, have also shown that it is possible to use different integrated modulator configurations in addition to the nested MZMs to generate QPSK and even more advanced modulation formats. Figs. 34 and 35 are examples. Fig. 33 shows a DQPSK modulator that uses two asymmetrical STAR couplers together with two EAMs to generate the 4-phase modulated constellation [64]. Also shown is the demodulated result at 20 Gb/s for one of the I or Q outputs.

Fig. 35 shows a 16 QAM modulator ($SE = 4$) integrated on InP also using STAR couplers and EAMs [65].

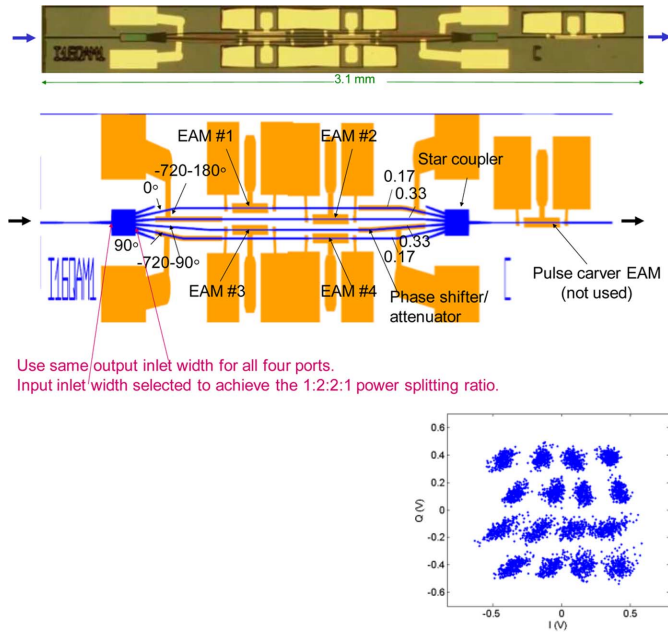


Fig. 35. Bell Labs 16 QAM modulator. Photo; mask layout (stretched); and experimental constellation. 10.7 Gbaud; $2^{15} - 1$; BER(Q) = 9.3×10^{-4} ; BER(I) = very high due to shifting.

Other high-level QAM work has shown 64-QAM results (SE = 6), but with a hybrid LiNbO₃—silica planar lightwave circuit, again with nested MZMs [66]. Much of the recent work on coherent appears to be aimed at reducing the basic data rates being transmitted along the fiber as well as into and out of the links while increasing the transmission spectral efficiency. This enables longer fiber runs before nonlinearities and dispersions of various kinds become problematic as well as somewhat simpler electronics at the ends, even though there are many more parallel elements at the ends.

Fig. 36 shows a PIC transmitter circuit recently presented by Infinera that lowers the basic baud rate to 10 Gbaud, but adds polarization multiplexing to a 10-channel QPSK chip to get back to the 400 Gb/s chip rate [67], similar to that of Fig. 32. This is clearly a fairly complex chip, but it was shown to function on all channels. Also included is the architecture of the doubly nested MZM modulator tree together with a typical characteristic of the InP MZMs employed.

Fig. 37 gives Infinera’s Roadmap for large-scale PIC transmitters on InP [67]. Although there are other competitive data points that could be added from other investigators, they have led in the area of scaling of InP-based highly-parallel transmitter PICs for telecommunications. As can be seen they predict that transmitter PICs will have capacities ~ 4 Tb/s by 2018 or so.

It is worth mentioning at this point that 40×40 Gb/s transmitter and receiver chips were demonstrated a few years ago, as mentioned above [58], but evidently it was found that due to fiber transmission impairments, these were of little use in practical systems. Thus, they do not currently list this 1.6 Tb/s result on their most recent roadmap.

C. Optical-Phase-Locked-Loops (OPLLs) Enabled by PIC Technology

Coherent Receiver for RF Photonics Using Phase-Modulation: Microwave photonic links using intensity modulation tend

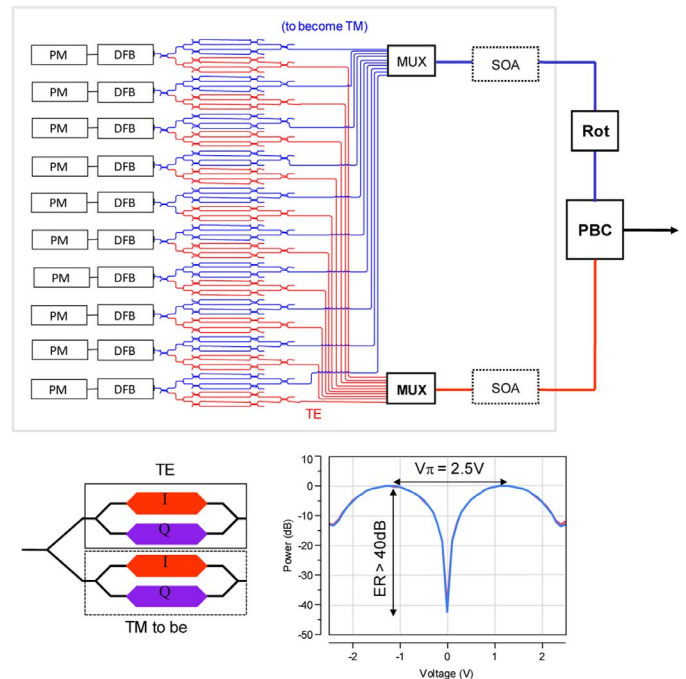


Fig. 36. Infinera PM-DQPSK transmitter chip concept together with a characteristic of the doubly-nested MZMs.

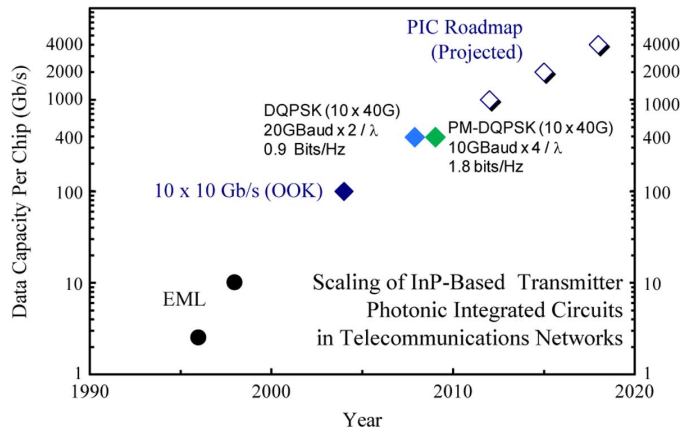


Fig. 37. Infinera Roadmap for large-scale DWDM transmitter PICs.

to be limited in dynamic range by the transmitter [68]. For direct modulation of a laser the modulation speed must be kept significantly lower than the relaxation resonance frequency of the laser, or nonlinearities result for any modest modulation depth as the carrier density becomes unclamped. For higher frequencies external modulation must be used. Unfortunately, there are no intensity modulators that inherently have a linear relationship between drive voltage and the optical output.

If phase modulation is used, then linear modulators do exist with the basic linear electro-optic effect. Also, an effectively much deeper modulation can be imparted to the optical signal because one is not limited to simple on/off, which might be viewed as a 180° modulation, but one in principle could modulate to many times this level to enhance the potential signal/noise. However, now the problem of linearity in the link has been switched to the receiver, and this is the problem addressed by the circuit of Fig. 38 [69].

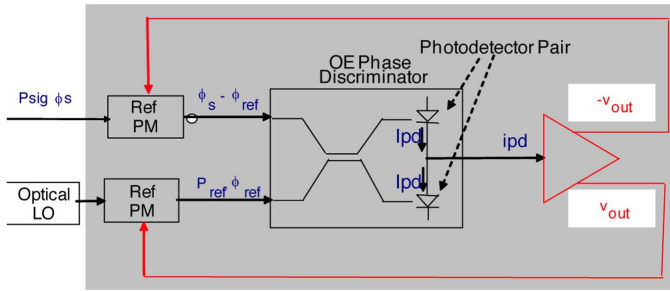


Fig. 38. Coherent receiver for phase-modulated input. Feedback from balanced photodetector is directed to tracking modulator pair.

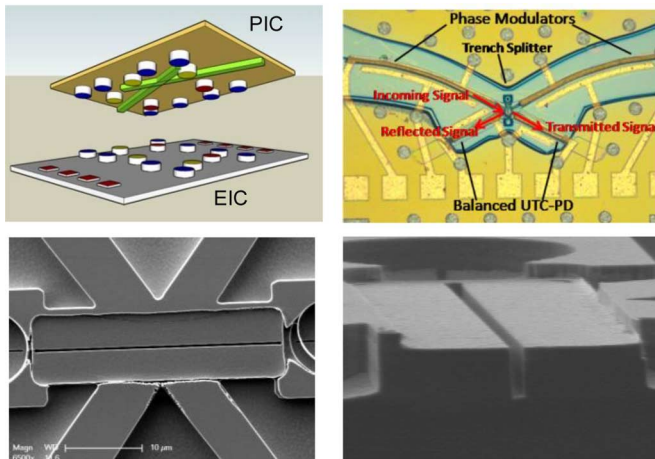


Fig. 39. (top) Schematic of flip-chipping of electronic and photonic ICs & layout of PIC; (bottom) SEMs of waveguide crossing at beam splitter from top & cross section of etched-slot beam splitter.

In Fig. 38 the negative feedback signal to the tracking modulator pair reduces the level of the interference signal on the detectors so that the output is reduced to the linear range. The differential pair also suppresses even order distortions that may exist in the semiconductor modulators as well as amplitude modulation. This approach also enables the use of $\gg \pi$ -modulation depth since the signals leaving the differential tracking modulators are made to be almost in-phase even if hugely out of phase because of a large phase modulation prior to them.

One major issue with this approach is that the tracking phase modulators must nearly instantly track the phase deviation detected in the diode pair. Thus, the delay must be very small. In fact, for the circuit to work in the GHz range, it has been found that delays >10 ps are unacceptable. This not only calls for monolithic integration of both the electronics and photonics, it also demands the elimination of any unwanted signal paths between the two. Fig. 39 illustrates the flip-chip bonding configuration that has been implemented to eliminate all additional delays in the practical implementation of the circuit of Fig. 38. The coupler has also been implemented as a beam-splitter to further eliminate propagation delay in a directional coupler embodiment, which was first explored.

Initial results from this configuration are shown in Fig. 40 [70], [71]. A calculated link gain of -2 dB and a spur-free dynamic range (SFDR) of $122 \text{ dB}\cdot\text{Hz}^{2/3}$ with a transmitter $V_{\pi} = 4.4$ V and only 2.8 mA on each photodetector is found. Also,

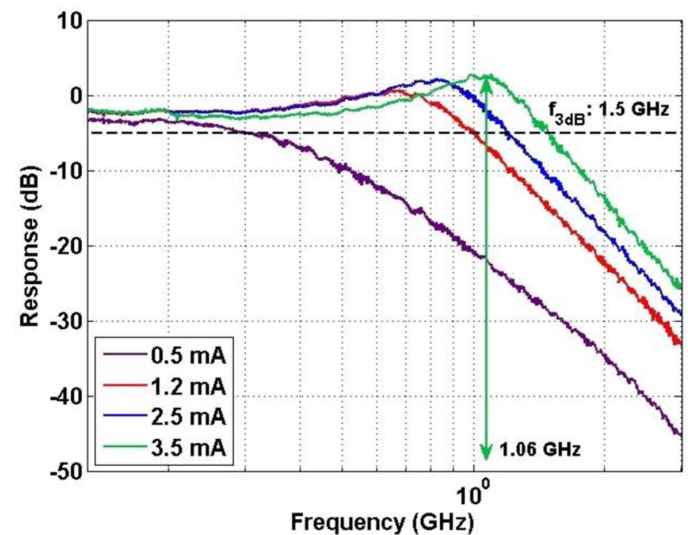
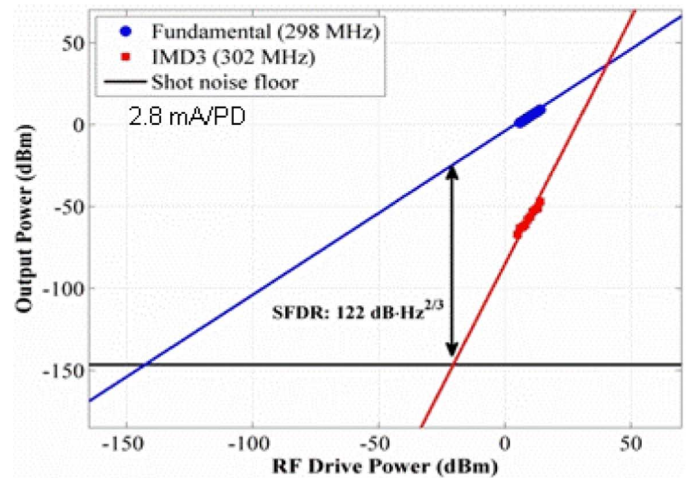


Fig. 40. (top) Plots of fundamental and third-order distortion levels versus RF drive power. (bottom) Output versus frequency for various photocurrents as input power is increased.

a peak-to-peak phase modulation depth of 1.62π was used for these results, demonstrating the ability to employ a significant modulation depth.

With higher photocurrents it is anticipated that significantly higher SFDRs will be obtainable. However, in the embodiment used, there were no optical mode transformers at the inputs and the slot beam splitters were also rather lossy, so a significant power loss was experienced.

Phase-Locked Tunable Lasers: Loop delay is also important for phase locking lasers together. Fig. 41 shows a chart of initial laser linewidth versus loop delay for various levels of phase error. Explicitly shown are lines that represent the phase error allowed for different types of digital multilevel phase and amplitude coding. The corresponding SNRs in the signal bandwidth are 9.5 dB (PSK), 12.5 dB (QPSK), 20 dB (16 QAM), and 26.2 dB (64 QAM).

Widely tunable lasers as the SGDBR shown in Fig. 6 tend to have inherent linewidths in the 1–3 MHz range. Fig. 41 would indicate a need for OPLL loop delay <100 ps for a correctable error rate of 10^{-5} in a 64-QAM digital system. But, this would actually be a fairly distorted signal from a microwave photonics

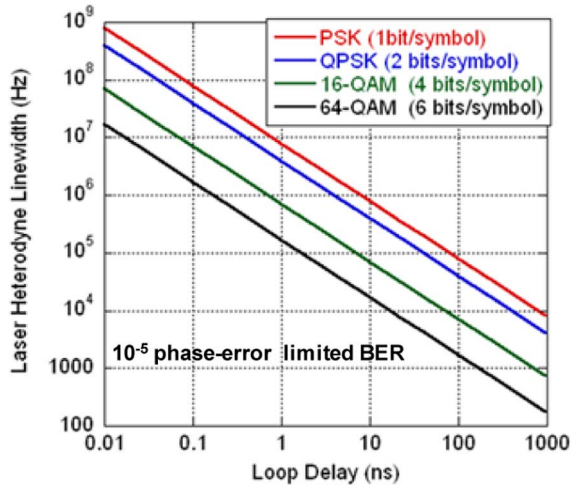


Fig. 41. Laser linewidth versus OPLL loop delay to enable 10^{-5} error rate for given modulation format.

perspective. Instead of an equivalent spectral efficiency of 6 bits/symbol, we would like to see the line for 10 or 12 bits/symbol, which would again require a loop delay <10 ps in the OPLL if we started with the rather noisy SGDBR. So, again very tight integration is called for.

Phase locking of semiconductor lasers is desired in order to make inexpensive arrays of coherent sources for such applications as phased-array LIDAR and other optical-coherence-tomography (OCT) and imaging applications. It is also desired to have temperature insensitive synthesized sources that are locked to an offset from some stable reference to allow much more efficient use of the spectrum as in the rf domain. As a result, some initial experiments have been done to demonstrate integrated OPLLs formed from a pair of widely-tunable SGDBRs together with most of the required optical elements.

Fig. 42 describes a heterodyne experiment in which two SGDBR lasers are offset-locked together [72]. The circuit schematic shows that an integrated modulator is used to generate sidebands on the mixed signal, so that the OPLL can lock on one of these. In this case a 5 GHz fundamental offset locking is illustrated. With deep phase modulation of the on-chip modulator it is possible to generate a number of side bands and such modulators can be made with bandwidths up to ~ 100 GHz, so it is anticipated that such offset locking might be possible up to the THz range without having to generate rf higher than 100 GHz.

Fundamental offset locking as high as 20 GHz was demonstrated with the current set up. Although a balanced detector pair was available on the chip, the electronics used only had a single-input amplifier, so only a single detector was used, and this resulted in more AM and noise in the feedback loop than necessary. Nevertheless, a respectable phase error variance $\sim 0.03 \text{ rad}^2$ was measured over the 2 GHz measurement window.

D. Future OPLL Directions

Fig. 43 illustrates a cartoon of a futuristic LIDAR system-on-a-chip that will be one of the long-term research directions of a newly formed “Photonic Integration for Coherent

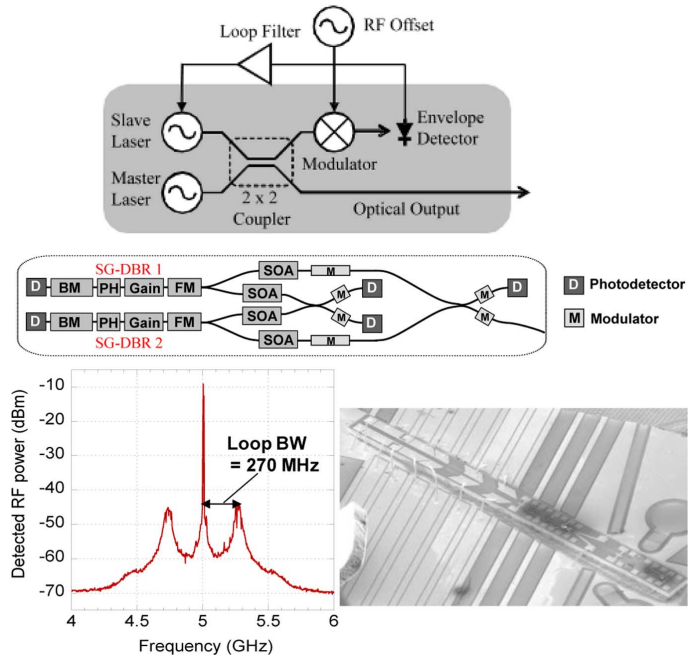


Fig. 42. Circuit schematic; PIC schematic; heterodyne result; and SEM of InP-based PIC.

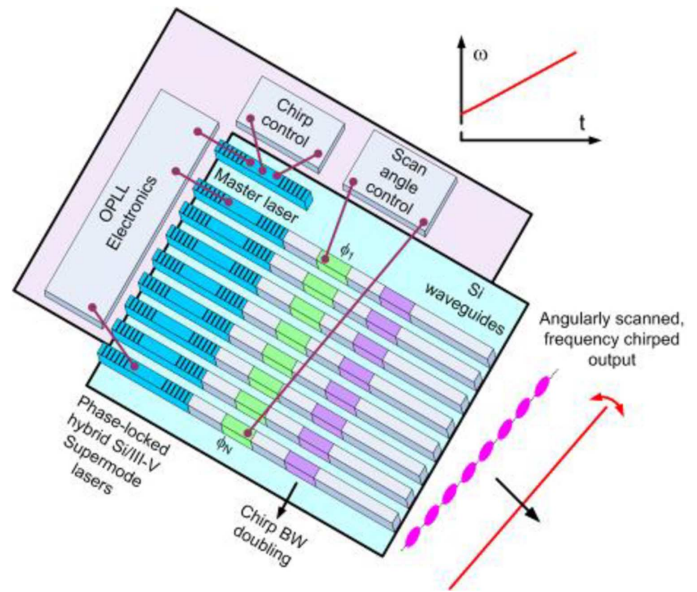


Fig. 43. Vision of future LIDAR system-on-a-chip [74].

Optics” (PICO) Center that involves five US universities [73]. As illustrated with OPLLs it is anticipated that both chirping of the beam in frequency as well as sweeping it in angle will be possible by rapid control of the offset locking as outlined in Fig. 41. This will involve significant developments in the control/feedback electronics as well as in the PICs themselves. As also noted, it is anticipated that much of this work may migrate to the hybrid-Si integration platform.

VI. SUMMARY

Some of the work that has led to current highly-functional, high-performance photonic integrated circuits (PICs) is re-

viewed, including a few of the basic integration approaches. A number of recent medium-to-large scale PIC examples are presented along with a sampling of results from them. Current work on PICs for coherent communication and sensing applications is introduced and some examples of integrated optical phase locked loops for such applications is given. It is suggested that there are still many significant opportunities for further improvements in the cost, size, weight, power consumption and performance of future systems by employing photonic integration.

ACKNOWLEDGMENT

The authors would like to thank the many former and present UCSB students and colleagues that have performed much of the work presented herein and especially the collaboration of Profs. J. E. Bowers and D. J. Blumenthal on much of the research over the years. Materials supplied by Dr. C. Joyner of Infinera and Dr. C. Doerr of Acatel-Lucent are also gratefully acknowledged.

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Larry A. Coldren (S'67–M'72–SM'77–F'82) received the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, in 1972.

He is the Fred Kavli Professor of Optoelectronics and Sensors and Acting Richard A. Auhll Dean of Engineering at the University of California, Santa Barbara (UCSB). After 13 years in the research area at Bell Laboratories, he joined UCSB in 1984, where he now holds appointments with the Department of Materials and the Department of Electrical and Computer Engineering. In 1990, he cofounded Optical Concepts, later acquired as Gore Photonics, to develop novel VCSEL technology, and, in 1998, he cofounded Agility Communications, later acquired by JDSU, to develop widely-tunable integrated transmitters. At Bell Labs, he initially worked on waveguided surface-acoustic-wave signal processing devices and coupled-resonator filters. He later developed tunable coupled-cavity lasers using novel reactive-ion etching (RIE) technology that he created for the then new InP-based materials. At UCSB, he continued work on multiple-section tunable lasers, in 1988 inventing the widely-tunable multi-element mirror concept, which is now used in some JDSU products. Near this same time period, he also made seminal contributions to efficient vertical-cavity surface-emitting laser (VCSEL) designs that continue to be implemented in practical devices to this day. More recently, his group has developed high-performance InP-based photonic integrated circuits (PICs) as well as high-speed VCSELs, and they continue to advance the underlying materials growth and fabrication technologies. He has authored or coauthored over a thousand journal and conference papers, seven book chapters and one textbook and has been issued 63 patents. He has presented dozens of invited and plenary talks at major conferences.

Prof. Coldren is a Fellow of the IEE and a member of the National Academy of Engineering. He was a recipient of the 2004 John Tyndall and 2009 Aron Kressel Awards.



Steven C. Nicholes received the B.S. degree in chemical engineering from Brigham Young University, Provo, UT, in 2005, and the Ph.D. degree in materials from the University of California, Santa Barbara (UCSB), in 2009.

At UCSB, his research focused on the design, growth and fabrication of widely tunable semiconductor lasers and semiconductor optical amplifiers for large-scale photonic integrated circuits. In 2009, he joined Aurion, LLC, Santa Barbara, where he focuses on the design of silicon

photonic integrated circuits.



Leif Johansson (M'04) received the Ph.D. degree in engineering from University College London, London, U.K., in 2002.

He is currently a Research Scientist with the University of California, Santa Barbara. His current research interests include design and characterization of integrated photonic devices for analog and digital applications and analog photonic systems and subsystems.



Sasa Ristic (M'02) received the Ph.D. degree in electrical and computer engineering from the University of British Columbia, Vancouver, BC, Canada, in 2007.

He has been a Post-doctoral Fellow with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, since 2007, supported in part by the Natural Sciences and Engineering Research Council of Canada (NSERC). His current research interests include design, fabrication, and characterization of integrated photonic

devices and their applications.



Robert S. Guzzon received the B.S. degrees in electrical engineering and physics from Lehigh University, Bethlehem, PA, in 2007. He is currently working toward the Ph.D. degree in electrical engineering at the University of California, Santa Barbara.

His interests include large-scale photonic integration, particularly applied to microwave photonic signal processing. His current work focuses on the design and fabrication of versatile microwave filter systems to achieve improved tunability and noise performance.



Erik J. Norberg received the B.S. and M.S. degrees in engineering nanoscience from Lund University, Lund, Sweden, in 2008. He is currently working toward the Ph.D. degree in electrical engineering at the University of California, Santa Barbara.

His past research experience includes MOCVD growth and characterization of InP-based nanowires. He is currently working on the development of monolithically integrated programmable optical filters.



Uppiliappan Krishnamachari received the B.S. degree in electrical engineering from the University of Illinois, Urbana-Champaign, in 2005. He is currently working toward the Ph.D. degree in electrical engineering at the University of California, Santa Barbara.

His research interests include the design, fabrication, and characterization of InP-based photonic integrated circuits incorporating nanophotonic devices. His current efforts are focused on integrated coherent receivers using ultra-compact trench waveguide couplers for high linearity microwave photonic links.

plers for high linearity microwave photonic links.

Integrated Photonics for Low-Power Packet Networking

Daniel J. Blumenthal, *Fellow, IEEE*, John Barton, Neda Beheshti, John E. Bowers, *Fellow, IEEE*, Emily Burmeister, Larry A. Coldren, *Fellow, IEEE*, Matt Dummer, Garry Epps, Alexander Fang, Yashar Ganjali, *Member, IEEE*, John Garcia, Brian Koch, Vikrant Lal, Erica Lively, John Mack, Milan Mašanović, Nick McKeown, *Fellow, IEEE*, Kim Nguyen, Steven C. Nicholes, Hyundai Park, Biljana Stamenic, Anna Tauke-Pedretti, Henrik Poulsen, and Matt Sysak

(Invited Paper)

Abstract—Communications interconnects and networks will continue to play a large role in contributing to the global carbon footprint, especially in data center and cloud-computing applications exponential growth in capacity. Key to maximizing the benefits of photonics technology is highly functional, lower power, and large-scale photonics integration. In this paper, we report on the latest advances in the photonic integration technologies used for asynchronous optical packet switching using an example photonic integrated switched optical router, the label switched optical router

architecture. We report measurements of the power consumed by the photonic circuits in performing their intended function, the electronics required to bias the photonics, processing electronics, and required cooling technology. Data is presented to show that there is room (potentially greater than $10\times$) for improvement in the router packet-forwarding plane. The purpose of this exercise is not to provide a comparison of all-optical versus electronic routers, rather to present a data point on actual measurements of the power contributions for various photonic integration technologies of an all-optical packet router that has been demonstrated and conclude, where the technology can move to reduce power consumption for high-capacity packet routing systems.

Manuscript received May 12, 2010; revised July 1, 2010; accepted April 3, 2010. Date of publication January 12, 2011; date of current version April 6, 2011. This work was supported in part by Defense Advance Research Project Agency Office of Microsystems Technology (DARPA/MTO) Data in the Optical Domain (DODN) Program under Award W911NF-04-9-0001 and DARPA/MTO Chip Scale Wavelength Division Multiplexing (CSWDM) Program under Award N66001-02-C-8026.

D. J. Blumenthal, J. Barton, J. E. Bowers, L. A. Coldren, J. Garcia, E. Lively, M. Mašanović, K. Nguyen, B. Stamenic, and H. Poulsen are with the University of California, Santa Barbara, CA 93106 USA (e-mail: danb@ece.ucsb.edu; jsbarton@ece.ucsb.edu; bowers@ece.ucsb.edu; coldren@ece.ucsb.edu; johngarcia@umail.ucsb.edu; elively@ece.ucsb.edu; mashan@ece.ucsb.edu; kim@ece.ucsb.edu; biljana@ece.ucsb.edu; henrik@ece.ucsb.edu).

N. Beheshti was with the Department of Computer Science, Stanford University, Palo Alto, CA 94305 USA, and is now with Ericsson Research Lab, San Jose CA 95134. USA (e-mail: neda.beheshti@gmail.com).

E. Burmeister and M. Dummer were with the University of California, Santa Barbara, CA 93106 USA. They are now with Ciena Corporation, Linthicum, MD 21090 USA (e-mail: eburmeis@ciena.com; dummer@enr.ucsb.edu).

G. Epps is with Cisco Systems, Inc., San Jose, CA 95134 USA (e-mail: gepps@cisco.com).

A. Fang and S. C. Nicholes are with Aurrion, Santa Barbara, CA 93117 USA (e-mail: alexander.fang@aurrion.com; steve.nicholes@aurrion.com).

Y. Ganjali was with the Stanford University, Palo Alto, CA 94305 USA. He is now with the University of Toronto, Toronto, ON M5S 1A1, Canada (e-mail: yganjali@cs.toronto.edu).

B. Koch is with the Photonics Technology Labs, Intel Corporation, Santa Clara, CA 95054 USA (e-mail: brian.r.koch@intel.com).

V. Lal is with the Infinera Corporation, Sunnyvale, CA 94089 USA (e-mail: vlal@infinera.com).

J. Mack was with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106 USA. He is now with the Laboratory for Telecommunications Sciences, University of Maryland College Park (e-mail: jmack805@gmail.com).

N. McKeown is with the Stanford University, Palo Alto, CA 94305 USA (e-mail: nickm@stanford.edu).

H. Park and M. Sysak were with the Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106 USA. They are now with Intel Corp. (e-mail: hyundaipark@gmail.com; matthew.n.sysak@intel.com).

A. Tauke-Pedretti is with Sandia National Laboratories, Albuquerque, NM 5800 USA (e-mail: ataukep@sandia.gov).

Color version of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSTQE.2010.2077673

Index Terms—Optical communications, optical packet switching, photonic integration.

I. INTRODUCTION

THE predicted carbon footprint of data communications networks and data centers to the global IT sector contributes almost one-half of the total expected contribution. With predicted exponential growth in capacity due to consumer applications like video demand taking off, technologies that can save power in the network communications, and data center infrastructures will be critical. Photonics has the potential based on fundamentally different power scaling laws, to enable high capacity and bandwidth systems to scale in a different manner than how systems are architected today based on electronic integrated technologies. The power savings from using photonics technologies will need to come about from rearchitecting these systems as well as pushing the state of the art in photonic integration. In this paper, we focus on results from the DARPA-funded label switched optical router (LASOR) project to illustrate how photonics can be used to offset power and footprint limits that will be imposed for high-capacity future routers and communications system. We will describe how the LASOR project systematically addresses, through design and measurements, the largest power consumer in today's router architectures as the fiber bit rate and router capacity increases. We will also describe how photonic circuits, positioned in the proper functions in a packet-based system provide better power scaling behavior as the line bit rate increases relative to electronic solutions that rely on heavy parallelism and fast transistors. In order to begin to understand, the potential photonic ICs (PICs) can have on the power consumption of packet switched systems, it

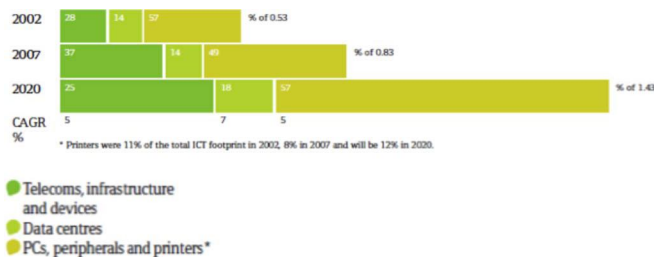


Fig. 1. Contributions of IT sectors to the global carbon footprint.

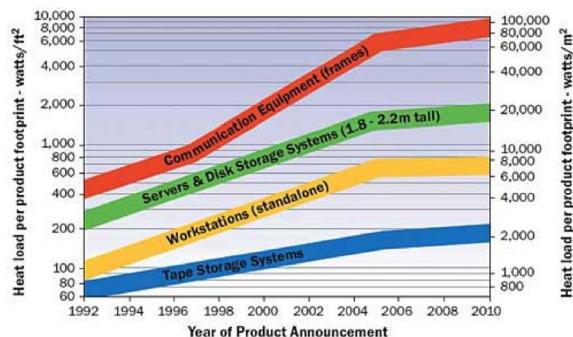


Fig. 2. Intel study showing the dominant contribution of communications equipment in data centers to the heat load per product footprint [1].

is important to build and measure prototype systems based on real PIC technologies.

II. CARBON FOOTPRINT OF IT SYSTEMS

IT systems continue to increase demands on energy supplies as computer usage, network bandwidth, data storage, and applications continue to increase at an ever-expanding rate. The problem has become quite severe, on the order of other major global emissions contributors including the global aviation industry. A study done on the global footprint by subsector in 2009, shown in Fig. 1, demonstrates the impact of PCs, peripherals and printer, and the telecommunications and data center infrastructures. The global telecommunications and data center infrastructures are expected to subsume almost half of the IT contributions to carbon footprint.

The heat-load contributions to data centers as a function of data centers release date was reported by Intel and is shown in Fig. 2, where the breakdown of the heat load per footprint illustrates that communications equipment continues to be an increasingly dominant contribution. New technologies, such as photonics, have the potential to flatten out or reduce this growth when architected properly into systems and integrated using next generation photonics integrated technologies, as discussed further on.

III. POWER LIMITATIONS OF TODAY’S COMMUNICATIONS SYSTEMS—SYSTEM SCALABILITY AND THE POWER SPREADING PROBLEM

The energy problem due to the communications infrastructure will grow as continued increase in IP traffic growth pushes demands on communications equipment. As shown in Fig. 3 increases in IP traffic growth due in particular to consumer

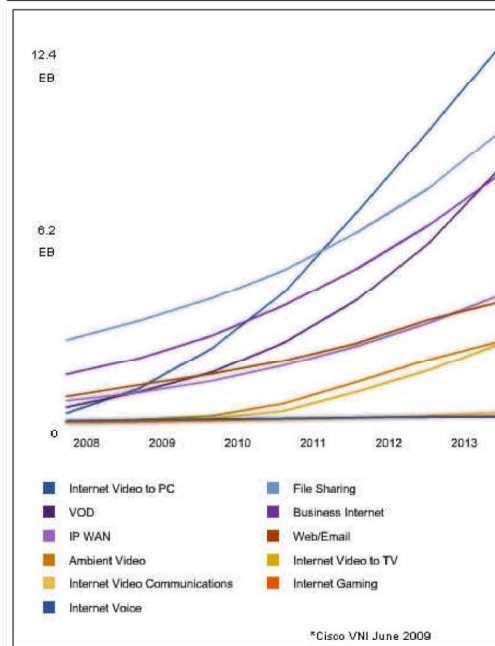
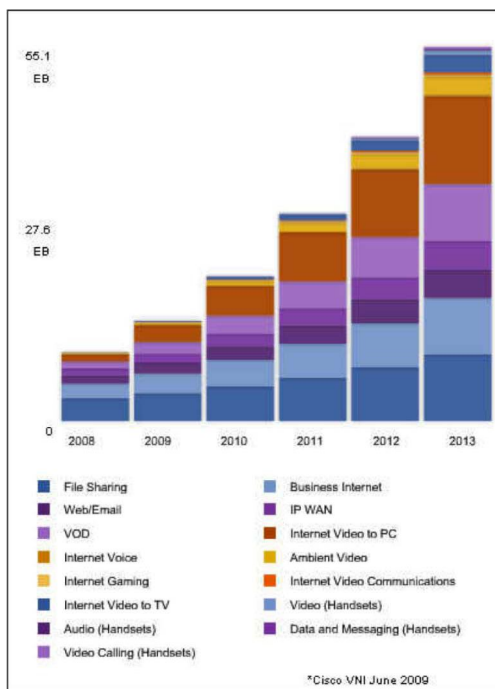


Fig. 3. Projected IP traffic growth due to video and new high bandwidth demands (Graphs courtesy of Cisco Visual Networking Index http://www.cisco.com/en/US/netsol/ns827/networking_solutions_sub_solution.html).

demand for services like video are projected to increase by a factor of fivefold by 2013.

The system bandwidth of high-capacity systems that need to support this growth, like routers, data centers, and telecommunications infrastructure, rely on continued improvements in electronic technologies in terms of metrics like megahertz-gate per milliwatt and megabits per second per watt in order to keep the system power flat, while providing for continual scaling in system bandwidth (BW).

As shown in Fig. 4, the power/performance efficiency improvements of high-performance electronic communication

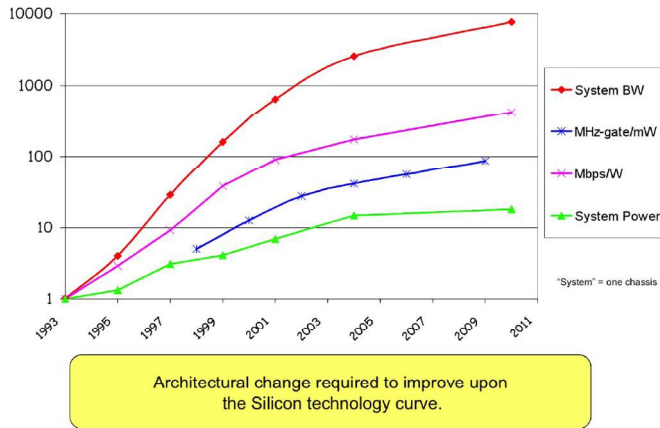


Fig. 4. Historical growth of high-end router capacity and improvements in power efficiency (relative to products of 1993) and dependence on continued improvements in electronic component efficiency.

systems are bound to the efficiency improvements of the underlying silicon technology. To scale systems at a higher rate than the component technology requires architectural innovation and/or a compromise in one or more areas of system functionality such as performance, programmability, or physical size/density. However, this architectural workaround is difficult to sustain long-term and fundamental improvements in the underlying technology is required to overcome projected shortfalls.

The capacity of single-rack Internet routers has grown by approximately threefold every 18 months and is limited by the power that can be delivered to, and dissipated from, a single rack of equipment. Power consumption has grown with capacity, and the largest single-rack routers today consume over 10 kW. Architecting electronic core routers with higher capacities continues to burden all aspects of system design and underlying technologies including switch fabric capacity and packet processing, such as forwarding, queuing, and buffering. Today's state-of-the-art core routers utilize multirack designs in order to spread the system power over multiple racks, reducing the power density, and push aggregate capacities to 100 s of Tb/s. However, these systems require as many as six optoelectronic conversions per input/output and multirack configurations dominated by interface cards. For example, a 25 Tb/s router with 128 40 Gb/s I/O ports can require 768 40Gb/s actual or equivalent optoelectronic/electrooptic (OE/EO) conversions, whose power dissipation and footprint increase with number of ports and bit rate per port.

One reason for the tradeoff in system BW (where system BW is defined as router capacity or throughput with a given packet loss rate and offered load at the input) with physical size/density even with faster and denser electronics is related to the power-spreading problem, as illustrated in Fig. 5. Today's transistors exhibit a fixed leakage current that is based on current manufacturing technology pervasive in the existing semiconductor processing foundry infrastructure that is very expensive to change on a large-scale basis even with fundamental improvements in transistor technology. Additionally, running transistors at ever increasingly high clock speeds adds to the power dis-

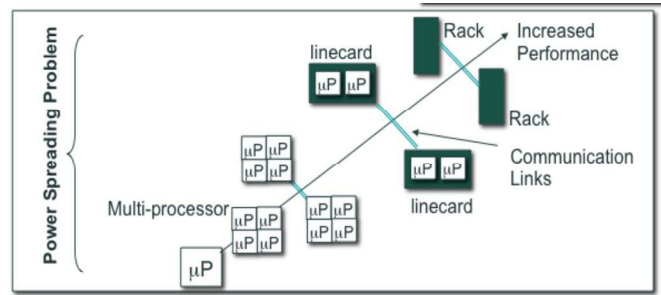


Fig. 5. Effect of power-spreading problem on system footprint and power dissipation.

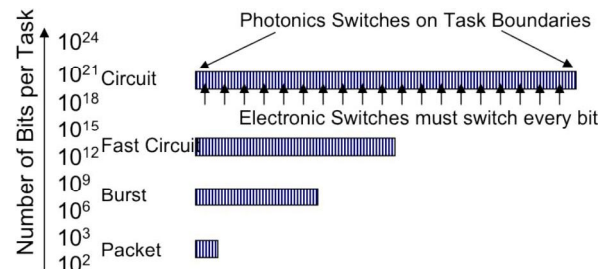


Fig. 6. Scaling of switching energy as a function of the size of switched information for photonics versus electronics.

sipation problem making multicore solutions more desirable. Since the power footprint of a system is practically constrained, single-chip solutions quickly become multichip solutions with an added power overhead for interchip communications, followed by the need to move to multiline card and multirack solutions, each with additional added communications power overhead between cards, shelves, and racks.

IV. POTENTIAL IMPACT OF PHOTONICS ON POWER SCALING LAWS

Photonics has the potential to change the power scaling laws of high bandwidth systems through proper architectural choices that combine photonics with electronics to optimize performance, power, footprint, and cost. The major types of data in a communications system are shown in Fig. 6 with circuit switching at one extreme of granularity and packet switching at the other extreme. Traditionally, digital electronics is used to switch these data units, and transistors must switch and expend energy at the bit rate for every bit. The faster the bit rate, the more energy is expended per bit and the longer the task the more energy is expended per task (e.g., circuit, burst (including packet flows), and packet).

Using analog photonics to switch or tasks requires switching only at the task boundaries. However, there does exist a tradeoff between the switching energy and the bias power depends on the photonics technology used. While electronics has very low switching energy and bias power, certain photonics technologies, like microelectromechanical system (MEMS) can have lower bias power while other technologies like semiconductor optical amplifiers (SOAs) require higher bias powers today. The tradeoff between initial bias power, switching energy, and

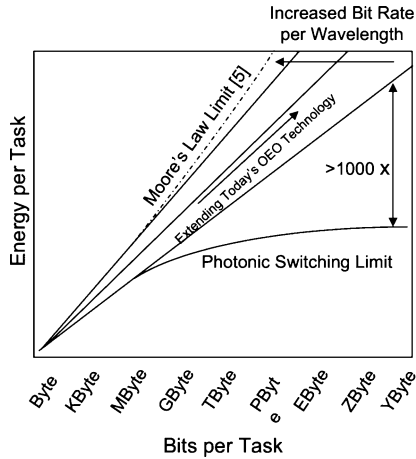


Fig. 7. Energy used to switch task for electronics and photonics as a function of task length.

switching at the bit level or task boundary leads to qualitative behaviors illustrated in Fig. 6. Today’s photonics and electronics dissipate roughly the same power for smaller tasks. The total bit level switching energy per task dominates the bias power for longer task for electronics as is shown in the curve “extending today’s OE optic (OEO) technology.” As the bit rate is increased for electronics, the power to switch transistors increases and the task curve moves to the left approaching Moore’s law limit. Photonics (analog) has a qualitatively different behavior, where the energy per task is dominated by the bias power and does not increase significantly as the bit rate and task length increases. This is shown qualitatively in the photonics limit curve in Fig. 7. It is important to note that the curves in Fig. 7 represent switching in the data plane and do not include a dominant component of processing packet forwarding or connection setup.

V. EXAMPLE SYSTEM—LASOR: A LABEL SWITCHED OPTICAL ROUTER

For purposes of the power analysis of PIC for this paper, the LASOR project [1], [3]–[5], funded by DARPA MTO, is presented as an example optical packet switching system, where the power dissipation of the integrated photonics and surrounding electronics has been quantified. The purpose of this exercise is not to provide a firm comparison of all-optical versus electronic routers as this is a very complex and problem with rapidly moving data points. The purpose of this paper is rather to present a data point on actual measurements of the power contributions for various components of an all-optical packet router that has been demonstrated and conclude, where the technology can move to.

An optical label switched network and the LASOR node block diagram are shown in Figs. 8 and 9. For the LASOR project, we have target 64×64 ports per packet routing section of the line cards shown in Fig. 9. In order to reach 100 Tb/s per node, 20 line cards are required. The number of fiber input and output ports will depend on the wavelength division multiplexing (WDM) channel plan at the node inputs and outputs and the bit rate per wavelength. Each LASOR node consists of WDM interfaces

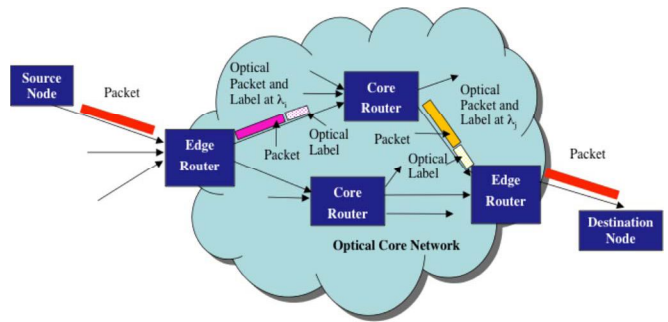


Fig. 8. High-level diagram of an optical label switched packet network and the interface to legacy systems.

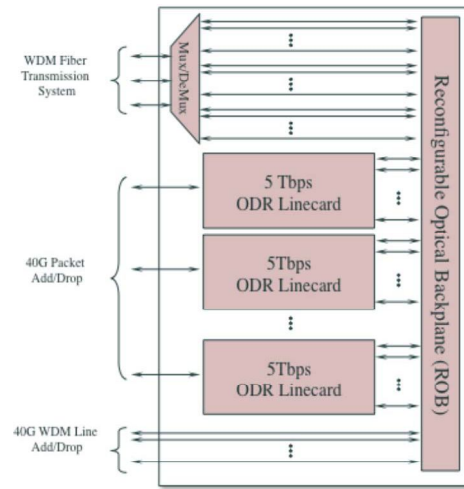


Fig. 9. LASOR optical routing node block diagram.

to transmission lines, optical WDM wavelength add/drop ports, and optical packet add/drop ports. Wavelengths from the transmission system can be quasi-statically connected to any choice of wavelength add/drop or optical data router (ODR) line card ports using a MEMS switch interconnect backplane.

The PIC components and subsystems presented in this paper comprise the LASOR ODR line card shown in Figs. 9 and 10. The primary building blocks that have been integrated using PIC technology include an optical payload envelope detector (PED), optical label burst mode recovery, an optical packet synchronizer (OPS), an optical random access memory (ORAM), a packet-forwarding chip (PFC), an arrayed-waveguide grating router (AWGR), a monolithic tunable optical router (MOTOR), and a 3R regenerative wavelength converter matched to the output line transmission system.

One of the key areas for optical routers is optical buffers and is among the most challenging technology to integrate. The ability to fabricate PIC buffers of a certain complexity must match the network buffer requirements for a router. One of these requirements is the depth of the optical packet buffers required for lossless packet routing (here lossless refers to the loss of packets that are dropped from buffers).

Electrical routers use electrical RAM to implement buffers that resolve contention and congestion, as shown in Fig. 11.

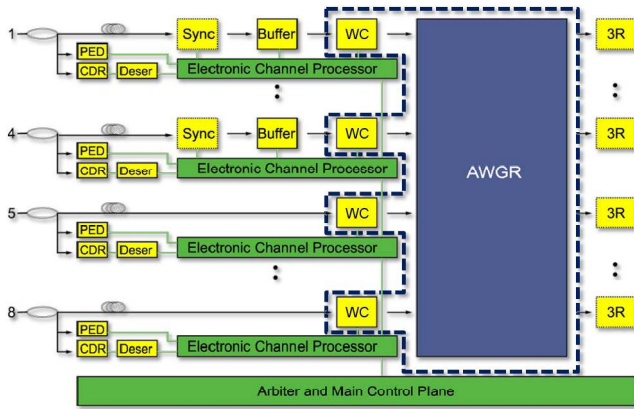


Fig. 10. Main components of the 8×8 LASOR ODR. The wavelength conversion (WC) element is the PFC PIC and the buffer is the ORAM PIC described in the following.

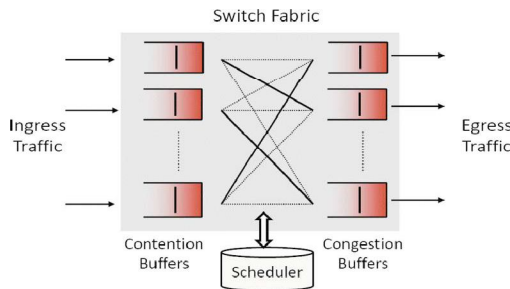


Fig. 11. Buffering in a combined input/output queuing (CIOQ) router. Input buffers store packets when there is internal contention. Output buffers store packets when output links are congested.

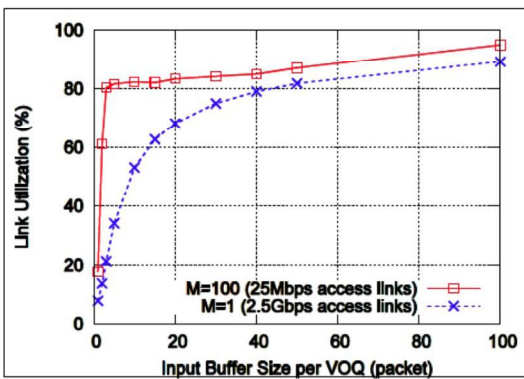


Fig. 12. Link utilization versus input and output buffer sizes. With 25 Mb/s access links, five-packet virtual output queues (VOQs) and 15-packet output buffers make the utilization above 80%.

This capacity is currently not feasible with any proposed optical buffering approach. But research has shown that much smaller buffering capacities are adequate, on the order of 10–20 packet deep buffers, within the reach of today’s PIC technology. Analysis, simulations, and experiments show that if access links run slower than backbone links, the traffic is smoothed, and hence, only 10–20 packet buffers per output port are needed for 80% throughput, as shown in Fig. 12 [6]–[8].

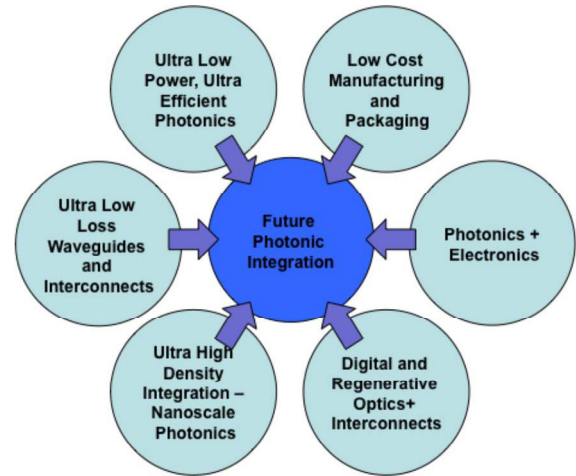


Fig. 13. Enabling technologies to allow for future photonic integration.

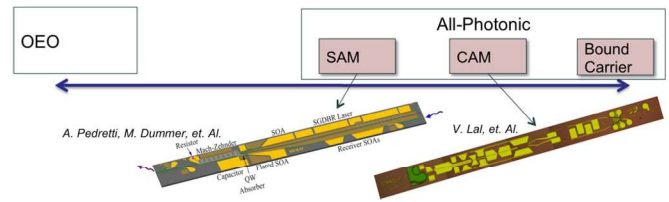


Fig. 14. All-photonic PICs using the SAM and CAM approach.

VI. LOW-POWER PICs

Photonic integration has the potential to save power for packet routing systems and other applications. However, in order for PIC technology to make in-roads to real systems and be an energy efficient, cost effective, and manufacturable technology that scales to a large number of on-chip components, multiple key issues must be addressed [9]–[11]. As shown in figure, new generation of PICs will require advances in ultralow power sources, detectors and amplifiers, ultralow-loss waveguides and interconnects, ultrahigh density components, digitally regenerative optics, efficient integration of electronics and photonics, and low cost packaging and manufacturing as well as high-yield PICs (see Fig. 13).

Under the LASOR program, we have investigated two categories of all-photonic devices, as depicted in Fig. 14. We define a spread of approaches to lie along a line that has OEO that lies at one extreme. We define OEO, where not only are photons converted to electrons and *vice versa*, but digital manipulation, using electronic transistors or logic gates, occurs between the optical input and output. We define three subcategories of *all-photonic*, where the first two, photocurrent-driven wavelength converters (SAM) and concurrent absorption and modulation wavelength converters (CAM) involve interactions of photons with free carriers and the third involves interaction of photons with bound carriers. The term all-photonic is used for all-optical, CAM, and SAM, since all processes that involve photons controlling photons involve intermediate interaction with electrons, either bound or free.

TABLE I
LASOR PIC FUNCTIONS AND PERFORMANCE

| Function | Integration Platform | Performance Summary | Est. PIC Power (W) |
|---|-------------------------|---|--------------------|
| Monolithic Tunable Optical Router (MOTOR) | InP, CAM | 640 Gbps routing capacity, 8 inputs 8 outputs, 40Gbps per input, 2R regenerative, C-band tunable | 16 |
| Optical Payload Envelope Detection (PED) | InP, Si/InP, CAM, SAM | 40 Gbps variable length, asynchronous payloads. C-Band operation. 300 ps recovered payload envelope rise time and 30ps rms jitter over 10dB dynamic input power range. 4-stage synchronizer with the relative delay through any configuration of the synchronizer given as $T(n) = n \times \Delta$ ($n = 0, 1, 2 \dots 15$), where $\Delta = 800$ ps and the tuning range is 12.8ns. Packet rate reconfiguration. 10Gbps asynchronous labels. < 20 bit lock time and > 380 bit hold time. | 3 |
| Optical Packet Synchronizer (OPS) | InP/Silica, Si/InP, CAM | 184ns storage of 40Byte 40Gbps packets with > 98% packet recovery after storage. | 4 |
| Burst Mode CDR | Si/InP Hybrid, CAM | 40Gbps asynchronous, variable length payload fast switchable wavelength conversion and 10Gbps optical label re-write. C-band operation. -27dBm sensitivity. <2dB PP. | 0.750 |
| Optical Random Access Memory (ORAM) | InP/Silica, Si/InP, CAM | 23ns delay, 40dB ER, <1ns load/unload switch times. | 3.5 |
| Packet Forwarding Chip (PFC) | InP, CAM, SAM | 184ns storage of 40Byte 40Gbps packets with > 98% packet recovery after storage. | 2 |

SAM devices utilize separate absorption and modulation sections, where the input light is absorbed/detected and used to remodulate the light onto a new optical signal via an externally modulated laser and these two sections are connected by a simple wire or electron waveguide. CAM devices utilize colinear optical and electronic waveguides, where the input photons directly interact with electrons as in a SOA to produce a modulation effect transferring the input optical data onto a new outbound optical signal. Bound carrier devices utilize nonlinear polarization interaction between the photon and a bound electron to produce new optical signals, such as with four-wave mixing in optical fibers or second harmonic generation in, e.g., lithium niobate.

In this paper, we focus on two types of all-photonic PICs integrated under the LASOR project, the SAM and CAM types. Table I lists the PIC devices that are covered in this paper, the integration platform used, a performance summary and list of relevant references for each.

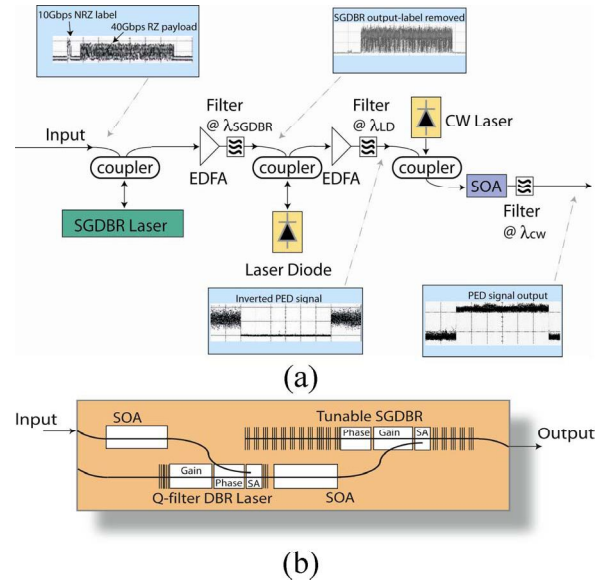


Fig. 15. All-optical PED principal, operation and PIC.

A. Optical PED

The PED function [12] is used to determine the location of the optical packet boundaries with high precision without processing the individual bits, saving power as the length of the packet increases and the bit rate increases.

The PED output is used to create a precise time reference of the payload in the electrical domain relative to the optical domain in order to make synchronization, buffering, label erasure and rewrite, and forwarding operations.

An all-photonic CAM implementation of the PED function provides very rapid rise and fall times of the envelope signal as well as low jitter. A discrete all-optical PED implementation along with an optical packet and the resulting optical envelope is shown in Fig. 15(a). Integration of the optical PED function onto a monolithic chip is shown in Fig. 15(b) [13]. The components are similar to those used in the PFC and the optical clock recovery chip.

B. Burst-Mode Optical Clock and Data Recovery

The task of recovering and processing headers in an asynchronous optical packet switching system poses many unique challenges. At each node input, the optical packet arrival time and the optical packet length are not known ahead of time. In the LASOR system, optical packets consist of payloads that are preceded by optical headers used to compute forwarding and new header information at each node. In order to process the optical headers using electronics, the header clock and data must be recovered burst mode (asynchronously) with a minimum of overhead bits (preamble). The recovered clock phase and frequency accuracy must result in error-free label recovery or the packet will be incorrectly routed. A conflicting requirement to rapid clock recovery is maintaining accurate clock frequency and phase over the length of packets that can vary in length from 40 to 1500 B, after the header terminates. We have

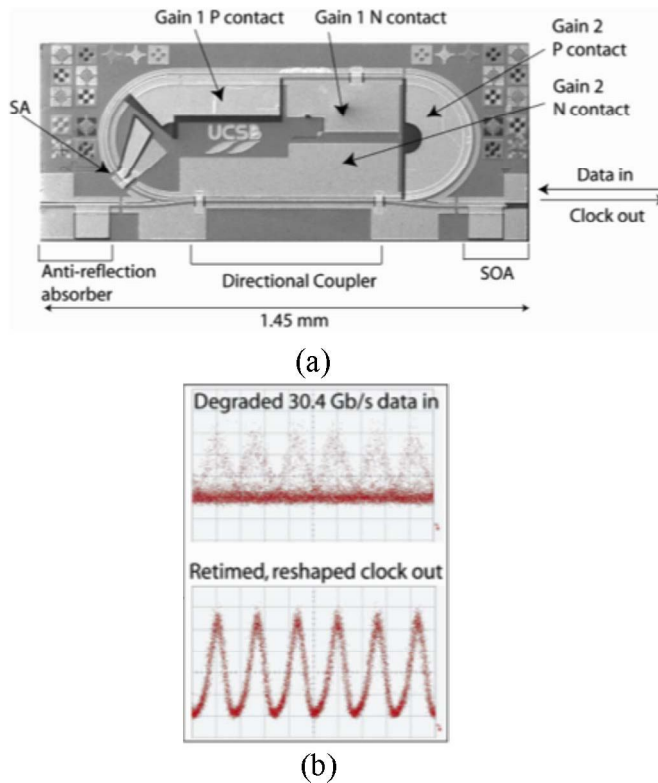


Fig. 16. (a) Si/InP ring laser used as 3R regenerative burst mode clock recovery (b) significantly improves degraded RZ data and will retimes and reshape the clock.

developed a nested feedback approach that addresses this issue and is amenable to integration [14].

A hybrid silicon evanescent ring mode-locked laser PIC has been demonstrated that realizes the rapid optical clock recovery portion of the clock and data recovery (CDR) [17]. The device, shown in Fig. 16, is capable of generating a reshaped and retimed clock signal from 30.4 Gb/s data, even when the input data is severely degraded. Interestingly enough, increasing the repetition rate of integrated ring lasers to 100 GHz and beyond becomes simpler with PIC technology as the size of the cavity becomes smaller, and therefore, more stable.

For input data with 3.8 dB extinction ratio (ER) and 14 ps of jitter, the recovered clock has an ER over 10 dB and 1.7 ps of jitter. Experiments show that the laser suppresses any noise that is outside the locking range (6 MHz). This implies that by carefully designing similar devices with predetermined locking ranges, it should be possible to reliably manufacture mode-locked lasers that can reduce jitter in compliance with International Telecommunications Union (ITU) specifications, suppressing jitter outside only specific frequency offsets from the carrier frequency.

Since the laser's ring cavity is defined using photolithography, it is possible to match the repetition rate of the laser to a specific data rate in future designs, which is essential for practical applications. The ring configuration also allows for integration with optical amplifiers and demonstrates potential for more complex PICs utilizing this mode-locked laser.

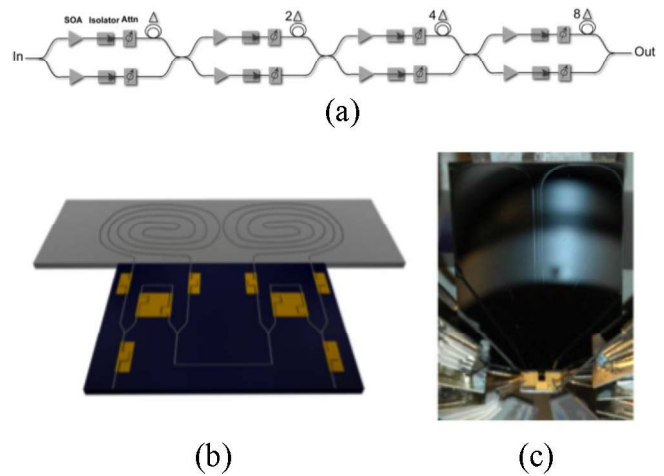


Fig. 17. (a) Optical synchronizer parallel path feedforward designed that can be integrated (b) using InP for the switching structure and silicon for the delay sections. (c) It shows a realized synchronizer.

When data is injected, most of the laser characteristics, such as output power, wavelength, pulsewidth, ER, and spectral width are unchanged from passive mode-locking conditions. The input data pulses modulate the carriers in the absorber and laser cavity and if the data rate matches the repetition rate of the laser, the laser pulses become synchronized to the data, generating a clock signal.

C. Optical Packet Synchronizer

Since packets arrive asynchronously at the router inputs, alignment to a local clock frame using optical synchronizers is required for efficient optical buffer management and output link utilization.

The optical synchronizer is based on a feedforward design that utilizes SOAs and a binary increasing length combination of optical delay lines, as shown in Fig. 17(a). Active monolithic 2×2 InP offset quantum-well (QW) SOA-based switches are used to select the required delays and compensate for delay lines losses.

The delays, fabricated using silica-on-silicon delay lines, are butt coupled to the 2×2 SOA switches shown schematically in Fig. 17(b) and in the chip form in Fig. 17(c). Requirements for the 2×2 switches include high switching ER (>40 dB), low crosstalk (<-40 dB), and fast switching times (<2 ns). The delay lines were chosen to be slightly longer than a 40-B packet (8 ns) at 40 Gb/s with an added 2 ns guard band to accommodate the SOA switching time.

D. Optical Random Access Memory

There are two major approaches to storing light: slowing light down (by decreasing its group velocity), or increasing the length of the waveguide. In [18], various buffering approaches were compared and the conclusion was that ORAM based on slow light was fundamentally limited to below 40 Gb/s and below 40 B packets. Our approaches are based on the latter technique [19], [20].

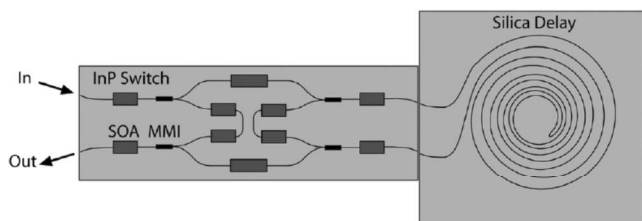


Fig. 18. InP 2×2 switch butt coupled to a silica delay line.

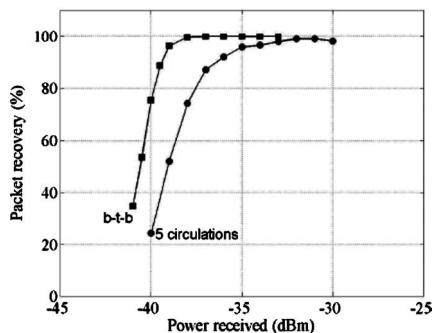


Fig. 19. Packet recovery for five recirculations shows up to 98% packet recovery.

One PIC design, we have implemented a 2×2 switch on InP butt coupled to a silica delay line, as shown in Fig. 18. Depending on the bias condition of the SOAs, the signal can be routed from the “in” port to the “out” port either with or without delay. The delay was a 2 m (12.8 ns) long waveguide that at 40 Gb/s provides 40 B of memory. Fig. 19 shows packet recovery against received power for this device. A packet recovery rate of 98% was achieved after five circulations.

Decreasing the delay loss, the loss between passive and active regions and regeneration (2R or 3R) are all approaches that can be used to increase the buffer hold time. While the propagation loss of the silica waveguide is very low (<0.04 dB/cm) and the ER of the InP switch is high (>40 dB), the butt couple can lead to reflections and the two chips have to be packaged. An integrated solution is required.

To address the loss-coupling issue between the active and passive sections, an integrated buffer was fabricated on the hybrid silicon platform [15]. Similar to the aforementioned design, a 2×2 switch is used to route a signal from the input to the output either with or without delay. Because of higher propagation losses (~ 2 dB/cm) compared to the silica-on-silicon, only delays of 7.6 cm (1.1 ns) were realized [2], which is more useful for packet synchronization than for memory. Fig. 20 shows the integrated buffer storing a packet for 1.1 ns.

For the earlier platform, a major part of the propagation loss in the integrated buffer is introduced in the definition of the amplifiers (III–V processing). To address this issue, proper passivation is needed to realize longer delay lines.

The latest generation of LASOR optical buffers in the hybrid silicon platform with a modification that the delay line (1.1 m) is protected by SiO_2 and SiN passivation layers to protect the delay line during the III–V processing. In addition, 2R regenerators for reamplification and reshaping have been integrated to amplify

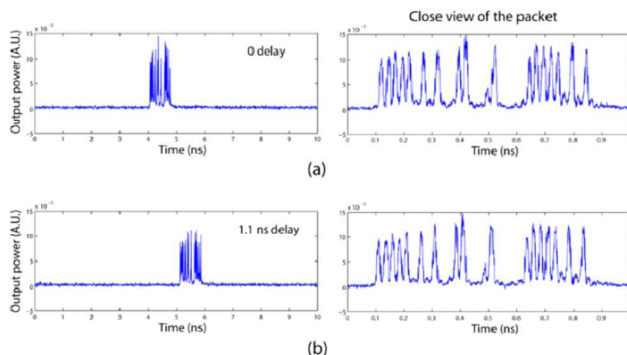


Fig. 20. Optically buffered packet (a) with no delay (b) and 1.1 ns of delay.

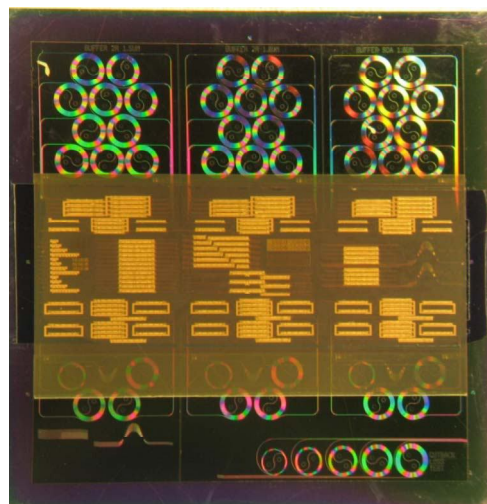


Fig. 21. Integrated buffer with 2R regenerators on a silicon-on-insulator substrate. A total of three buffers having 1.1 m of delay each are shown. In addition, various test structures and shorter buffers are on these chips.

and filter the signal. A photograph of the first fabricated chip is shown in Fig. 21.

E. Optical Wavelength Converters

Optical wavelength converters are used in LASOR for packet forwarding and are one of the two basic building blocks for the switching fabric in addition to an AWGR. PIC realizations have demonstrated wide tunable laser function, fast wavelength switching, and wavelength conversion without any electrical signal conditioning at data rates of 40 Gb/s. In the LASOR project, we have developed, demonstrated, and incorporated into the final router test bed two types of devices: concurrent absorption and modulation devices (such as Mach–Zehnder interferometric (MZI)-SOA wavelength converters), and separate absorption and modulation devices (such as a photocurrent driven externally modulated laser architecture). This level of integration significantly improves the performance, mainly through insertion loss reduction between the components, which translates into lower chip bias needs, and thus, lower thermal dissipation.

The overall power consumption for both device types was dominated by the need for devices cooling, and more than half

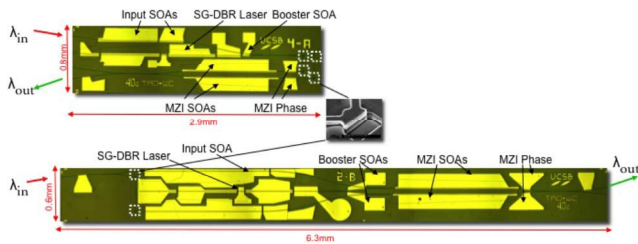


Fig. 22. Folded and unfolded versions of 40 Gb/s fast widely tunable CAM differential pulse MZI-SOA wavelength converters.

of the total power (2–2.5 W) was used up by the thermoelectric cooler.

Improvements that can be made to make these devices more power efficient have to do with reduction of insertion losses, reduction of on-chip losses, and possible optimization of the chip integration platform, to allow for hotter operation of the devices without performance degradation (which would reduce the need for cooling).

1) *Concurrent Absorption and Modulation Wavelength Converters*: In these device types, the interaction of photons and electrons happens in adjacent waveguides, where the optical mode overlaps the optical confinement and gain modulation region at the same time (as in an SOA), and the wavelength conversion function is performed through nonlinear behavior in the SOA between the optical mode and the carrier population. This interaction affects both phases and power levels of the signals, which is converted into an amplitude response through a use of an interferometer. In LASOR program, we have demonstrated five generations of tunable CAM wavelength converters operating at 40 Gb/s, with the goal of improving their efficiency, and reducing the footprint.

Two implementations are shown in Fig. 22. Both designs are based on a differentially driven SOA-based MZI. A folded compact version of the device (top, 2.9 mm × 0.8 mm), and a more advanced design in terms of ability to independently control the phase and amplitude (bottom, 6.3 mm × 0.6 mm) are shown. The power dissipation on chip was dominated by the nonlinear SOAs in the branches of the MZ (~1.2 W). The power consumption did scale with bit rate, since higher SOA bias currents were needed at 40 Gb/s to speed up the response of the carriers (0.8 W at 10 Gb/s and 1.2 W at 40 Gb/s).

2) *Photocurrent-Driven Wavelength Converters*: This type of fast widely tunable wavelength converter operates by detecting the optical input using a preamplified photodiode. The photodiode electrode is shared with an optical modulator electrode, which is adjacent to the widely tunable laser, as shown in Fig. 23. Five different generations of these devices were explored, with performance continually improving, and with maximum data rate reaching 40 Gb/s return to zero (RZ), after implementation of low capacitance, traveling wave electrodes.

Constant bias set-point operation of these devices was demonstrated across the data rates of 2.5 to 40 Gb/s, implying the possibility of constant power consumption. However, it is possible to optimize the biasing conditions for lower bit rates, and thus, reduce the consumption in this region of operation. An-

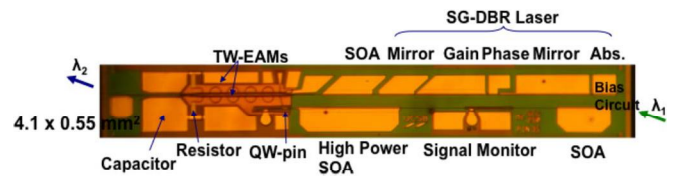


Fig. 23. SAM version of the monolithic fast widely tunable 40 Gb/s wavelength converter.

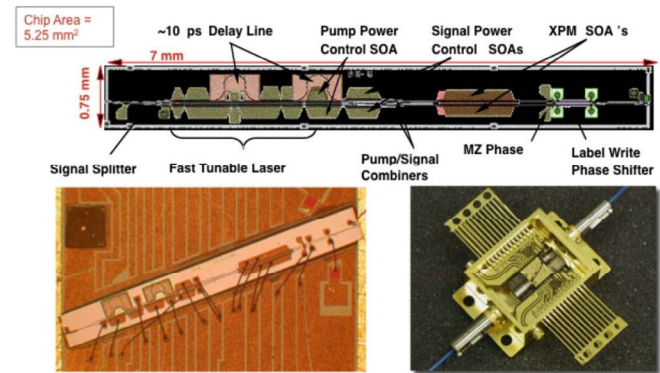


Fig. 24. Differential 40 Gb/s PFC with integrated optical label rewrite (upper), mounted chip on carrier (lower left) and packaged (lower right).

other advantage of this approach is that it does not use large MZI-SOAs, which improves this chip's efficiency significantly. Besides common improvements already discussed, these device types would benefit from more optimized photodetectors (PDs) and modulators. We are now seeing much lower waveguide losses in both the deeply etched structures as well as the QW intermixing (QWI) structures, and we have more ideas, which the modeling indicates should get us to significantly better devices

F. Packet Forwarding Chip

CAM and SAM wavelength converters are used as a building block for the PFCs of the optical switching fabric. The PFC adds to the differential tunable wavelength converter, the function of label modulation is added to the tunable wavelength converter platforms. By using small modifications to the wavelength converter platforms, higher level of integration was achieved with additional power saving. The PFCs illustrates the benefits of integrated photonics, through all the functions it provides: light splitting and amplification, new tunable wavelength generation, label erase function, label rewrite function, and payload wavelength conversion, all at 40 Gb/s line rate, and with less than 6 W (see Fig. 24). Two of the most important features of monolithic integration are stability of phase sensitive delays and preservation of photons by reducing losses normally required moving onto and off of several photonic chips.

G. Monolithic Tunable Optical Router

The MOTOR chip was the next step in evolution of moving the LASOR switching fabric onto a single chip, further improving performance, footprint, and power consumption. Improved energy efficiency is achieved by scaling the number of

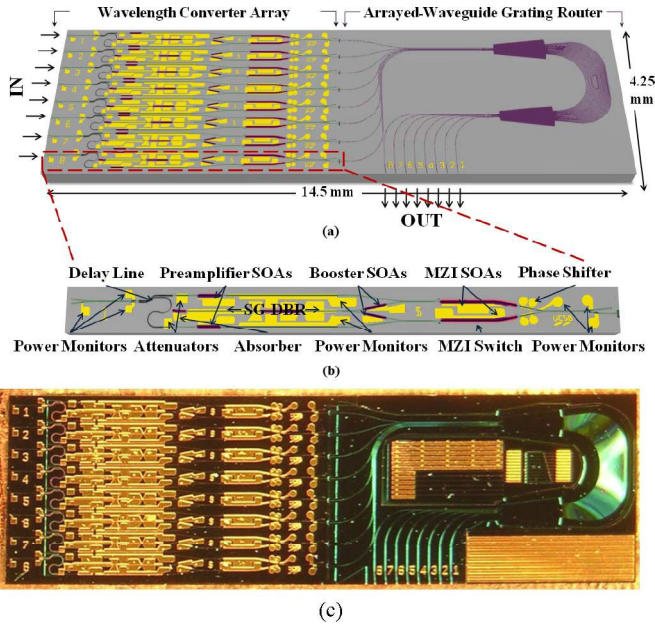


Fig. 25. (a) Diagram of the MOTOR PIC illustrating eight input full-functioning PFCs connected to a low loss 8×8 AWGR. (b) Details of the individual PFCs. (c) Photomicrograph of the device.

photonic elements in a given chip. These large-scale PICs replace many of the high-loss fiber-to-fiber connections between optical components with low-loss waveguide transitions, reducing the amount of power required for functions like signal amplification to compensate for optical losses. For a function with complexity of that of the optical switching fabric, monolithic integration has fairly significant impact.

We demonstrated integration of the elements within the dotted line in Fig. 10. The chip is called a MOTOR chip. The first generation consisted of an array of eight 40 Gb/s wavelength converters and a passive AWGR. The device is one of the most functionally complex InP photonic ICs ever reported, with more than 200 integrated elements in a single chip, including multiple SOAs, a widely tunable sampled grating distributed Bragg reflector (SG-DBR) laser, a passive differential delay line, variable optical attenuators, an AWGR, and phase shifters. Single-channel 40 Gb/s wavelength conversion and channel switching required less than 2 W drive power and showed a power penalty as low as 4.5 dB with a 2^{31-1} pseudorandom binary sequence data signal. MOTOR chip was part of the final technology demo, whose goal was to prove the extent of integration possible in the router optical switch fabric. Therefore, the MOTOR chip consisted of eight CAM PFC chips, integrated with an AWGR, forming an 8×8 optical switch fabric with total capacity of 640 Gb/s and less than 50 W power consumption. At the time of the demonstration, this was one of the most complex PIC chips designed to date (see Fig. 25).

VII. POWER AND BIT-SWITCHING ANALYSIS

The power consumed by the synchronizers and buffers were measured. For the top port, the power consumed by the synchronizer and buffer was 8.2 and 7.7 W, respectively. It is important

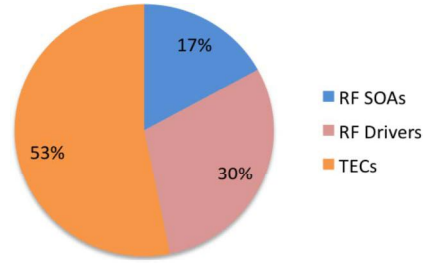


Fig. 26. OPS estimated power consumption breakdown of the total measured power consumption of 7.5 W.

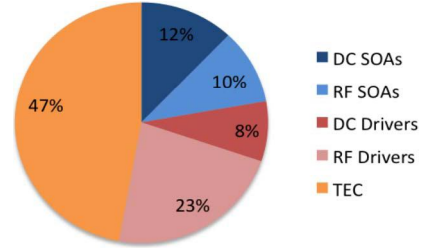


Fig. 27. ORAM estimated power consumption breakdown of the total measured power consumption of 7.7 W.

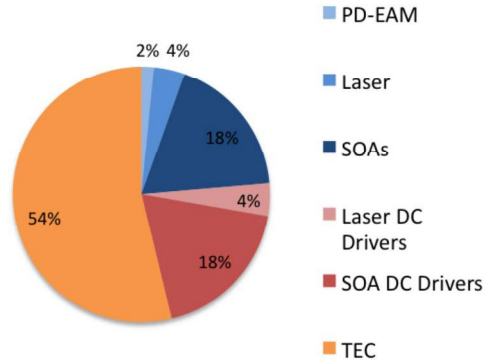


Fig. 28. PFC estimated power consumption breakdown of the total measured power consumption of 5.6 W.

to note that the calculations include the power needed to drive the photonic devices as well as the power required to regulate the temperature of each device. Photonics are highly temperature dependent, therefore, temperature controllers are required for proper operation. Furthermore, the photonic devices require electronic drivers to make the devices operational, so the power consumed in the drivers must go hand in hand with the power consumed in the optics. In order to further investigate, where the majority of power is consumed in the optical technologies, power estimates were calculated for the synchronizer and buffer. Packaged components were used that had the optical devices, electronic drivers, and temperature controllers powered by a common power supply. The power consumption of the optical devices can be estimated assuming that the power consumed was at maximum biasing of the SOAs, and the rest was consumed by electronic power dissipation and temperature control.

The results for the estimated breakdown of power consumed in the OPS, optical buffer, and PFC are shown in Figs. 26–28.

A majority of the power is not consumed in the photonics, but rather in the electronic drivers and temperature controllers. All of the photonic devices required SOAs for switching as well as to compensate for losses due to coupling, splitting, and propagation. If these losses can be reduced, then fewer and smaller SOAs can be used, which would reduce power. Additionally, more efficient SOA technology will further reduce power consumption. It should be noted that in the LASOR experiment, the electronic drivers for operating photonic devices were not optimized for low-power operation.

Using state-of-the-art efficient electronic technologies will reduce this measured component. Most photonic devices are currently highly temperature dependent, therefore, temperature regulation is required, which consumes the majority of power. If alternative means of temperature control that draw less power are implemented or temperature-independent photonics are used, then the power consumed by the photonic devices can be reduced drastically. It should be noted that although the use of synchronous buffers increases total power consumption compared to architectures that do not implement synchronization, overall control logic complexity is reduced that may reduce electronic power consumption.

A rough calculation of the switching energy per bit for the LASOR system demonstration technology can be estimated by the 110 W required to route 640 Gb/s or approximately 0.2 nJ/bit (see Fig. 29). It is important to note this switching energy is achieved with first generation PICs and nonpower optimized support electronics. Compared to the 3 nJ/bit switching energy for today's state-of-the-art router, the initial LASOR work shows potential for orders of magnitude improvement. It is important to emphasize that the LASOR technologies are used as a proof of principle and first-order analysis for power and energy and strict conclusions should not be drawn from these numbers, rather the potential for trends by architecting new packet systems that combine PIC and electronic technologies.

VIII. SUMMARY AND CONCLUSION

In this paper, we have reviewed the role communications interconnects and networks play in the future contribution to the global carbon footprint, especially in data center and cloud-computing applications, which are expected to grow exponentially in traffic. We have also described the potential power consumption savings by integrating photonic technology into system architecture designs along with electronics technology. Key to maximizing the benefits of photonics technology is photonics integration. In the context of an example packet routing system, the DARPA/MTO funded LASOR project, we have reviewed the key PIC functions that have been realized and the power contributions of these PIC technologies as more and more functions are integrated onto a single chip.

We have also quantified, through measurements, the power consumed by the photonics in performing their intended function, the electronics required to bias the photonics, processing electronics, and required cooling technology. In moving the optical forwarding, buffering and other data plane functions to photonics, the dominant contributions to power in packet routing

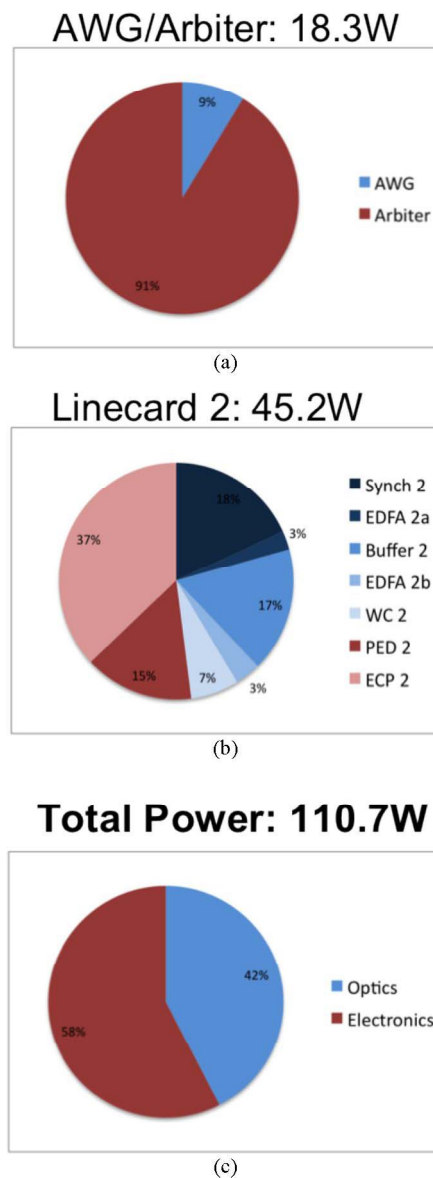


Fig. 29. Power consumption breakdown for the (a) arbiter, (b) line card, and (c) total power consumption for a two line card router.

have moved from the forwarding plane to the packet-processing plane.

There is still much room (potentially greater than 10 \times) for improvement in the forwarding plane in the PIC technology and supporting electronics, however, moving forward the focus will most likely need to be on investigating photonic technologies that can impact the power consumption of the packet forwarding processing plane and in reducing cooling requirements in the data forwarding plane as well as higher levels of monolithic integration.

In the future, as the bit rates increase to 100 Gb/s and beyond, and coherent transmission technologies are employed, LASOR type technologies will need to scale to these new rates and be adapted to new modulation formats. There is also the potential for the Internet to utilize packet sizes greater than 1500 B (e.g., 5000 B super packets), and all the LASOR technologies will work as the packet size increases. The major issue

will be with optical buffering that will require larger storage delays with lower loss waveguides and regenerative buffers. Work is underway to design, fabricate, and test these new LASOR technologies and reports of progress will appear in future publications.

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Daniel J. Blumenthal (S'91–M'93–SM'97–F'03) received the B.S.E.E. degree from the University of Rochester, Rochester, NY, in 1981, the M.S.E.E. degree from Columbia University, New York, NY, in 1988, and the Ph.D. degree from the University of Colorado, Boulder, in 1993.

He is currently a Professor in the Department of Electrical and Computer Engineering, University of California, Santa Barbara (UCSB). He is also the Director of the Terabit Optical Ethernet Center and the LASOR project at UCSB, a project funded by the DARPA/MTO Data in the Optical Domain Network program. He is currently on the Board of Directors for National LambdaRail and on the Internet2 Architecture Advisory Council. He is a Co-Founder of Calient Networks, and more recently, Packet Photonics, LLC. He has authored or coauthored more than 350 papers in various areas. His research interests include optical communications, photonic packet switching and all-optical networks, all-optical wavelength conversion and regeneration, ultrafast communications, InP photonic integrated circuits, and nanophotonic device technologies.

Dr. Blumenthal is a Fellow of the IEEE Photonics and Communications Societies and a Fellow of the Optical Society of America. He is the recipient of a 1999 Presidential Early Career Award for Scientists and Engineers from the White House, a 1994 National Science Foundation Young Investigator Award, and a 1997 Office of Naval Research Young Investigator Program Award.

John Barton, photograph and biography not available at the time of publication.



Neda Beheshti received the B.S. degree from Sharif University of Technology, Tehran, Iran, the M.S. degree from Northeastern University, Boston, MA, and the Ph.D. degree from Stanford University, Palo Alto, CA, all in electrical engineering.

She joined Ericsson Research Lab, San Jose CA, in 2009. Her current research interests include router and switch architectures, wireless networking, and the architecture of the future Internet.

Dr. Beheshti was the recipient of the Best Paper Award of the Internet Measurement Conference 2008

and the Second Best Demo Award of Annual Meeting of the Special Interest Group on Data Communication (SIGCOMM) 2008 for her work on router buffer sizing.



John E. Bowers (F'93) received the M.S. and Ph.D. degrees from Stanford University, Palo Alto, CA.

He was with AT&T Bell Laboratories and Honeywell. He holds the Fred Kavli Chair in nanotechnology and is currently the Director of the Institute for Energy Efficiency and a Professor in the Department of Electrical and Computer Engineering, University of California, Santa Barbara. His research interests include silicon photonic integrated circuits for the next generation of coherent optical systems.

Dr. Bowers is a member of the National Academy of Engineering, and a Fellow of the Optical Society of America (OSA) and the American Physical Society. He is also the recipient of the OSA Holonyak Prize, the IEEE Lasers and Electrooptics Society (LEOS), (now the IEEE Photonics Society) William Streifer Award, and the South Coast Business and Technology Entrepreneur of the Year Award. He was the corecipient of the Annual Creativity in Electronics Award for Most Promising Technology for the hybrid silicon laser in 2007.



Emily Burmeister received the B.S. degree in engineering physics from the University of Michigan, Ann Arbor, MI, in May 2002, and the Ph.D. degree from the University of California, Santa Barbara, in May 2008. Her thesis was titled as Integrated Optical Buffers for Packet-Switched Networks.

She is currently with Ciena Corporation, Linthicum, MD.



Larry A. Coldren (S'67–M'72–SM'77–F'82) received the Ph.D. degree in Electrical Engineering from Stanford University, CA, in 1972.

He is the Fred Kavli Professor of Optoelectronics and Sensors and Acting Richard A. Auhl Dean of Engineering at the University of California (UCSB), Santa Barbara. He joined UCSB in 1984, where he now holds appointments in Materials and Electrical and Computer Engineering. In 1990, he cofounded Optical Concepts, later acquired as Gore Photonics, to develop novel VCSEL technology, and in 1998, he

cofounded Agility Communications, later acquired by JDSU, to develop widely-tunable integrated transmitters. For 13 years, he was at Bell Laboratories, where he was initially involved in wave-guided surface-acoustic-wave signal processing devices and coupled-resonator filters. He later developed tunable coupled-cavity lasers using novel reactive-ion etching technology that he created for the then new InP-based materials. At UCSB, he continued to be engaged in multiple-section tunable lasers, and in 1988 invented the widely tunable multi-element mirror concept, which is now used in some JDSU products. Near this same time period, he also made seminal contributions to efficient vertical-cavity surface-

emitting laser (VCSEL) designs that continue to be implemented in practical devices to this day. More recently, his group has developed high-performance InP-based photonic integrated circuits as well as high-speed VCSELs, and they continue to advance the underlying materials growth and fabrication technologies. He has authored or coauthored over a thousand journal and conference papers, 7 book chapters, 1 textbook, and has been issued 63 patents. He has presented dozens of invited and plenary talks at major conferences.

Dr. Coldren is a Fellow of the Optical Society of America and Institution of Electrical Engineers, a recipient of the 2004 John Tyndall and 2009 Aron Kressel Awards, and a member of the National Academy of Engineering.

Matt Dummer, photograph and biography not available at the time of publication.



Garry Epps has been with Cisco Systems since 1992, where he is now a Distinguished Engineer. During his career at Cisco he has helped pioneer many firsts in the routing industry including ATM and packet over synchronous optical networking (POS) interface technologies. He was one of the lead architects of the widely deployed Cisco 12000 series (GSR) router family, which was the industry's first carrier-grade IP router. He was the architect of several generations of application-specified integrated circuits used for IP packet forwarding. He continues in a leading role in

architecting the next-generation high-end routing platforms within Cisco. He actively participates in research relating to system power reduction and optical packet switching.



Alexander Fang (S'04–M'09) received the B.S. degree in electrical engineering with minors in physics and mathematics from San Jose State University, San Jose, CA, in 2003, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Santa Barbara, in 2005 and 2008, respectively. His Ph.D. dissertation focused on "silicon evanescent lasers."

He is the CEO and co-founder of Aurion, Santa Barbara, CA. He was also with Lawrence Livermore National Laboratory and Intel Prior to founding Aurion.

Alex is a leader in the field of silicon photonics and photonic integrated circuits. He is the author or coauthor of more than 70 papers in his field and has filed 6 patents.

Dr. Fang has won a number of awards for the technology he developed together with Prof. Bowers and colleagues.



Yashar Ganjali (S'03–M'07) received the B.Sc. degree in computer engineering from Sharif University of Technology, Tehran, Iran, in 1999, the M.Sc. degree in computer science from the University of Waterloo, Waterloo, ON, in 2001, and the Ph.D. degree in electrical engineering from Stanford University, Palo Alto, CA, in 2006.

He is currently a Faculty Member in Computer Science Department, University of Toronto, Toronto, ON. His research interests include packet-switching architectures/algorithms, network protocols and measurement, network management, and online social networks.

Dr. Ganjali was the recipient of several awards for his research including Best Paper Award in Internet Measurement Conference 2008, Best Paper Runner up in Conference on Information Communications Marketplace (INFOCOMM) 2003, Best Demo Runner up in Annual Meeting of the Special Interest Group on Data Communication (SIGCOMM) 2008, Best Demo in NetFPGA Workshop 2009, Leaders Opportunity Fund from Canada Foundation for Innovation, and Cisco Research Award.

John Garcia, photograph and biography not available at the time of publication.

Brian Koch, photograph and biography not available at the time of publication.

Vikrant Lal, photograph and biography not available at the time of publication.

Erica Lively, photograph and biography not available at the time of publication.

John Mack, photograph and biography not available at the time of publication.



Kim Nguyen received the B.S. and M.Eng. degrees from the University of Louisville, Louisville, KY, in 2005 and 2007, respectively. She is currently working toward the Ph.D. degree at the University of California, Santa Barbara.

Her research interests include photonic integrated circuits, advanced modulation formats, coherent optical receivers, and optical regenerators.



Steven C. Nicholes received the B.S. degree in chemical engineering from Brigham Young University, Provo, UT, in 2005, and the Ph.D. degree in materials from the University of California, Santa Barbara in 2009. His Ph.D. thesis focused on the design, growth, and fabrication of large-scale photonic integrated circuits.

Since 2009, he has been with Aurrion, LLC, Santa Barbara, CA, where he is involved in silicon photonics.

Hyundai Park, photograph and biography not available at the time of publication.



Milan Mašanović (S'98–M'04) received the Dipl. Ing. degree from the School of Electrical Engineering, University of Belgrade, Belgrade, Yugoslavia, and the M.S. and Ph.D. degrees from the University of California at Santa Barbara, Santa Barbara, in 1998, 2000, and 2004, respectively, all in electrical engineering.

He is currently an Adjunct Assistant Professor at the University of California at Santa Barbara, and a principal and a founder of Freedom Photonics LLC, a photonic integration company in Santa Barbara, CA.

He is the author or coauthor of more than 75 research papers. His current research interests include InP photonic integration related to applications in packet-switched optical networks.

Dr. Mašanović was the recipient numerous awards and fellowships, including the 2004 IEEE Lasers and Electro-Optics Society Graduate Student Fellowship Award and the 2003 Best Student Paper Award at the Indium Phosphide and Related Materials Conference.



Biljana Stamenic received the Dipl. Ing. and the M.S. degrees in metallurgy of nonferrous metals from the School of Technology and Metallurgy University of Belgrade, Belgrade, Yugoslavia, in 1994 and 1999, respectively, all in metallurgy engineering. Her M.S. thesis focused on metallurgy of nonferrous metals.

From 1994 to 1999, she was a Research Assistant at the Institute for Technology of Nuclear and Other Mineral Row Materials, Belgrade. From 2002 to 2006, she was a Device Fabrication Technician at DuPont Displays, Santa Barbara, CA. She is currently

a Senior Development Engineer at the University of California at Santa Barbara, where the majority responsibilities of her work include layout and prototyping of the advanced photonic integrated circuit chips and fabrication process development duties related to device fabrication.



Nick McKeown received the B.E. degree from the University of Leeds, Leeds, U.K., in 1986, and the Ph.D. and M.S. degrees from the University of California, Berkeley, in 1995 and 1992, respectively.

He is currently a Professor of Electrical Engineering and Computer Science, and the Faculty Director of the Clean Slate Program at Stanford University, CA. From 1986 to 1989, he was with Hewlett-Packard Labs, Bristol, England. In 1995, he assisted architect Cisco's GSR 12000 router. In 1997, he cofounded Abrizio, Inc., (acquired by PMC-Sierra), where he

was CTO. He was also the cofounder and CEO of Nemo ("Network Memory"), which is now a part of Cisco. His research interests include the architecture of the future Internet, and tools and platforms for networking teaching and research.

Dr. McKeown is the STMicroelectronics Faculty Scholar, the Robert Noyce Faculty Fellow, a Fellow of the Powell Foundation, the Alfred P. Sloan Foundation, the Royal Academy of Engineering (U.K.), and the Association for Computing Machinery (ACM). He is the recipient of a CAREER award from the National Science Foundation. In 2000, he received the IEEE Rice Award for the best paper in communications theory. In 2005, he was awarded the British Computer Society Lovelace Medal, and in 2009 the IEEE Kobayashi Computer and Communications Award.



Anna Tauke-Pedretti (S'02–M'08) received the B.S. degree in physics and electrical engineering from the University of Iowa, Iowa City, in 2001, and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of California, Santa Barbara, in 2002 and 2007, respectively. Her Ph.D. dissertation focused on the design, fabrication, and testing of InP-based photonic integrated circuits for high-speed wavelength conversion.

In 2008, she joined Sandia National Laboratories, Albuquerque, NM, as a senior member of technical staff, where she continues to be involved in the development of novel photonic integrated circuits. Her current research interests include optical injection locking, high-speed modulators, and high-power integrated receivers.

Henrik Poulsen, photograph and biography not available at the time of publication.

Matt Sysak, photograph and biography not available at the time of publication.

Photonic Integrated Circuits for Optical Routing and Switching Applications

Milan L. Mašanović, Jonathon S. Barton, John Parker, Steven Nicholes, Emily F. Burmeister,
Biljana Jevremović, John E. Bowers, Larry A. Coldren, Daniel J. Blumenthal

Electrical and Computer Engineering Department, University of California at Santa Barbara, Santa Barbara, California 93106-9560
mashan@ece.ucsb.edu

Abstract: We report on the latest advances in implementation of integrated photonic components required for optical routing and switching: tunable wavelength converters, mode-locked lasers, active optical switches and optical buffers.

OCIS codes: (060.1810) Buffers, couplers, routers, switches, and multiplexers; (250.3140) Photonic integrated circuits

1. Introduction

Optical networking allows for reconfiguration of large data bandwidth directly in the optical layer, with little electronic processing required in the data plane. Optical circuit switching (wavelength routing) is supported in the currently deployed second generation of optical networks. With further increases in traffic in optical networks, optical packet switching and routing technologies hold promise to provide the largest granularity with more efficient power and footprint scaling, relative to electronic processing [1,2]. Integration of the switching and routing function onto photonic integrated circuits has been a major contributing factor in the optical network development, and it will be required for future improvements and implementations of novel switching functions in optical networks.

Some of the key photonic functions that are of interest for optical routing and switching, and that will be covered in this paper are: widely tunable and fast wavelength-switched integrated optical transmitters and transceivers/wavelength converters, which form the core of wavelength and packet switch fabric; mode-locked laser technologies, which can be used for optical signal regeneration; active optical switch/router cores, used as a more integrated version of the optical switch fabric; and optical buffers, needed to mitigate the contention between different packets directed to the same switch output port. These photonic functions have been investigated and realized by our team at U.C. Santa Barbara, mainly as part of DARPA/MTO DOD-N program's sponsored Label Switched Optical Router project (LASOR) [1]. The final goal of this program was a 100 Terabit optical router demonstration.

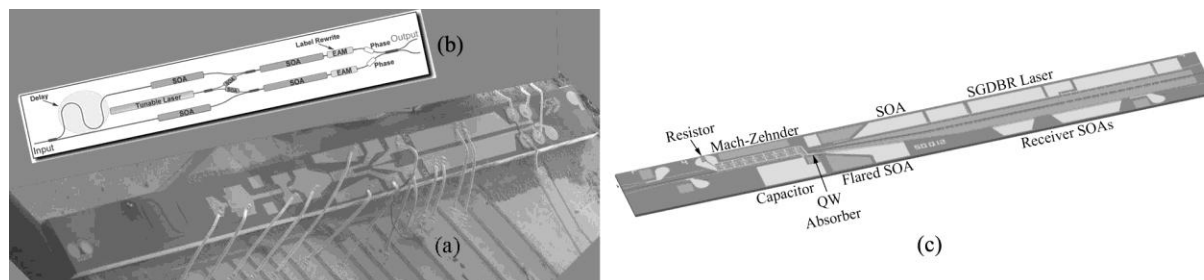


Figure 1 – (a) 40 Gbps MZI-SOA packet forwarding chip (PFC) electron micrograph (b) PFC schematic (c) 40 Gbps separate absorption and modulation (SAM) tunable wavelength converter

2. Widely Tunable and Fast Switchable Optical Transmitter and Wavelength Converter Technologies

Wide tunability in optical PICs is an attractive feature, as it allows for a single PIC to be used for wavelength and packet routing across an entire optical band. The wavelength tuning/switching speed requirement is determined by the actual application in the network: while milliseconds are adequate for optical circuit and protection switching, optical burst switching requires <100 ns speeds, and optical packet switching <5ns speeds. Carrier injection tuned lasers, with proper emphasis can achieve around 50 ns of tuning speed [3]. Dual laser implementations have been demonstrated for nanosecond speed applications [3]. Fast wavelength tuning enables packet forwarding in an optical router, where the payload is wavelength converted to a new wavelength corresponding to the desired output port. There are two main mechanisms exploited for monolithically integrated tunable wavelength converters – non-linear effects in a semiconductor optical amplifier (SOA) caused by the pump-probe signal interaction [4], and traveling wave effects of signal detection and remodulation in a photodiode-modulator based system [5,6]. 40 Gbps, error

free, RZ data operation of both MZI-SOA and separate absorption and modulation (SAM) tunable device types has been achieved (Figure 2). In addition, fully integrated packet forwarding chips (PFC), operating with 40 Gbps payloads and 10 Gbps labels have been successfully demonstrated and used in optical switch demonstrations,[1].

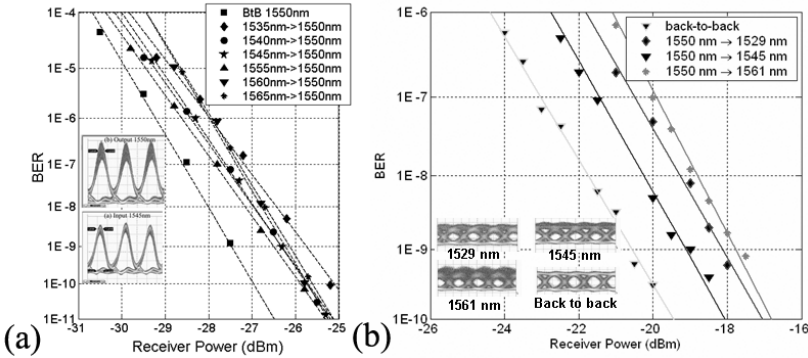


Figure 2 – (a) PFC - Bit error rate results for 40 Gbps RZ operation (b) SAM - Bit error rate results for 40 Gbps NRZ operation

In SAM devices, a transmitter and a preamplified photodiode are monolithically integrated on a single chip. The photodiode is directly connected to the modulator through an on-chip terminated traveling wave electrode, allowing the photocurrent from an absorbed input signal to directly drive an optical modulator. Since the photodiode produces enough photocurrent to drive the optical modulator there is no need for any electrical amplification. Due to the spatial separation of the receiver and transmitter waveguides, SAM wavelength converters have no optical filtering requirements. Additionally, bit rate transparent operation had been achieved [6].

3. Monolithic Mode-Locked Lasers

Mode locked lasers (MLLs) are key components for 3R regeneration applications in optical networks. Some qualities of MLLs utilized in optical clock recovery are their ability to perform jitter reduction, pulse reshaping, and amplification. Since the frequency of mode locking is determined by the cavity length, traditional MLLs with cleaved facets are not reproducible at a specific frequency. Thus, special MLL designs, with non-facet determined cavities and compatible with further integration into complex 3R PICs, such as [10], are of particular interest.

Previously, our team members have experimentally demonstrated optical clock recovery using a novel mode-locked laser (MLL) [8] monolithically integrated with an output semiconductor optical amplifier. The laser’s distributed Bragg reflector (DBR) mirror positions are determined using lithography, allowing for mode locking and clock recovery at the exact frequency of the design (35.00 GHz), which is easily scalable to 40 GHz or higher. More recent work in this area has yielded an integrated InGaAsP/InP ring mode-locked laser with a gain flattening filter that doubles the locking bandwidth and decreases the pulse width from 840fs to 620fs [9], shown in Figure 3. The laser design and fabrication platform are compatible with other photonic integrated circuit components, enabling integrated signal processing using these MLLs in the future.

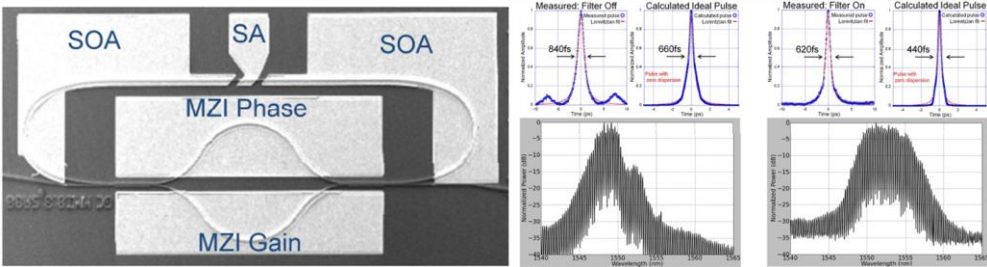


Figure 3 – (left) Electron micrograph of a mode-locked laser with an integrated Mach-Zehnder gain filter for flattening. (right) Optical spectra and pulse shapes and widths with the optical filter turned on, and off.

4. Optical Switches

Monolithic integration of a fast switch fabric for an optical router has been performed by incorporating 8 MZI-SOA tunable wavelength converters operating at 40 Gbps and an arrayed waveguide grating on a single chip [10]. The Monolithic Tunable Optical Router (MOTOR) chip contains more than 200 integrated functional elements. The device schematic, and the bit error rate measurements at 40 Gbps are shown in Figure 4. The integration platform supports both active and low-loss elements using a novel, single regrowth, quantum-well intermixing approach. This

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platform allowed us to reduce absorption losses in the AWGR and delay line regions by exploiting an undoped InP setback layer in the passive sections of the device while optimizing active functions. The chip has 3 different waveguide types: a surface ridge waveguide design in the wavelength converter section, a high-contrast deeply etched waveguide in the delay line for compactness, and a buried rib waveguide in the AWGR region for low scattering losses.

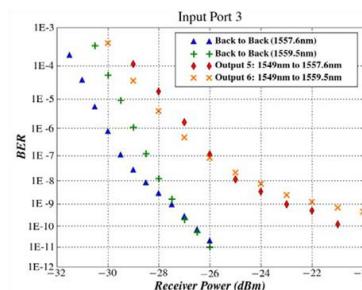
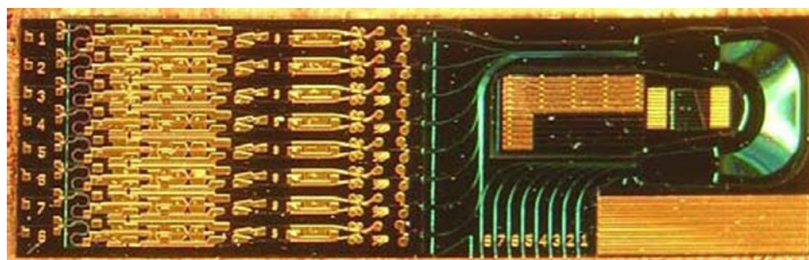


Figure 4 – Photograph of fabricated 8-channel MOTOR device; Bit error rate testing results, showing error-free operation at 40 Gbps

5. Integrated Optical Buffers

The realization of practical optical memory elements to resolve packet contention is necessary before optical routers can become viable. The most successful optical buffering demonstrations have used either feedback or feed-forward buffers, many of which implement two-by-two or one-by-two switches [7]. We have developed a simple recirculating buffer that operates without additional control components in the delay loop. Up to 184 ns of storage was demonstrated with greater than 98% packet recovery for 40 Gb/s, 40-byte packets, Figure 3. To the authors' knowledge, this device has the best performance for a buffer approach amenable to integration. Further work on all photonic chip based buffers is underway.

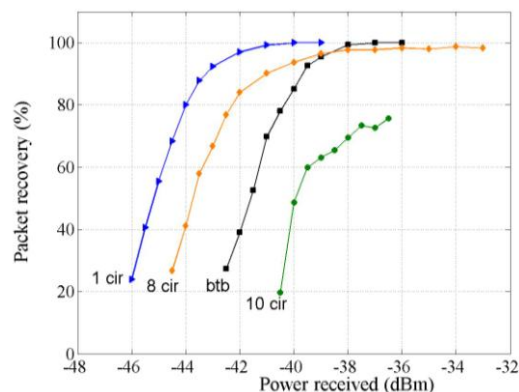
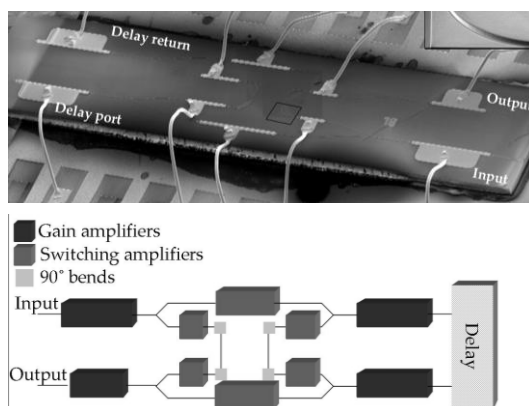


Figure 5 (top-left) Schematic of 2x2 switch with amplifiers (bottom left) SEM image of the switch affixed and wire-bonded to a submount (right) Packet recovery of 98% for up to 8 circulations (184 ns delay).

This work is supported by DARPA and the Army under contract #W911NF-04-9-0001.

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8-channel InP Monolithic Tunable Optical Router for Packet Forwarding

Steven C. Nicholes^{*}, Milan L. Mašanović[†], Biljana Jevremović[†],
Erica Lively[†], Larry A. Coldren^{†,*}, and Daniel J. Blumenthal[†]

^{*}Department of Materials

[†]Department of Electrical and Computer Engineering
University of California, Santa Barbara 93106

Email: snicholes@engineering.ucsb.edu

Abstract: Advancements in photonic integration allow development of complex, large-scale circuits suited for future optical packet switched networks. We review our 8-channel InP monolithic tunable optical router chip capable of 40 Gbps operation per port.

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OCIS codes: (250.5300) Photonic integrated circuits; (130.0250) Optoelectronics

1. Introduction

Optical packet switching (OPS) is a potential option to deal with the increasing power demands of future networks as data rates scale [1]. If packets at a router node remain in the optical layer, many of the power-consuming optical-to-electrical and electrical-to-optical data conversions could be eliminated. In order for OPS to become competitive with traditional electronic routers, the functions of dynamic buffering, wavelength conversion and packet forwarding must be available in low-power, multi-channel, small-footprint photonic modules. Large-scale photonic integration has emerged as a commercially viable approach that may be able to meet these demands in the near future [2].

In this paper, we review our 8-channel monolithic tunable optical router (MOTOR) chip designed for optical packet forwarding at a data rate of 40 Gbps per port [3]. This device demonstrates the switching core of a label-switched optical router (LASOR), developed at UC Santa Barbara [4]. The InP/InGaAsP device combines more than 200 functional elements in a single chip and consists of an array of 8 widely-tunable wavelength converters (TWC) with a passive 8x8 arrayed-waveguide grating router (AWGR). Single-channel error-free wavelength conversion and switching has been demonstrated with the device at bit-error rates below 10^{-9} .

2. Device Design

As shown in Fig. 1, the MOTOR chip replaces an array of discrete tunable wavelength converters and a discrete AWGR in the LASOR architecture. Several different monolithic approaches to 40 Gbps wavelength conversion have been realized in the past few years, but these were typically single-port devices [5-7]. Because MOTOR combines eight independent channels on the same chip, we use an SOA-based approach to wavelength conversion similar to [5] as it is simpler to fabricate. However, these TWCs still have a high degree of complexity, each consisting of a sampled-grating DBR (SG-DBR) laser, semiconductor optical amplifiers (SOAs) with different desired levels of linearity, passive phase shifters, MMIs, and variable optical attenuators (Fig. 2). Unlike the 8x8 routing switch of [8] that was limited to only 10 Gbps per port, our TWC architecture incorporates an integrated differential waveguide delay line in each channel to enable operation at 40 Gbps. However, this delay line creates a switching window that requires an RZ data modulation format at high-speeds.

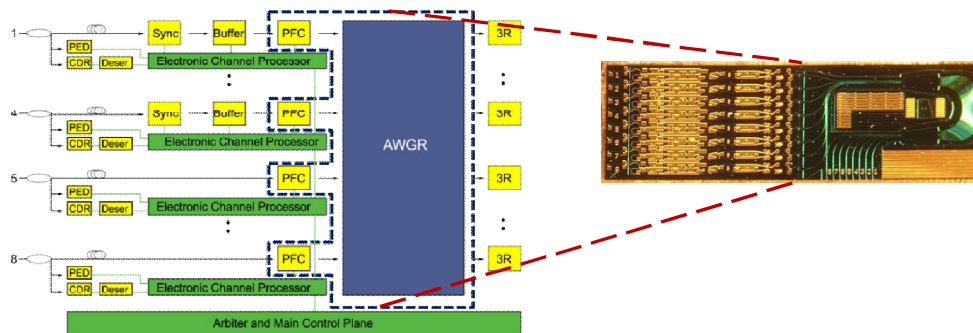


Figure 1. Schematic of the LASOR router. The discrete array of 8 WCs and the AWGR can be replaced by a single MOTOR chip.

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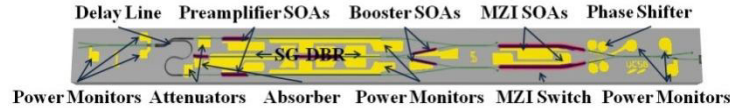


Figure 2. Schematic of a single MOTOR input TWC showing monolithic integration of many “off-the-shelf” components.

The photonic integration scheme used for the MOTOR chip was designed with a view towards fabrication simplicity. Because yield was our major concern, we sought to minimize the process risk wherever possible. Inevitably, this means not all device components can be simultaneously optimized. Future improvements to device performance are therefore possible with more complex integration platforms, which are more suitable to an industrial environment and require better process control. Our device employs a robust quantum-well intermixing technique to create active and passive band-edges [9] and only one epitaxial regrowth to clad the waveguide. We also use 3 different waveguide architectures across the chip to better optimize particular functions and components. This includes a surface ridge waveguide in the wavelength converter section, a high-contrast deeply etched waveguide in the differential delay line region, and a buried rib waveguide in the AWGR region.

3. Device Performance

The fabricated chip was soldered to a copper block and held at a constant temperature of 16°C during operation. The performance of the AWGR was measured using SOAs within the TWCs as on-chip amplified spontaneous emission (ASE) sources. First, SOAs in a single TWC were forward biased and the output of each egress port of the AWGR was fiber coupled to an optical spectrum analyzer (OSA) (Fig. 3a). We measured a well-defined response with an average channel spacing of 1.36 nm, corresponding to 173 GHz at 1536.2 nm (the design target was 200 GHz). The free spectral range (FSR) for the 8-port router was measured to be approximately 11.1 nm and the single-channel crosstalk was between -15.8 to -20.9 dB across all eight output ports. Next, the SOAs of each TWC were biased one at a time and the spectrum was measured from a constant output port (Fig. 3b). This measurement shows some deviation in crosstalk performance between different TWCs, likely due to fabrication variations across the device. With the AWGR response mapped, we then demonstrated the switching capacity of the device by tuning the SG-DBR signal to each of the different allowed output wavelengths of a given port (Fig. 3c).

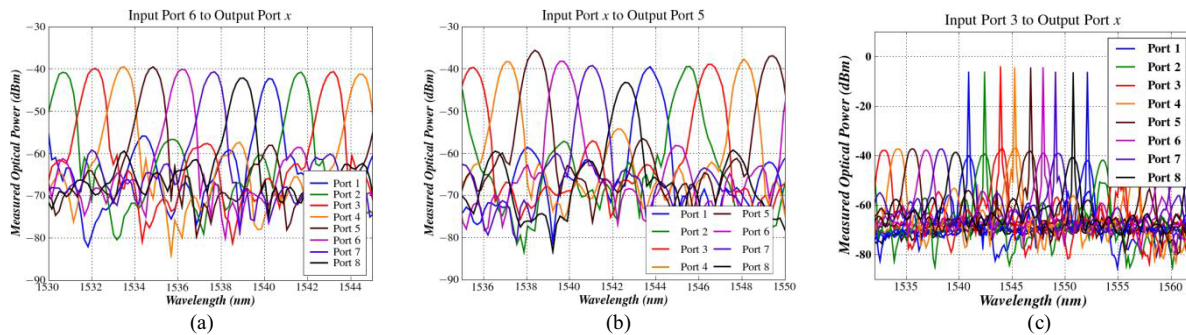


Figure 3: (a) measured AWGR response to ASE from input WC port #6 at each output port; (b) measured AWGR response at output port #5 from each input WC port; and (c) lasing spectra at different SG-DBR biasing conditions (the ASE spectrum for that channel is superimposed).

The wavelength conversion and routing capacity of MOTOR were next tested using a single input channel. The LASOR router is designed to operate with 40 byte packets, but we used longer PRBS data streams at 40 Gbps to better gauge device performance. The initial RZ data pattern was generated and amplified off-chip and then transmitted through an attenuator (to control the input power level), a 5-nm filter (to remove ASE from the EDFA), and a polarization controller (to ensure TE polarization) before it was coupled into the chip. The fiber-coupled output signal was passed through a 5-nm filter to remove the original input signal and was then transmitted to a preamplified receiver. Bit-error-rate (BER) measurements were made using a 40 Gbps SHF BERT.

Fig. 4a shows the BER for wavelength conversion and routing of a 2^7-1 PRBS using a single input channel at multiple output ports. Power penalties as low as 3.5 dB at a BER of 10^{-9} were measured. The pattern length was then increased to $2^{31}-1$ bits (Fig. 4b) and power penalty increased to 4.5 to 7 dB depending on the input/output port combination used. A noticeable error floor is apparent at low BERs with longer pattern lengths but open eyes were still obtained for all output ports. This increased power penalty is believed to be the result of nonlinearities in

preamplifier SOAs at the front-end of the WCs. These SOAs are used only to amplify the input data signal prior to wavelength conversion and hence should be linear. In the future this could be overcome by adjusting our integration platform to enable highly linear SOAs or lower loss optical waveguides to reduce the required input power level.

Under normal operating conditions, the single-channel drive power of the device is less than 2 W. An additional ~ 0.5 W was required for TEC cooling. This translates into an overall power consumption of 0.0625 W/Gbps. The TEC demand and overall drive power will increase with multiple channels running, but it unknown how this will scale. Thermal crosstalk between channels could also lead to higher required bias levels.

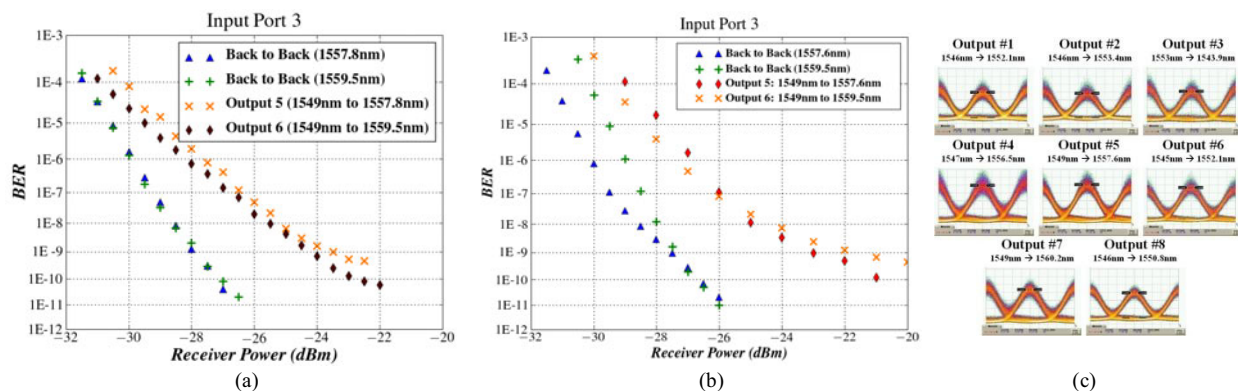


Figure 4. Single-channel BER measurements at: (a) 2^7-1 data rates; (b) $2^{31}-1$ data rates; and (c) open eye diagrams at $2^{31}-1$ data rates.

4. Future Implementation

These results suggest the future potential of a label-switched router architecture with a switch fabric based on photonic ICs. However, there are still hurdles to reach a commercial technology maturity level. For instance, reduction in power consumption is still needed to make our approach competitive with electronic routers. From the perspective of the MOTOR chip, efforts to improve our metallization schemes indicate we can appreciably reduce our probe pad contact resistance to lower our drive power. Furthermore, implementing an optimized packaging scheme can help with heat sinking to reduce the TEC drive requirements. This will be especially important for multi-channel operation where thermal crosstalk will impact performance.

5. Acknowledgements

This work was funded by DARPA MTO and the Army under the DOD-N LASOR Project (W911NF-04-9-0001). Fabrication was done in the UCSB nanofabrication facility, part of the NSF funded NNIN network.

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Plenary Session

11.30 to 12.10

“Photonic ICs for Coherent Communications and Sensors”



Larry A. Coldren,
Univ. of California, Santa Barbara

Abstract: Photonic ICs for Coherent Communications and Sensors-- The integration of many photonic components on a single chip has been shown to improve the efficiency of both transmitter and receiver systems as well as their size, weight and overall power consumption. As the technology has improved the performance is now also exceeding that of discrete solutions in

many cases. Many years ago a key driver for photonic integration was the enhanced receiver sensitivity achievable in coherent communication systems. Somewhat ironically, as the need for more spectral efficiency, spectral selectivity, overall system efficiency, and cost have become critical issues today, coherent communication and sensor systems now again look to integrated coherent solutions. In this presentation we explore recent developments.

Biography: **Larry A. Coldren** is the Fred Kavli Professor of Optoelectronics and Sensors and Acting Richard A. Uhll Dean of Engineering at the University of California, Santa Barbara, CA. After receiving his Ph.D. Electrical Engineering from Stanford University and spending 13 years in research at Bell Laboratories, he joined UC-Santa Barbara in 1984 where he now holds appointments in Materials and Electrical & Computer Engineering. In 1990 he co-founded Optical Concepts, later acquired as Gore Photonics, to develop novel VCSEL technology; and in 1998 he co-founded Agility Communications, later acquired by JDSU, to develop widely-tunable integrated transmitters.

At Bell Labs Coldren worked on surface-acoustic-wave filters and later on tunable coupled-cavity lasers using novel reactive-ion etching (RIE) technology. At UCSB he continued work on multiple-section tunable lasers, in 1988 inventing the widely-tunable multi-element mirror concept, which is now used in numerous commercial products. Near this same time, he also made seminal contributions to efficient vertical-cavity surface-emitting laser (VCSEL) designs that continue to be implemented in practical devices. More recently, Prof. Coldren's group has developed high-performance InP-based photonic integrated circuits (PICs) as well as high-speed VCSELs, and they continue to advance the underlying materials growth and fabrication technologies.

Professor Coldren has authored or co-authored over a thousand journal and conference papers, a number of book chapters, a textbook, and has been issued 64 patents. He has presented dozens of invited and plenary talks at major conferences, he is a Fellow of the IEEE, OSA, and IEE, a recipient of the 2004 John Tyndall and 2009 Aron Kressel Awards, and a member of the National Academy of Engineering.

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**Photonic ICs for Coherent
Communication
and Sensing**

Larry A. Coldren

Fred Kavli Professor of Optoelectronics and Sensors

L. Johansson, M. Rodwell, M. Lu, A. Sivanathan,
J. Parker

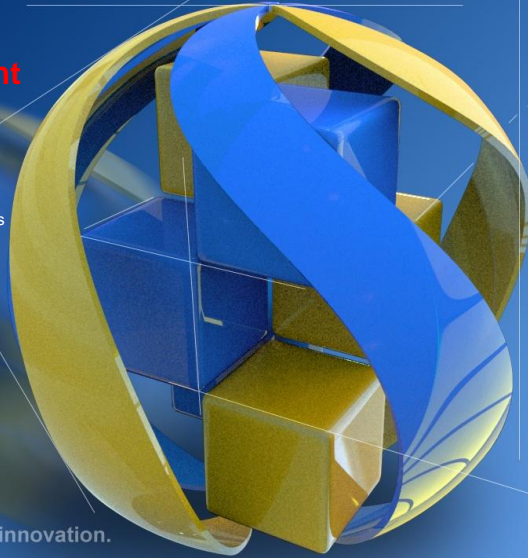
ECE and Materials Departments
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Acknowledgements

Funding from: DARPA, Rockwell-Collins

Content contributions from: P. Winzer, C. Joyner, B.
Mason, M. Minneman and R. Tkach

The convergence of research and innovation.



- Photonic ICs and coherent approaches are not new ideas, and in fact, synergistic
- Coherent for fiber optics delayed by WDM → due to EDFA
- PIC technology continued to develop (for WDM) → power (energy efficiency) a key attribute
- Coherent makes a comeback—mostly due to spectral efficiency, not sensitivity (spectral selectivity still important)
- Heterodyne vs. Intradyne—optical phase locked loops (OPLLs) for energy efficiency in sensors and communication
- Concepts & results for OPLL-based transmitters and receivers

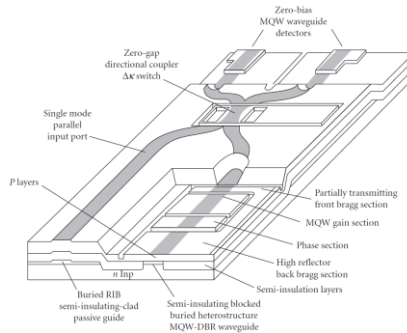
but these goals also motivated Photonic Integration activities

• In the 1980's coherent communication was widely investigated to increase receiver sensitivity and repeater spacing. It was also seen as a means of expanding WDM approaches because optical filters would not be so critical.

Y. Yamamoto and T. Kimura, "Coherent optical fiber transmission systems," *IEEE J. Quantum Electron*, vol. 17, no. 6, pp. 919-925, Jun. 1981.

• This early coherent work drove early photonic integration efforts—Stability; enabled phase-locking
T. L. Koch, U. Koren, R. P. Gnall, F. S. Choa, F. Hernandez-Gil, C. A. Burrus, M. G. Yung, M. Oron, and B. I. Miller, "GainAs/GainAsP multiple-quantum-well integrated heterodyne receiver," *Electron. Lett.*, vol. 25, no. 24, pp. 1621-1623, Nov. 1989

Integrated Coherent Receiver



• The EDFA enabled simple WDM repeaters (just amplifiers) and coherent was put on the shelf



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KEY FEATURES AND PRODUCT HIGHLIGHTS

- Easily locate, identify and troubleshoot macro-bends, splices, connectors and breaks
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- Look inside components to evaluate each interface for RL and IL
- Measure 30 m with 10 μm resolution in less than 7 seconds
- Continuously measure a 1 m segment at up to 3 Hz
- Test and troubleshoot short-run networks (<2 km)
- Automate pass/fail verification of fiber assemblies
- Monitor distributed temperature and strain profiles along network or inside a component or module

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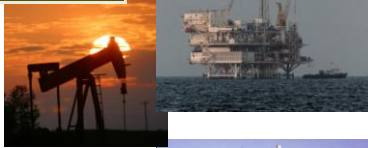
MEASUREMENT PERFORMANCE HIGHLIGHTS

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- 70 dB dynamic range
- 2 kilometer length range with no dead-zone
- Micrometer resolution up to 70 meters
- < 0.05 dB insertion loss resolution

The OBR 4600 offers unbeatable testing and troubleshooting capabilities now at unprecedented measurement speeds.

The convergence of research and innovation.

Oil & Gas



Structures



Aerospace



Bragg gratings:

- Temperature
- Pressure
- Displacement / Strain
- Damage/Delamination

Coherent Fiber Sensing

- Distributed Acoustics
- Vibration
- Flow
- Intrusion
- Perimeter Monitoring



New lasers, such as all-semiconductor very high-speed swept lasers (>kHz rates), are enabling new methodologies (photo courtesy of Insight Photonic Solutions)

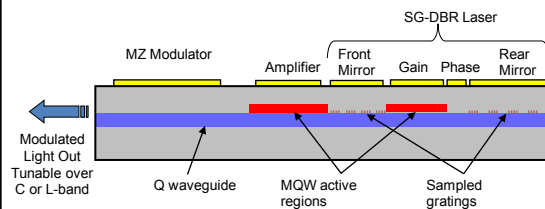
The convergence of research and innovation.

SGDBR+X widely-tunable transmitter:

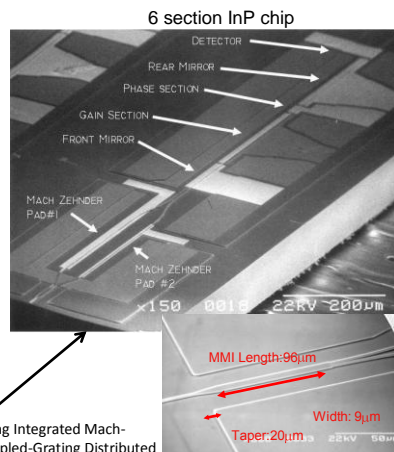
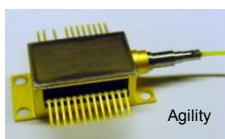
- Foundation of PIC work at UCSB

"Multi-Section Tunable Laser with Differing Multi-Element Mirrors," US Patent # 4,896,325 (January 1990)

(UCSB'90-- → Agility'99-'05 → JDSU'05→)



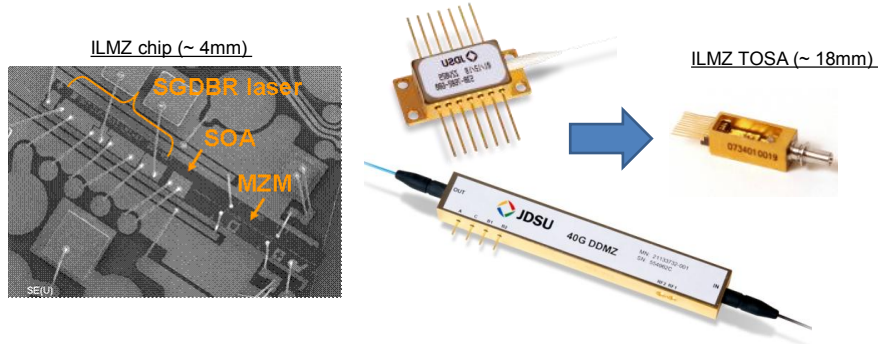
- Vernier tuning over 40+nm near 1550nm
- SOA external to cavity provides power control
- Currently used in many new DWDM systems (variations)
- Integration technology for much more complex PICs



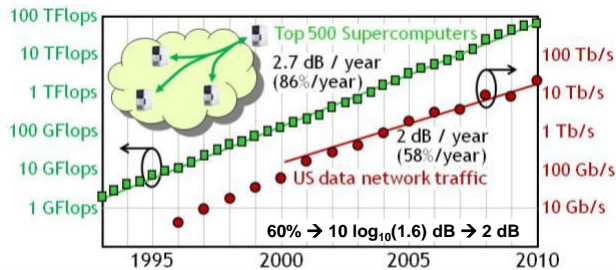
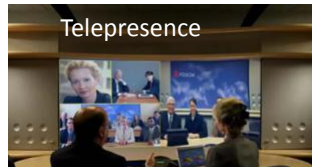
J. S. Barton, et al, "Tailorable Chirp using Integrated Mach-Zehnder Modulators with Tunable Sampled-Grating Distributed Bragg Reflector Lasers," ISLC, TuB3, Garmish, (Sept, 2002)

The convergence of research and innovation.

- Volume deployment typically needs form factors optimized for port count, size, power dissipation and cost
 - Transceiver module form factors are MSA driven and ecosystem is more mature
 - Photonic integration is essential to achieve cost, power and size roadmap
 - ILMZ is a good example of photonic integration



The convergence of research and innovation.

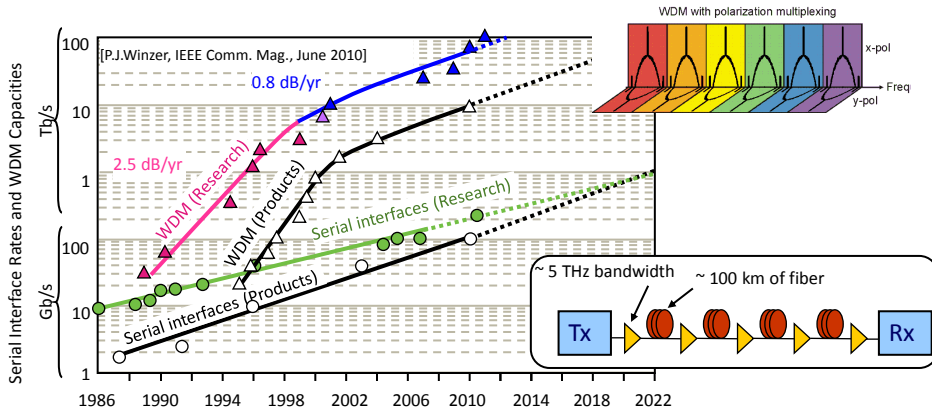


Exponential network traffic growth is driven by high-bandwidth digital applications
Video-on-demand, telepresence, wireless backhaul, cloud computing & services

Courtesy P. Winzer

Scaling spectral efficiency through WDM

The convergence of research and innovation.



~10 Terabit/s WDM systems are now commercially available

~100 Terabit/s WDM systems have been demonstrated in research

Growth of WDM system capacities has noticeably slowed down

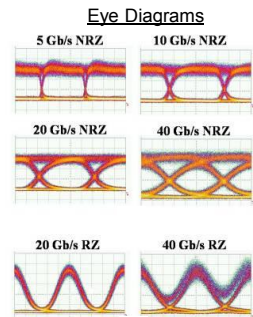
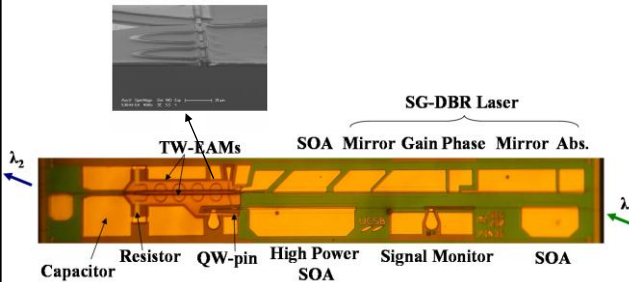
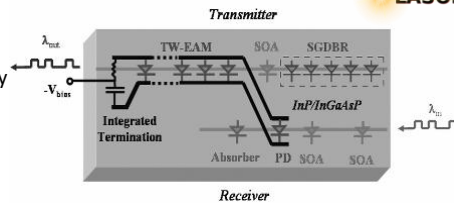
Courtesy P. Winzer

Evolution of InP Integration technology enables more functionality: (transceiver/wavelength-converter)

The convergence of research and innovation.

High-efficiency SOA-PIN Receiver & SGDBR-TW/EAM Transmitter

- Data format and rate transparent 5-40Gb/s
- No filters required (same λ in and out possible)
- Two-stage SOA pre-amp for high sensitivity & efficiency
- 2R regeneration possible
- Traveling-wave EAM with on chip loads; ~ 0 dB out/in optical insertion loss
- Only DC biases applied to chip—photocurrent directly drives EAM \rightarrow 1W/40 Gb/s \rightarrow 25 pJ/bit
- 40 nm wavelength tuning range

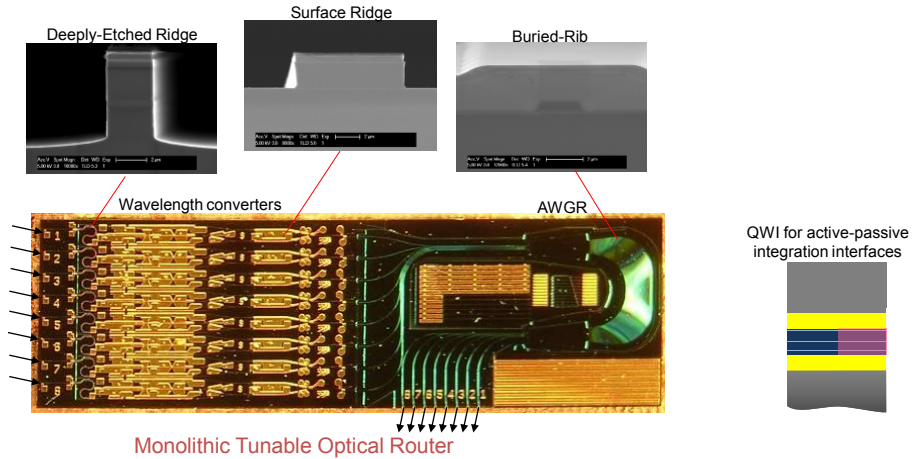


M. Dummer et al. Invited Paper Th.2.C.1, ECOC 2008.

More functionality: 8 x 8 MOTOR Chip: (40 Gb/s per channel)

The convergence of research and innovation.

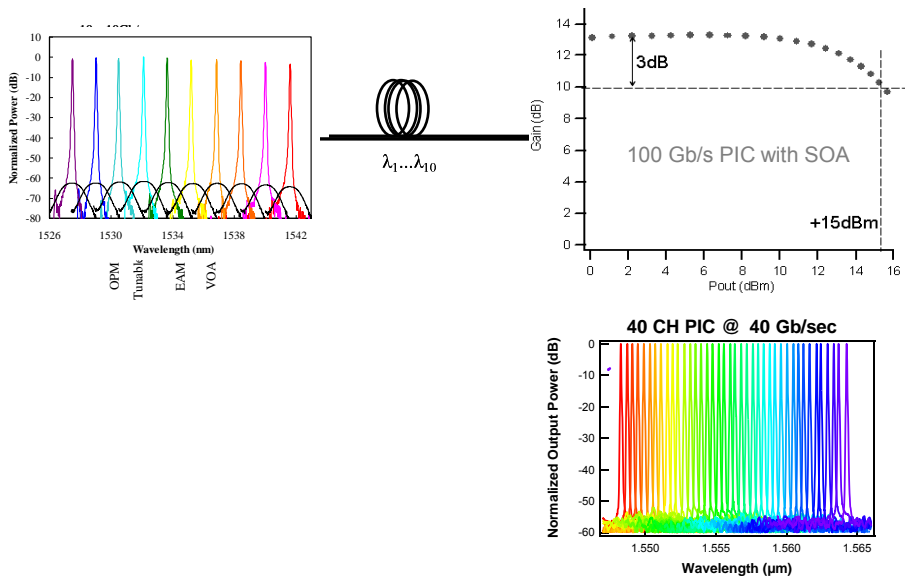
- 8 x 8 'all-optical' crossbar switch
- SOA – Mach-Zehnder Wavelength Converters
- Quantum-well intermixing (QWI) to shift bandedge for low absorption in passive regions
- Three different lateral waveguide structures for different curve/loss requirements
- Single 'blanket' regrowth—Vendor growth, regrowth, & implants



See S. Nicholes, et al, "Novel application of quantum-well intermixing implant buffer layer to enable high-density photonic integrated circuits in InP," *IPRM '09*, paper WB1.2, Newport Beach (May, 2009)

Infinera Commercial WDM PICs: Parallel Integration

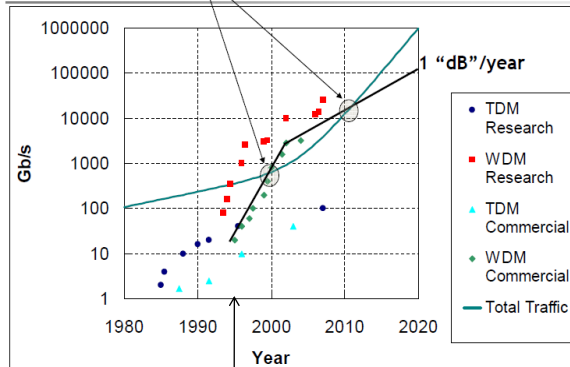
The convergence of research and innovation.



Courtesy C. Joyner

- Spectral efficiency increases accompanying WDM not enough

Two Special Years 2000 and 2011



Introduction of EDFA and WDM
→ OEO repeaters vastly reduced

Courtesy Bob Tkach

- Vector modulation/coherent detection utilizes full complex field to enhance spectral efficiency
- Increase bit-rate without increasing baud rate

Binary modulation formats

(1 bit/symbol):

- Optical duobinary / PSBT

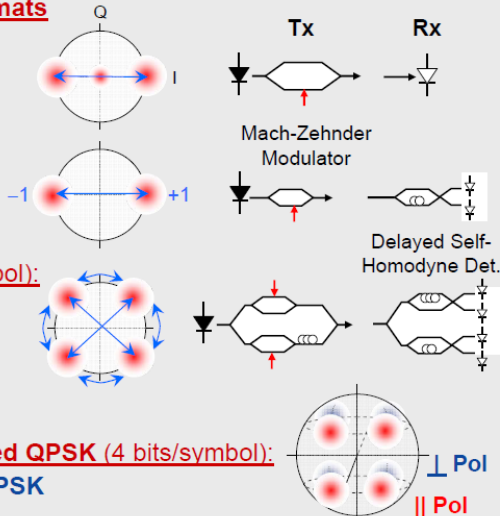
- NRZ- / RZ-DPSK ("bipolar" ASK)

Quaternary (2 bits/symbol):

- NRZ- / RZ-DQPSK

Polarization-multiplexed QPSK (4 bits/symbol):

- Dual-Polarization QPSK

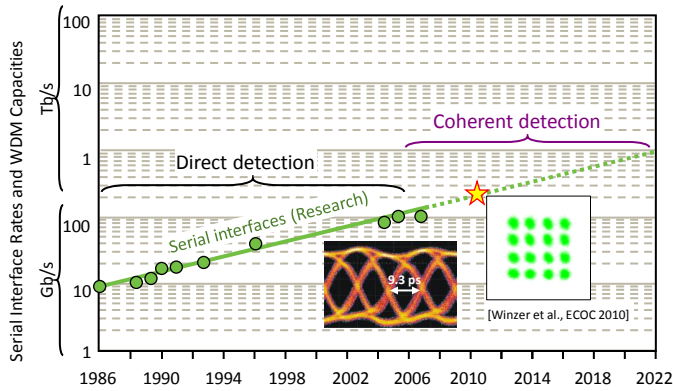


Other approaches for S.E. improvement include QAM (both amplitude and phase) and OFDM (Orthogonal Frequency Division Multiplexing → no guardbands)

Courtesy B. Mason

The evolution of high-speed optical interfaces

The convergence of research and innovation.



Optical interfaces switched to coherent detection at 100 Gbit/s

Higher spectral efficiency

More networking flexibility through digital signal processing (CD, PMD, filters)

400-Gbit/s interfaces have been demonstrated in research

(200 Gb/s per polarization)

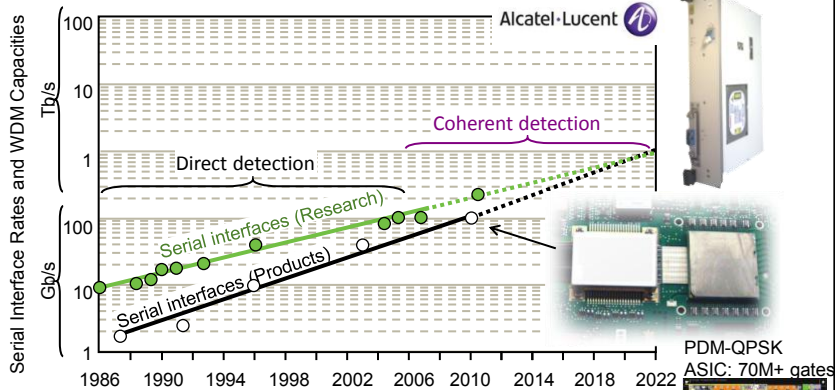
CD: Chromatic dispersion

PMD: Polarization-mode dispersion

Courtesy P. Winzer

The evolution of high-speed optical interfaces

The convergence of research and innovation.



100-Gbit/s interfaces are commercially available (June 2010)

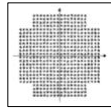
Consistent exponential growth of interface rates ...

... but only at ~0.5 dB/year

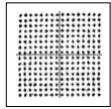
Courtesy P. Winzer

Increase modulation complexity or Baud rate?

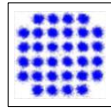
The convergence of research and innovation.



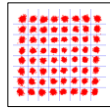
PDM 512-QAM
3 GBaud (54 Gb/s)
[Okamoto et al., ECOC'10]



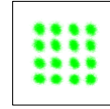
PDM 256-QAM
4 GBaud (64 Gb/s)
[Nakazawa et al., OFC'10]



PDM 32-QAM
9 GBaud (90 Gb/s)
[Zhou et al., OFC'11]



PDM 64-QAM
21 GBaud (256 Gb/s)
[Gnauck et al., OFC'11]

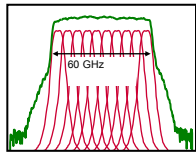


PDM 16-QAM
56 GBaud (448 Gb/s)
[Winzer et al., ECOC'10]



- More parallel channels
- More 'linear' electronics needed

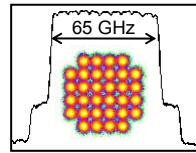
- More dispersion/impairments
- Costly/non-existent electronics



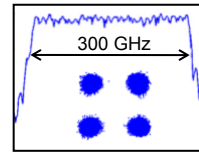
448 Gb/s (10 subcarriers) 16-QAM
5 bit/s/Hz
2000 km transm.
[Liu et al., OFC'10]



Or, use superchannels??



606 Gb/s (10 subcarriers) 32-QAM
7 bit/s/Hz
2000 km transm.
[Liu et al., ECOC'10]

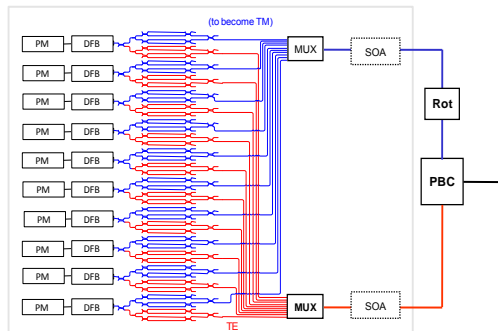


1.2 Tb/s (24 subcarriers) QPSK
3 bit/s/Hz
7200 km transm.
[Chandrasekhar et al., ECOC'09]

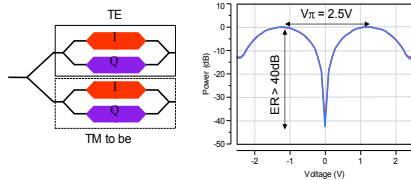
Courtesy P. Winzer

Infinera Coherent PIC Architecture: 400 Gb/sec PM-DQPSK Transmitter—parallel + serial integration

The convergence of research and innovation.



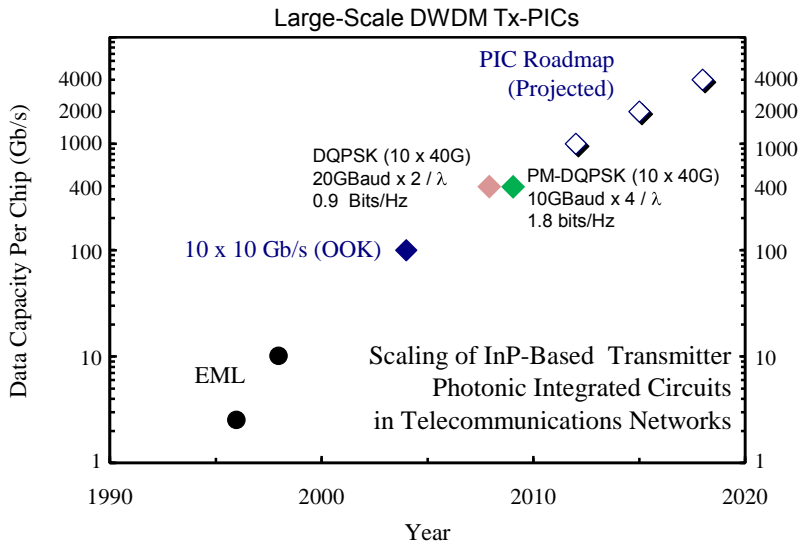
PM-DQPSK (10 x 40G)
10GBaud x 4 / λ
1.8 bits/Hz



Vector Modulation

C. Joyner, P. Evans, S. Corzine, M. Kato, M. Fisher, J. Gheorma, V. Dominic, P. Samra, A. Nilsson, J. Rahn, A. Dentai, P. Studenkov, M. Missey, D. Lambert, R. Muthiah, R. Salvatore, S. Murthy, E. Strzelecka, J. Pleumeeckers, A. Chen, R. Schneider, R. Nagarajan, M. Ziari, J. Stewart, F. Kish, and D. Welch, "Current View of Large Scale Photonic Integrated Circuits on Indium Phosphide," OFC, San Diego, CA, Mar. 21-25, 2010, OWD3.

Courtesy C. Joyner



Courtesy C. Joyner

Courtesy Bob Tkach

System Evolution Roadmap

| 1990s | 2000 | 2010 | 2020 |
|--------------------------|----------------------|-----------------------|-----------------------|
| 2.5-10 Gb/s channel rate | 10 Gb/s channel rate | 100 Gb/s channel rate | 1 Tb/s ! channel rate |
| 8, 16, 40 Channels | 100 Channels | 100 channels | 100 Channels |
| 20-160 Gb/s Capacity | 1 Tb/s Capacity | 10 Tb/s Capacity | 100 Tb/s Capacity |
| SE = .025-.05 | SE = 0.2 | SE = 2.0 | SE = 20 ! |
| History | History | Achieved | Needed |

SE = Spectral Efficiency = Channel Rate / Channel Spacing

Even with this aggressive 2020 target, traffic growth will exceed capacity growth by a factor of 10

13 | R. W. Thomas | OFSA Annual Forum 2009 | 3 December 2009

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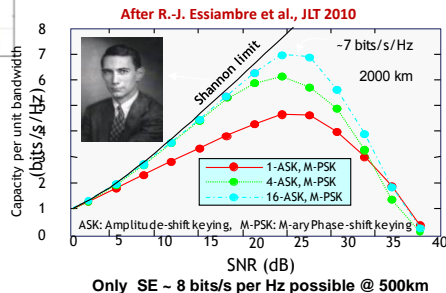
Alcatel-Lucent

• Must make vast improvements in Spectral Efficiency (SE) → Bits/s/Hz of bandwidth to meet demand

• But, complex modulation formats are called for, and these require high-dynamic range

• Excess fiber capacity disappears after 2015 → lay more standard fiber, use multicore fiber, or multimode, or ??

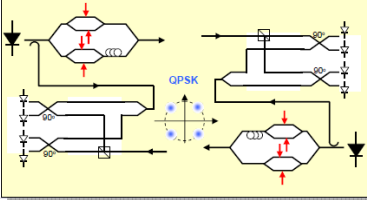
• Going parallel may be better than continuing to evolve more complex modulation formats



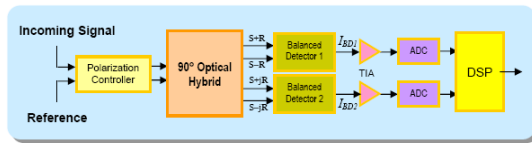
Intradyne or Heterodyne for generic sensor and short-reach communication applications?

Intradyne Coherent Detection

- Phase and polarization diversity
- Frequency-locked local oscillator
- Digital signal processing of received electrical signals
 - Electronic CD compensation
 - Electronic polarization demultiplex
 - Adaptive PMD compensation



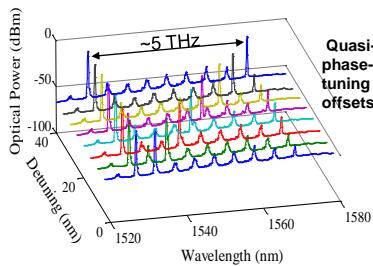
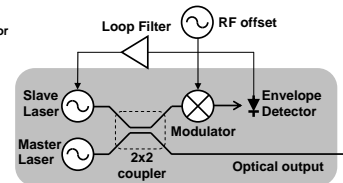
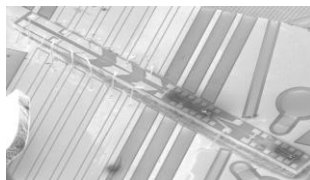
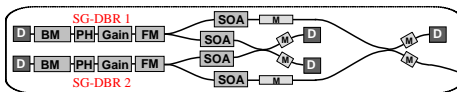
Typical Intradyne receiver architecture



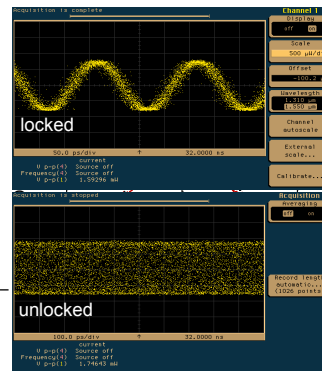
- ❖ Use 'Intradyne' without phase-locked LOs, or do we need true Heterodyne detection?
 - Desire data-rate independent generic chips—when are phase-locked narrow-linewidth LOs desired?
 - High-speed A/Ds & DSPs require lots of power and are expensive to design, especially as data rate increases
 - Some impairments can be removed with much slower, lower-power, lower-cost signal-processing circuits

Integrated Optical Phase Locked Loops (OPLLs): provide a new stable control element

Offset locking of two SGDBRs → viable using close integration of PICs with electronics in a OPLL



Quasi-continuous phase-locked digital tuning up to 5 THz offsets possible

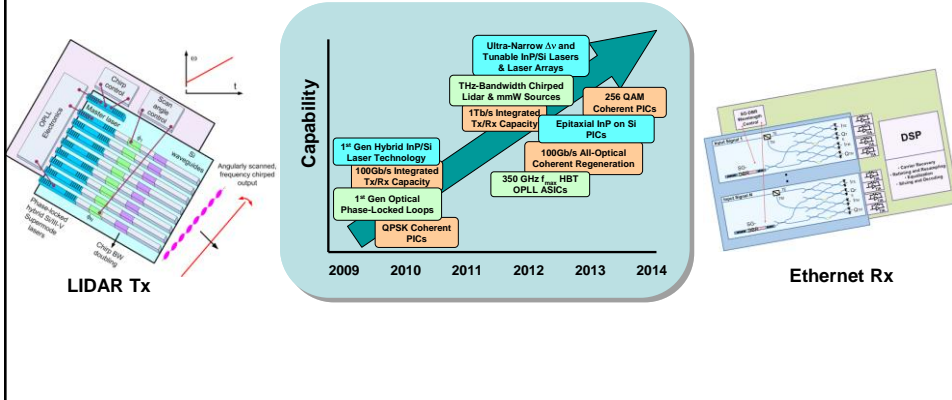


Ristic, et al: JLT v.28 no.4, pp526-8, Feb., 2010

Coldren, Bowers, Rodwell, Johansson (UCSB),
Yariv (Caltech), Koch (Lehigh), Campbell (UVA), Ram (MIT)

Goal: Create a new generation of photonic integration engines that provide unprecedented and practical control of optical frequency and phase, driving a level of sophistication that is routine today for RF into the optical domain.

- Enabling revolutionary capabilities in sensing & communications
- Advancing the intimacy of electronic and photonic integration with new monolithic and hybrid materials as well as integration platforms



Coherent receiver

Costa's Loop for BPSK, QPSK demodulation
Complex DSP circuits not required, but simpler ones can be added for CD and PMD
Challenge: Develop receivers for high speed (>100Gbaud) or high constellations (n-QAM)
Matched with development of coherent sources

LIDAR

Very rich/challenging area
Locking tunable lasers
Arrays of locked OPLLs
Swept microwave reference
Time / Phase encoding of directed output
Need for rapid scanning and locking rates

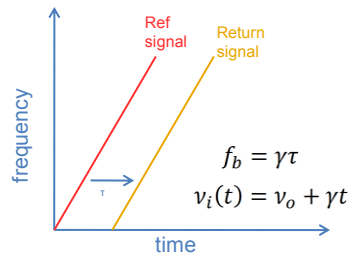
mmW / THz generation

Locking of two tunable lasers
Requires high-speed, high-power UTC photodiode
Speed determined by UTC photodiode and feedback electronics: Can be very high
Combined with antenna designs for complete TRX links with free-space path

All require close integration of electronics with photonics

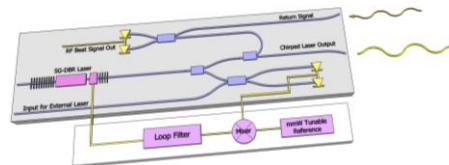
The convergence of research and innovation.

- Spatial Resolution related to Frequency Span
 - SG-DBR has 5 THz tuning range → 30 μm resolution
 - $\Delta z_r = \frac{c}{2n_g \Delta \nu_s}$
- Range $\sim c/(\pi \Delta \nu)$;
 - For 100 kHz linewidth, range could be 750m



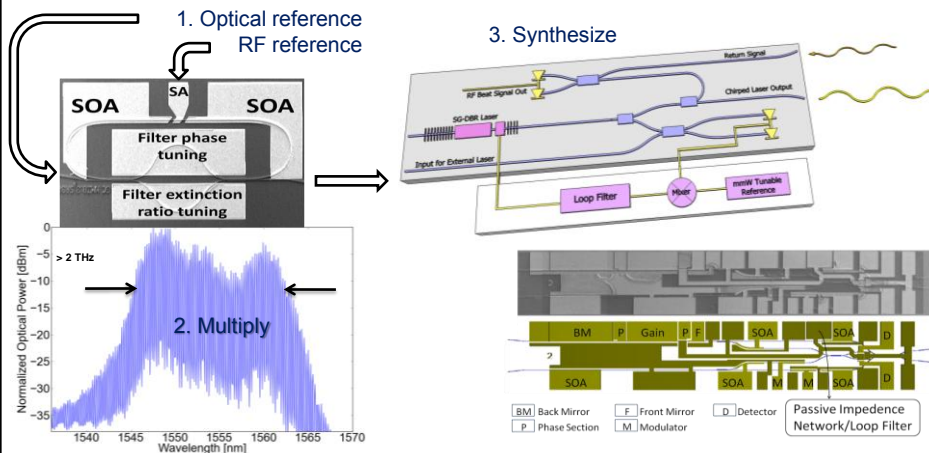
Integrated LIDAR Transmitter

- SG-DBR Laser
- Balanced Detectors
- MMI Couplers
- Modulators
- 90 Degree Hybrid
- Transmission Lines



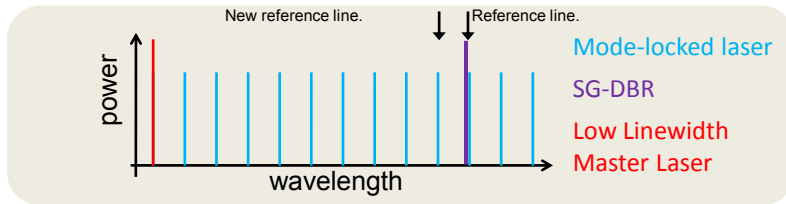
The convergence of research and innovation.

- Multiply RF reference to $>2\text{THz}$ (5 THz projected) using gain-flattened mode-locked laser (MLL)
- Phase-lock widely tunable LIDAR transmitter with sub-Hz relative accuracy
- $>2\text{ THz}$ Swept LIDAR or pulse-compression LIDAR waveforms available

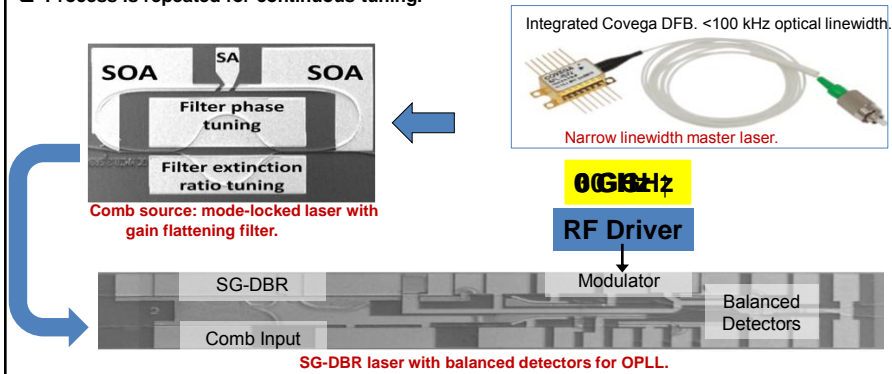


Tuning Across the Comb

The convergence of research and innovation.

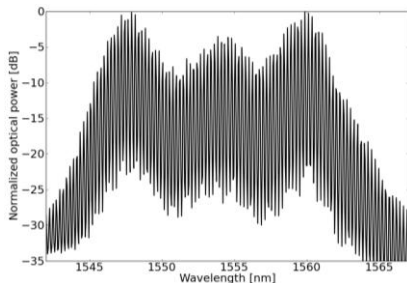


- Frequency offset is increased until adjacent reference line can be locked at DC.
- Process is repeated for continuous tuning.



Broadband Comb Generation

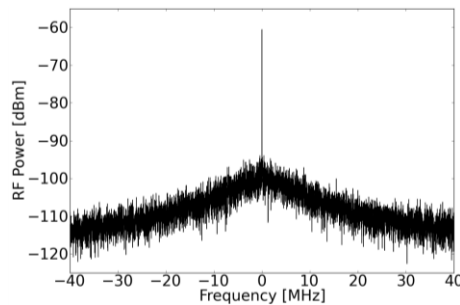
The convergence of research and innovation.



Measured 2 THz comb span from gain flattened MLL under hybrid mode-locking.

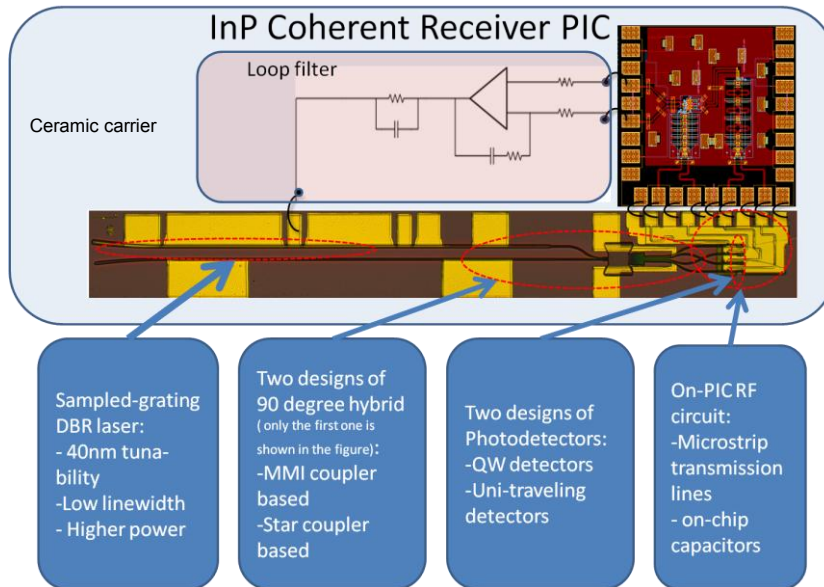
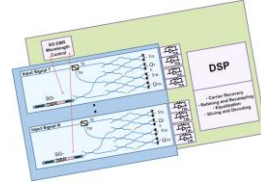
- With hybrid mode-locking (using an RF reference) the RF linewidth is < 10 Hz.
- This corresponds to the frequency error over the entire comb.
- < 10 Hz error over a 2 THz range.

- Comb spans over 2 THz have been demonstrated with the current gain flattened mode-locked laser.
- There are 70 lines spaced by ~29.6 GHz.
- This far exceeds the spans available without the use of the gain flattening filter.



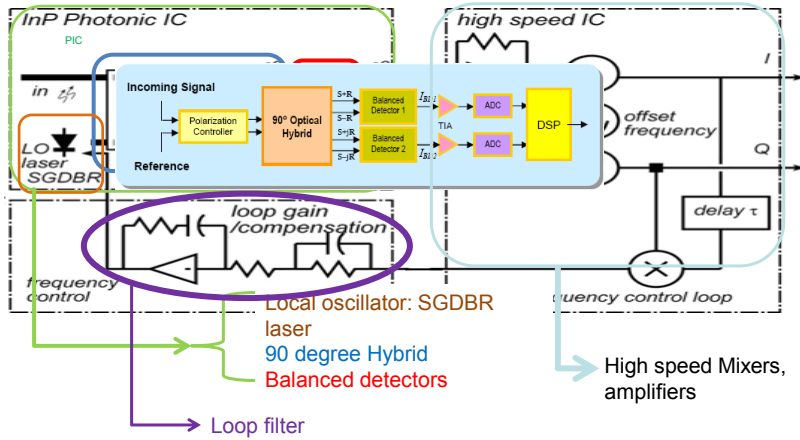
Measured RF power at 29.6 GHz, from a high-speed photodiode with electrical signal analyzer (ESA). FWHM < 10 Hz. (RBW = 30 KHz).

- Advantages of coherent receivers
 - Tolerance to noise
 - Compatibility with different modulation formats
 - No optical filter needed to demultiplex WDM channels
- Typical limitations and drawbacks
 - Phase noise limitation -- LO laser linewidth
 - For Intradyne, high-speed DSP is required
 - [High power consumption](#)
 - High design and [production cost](#)
 - Limited speed
- Alternative -- Coherent receivers with OPLL (Costa's loop)
 - No phase and frequency tracking and correction
 - Lower relative LO phase noise
 - Low power, [high-efficiency](#) solution
 - Cannot pre-correct for large impairments



The convergence of research and innovation.

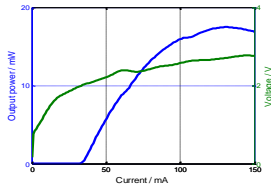
Coherent receiver with a free-running LO (Intradyn):



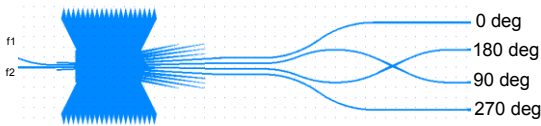
Optical Phase-Locked Loop (OPLL) with frequency lock (data removal also designed in)

The convergence of research and innovation.

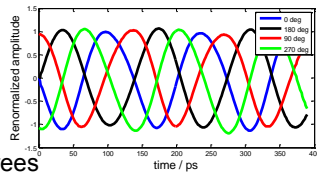
- SG-DBR laser
 - 20mW output power
 - 40 nm tuning range
 - 40mA threshold current



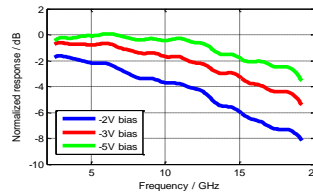
- Novel 2-by-4 Star coupler



- Phase error between I and Q is within 3 degrees



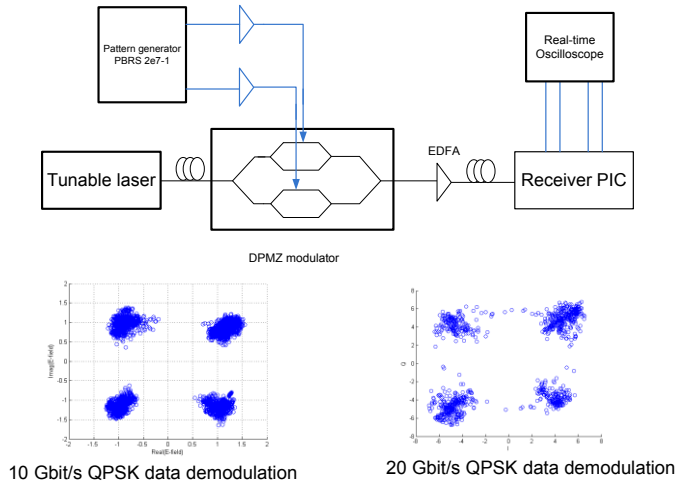
- QW photodetector (same as gain regions)
 - 18 GHz 3-dB bandwidth with -5V bias



PIC Testing (no feedback)

The convergence of research and innovation.

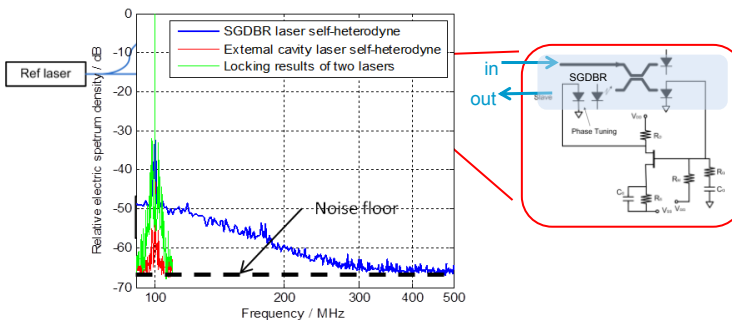
- As a QPSK coherent receiver
 - Back-to-back measurement
 - 10 Gbit/s and 20 Gbit/s signals were demodulated



Homodyne Locking (Loop filter only)

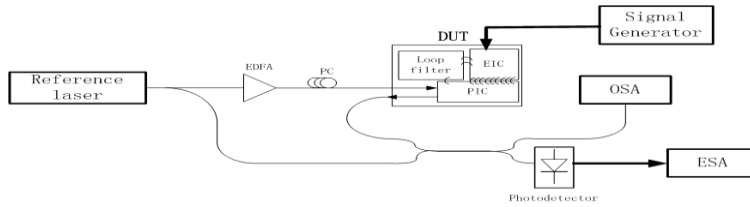
The convergence of research and innovation.

- Phase-lock SG-DBR L.O. laser to reference laser
 - Design loop bandwidth: $\sim 1\text{GHz}$
 - Using HEMT based active loop filter



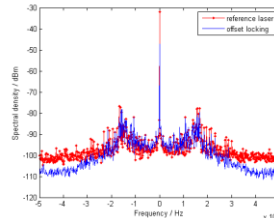
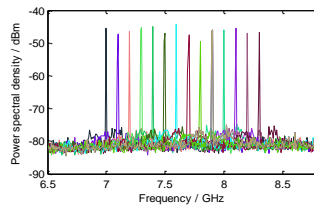
- Issue: For high input signal levels, injection locking observed due to intra-chip reflections

- Test setup



- Preliminary offset locking results

- Successfully lock at 3.5 -11 GHz offset frequency range (identical linewidth to reference)
- Illustrate frequency sweeping between 7-8.3 GHz



- 5.5 GHz offset locking
- SGDBR completely 'clones' reference—even its sidelobes
- $\Delta\lambda < 100$ kHz

- Active InP-based Photonic ICs can be created with size, weight, power and system performance metrics superior to discrete solutions in many situations. If produced in some volume, the cost can be much lower.
- Coherent approaches will be greatly improved by the use of Photonic Integration, and numerous sensor applications may be enabled in addition to higher-spectral-efficiency communications.
- Efforts to increase the spectral efficiency of communication systems employing coherent approaches using vector modulation and reception with increasingly complex formats have yielded significant advances; however, the cost is significant, and we appear to be approaching practical limits. Parallel paths may be a practical alternative to higher levels of QAM.
- Close integration of control/feedback electronics will be desirable in many future PIC applications—it is required for Optical Phase Locked Loops (OPLLs) with conventional semiconductor lasers, but efficiency can be high.
- OPLL-based transmitters and receivers, incorporating all of the photonics on a single PIC, have demonstrated Hz-level relative frequency accuracy, and duplication of the linewidth and noise levels of the reference source.

I. Photonic Integrated Circuits

B. Ring Lasers and Filters

Compact InGaAsP/InP Flattened Ring Lasers with Etched Beam Splitters

John S. Parker¹, Erik J. Norberg¹, Yung-Jr Hung², Robert S. Guzzon¹, Larry A. Coldren¹

¹Electrical and Computer Engineering Department, University of California at Santa Barbara, Santa Barbara, CA 93106-9560

²Department of Electronic Engineering, National Taiwan University of Science and Technology, 43 Keelung Rd., Sec. 4, Taipei 106, Taiwan

Corresponding Author: jparker@ece.ucsb.edu

Abstract: We present results from novel compact InGaAsP/InP based flattened micro-ring resonators and lasers. Resonators with circumferences 30-300 μm by using etched beam-splitters (EBS) are demonstrated. EBS coupler insertion loss is measured as low as 0.6dB.

OCIS codes: 230.5750 Resonators, 250.5300 Photonic integrated circuits

1. Introduction

Ring resonators are a critical building block in a variety of photonic components including: optical switches [1], serial and cascaded filters [2], tunable lasers [3], optical memory elements [4], tunable optical delay lines [5], and biosensors [6]. The multitude of uses for rings makes them extremely versatile in photonic integrated circuits (PICs) as a single dry etch can be used to define a variety of functional elements. Furthermore, low-cost photolithography can be used for the entire mask set, whereas the alternative for integrated cavities using gratings requires expensive electron-beam lithography or holography. Small active rings with a large free spectral range (FSR) are needed in channelizing filters for wavelength-division-multiplexing (WDM) and narrowband optical pre-filtering to reduce the data load before analog-to-digital conversion. In addition, smaller rings have a reduced cavity flight time allowing for faster optical switching and routing, and more rapid state changes in optical memory. As ring dimensions are reduced, smaller footprints for the functional elements and lower energy consumption makes compact rings an economically viable choice for the next generation of PICs.

The length of traditional ring resonators is limited by the size of the directional or multi-mode interference (MMI) coupler used. From recent ultra-compact coupler fabrication in InP (without the use of electron-beam lithography), a 55 μm directional coupler [7] and a 20 μm MMI coupler [8] were demonstrated. Traditional ring lengths are typically $>4x$ larger than the coupler, that is $>80\mu\text{m}$.

Etched beam-splitter (EBS) couplers rely on evanescent wave coupling across a narrow lower index gap by the process of Frustrated Total Internal Reflection (FTIR). EBS couplers with straight connecting waveguides have been demonstrated in GaAs [9-10] and InP [11] for use as add-drop filters. The EBS couplers have a sub-micron footprint making them ideal for use in compact resonators. The flattened ring resonator uses a radius of curvature $3x$ larger than the traditional ring resonator or racetrack resonator; this is made possible because the flattened ring requires arcs to cover only 120° of a full circle while each EBS coupler reflection adds an additional 120° . As ring radius is reduced, the highly confined optical mode is pushed towards the outside of the waveguide and has a greater overlap with the sidewall roughness, which causes the scattering loss to increase exponentially. Allowing a larger radius of curvature thus translates to a significant improvement in roundtrip loss for micro-ring resonators. Previous work demonstrated flattened rings with greater than 800 μm circumference [2]; here we present device results from ring with lengths 30, 60, 90, 150, and 300 μm and lasing results from the largest three rings.

2. Design and fabrication

The device is fabricated on an InGaAsP/InP centered quantum well (CQW) platform with 10 compressively strained QWs centered in a 350nm waveguide layer. Passive waveguides are defined by an intermixing process of phosphorous implantation and rapid thermal annealing at 675 $^\circ\text{C}$ to shift the bandgap of the CQWs from 1545nm to 1410nm. A single blanket regrowth is used to cover the device with a 1.8 μm p-InP cladding layer and p-InGaAs contact layer.

A bilayer Cr/SiO₂ (50/650nm) hardmask and a single lithography are used to define the waveguides and EBS couplers to avoid any misalignment between the coupler and the waveguide. The photoresist (PR) used is a 200nm thick THMR-M100 with a 300nm thick contrast enhancer CEM365iS. The thin PR was necessary to define 300nm gaps for the smallest EBS, and assured that all feature dimensions were conserved from the photolithography mask. The Cr was etched in a low power Cl₂ based inductively coupled plasma (ICP) etch, the PR removed, and 550nm of SiO₂ etched in a SF₆ based ICP etch. A PR lift-off and second Cr deposition was used to cover the waveguides away from the EBS in 40nm of additional Cr that served as a mask for a final 100nm SiO₂ etch in the EBS regions. The final mask provided a 100'' etch delay for the waveguides, this accounted for the difference in etch speed in the

narrow EBS gaps due to the RIE lag effect, which reduces the etch rate of high-aspect ratio features. The InGaAsP/InP was deeply etched in a Unaxis ICP RIE with $\text{Cl}_2/\text{H}_2/\text{Ar}$ chemistry and a 200°C heated chuck. The etch depth was $5\mu\text{m}$ for the waveguides and $7\mu\text{m}$ in the EBS regions. The processed devices are shown in fig. 1.

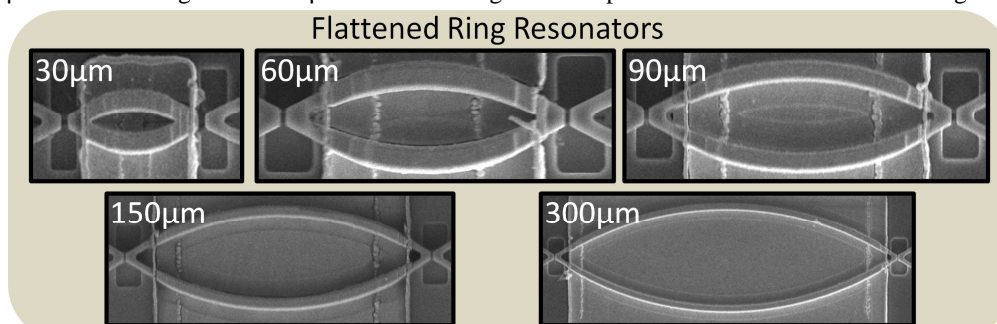


Fig. 1. Scanning electron microscope (SEM) images of flattened ring resonators with circumferences 30-300 μm

The semiconductor optical amplifiers (SOAs) have a peak large signal gain of 50dB/mm at 1530nm for TE polarized light, and the internal losses, as calculated from $2\mu\text{m}$ width pulsed laser cleave-back measurements, were $\alpha_{i,\text{passive}} = 7.5\text{cm}^{-1}$ and $\alpha_{i,\text{active}} = 11.9\text{cm}^{-1}$.

3. Lasing in flattened rings

The flattened ring lasers were tested CW and the lasing curves for 90 μm , 150 μm , and 300 μm circumference devices are shown in fig. 2. The extinction ratio on the non-lasing devices was measured to be 5.5dB and 4dB for the resonators with lengths 30 μm and 60 μm respectively. The net cavity losses (losses minus gain) per roundtrip (RT) for these resonators were calculated from their extinction ratios to be 3.97dB and 2.85dB respectively. Therefore, an additional 3-4dB of gain/RT is necessary to reach lasing in these cavities.

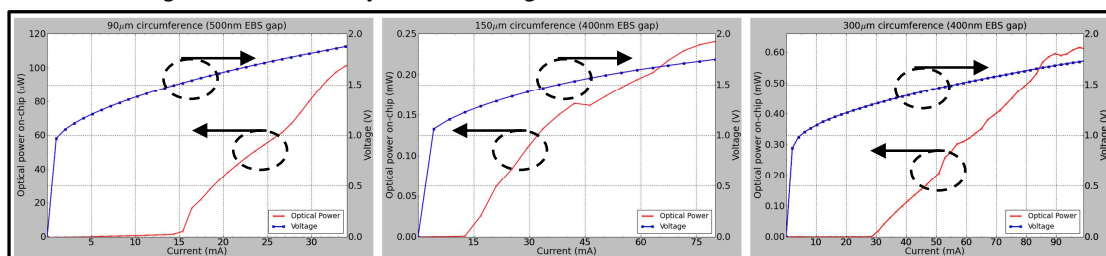


Fig. 2. LIV lasing curves for 90 μm , 150 μm , and 300 μm circumference flattened rings.

The lasing spectra of the flattened rings are shown in fig. 3. The corresponding FSR and side-mode suppression ratio (SMSR) are listed in table 1. The lasing peak shifts to lower wavelengths as the ring dimensions are reduced. This is due to increased pumping of the partially intermixed material at the edges of the active region. The phosphorous implant used in intermixing diffuses during the RTA process causing the nearby active region to shift partially, resulting in a border region with a 1500nm bandgap. The design of the active regions was conservative to avoid large losses from unpumped active material. However since the partially intermixed region has a dominant effect in the smaller flattened rings, future designs may benefit from an offset quantum well platform so that quantum wells can be removed using a wet-etch. This approach would provide a more digital transition between the active and passive regions, while the trade-off would be reduced gain in the active region.

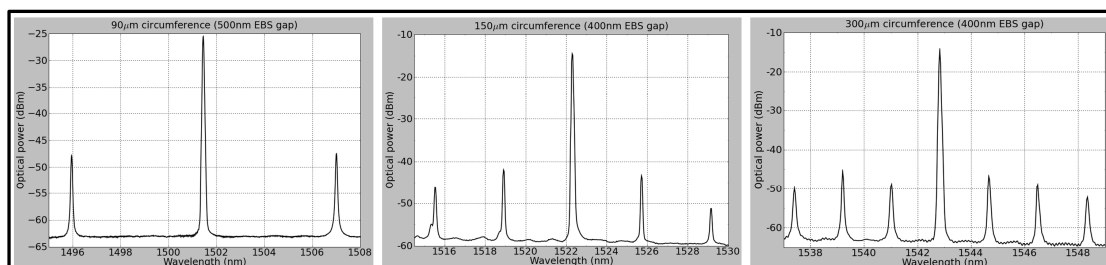


Fig. 3. Lasing spectrum of 90 μm , 150 μm , and 300 μm circumference flattened rings.

Table 1: Flattened ring FSR and SMSR

| Ring Length (μm) | 30 | 60 | 90 | 150 | 300 |
|-------------------------------|-----|-----|-----|-----|-----|
| FSR (nm) | 13 | 7.2 | 5.5 | 3.4 | 1.8 |
| SMSR (dB) | N/A | N/A | 22 | 27 | 31 |

4. EBS coupler losses

The maximum SOA gain per RT in the $90\mu\text{m}$ ring is 3.5dB ($L_{\text{active}}=70\mu\text{m}$), therefore each 500nm EBS coupler must have losses $<1.75\text{dB}$ assuming no other losses from waveguide scattering. The EBS couplers have an incident angle of 30° , which is set far from the critical angle of 18° in order to minimize loss on reflection. The high incident angle reduces the evanescent field coupling, and EBS gaps $<600\text{nm}$ are necessary to have coupling $>5\%$. For TE polarization, the wavelength dependence of the reflection, transmission, and cross-talk transmission of the EBS couplers was characterized by sweeping an external tunable laser and measuring on-chip reversed biased SOAs as illustrated in fig. 4a. The wavelength dependence of a 400nm gap EBS coupler on a $300\mu\text{m}$ circumference flattened ring is shown in fig. 4b. We calculate the power inside the $300\mu\text{m}$ cavity is around 11dB larger than detected outside the cavity, or 7mW at peak lasing. A minimum EBS loss of 0.6dB was measured at 1530nm, and $<2.5\text{dB}$ variation in reflection over the C-band. There is 0.5dB of uncertainty due to the bias point for transparency current density, which results in gain variation between SOAs.

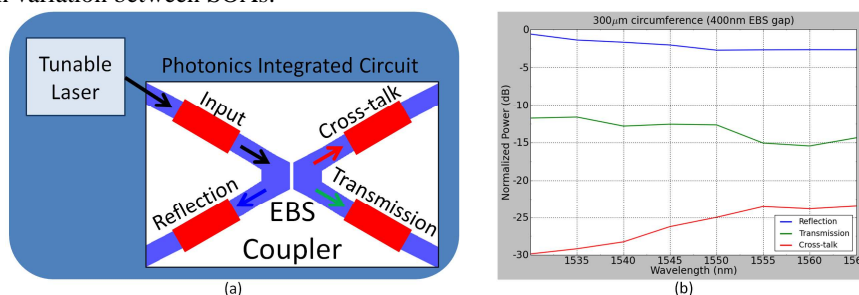


Fig. 4.(a) EBS coupler test set-up, (b) Reflection, transmission, and cross-talk transmission of a 400nm EBS coupler.

5. Conclusion

Compact flattened ring resonators with circumferences $30\text{--}300\mu\text{m}$ have been fabricated and lasing spectra observed for the $90\mu\text{m}$, $150\mu\text{m}$ and $300\mu\text{m}$ designs. The on-chip lasing power is greater than 0.6mW for the $300\mu\text{m}$ rings. The EBS coupler insertion loss was as low as 0.6dB with $<2.5\text{dB}$ variation in reflection over the C-band. As the transmission is generally low through the EBS couplers, flattened rings are ideal for applications involving weakly coupled resonators such as coupled cavity tunable lasers, channelizing filters, and narrowband pre-filters.

Acknowledgements

This work was supported by the Office of Naval Research. A portion of the work was done in the UCSB nanofabrication facility, part of the NSF funded NNIN network.

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Integrated InP-InGaAsP tunable coupled ring optical bandpass filters with zero insertion loss

Robert S. Guzzon,* Erik J. Norberg, John S. Parker, Leif A. Johansson, and Larry A. Coldren

Department of Electrical and Computer Engineering, University of California Santa Barbara, Santa Barbara, California 93116, USA

*guzzon@ece.ucsb.edu

Abstract: Second and third-order monolithically integrated coupled ring bandpass filters are demonstrated in the InP-InGaAsP material system with active semiconductor optical amplifiers (SOAs) and current injection phase modulators (PMs). Such integration achieves a high level of tunability and precise generation of optical filters in the RF domain at telecom wavelengths while simultaneously compensating for device insertion loss. Passband bandwidth tunability of 3.9 GHz to 7.1 GHz and stopband extinction up to 40 dB are shown for third-order filters. Center frequency tunability over a full free spectral range (FSR) is demonstrated, allowing for the placement of a filter anywhere in the telecom C-band. A Z-transform representation of coupled resonator filters is derived and compared with experimental results. A theoretical description of filter tunability is presented.

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OCIS codes: (250.5300) Photonic integrated circuits; (230.5750) Resonators; (350.2460) Filters, interference; (130.7408) Wavelength filtering devices.

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#142453 - \$15.00 USD Received 11 Feb 2011; revised 18 Mar 2011; accepted 30 Mar 2011; published 7 Apr 2011
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1. Introduction

Filtering in the optical domain can be useful for many systems in which data is modulated on an optical carrier. In the telecom world, applications can be found in WDM channel add-drop filters and gain flattening filters [1]. For analog signal processing at RF frequencies, microwave photonic filters can have advantages over all-electronic systems due to their wide tunability, programmability, and immunity to electromagnetic interference. For example, radio-over-fiber (RoF) systems that employ an array of remote antennas benefit from the low loss transmission properties of optical fiber, thus opening up the possibility of pre-filtering in the optical domain before analog-to-digital conversion. In particular, radar systems can benefit from the ultra-wide bandwidth of a tunable optical filter in channelizing and matched filter applications [2].

System performance depends greatly on the accuracy with which optical filter responses are synthesized. For example, an ideal bandpass filter has a flat passband, high extinction, fast roll-off, and is linear-time-invariant (LTI). Optical fiber and bulk optical component based photonic filters suffer from thermal and mechanical instability, and are therefore limited mostly to the incoherent regime, which has significant performance drawbacks [2]. Size, weight, power, and cost are also an issue with bulk optical systems. Monolithic integration offers a stable, compact scheme for construction of filter geometries, and recently many filters have been demonstrated in various integration platforms to realize both telecom and microwave photonic filters [3–10]. Integration in passive systems (those without optical gain) relies on low loss waveguides to maintain filter shape and minimize insertion loss. Silicon photonics and polymer waveguide photonics are two such solutions [3–8]. However, generating optimal filter shapes in such systems depends strongly on setting waveguide coupling values accurately and creating extremely low loss waveguides. Furthermore, these systems are ultimately limited in complexity by accrued loss, which degrades the system dynamic range [11]. Active systems, utilizing direct-bandgap semiconductors with gain at telecom wavelengths have been shown in a variety of material systems including InP/InGaAsP and hybrid SOI/InP [9,10]. The optical gain provided in these integration platforms can account for accumulated losses and more easily synthesize optimal filter shapes by adding a degree of amplitude tunability unavailable in passive systems. However, degradation of dynamic range from amplified spontaneous emission (ASE) noise and non-linear saturation of gain in semiconductor optical amplifiers (SOAs) is a concern that must be addressed [11].

Filters can be constructed of infinite impulse response (IIR) and/or finite impulse response (FIR) elements. Filters with IIR elements are better able to synthesize high-quality bandpass filters using fewer stages [12], and are the focus of this effort. IIR filters constructed out of

integrated waveguide rings can be arranged in one of two geometries: cascaded or coupled. In a coupled system, there is optical feedback from each ring to the previous ring, contrary to the cascaded geometry. Each design has advantages, but the coupled geometry can easily synthesize the complex-conjugate poles required of bandpass filters, and do so while requiring lower amplifier gain (or tolerating higher waveguide losses) than a comparable cascaded system. Previously, we have reported on 3rd order coupled-ring filter photonic integrated circuit (PIC) and published preliminary results [10]. Here we examine the system in more theoretical detail, show good agreement between theory and experiment, and demonstrate high levels of tunability while maintaining an optimal filter shape.

2. Coupled-ring optical filters and their z-transform representation

2.1 Z-transform for optical systems

The Z-transform is a convenient method for representing the transfer function of optical filters if all optical delays are assumed to be an integer multiple of some unit delay [12,13]. This discrete-time approach accurately models the set of identical filter responses each separated in frequency by a free spectral range (FSR) that are obtained in an LTI optical system. In general, optical feedback from rings or Fabry-Perot cavities creates system poles, while feed-forward geometries such as a Mach-Zehnder Interferometer (MZI) create system zeros. The poles and zeros of such a system can be represented on the complex frequency plane. This pole-zero plot is a convenient tool for understanding the effect of varying device parameters on the filter shape.

An active optical system with feedback must remain below the lasing threshold in order to maintain gain tunability. Above threshold, the carrier density and gain in each SOA is clamped. While higher SOA linearity can be achieved in this regime [14], the loss of tunability is detrimental to a large system such as the one described here. From a signal processing standpoint, the pole magnitude generated across the spectrum varies due to variations in gain and loss with wavelength. Therefore, at the operating wavelength, the pole magnitude may be suboptimal in order to keep the entire system below lasing. Pole magnitudes of < 0.9 are typically achievable in practice.

There are a variety of ways to determine the scattering parameters of an optical circuit, including transfer matrix approaches, block diagram simplification, and Mason's formula for single-input single-output systems [12,15]. The equation

$$z = e^{j\omega_n} = e^{j\beta L_U} \quad (1)$$

transforms device scattering parameters to the z-domain. ω_n is the normalized frequency, L_U is the unit length, taken as the ring length in our devices, and β is the propagation constant given by

$$\beta = \frac{2\pi n_{\text{eff}}}{\lambda} \quad (2)$$

where n_{eff} is the effective index of refraction and λ is the optical wavelength.

Optimal bandpass filters are generated with the fewest amount of stages using IIR-type filters [12]. Optimal Chebyshev Type I and Butterworth filters are created in the Z-domain using equal numbers of poles and zeros. However, reasonable approximations can be synthesized with pole-only filters. In the next section, we analytically compare the Z-transform representations of two types of 2nd order IIR filters.

2.2 Second-order cascaded and coupled rings

Figure 1 shows schematic representations of ring geometries that can synthesize two poles anywhere in the complex plane. Pole angles are set by phase modulators, and pole magnitudes are set by intracavity loss. The total intracavity loss is made up of waveguide propagation loss and losses from coupling out of the ring. The loss is offset by intracavity amplifier gain. In the

cascaded case, there is no optical feedback from the 2nd ring into the 1st ring, and so the pole locations and magnitudes are independently set by each ring's tuning parameters. In contrast, the poles generated by the coupled ring system are dependent on the tuning parameters from both rings. In particular, the poles from a coupled ring geometry cannot be located at the same frequency. They will split into two peaks of equal magnitude. The distance between the peaks is determined by the inter-ring coupling value.

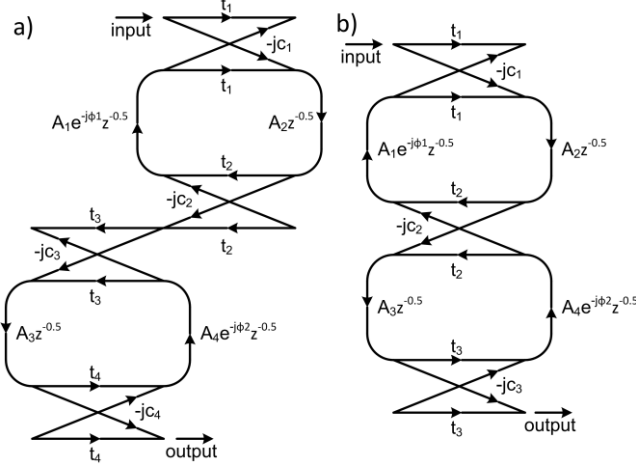


Fig. 1. Signal flow graphs of 2nd order ring filters. (a) Cascaded case with no feedback from the 2nd ring to the 1st ring. (b) Coupled case with feedback. c and t are amplitude coupling and transmission values for the couplers, the ϕ 's are the added phase from phase modulators, and the A 's are the multiplicative gain through a waveguide section.

Mason's formula for determining the transfer function from a signal flow graph can be used to write the scattering parameters for these two systems [15]. The amplitude transfer functions for two cascaded rings and two coupled rings are as follows

$$H_{cascaded}(z) = \frac{c_1 c_2 c_3 c_4 A_2 A_3 z^{-1}}{1 - B_1 z^{-1} + B_2 z^{-2}} \quad (3)$$

$$H_{coupled}(z) = \frac{j c_1 c_2 c_3 A_2 A_3 z^{-1}}{1 - D_1 z^{-1} + D_2 z^{-2}} \quad (4)$$

where

$$B_1 = t_1 t_2 A_1 A_2 e^{-j\phi_1} + t_3 t_4 A_3 A_4 e^{-j\phi_2} \quad (5)$$

$$B_2 = t_1 t_2 t_3 t_4 A_1 A_2 A_3 A_4 e^{-j(\phi_1 + \phi_2)} \quad (6)$$

$$D_1 = t_1 t_2 A_1 A_2 e^{-j\phi_1} + t_2 t_3 A_3 A_4 e^{-j\phi_2} \quad (7)$$

$$D_2 = t_1 t_3 A_1 A_2 A_3 A_4 e^{-j(\phi_1 + \phi_2)}. \quad (8)$$

where c_i is the amplitude coupling value of the i^{th} coupler, and there is assumed to be no coupler insertion loss, implying $t_i = \sqrt{1 - c_i^2}$. ϕ_i is the phase introduced by the phase modulator in the i^{th} ring, A_i is the fractional amplitude loss in each waveguide segment given by

$$A_i = e^{-\frac{\Gamma g_i - \alpha_a}{2} L_{SOA}} e^{-\frac{\alpha_p}{2} \left(\frac{L}{2} - L_{SOA} \right)} \quad (9)$$

where Tg_i is the modal power gain and α_a is the modal loss from the Semiconductor Optical Amplifier (SOA) in the i^{th} waveguide segment, L_{SOA} is the length of the SOAs, α_p is the passive modal waveguide loss, and L is the ring length. Equation (3) and (4) are very similar, but result in different behavior due to the coupled nature of the z^{-1} and z^{-2} terms in the coupled ring equation.

The pole magnitudes of the cascaded system are set independently by each ring, and are equal simply to the round-trip gain minus loss. In the coupled system, the poles can be determined by finding the roots of the denominator, which can be written in terms of the intrinsic ring round-trip gain minus loss, p_r . This ‘‘intrinsic pole’’ is the pole obtained from the ring independent of any feedback from other rings, as in the cascaded system. These intrinsic poles are given by

$$p_{r,1} = t_1 t_2 A_1 A_2 e^{-j\phi_1} \quad (10)$$

$$p_{r,2} = t_2 t_3 A_3 A_4 e^{-j\phi_2} \quad (11)$$

Substituting Eq. (10) and (11) into Eq. (4) and solving for the roots of the denominator, the actual poles of the coupled system are determined to be

$$p_{\text{coupled},\pm} = \frac{1}{2}(p_{r,1} + p_{r,2}) \pm \frac{1}{2} j \sqrt{\frac{4p_{r,1}p_{r,2}}{1-C_2} - (p_{r,1} + p_{r,2})^2} \quad (12)$$

where C_2 is the power coupling in coupler 2 (i.e. $C_2 = c_2^2$). If the term under the square root is real, then the poles are complex conjugates of each other. When $\phi_1 = \phi_2$, the ring resonances are located at the same frequency which is most interesting for the bandpass filter application. For this case, $p_{r,1}$ and $p_{r,2}$ are real, and the pole magnitudes are both given by

$$|p_{\text{coupled},\pm}| = \sqrt{\frac{p_{r,1}p_{r,2}}{1-C_2}} \quad (13)$$

This situation has important implications. The first is that the magnitudes of the two poles are always equal, regardless of the individual intrinsic pole magnitudes. The second is that the pole magnitudes are enhanced above the level of the intrinsic (cascaded) pole magnitudes by a factor of $1/\sqrt{1-C_2}$. These effects make the coupled-ring geometry advantageous for easily synthesizing bandpass filters, by simply creating a symmetric response and requiring less gain than the cascaded system in order to reach the same pole magnitudes.

Taken a step further, if the intrinsic pole magnitudes are equal, the pole angles can be written from Eq. (12) simply as

$$\angle p_{\text{coupled},\pm} = \tan^{-1} \sqrt{\frac{C_2}{1-C_2}} \quad (14)$$

The pole angle determines the bandwidth of the filter; as C_2 increases, the bandwidth increases.

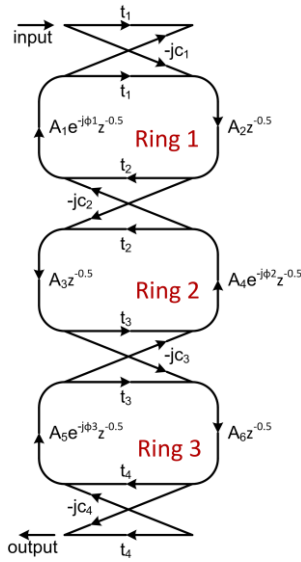


Fig. 2. Signal flow graph for a 3rd order coupled ring filter.

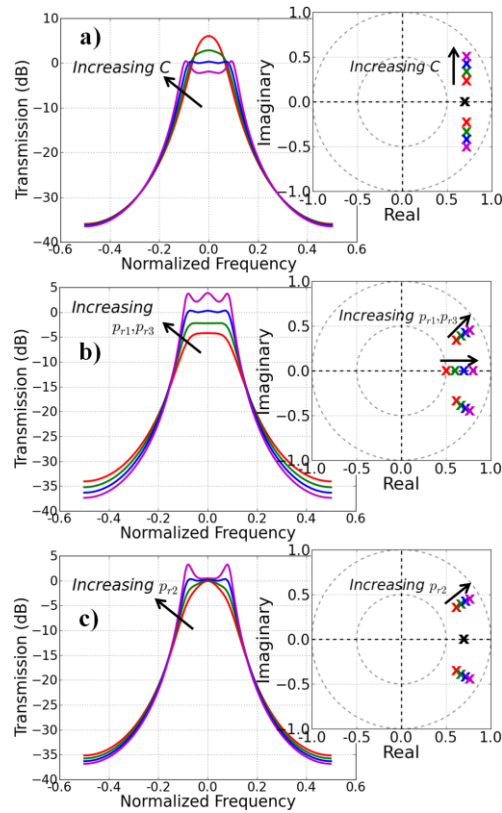


Fig. 3. Theoretical filter shapes and pole-zero plots for a 3rd order coupled ring filters showing variation with (a) tuning inter-ring coupling, (b) tuning the intrinsic pole magnitude of the 1st and 3rd rings, and (c) tuning the intrinsic pole magnitude of the 2nd ring. In all cases, the blue filter is the same, employing an inter-ring coupling value of 0.15, and intrinsic pole magnitudes of 0.7 for rings 1 and 3, and 0.73 for ring 2.

2.3 Third-order coupled rings

The 3rd order coupled system is similar in operation to the 2nd order system. However, due to the complexity of the equations, we will present the operation here qualitatively. A signal flow graph of a 3rd order coupled system is shown in Fig. 2. Like the 2nd order system, when all three ring resonances are located at the same frequency, there is a splitting in the system poles. In this case, there is one real pole located at zero normalized frequency, and two complex conjugate poles. Similarly to the 2nd order system, the complex conjugate poles share a pole magnitude that is dependent on all three of the intrinsic ring pole magnitudes.

Figure 3 shows how the poles move in the complex plane when various tuning parameters are adjusted. When the inter-ring coupling values are increased, the complex part of the complex conjugate pair of poles is increased (Fig. 3(a)). The two coupling values, C_2 and C_3 , do not need to be equal for the filter to be symmetric, and adjusting just one of them affects both complex conjugate poles.

When the intrinsic pole magnitude of the 2nd ring is increased, the center system pole does not change, but the complex conjugate poles move towards the unit circle (Fig. 3(b)). In effect, this sets the “evenness” of the three filter passband maxima. Once the evenness is set, the magnitude of the passband ripple can be varied by adjusting the intrinsic ring pole magnitudes of the 1st and 3rd rings (Fig. 3(c)). Again, similarly to the 2nd order filter, these do not need to be the same to achieve a symmetric filter. In this way, a bandpass filter with a specified passband ripple can be set over a range of bandwidths. As long as the ring resonances are located at the same frequency, a symmetric bandpass filter is synthesized, even if the intrinsic ring pole magnitudes and the inter-ring coupling values are not equal.

3. Design of the monolithically integrated filter

3.1 System design

Figure 4 shows a schematic representation of the 3rd order coupled-ring filter, termed a unit cell. The 3-ring structure can synthesize 1st order poles, 2nd order coupled poles, 2nd order cascaded poles, and 3rd order coupled poles. In addition, a 1st order zero is formed by the interference of the feed forward path and the path through the rings. The rings are 3 mm long, producing an FSR of 0.212 nm or 26.5 GHz.

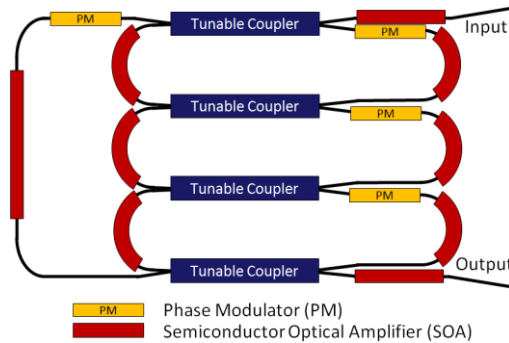


Fig. 4. Schematic representation of our proposed 3rd order coupled ring unit cell with SOAs in red, phase modulators (PMs) in yellow, and MZI tunable couplers in blue. The feed-forward waveguide on the left forms an MZI with the path through the rings.

The SOAs and phase modulators are P-i-N diodes, and are operated by forward-bias current injection. The SOAs can also be operated under reverse-bias as detectors that effectively “shut-off” waveguide paths to change the filter configuration. The tunable couplers are symmetric MZIs with a 300 μm phase modulator in each waveguide path. Splitting in the MZI is provided by 3 dB 2x2 restricted interference multi-mode-interference (MMI) couplers, each 100 μm long. By tuning the phase in one waveguide, the coupling is fully tunable. Power cross-coupling values less than -20 dB of total output power were demonstrated [16]. As the

inter-ring coupling determines the frequency splitting of coupled poles [Eq. (14)], this metric is critical for creating narrow bandwidth and high extinction ratio filters. Total tunable coupler insertion loss was measured to be < 1.5 dB. Light is coupled on and off chip via a flared and angled waveguide at the facet to lensed fiber. Flaring the waveguides adiabatically from $2.8 \mu\text{m}$ to $5.0 \mu\text{m}$ helps provide better matching to the lensed fiber mode, while a 7° angle at the facet reduces reflections.

While the unit cell is highly tunable in both frequency and bandwidth, a lower limit on bandwidth is imposed by the minimum coupling values and the maximum pole magnitudes that can be obtained. In order to create filters narrower than the 3 GHz shown in the results, longer delay lengths are needed. Extension of the unit cell to longer rings and narrower bandwidths would require appropriate SOA gain to compensate for additional waveguide loss. To create wider filters, or to enhance extinction and roll-off, multiple unit cells can be cascaded monolithically. In this way, filter transfer functions are multiplied together. The FSR of an optical filter is also crucial to its functionality. The 1st order zero is designed such that it can enhance the FSR by a factor of 2 if two unit cells are cascaded together. The FSR of the zero is twice that of the poles, and when cascaded with a unit cell synthesizing a bandpass filter, can reduce the passband level in every other filter order. This in effect would enhance the FSR by a factor of 2. Other, more elaborate designs could be envisioned where bandpass filters of different FSR (and passband bandwidths) could be cascaded to create a narrowband filter with a large FSR.

3.2 Active/passive integration and waveguide design

In order to fabricate on the same device active SOAs with gain in the telecom C-band, passive low-loss waveguides, and fast phase modulators, a multi-purpose integration scheme is needed. Many different methods of integration in InP/InGaAsP have been proposed and demonstrated in the centered quantum well (CQW) or offset quantum well (OQW) epitaxial structures [17]. Here we utilize an OQW integration platform because of its ease of fabrication and high linearity compared to CQW designs. The OQW material structure consists of quantum wells grown above the transverse waveguide layer. This offset from the center of the optical mode decreases the confinement factor with the quantum wells, decreasing the gain, increasing the saturation power, and increasing RF linearity [17,18]. Since the required gain in each SOA is very low for this application and linearity is important, the OQW structure is suitable. Advantageously, active / passive definition is relatively simple, involving a selective wet etch of the quantum wells and a single blanket regrowth to provide the p-InP cladding and p-InGaAs contact layer. The OQW platform also creates low-loss passive waveguide sections (~ 1 dB/mm [19]) which are crucial for developing a system with low noise Fig [20]. Due to the use of compressively strained quantum wells, the SOAs display high polarization dependence, providing much higher gain for TE than TM polarized light. This dependence would need to be addressed in the context of the final RF photonic link. More details about the material structure can be found in [17].

To provide lateral confinement of the optical mode, a deeply-etched waveguide geometry was chosen. In such a design, the lateral waveguide is defined with a deep dry etch through the transverse waveguide layer. This provides high optical confinement, allowing for tight waveguide bends with minimal radiation loss. The etch quality is important for avoiding excess optical scattering loss, and we have developed such an etch using an $\text{H}_2/\text{Cl}_2/\text{Ar}$ ICP-RIE recipe [21]. Previously, we have demonstrated low loss waveguides (~ 1 dB/mm) and sufficient SOA gain (26 dB/mm) for our devices using this integration platform [19]. The waveguides are $2.8 \mu\text{m}$ wide in the SOAs and taper down to $1.8 \mu\text{m}$ at the MMI couplers. While the waveguides are multi-mode, the device structure operates in a single-mode fashion due to 2nd order mode excess loss in the MMIs, estimated to be ~ 5 dB. The OQW material structure paired with the low loss deeply-etched waveguide is a robust and simple integration platform that, together with standard optical lithography, promises a high yield suitable for commercial volume production schemes.

3.3 Fabrication

The fabrication of the filters was performed with a simple 4 mask-layer process. After active / passive patterning and regrowth of the p-InP cladding and p-InGaAs contact layer, the waveguides were defined using standard i-line stepper lithography. In order to accurately transfer the waveguide mask to the InP, a Cr/SiO₂ hardmask was defined with photo-resist [21]. After the waveguide etch, 300 nm of protective nitride was deposited to act as an electric insulator, and to protect the etched waveguide sidewalls. Vias were then opened to the InGaAs contact layer for electrical contact to the SOAs and phase modulators. P-contacts were evaporated onto this surface while the n-contact was evaporated onto the backside of the n-conducting substrate. Figure 5 shows a mounted device and a close-up view of an MMI-coupler highlighting the smooth and anisotropic waveguide etch.

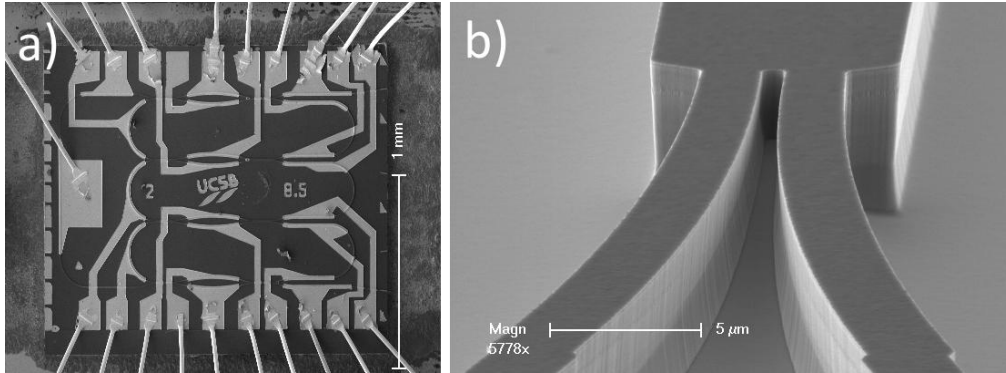


Fig. 5. Scanning electron microscope (SEM) image of (a) a fabricated, mounted, and wire-bonded unit cell; and (b) input/output waveguides of a deeply-etched MMI coupler.

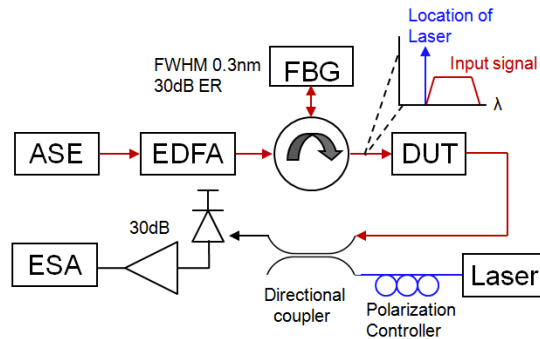


Fig. 6. Schematic of the measurement setup. A broadband ASE source is band-limited by a fiber Bragg grating (FBG) filter and then propagated through the device under test (DUT). The response is viewed on an ESA after heterodyne down conversion by a tunable laser.

4. Measured filter results

4.1 Measurement setup

The bandpass filters shown in Fig. 7 were measured at microwave frequencies by heterodyne down conversion of a filtered broadband optical signal. In order to create this broadband input, an Erbium-doped fiber ASE source was used. Figure 6 is a schematic of the measurement setup.

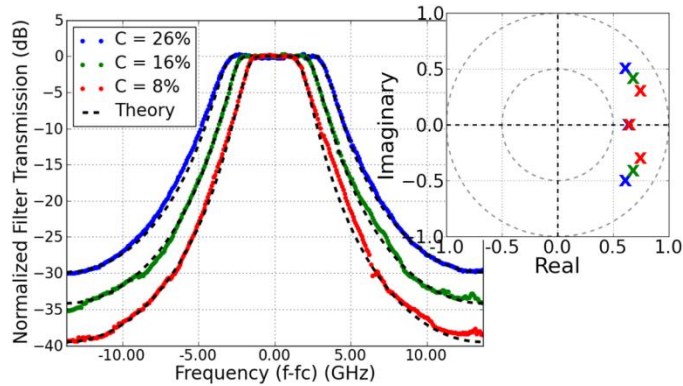


Fig. 7. Measured coupled-ring 3rd order bandpass filters with theoretical fits and their respective pole locations. The three filters are for coupling values of 25.5%, 15.6%, and 8.41%, producing bandwidths of 7.06, 5.50, and 3.90 GHz and extinction ratios of 30, 35, and 40 dB. The theoretical fits are good, indicating that the device was operating in the linear regime.

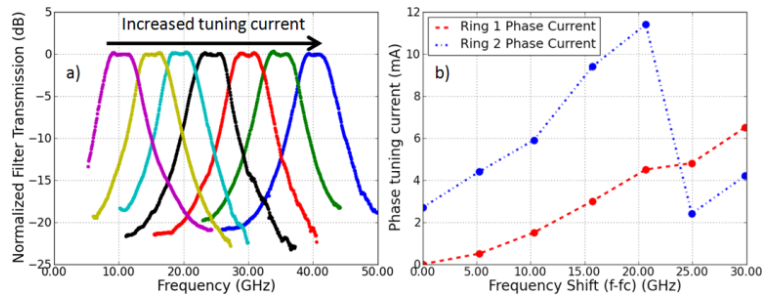


Fig. 8. (a) Measured 2nd order coupled ring filters showing tunability in frequency. The overall response is normalized to 0 dB, but the relative amplitudes of the filters are real. The unit cell itself had a throughput optical gain during this test of ~ 3 dB. (b) PM currents required in each of the two rings in order to tune the filter. The large shift in the ring 2 phase current at 25 GHz occurred when the next longitudinal mode (located 1 FSR away) was utilized, demonstrating the smooth tunability of filters across multiple FSRs. In this way, filters can be placed anywhere in the telecom C-band.

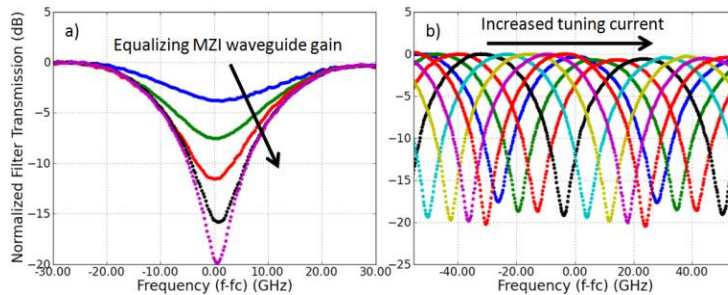


Fig. 9. Optically measured MZI zero filters. (a) Showing tunability in extinction by equalizing the gain through each of the MZI's two waveguide paths. While the filters are normalized in passband amplitude, the filter frequency was re-normalized in real-time using on-chip PMs. (b) Showing tunability in frequency across a full FSR. The parasitic loss of the phase modulators is demonstrated in this measurement as an increase in the extinction of the zero filter as the loss equalizes the optical amplitude in the two waveguides of the MZI.

To ensure that only a single sideband of the LO was down-converted, the reflection spectrum of a fiber Bragg grating (FBG) was utilized. This band-limited reflection spectrum was 0.3 nm (37.2 GHz) wide and had 30 dB out of band extinction, and so the output of the filter illuminated only the upper sideband of the LO. The resultant optical signal was

impinged upon a high-speed photodetector and the electrical spectrum viewed on a 50 GHz ESA. All measurements were made continuous-wave and at room temperature, with constant device temperature maintained with a thermoelectrically cooled stage. The device was wire bonded onto a Al_2O_3 carrier and light was coupled in and out via lensed fiber.

4.2 Measured filters

Single unit cells were fabricated and evaluated. Measured 3rd order coupled-ring bandpass filters are shown in Fig. 7 together with theoretical fits and accompanying pole-zero plots. These Chebyshev Type I approximations have bandwidths of 7.06, 5.50, and 3.90 GHz, set by inter-ring power coupling values of 25.5%, 15.6%, and 8.41%. Extinction increases with decreased inter-ring coupling, and up to ~40 dB was measured here. In order to synthesize the 3.90 GHz filter, the 400 μm long SOAs were biased at 16.5 mA, giving a gain of about 1.3 dB to achieve the desired intrinsic pole values of 0.65 for the outer rings and 0.84 for the center ring. At this setting, the chip consumed approximately 200 mW. The 1.3 dB gain is significantly lower than the 10 dB max gain available in the fabricated SOAs, indicating room for optimization of material and device design. The electrical spectrum of the 3rd order filters are normalized in amplitude for clarity. However, there is zero optical insertion loss through the chip as the coupling and waveguide losses are negated by the on-chip amplifiers. In this measurement, input and output SOAs placed before and after the 3 coupled rings were used to account for the coupling losses. It is possible to eliminate the input and output amplifiers (and hence their added noise) and instead tune the desired system gain by biasing the intra-ring SOAs accordingly. For example, in Eq. (4) the 2nd order coupled-ring response gain can be increased without changing the filter shape by increasing A_2 and decreasing A_1 such that A_1A_2 remains the same. The results are also normalized in frequency, but are tunable across a full FSR, indicating the ability to place a filter anywhere in the c-band.

Figure 8 displays 2nd order coupled-ring bandpass filters showing such tunability across 30 GHz. Filters are tuned by adjusting the phase modulators in both rings and compensating for the resulting parasitic loss by re-tuning the SOAs to obtain a flat topped filter. Tunability of the 1st order zero is also shown via an all-optical measurement in Fig. 9, utilizing a broadband ASE input and an optical spectrum analyzer (OSA). The parasitic loss of the phase modulators is demonstrated in this measurement as an increase in extinction as the loss equalizes the optical amplitude in the two waveguides of the MZI. In practice, the zero filter extinction can be tuned from 0 dB to its maximum value of about 20 dB by adjusting the SOA gain in each MZI arm.

5. Conclusion

Coupled-ring optical filters are a promising solution for telecom and RF filtering applications. Here we have described the z-transform representation of 2nd and 3rd order filters. A 3rd order coupled-ring filter was monolithically integrated in the InP/InGaAsP material system and new measured filter results were shown along with theoretical fits demonstrating tunability in bandwidth and frequency. Future work will explore the effects of ASE noise and RF distortion on the dynamic range of a microwave photonic system employing such an active filter. Other areas of further study include active control systems to ensure filter stability with regards to temperature fluctuations. For applications that require near-ideal filter approximations with high extinction, fast roll-off, and a flat passband, active solutions provide benefits over all-passive approaches.

Acknowledgments

This work was supported by DARPA under the PhASER program, a portion of this work was completed in the UCSB nanofabrication facility, part of the NSF funded NNIN network.

InP/InGaAsP Flattened Ring Lasers With Low-Loss Etched Beam Splitters

John S. Parker, Erik J. Norberg, Yung-Jr Hung, Byungchae Kim, Robert S. Guzzon, and Larry A. Coldren, *Fellow, IEEE*

Abstract—Compact flattened InP/InGaAsP multiquantum-well (MQW) resonators based on etched beam splitters (EBS) with 300- to 800-nm gaps and circumferences of 30–300 μm are demonstrated. Comparison of the EBS coupler reflection and transmission to 3-D finite-difference time-domain (FDTD) simulations shows good agreement in the wider EBS gap devices. Lasing is observed in 90-, 150-, and 300- μm length rings at threshold currents of 15, 14, and 29 mA, respectively.

Index Terms—Beam splitter, integrated optics, optical resonators, photonic integrated circuits.

I. INTRODUCTION

COMPACT integrated ring resonators can provide diverse functionality in photonic integrated circuits (PICs) due their multitude of uses as delay lines [1], programmable memory elements [2], optical switches [3], optical filters [4] tunable lasers [5], and biological sensors [6]. Ring resonators have been demonstrated with several geometries including: standard circular rings [2], racetrack resonators [3], rectangular rings [7], and flattened rings [8]. The flattened ring design uses a larger bending radius with arcs covering $\sim 120^\circ$ and two etched beam splitters (EBS) to provide the remaining 240° necessary to complete the loop. Increasing the bending radius decreases the scattering losses, which becomes significant in small rings. Therefore, the use of flattened rings with EBS couplers can enable lower loss compact cavities.

EBS couplers are based on frustrated total internal reflection (FTIR), using a low refractive index trench to separate two etched mirrors [9]. The couplers are designed for an incident angle greater than the critical angle (i.e., for the In/InGaAsP material platform the critical angle is 18° for an air-trench [8], or higher for a trench filled with dielectric such as Benzocyclobutane [10]). As the incident optical mode is reflected by the trench, the evanescent field couples a portion of the modal power across the low index gap. Semiconductor based EBS, also known as FTIR couplers, were first demonstrated in 1987 on the GaAs/AlGaAs material platform using an ion milled air trench

[11]. Recently, demonstrations of EBS couplers have been realized in Si [12], GaAs/AlGaAs [13], and InP/InGaAsP [8], [10]. The compact size of the EBS provides the capability to create small devices. The minimum size of ring resonators is ultimately limited by the coupler length. As an example, for ultra-compact InP designs realized by lithography, the minimum length demonstrated is 55 μm for a directional coupler [14], 20 μm for a multimode interference (MMI) coupler [15], and 8 μm for an etched beam splitters [8].

We present EBS couplers designed with low insertion loss for use in compact ring lasers, and the smallest flattened ring cavities yet reported with circumference of 30 μm and a cavity footprint of 8 $\mu\text{m} \times 20 \mu\text{m}$. For these compact photonic devices, ease of integration is vital for combining components with diverse functionality on a single PIC. To address this, we have developed a fabrication process for defining waveguides and 300 nm EBS trenches using a single i-line (365 nm source) photolithographic exposure. Furthermore, the waveguides and trenches are created in one dry etch by using an SiO₂ etch delay mask for the waveguides. Previous studies have used expensive electron-beam-lithography (EBL) for narrow trench definition [9], [10], [12], [13]. Using only stepper lithography, we demonstrate that narrow EBS trenches can be realized on PICs with relatively low added cost for integration of compact flattened ring lasers with other deeply etched components.

II. FABRICATION

The device is fabricated on an InP/InGaAsP centered quantum well (CQW) platform with 10 compressively strained QWs sandwiched in-between two 105 nm 1.3Q InGaAsP layers. Passive waveguides are defined by an intermixing process of phosphorous implantation and rapid thermal annealing at 675°C to shift the bandgap of the CQWs from 1545 nm to 1410 nm. A single blanket regrowth is used to cover the device with a 1.8 μm p-InP cladding and p-InGaAs contact layer.

A bilayer Cr/SiO₂ (50/650 nm) hardmask and a single lithographic exposure are used to define the waveguides and EBS couplers to avoid any angular misalignment between the coupler and the waveguide. The photolithography is done using a GCA Autostep200 stepper with a numerical aperture of 0.45. The photoresist (PR) used is 200 nm thick THMR-M100 with 300 nm thick contrast enhancer CEM365iS. The thin PR was necessary to define 300 nm gaps for the smallest EBS as shown by the scanning electron microscope (SEM) image in Fig. 1(a). A diagram of this ring is shown in Fig. 1(b).

The Cr was etched in a low power Cl₂ based inductively coupled plasma (ICP), the PR removed, and 550 nm out of the 650 nm of SiO₂ was etched in a SF₆ based ICP. An additional 40 nm of Cr was deposited and defined by liftoff to cover the

Manuscript received November 09, 2010; revised January 20, 2011; accepted February 12, 2011. Date of publication February 17, 2011; date of current version April 08, 2011. This work was supported by the Office of Naval Research (ONR). A portion of this work was done in the UCSB nanofabrication facility, part of the National Science Foundation (NSF) funded NNIN Network.

J. S. Parker, E. J. Norberg, B. Kim, R. S. Guzzon, and L. A. Coldren are with the Department of Electrical Engineering, University of California, Santa Barbara, CA 93116 USA (e-mail: JParker@ece.ucsb.edu).

Y.-J. Hung is with the Department of Electronic Engineering, National Taiwan University of Science and Technology, Taipei 106, Taiwan.

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Digital Object Identifier 10.1109/LPT.2011.2116777

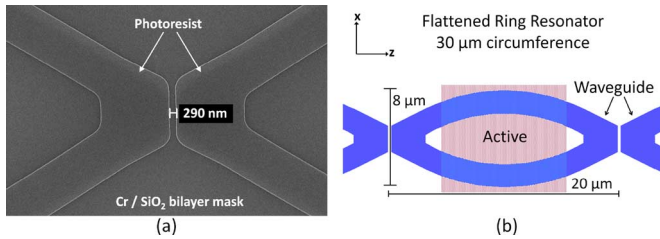


Fig. 1. (a) Scanning electron microscope image of the photoresist after waveguide and EBS trench have been defined (290-nm measured gap). (b) Diagram of 30- μm circumference flattened ring (top view).

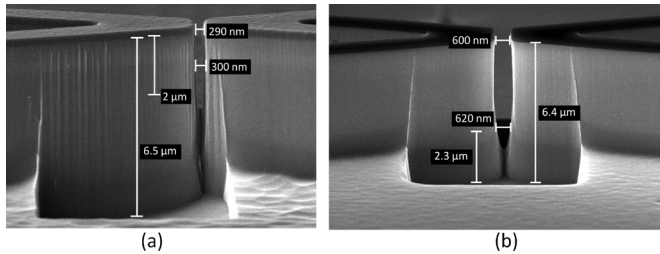


Fig. 2. SEM images of deeply etched waveguides and trenches with gap sizes of (a) 300 nm and (b) 600 nm. A SiO₂ etch delay allows the EBS trench to etch for longer than the waveguides to account for the RIE lag effect in the high aspect-ratio trench.

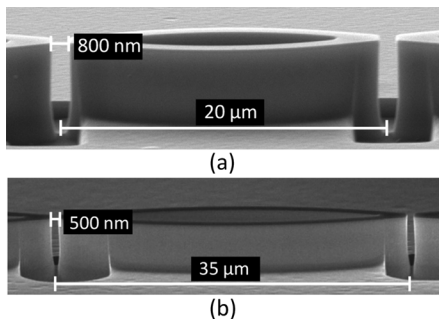


Fig. 3. SEM images of flattened ring resonators with circumferences of (a) 30 μm and (b) 60 μm , with EBS couplers on both sides.

waveguides outside the EBS. This Cr served as a mask to etch the remaining 100 nm of SiO₂ inside the EBS regions. The Cr was removed prior to InP etching and the final SiO₂ mask provided a 100-second etch delay for the waveguides. This delay helps account for the difference in etch speed in the narrow EBS trench due to the RIE lag effect, which reduces the etch rate in small features. The InP/InGaAsP was deeply etched in a Uniaxial ICP reactive ion etch (RIE) with Cl₂/H₂/Ar chemistry and a 200°C heated chuck. From Fig. 2, the etch depth was 5 μm for the waveguides and 6.5 μm inside the EBS regions. The benefit of this SiO₂ lag mask etching technique was that it allowed two etch depths to be achieved in a single dry etch. Previous multilevel dry etches have required multiple etches, which caused undesirable sidewall kinks [7].

A 30 μm and a 60 μm circumference flattened ring are shown in Fig. 3 after dry etching. The finished devices have ohmic Pt/Ti/Pt/Au contacts evaporated on the p-InGaAs layer and Ti/Au contacts on the backside of the InP:S substrate.

III. LASING RESULTS

The 90, 150, and 300 μm circumference rings lase at threshold currents of 15, 14, and 29 mA respectively. No unidirectional lasing or bistability was observed. The lasing spectra for the three resonators are shown in Fig. 4. The shift

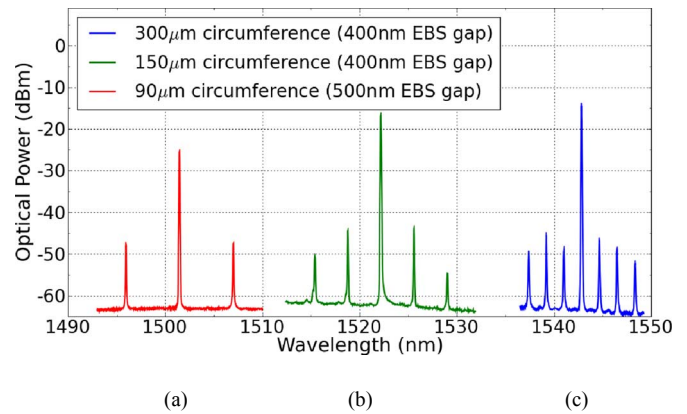


Fig. 4. Optical spectra of flattened ring lasers with circumferences of (a) 90 μm , (b) 150 μm , and (c) 300 μm . The shift in lasing wavelength is due to partially intermixed quantum wells at the edge of the active region.

in lasing wavelength for the shorter rings was due to partial intermixing at the edge of the active region. As the ring length is decreased, the effects at the edge of the active region become more significant. In future devices, the implant and intermixing process will need to be optimized for a sharper transition to minimize these edge effects.

Rings with 30 μm and 60 μm circumference did not lase, however they did produce pole filter responses with extinction ratios of 4 and 5.5 dB respectively, hence, these resonators can be used in wide bandwidth and channelizing applications. The free spectral range (FSR) of the resonators varied from 13 nm for the 30 μm ring to 1.8 nm for the 300 μm ring.

IV. EBS COUPLER RESULTS AND SIMULATIONS

Three-dimensional finite-difference time-domain (FDTD) method simulations using Rsoft software with optical power monitors were used to study the EBS reflection and transmission properties. The 3-D-FDTD provided more accurate simulations for EBS losses than the 2-D-FDTD, due to significant transverse diffraction for which the 2-D-FDTD does not account.

The devices were built and tested for TE polarized light only, as the compressively strained InGaAsP QWs have a large TE gain and a small TM gain. The peak measured gain of the semiconductor optical amplifiers (SOAs) was 50 dB/mm. From this we calculated that the 30 μm ring had only 1.5 dB of gain per cavity round-trip. With such small net gain, minimizing insertion loss was crucial to realize compact filters and lasers. For this reason, the EBS couplers were designed for large incident angles of 30° to 32° to reduce insertion loss for the compact ring lasers. As shown in Fig. 5, simulated insertion loss decreases from 1 dB to 0.2 dB by increasing the incident angle from 20° to 32°.

To measure the insertion loss of the EBS coupler, a separate test structure as outlined in Fig. 6(a) is utilized. By fiber coupling a tunable laser, the optical power is recorded by an on-chip reverse biased SOA detector at the EBS input. Once the coupled-in optical power is determined, the detector is forward biased at its transparency current and the EBS reflection and transmission are measured by on-chip detectors. The measured insertion loss at 32° incident angle is 0.6 ± 0.5 dB. The

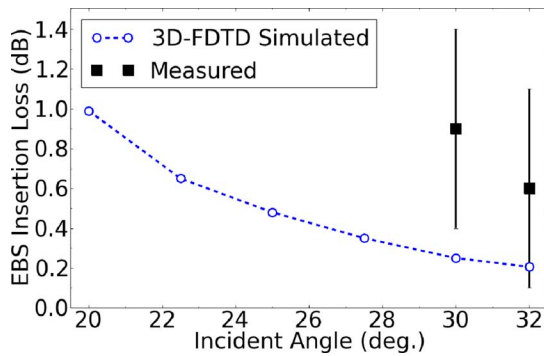


Fig. 5. Measurements and 3-D finite-difference time-domain simulations of the EBS coupler insertion loss versus incident angle for a 400-nm air gap.

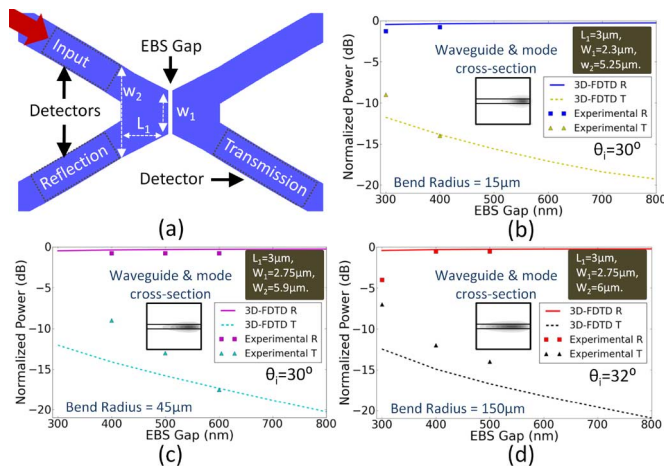


Fig. 6. (a) Schematic of trench test setup using an external tunable laser input and on-chip detectors on all ports. The input detector is used to measure the power coupled on-chip and then forward biased at transparency to test trench reflection (R) and transmission (T). Measured data and 3-D-FDTD coupling simulations for ring circumferences of (b) 30 μm , (c) 90 μm , and (d) 300 μm .

uncertainty occurs due to variation in the SOA transparency currents.

Simulations and experimentally measured values for reflection and transmission of the 30, 90, and 300 μm circumference rings are shown in Fig. 6. The wider gap EBS devices show the best agreement with the simulations. This is likely due to non-vertical trench sidewalls on the smaller EBS gaps. As shown in Fig. 2(a), the gap at the waveguide layer ($\sim 2 \mu\text{m}$ below the top layer) is narrower than the gap on the mask and has a nonvertical sidewall angle. These deviations results in higher transmission, due to the narrower gap, and increased insertion loss due to the nonvertical sidewall.

Variations to the EBS design were made for each bending radii to account for the differences in modal shape in the tightly curved waveguides. For tight bends, the mode is squeezed towards the outside of the waveguide. To accommodate this mode profile, the coupler width is reduced in devices with tighter bending radius as shown in Fig. 6(b)–(d). Unlike previous EBS couplers for straight and large radius of curvature waveguides that used a wide multimode platform region around the EBS trench [8], [10], the current design uses a “restricted” beam splitter keeping the mode highly confined up to the trench similar to work done in GaAs/AlGaAs [11]. The restricted EBS is

necessary for bending radius $\leq 150 \mu\text{m}$ to prevent excitation of higher-order-modes as the tight bending radius transitions to the straight beam splitter.

V. CONCLUSION

We have demonstrated compact flattened ring resonators down to 30 μm circumference with free spectral range of 13 nm. A novel process, using an etch delay mask, created deeply etched waveguides and air trenches in a single etch. The EBS couplers were designed with incident angles $\geq 30^\circ$ to minimize insertion losses for small rings with tight bending radii. Compact flattened rings are promising devices for use in the next generation of PICs as integrated lasers and WDM filters.

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Comparison of Comb-line Generation from InGaAsP/InP Integrated Ring Mode-locked Lasers

John S. Parker,¹ Pietro R.A. Binetti,¹ Ashish Bhardwaj,¹ Robert S. Guzzon,¹ Erik J. Norberg,¹
Yung-Jr Hung,² Larry A. Coldren¹

¹Electrical and Computer Engineering Department, University of California, Santa Barbara, CA 93106

²Dept. of Electronic Engineering, National Taiwan University of Science and Technology, 43 Keelung Rd., Sec. 4, Taipei 106, Taiwan
E-mail: JParker@ece.ucsb.edu

Abstract: We compare comb-line generation from a 30 GHz gain flattened ring mode-locked laser and two standard 30 GHz ring mode-locked lasers. The gain flattened ring has a 1.32 THz spectral width whereas the other devices have 420 and 630 GHz spectral widths.

OCIS codes: (250.5300) Photonic integrated circuits; (140.4050) Mode-locked lasers.

1. Introduction

InGaAsP/InP mode-locked lasers (MLLs) operating at 1.55 μ m wavelength are very stable pulse sources, which makes them attractive components for high-speed optical fiber communication [1]. Due to the multiple lasing modes that are necessary to form pulse-trains, these mode-locked lasers can also be used for frequency comb-line generation [2] and as multi-wavelength sources for coherent wavelength-division-multiplexing (WDM) [3]. Since the comb-line spacing is determined by the cavity length, integrated mode-locked lasers typically provide lines spaced at 10-100 GHz, which makes them suitable for the current and projected ITU grids. For this reason, a MLL that provides stable and broad comb-line generation has the potential to replace tens or hundreds of single channel DFB lasers. MLLs built on a highly versatile InGaAsP/InP material platform provide the capability to create photonic integrated circuits (PICs) with diverse functionality and systems-on-chip when combined with components that include: widely-tunable transmitters [4], tunable optical filters [5], and wavelength converters [6]. Furthermore, new applications in integrated offset frequency locking and light detection and ranging (LIDAR) will require stable and wide optical comb sources with lines spaced by 20-40 GHz. Such devices are based on the recently demonstrated integrated Optical Phase-Lock-Loop (OPLL) built on the InGaAsP/InP material platform [7]. The need for on-chip optical comb sources with GHz line spacing makes integrated mode-locked lasers a promising solution.

In a semiconductor mode-locked laser, the width of the generated comb spectrum is determined by the cavity dispersion and gain competition between the lasing modes. This gain competition occurs due to nonuniform material gain across wavelength. Intra-cavity gain flattening creates a more uniform gain profile by applying a filter with the inverse shape of the gain profile. Previously, sub-picosecond pulses with 4 nm spectral widths have been shown in a 30 GHz integrated MLL with a gain flattening filter [8].

By growing a broad distribution of different sized dots, quantum dot (QD) gain material can be grown to have a substantially broader gain bandwidth than quantum wells (QWs) or bulk. For this reason, integrated mode-locked lasers based on InGaAs QDs have shown a -3 dB spectral width of 14 nm at 1.3 μ m [9], while MLLs based on silicon evanescent material platform using QWs have shown a -10 dB spectral width of 8 nm at 1.5 μ m [2]. We present an InGaAsP/InP QW based ring mode-locked laser with a gain flattened filter (GFF) that provides -3dB and -10dB spectral widths of 10.5 nm and 15 nm respectively. We compare this result to two MLLs on the same material platform, without the GFF, which have -3dB spectral widths of 3.5 and 5 nm. The GFF incorporates an asymmetric Mach-Zehnder interferometer with one gain arm and one phase shift arm. This allows it to have a tunable extinction ratio and placement of the filter zero across the C-band. The GFF requires no additional processing steps and the entire device is defined by stepper lithography. The GFF can be used to improve the gain flatness on any material platform, including: QDs, QWs, and bulk. We have built the GFF on a standard QW material platform for ease of integration with other photonic devices previously demonstrated on this platform.

2. Experiments and Discussion

A standard offset quantum well (OQW) InGaAsP/InP integration platform was used with 7 QWs positioned above a 300nm thick 1.3Q waveguide (WG) with a confinement factor of 7.1%. A wet-etch removes the QWs for low loss passive WGs followed by a single blanket p-cladding regrowth. WGs were defined by stepper lithography on a photoresist/Cr/SiO₂ triple-layer mask. The patterned SiO₂ mask is used to mask the InGaAsP/InP in Cl₂/H₂/Ar etch chemistry with Inductively Coupled Plasma (ICP) Reactive Ion Etching (RIE).

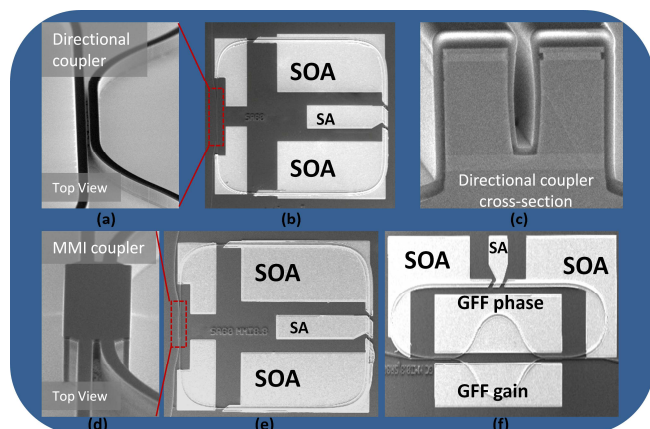


Fig. 1. Scanning electron microscope (SEM) images of (a) directional coupler (top view), (b) directional coupler based MLL, (c) directional coupler cross-section, (d) multimode interference (MMI) coupler, (e) MMI based MLL, and (f) MLL with gain flattening filter (GFF).

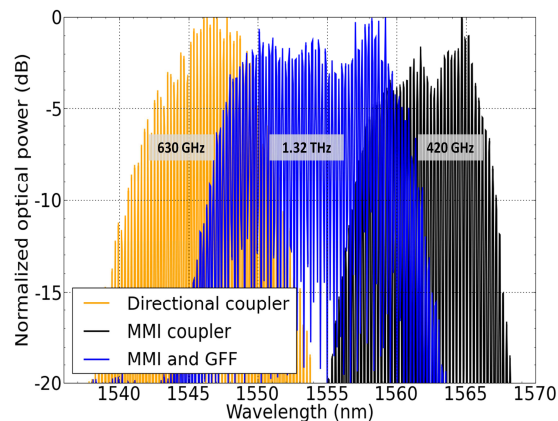


Fig. 2. Optical spectra from 30 GHz mode-locked lasers with a directional coupler, a multimode interference (MMI) coupler, and a gain flattening filter (GFF) with MMI couplers (-3dB freq. comb bandwidth is listed on each spectrum).

As seen in Fig. 1(a) and 1(b), the RIE lag effect, which acts to slow the etch rate of smaller features, was used to define a 125 μm long directional coupler with $\sim 2\%$ power coupling on a deeply etched ring with a single etch-step [10]. As shown in Fig. 1(c), the directional coupler gap is 700 nm wide with an etch depth of $\sim 2.5 \mu\text{m}$, terminated right above the InGaAsP WG layer. As shown in Fig. 1(d) and 1(e), the ring waveguide and the 100 μm long MMI with 50% power coupling, were created using a single 5 μm deep etch. These same MMI couplers were used to create the GFF, as shown in Fig. 1(f).

The drive current and absorber bias were varied to find the widest optical spectrum for each of the three devices. The laser outputs were measured with an optical spectrum analyzer (OSA), as shown in Fig. 2. To verify stable mode-locking, the devices were measured on an autocorrelator to observe pulse-trains and an electrical spectrum analyzer (ESA) to observe RF power. The -3dB spectral bandwidth of the MMI coupler based MLL, directional coupler based MLL, and GFF-MLL were 3.5 nm, 5 nm, and 10.5 nm respectively. These wavelength spans correspond to frequency comb widths of 420 GHz, 630 GHz, and 1.32 THz. The RF linewidth of the GFF-MLL was measured to be 600 KHz. This RF linewidth is typical for a passively mode-locked ring laser with QW gain material and can be reduced dramatically by active mode-locking using an RF drive signal. The optical linewidth was measured to be 30-60 MHz across the range of comb-lines using a heterodyne method with a high-speed photodiode, ESA, and a <1 MHz linewidth tunable laser. Narrower RF and optical linewidths improve the stability of integrated optical phase-locked loops and allow for higher QAM transmission in WDM.

In conclusion, we have fabricated integrated InGaAsP/InP comb generators based on 30 GHz ring mode-locked lasers. The mode-locked laser with a gain flattened filter generates a frequency comb that spans 1.32 THz.

This work was supported by the Office of Naval Research (ONR). A portion of this work was done in the UCSB nanofabrication facility, part of the National Science Foundation (NSF) funded NNIN network.

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Programmable Photonic Microwave Filters Monolithically Integrated in InP–InGaAsP

Erik J. Norberg, Robert S. Guzzon, John S. Parker, Leif A. Johansson, *Member, IEEE*, and Larry A. Coldren, *Fellow, IEEE*

Abstract—We demonstrate an integrated programmable photonic filter structure capable of producing bandpass filters with both tunable passband bandwidth and center frequency. Such filters could provide dynamic pre-filtering of very wide bandwidth analog microwave signals, essential to the next generation RF-front ends. The photonic filter is constructed from an array of uncoupled identical filter stages, each reconfigurable as a zero or a pole using an asymmetrical Mach-Zehnder Interferometer (MZI) structure with feedback. Integrated on a standard InP–InGaAsP material platform, semiconductor optical amplifiers (SOAs) and current injected phase modulators (PMs) are used to rapidly adjust the individual pole and zero locations, thereby reconfiguring the overall filter function. In this paper, we demonstrate cascaded filter structures with up to four filter stages, capable of producing a variety of higher order filters. Demonstrated filters have a free spectral range (FSR) of 23.5 or 47 GHz. A center frequency tunability over 28 GHz is demonstrated for a 2nd order bandpass filter, and a passband tunability of 1.9–5.4 GHz with stopband rejection >32 dB using 3rd and 4th order filters. Finally, the linearity of our active filters is investigated; a preliminary spurious-free dynamic range (SFDR) of 86.3 dB·Hz^{2/3} is obtained. However, we believe this number can be improved significantly by optimizing the design.

Index Terms—Microwave filters, optical filters, optical waveguide components, photonic integrated circuits (PIC), resonators.

I. INTRODUCTION

BOTH for commercial communication and military electronic warfare and radar, there is an ever increasing interest in RF-systems that can handle very wide instantaneous bandwidths as well as high frequency bands. Thus, RF-front ends with instantaneous bandwidths up to 100 GHz might soon be desired [1]. For the signal processing of such ultra-wide bandwidth signals, photonics can find indispensable utility, drawing on the inherent wide bandwidth tunability, low loss, and size, weight and power (SWaP) performance, compared to their electronic counterparts. For example, by rapidly pre-filtering wide bandwidth analog signals in the optical domain the analog-to-digital conversion (ADC) and subsequent digital

signal processing (DSP) can be significantly relieved [2]. Such photonic filters should have a tunable passband and center frequency, to accommodate different channel widths and frequencies, as well as enable tracking and sweeping in the RF domain.

Optical signal processing was proposed almost three decades ago [3], and has been immensely investigated since [2]. However, fiber and bulk optics is inevitably limited by incoherent filtering due to the limited stability against environmental changes. This makes it difficult to achieve negative filter coefficients and the very complex filter characteristics needed for the RF signal processing application. Integrated optics, on the other hand, can provide the stability needed for coherent filtering, and have already demonstrated usefulness as channelizing add/drop filters in wavelength division multiplexing (WDM) applications [4], [5]. Recently, there have also been significant advances in the realization of integrated photonic filters pushing towards the RF domain [1], [6]–[12]. We have previously proposed and demonstrated the basic building block for a cascaded filter structure, that incorporates a resonator and Mach-Zehnder Interferometer (MZI) for reconfigurable filter functions [6]. Similar filter building blocks have in parallel been proposed and demonstrated on other integration platforms including: silicon-on-insulator (SOI) with no optical gain [7], [8] and SOI-IIIIV hybrid [9]. We have also demonstrated the ability to cascade several filter stages to produce higher order filters with tunable filter characteristics [11], [12]. In this paper, we present a deeper investigation and description of our optical filter design, and present more cascaded stages together with improved results on passband bandwidth and center frequency tunability. Additionally, we investigate the linearity performance of our active devices by measuring the spurious-free dynamic range (SFDR).

II. FILTER DESIGN

A. Programmable Filter Design

Working within the coherent filter regime, versatile tunable filters can be achieved using a cascaded filter design that incorporates both ring resonators and MZIs, to provide poles and zeros respectively [13]. For such cascaded filters, there are two main design categories, coupled and uncoupled arrays; each approach has its advantages and drawbacks. The main advantage of a coupled resonator arrangement is the enhanced filter roll-off and improved extinction compared to the uncoupled design, resulting from the higher pole magnitudes obtained from the same number of resonators [13]. For the coupled system, the filter passband bandwidth is set by the inter-stage coupling strength.

Manuscript received December 24, 2010; revised March 12, 2011; accepted March 20, 2011. Date of publication March 28, 2011; date of current version May 20, 2011. This work was supported in part by the Defense Advanced Research Projects Agency (DARPA) under the PhASER project. A portion of this work was performed in the UCSB Nanofabrication Facility, part of the NSF funded NNIN network.

The authors are with the Department of Electrical and Computer Engineering, University of California Santa Barbara, Santa Barbara, CA 93106 USA (e-mail: norberg@ece.ucsb.edu).

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Digital Object Identifier 10.1109/JLT.2011.2134073

This requires tunable couplers, which entails additional control and can be more difficult to implement. On the contrary, for an uncoupled system, the filter shape is independent of coupling strength and the filter synthesis is made very simple through multiplied transfer functions. Although the coupled and uncoupled design is fundamentally different, very comparable filter functions can be achieved, as we have previously demonstrated [10], [11].

In this work, in favor of control and simplicity in filter synthesis, we focus on entirely uncoupled filter arrays. For maximum flexibility in filter synthesis, each filter stage should be designed to be reprogrammable as either a zero or a pole, with arbitrary magnitude and phase. The scattering parameters and magnitude response for the individual filter stage and the overall filter array are then given by:

$$\begin{aligned} |S_{21}^{\text{pole}}|^2 &= \left| \frac{A}{1 - G_p e^{-j\beta L_p}} \right|^2 \\ &= \frac{A^2}{1 - 2G_p \cos[\beta L_p] + G_p^2} \end{aligned} \quad (1)$$

where $\beta L_p = (2\pi)/(FSR)(f - f_c) + \varphi_p$, or,

$$\begin{aligned} |S_{21}^{\text{zero}}|^2 &= \left| B(1 - G_z e^{-j\beta L_z}) \right|^2 \\ &= B^2 (1 - 2G_z \cos[\beta L_z] + G_z^2) \end{aligned} \quad (2)$$

with $\beta L_z = (2\pi)/(FSR)(f - f_c) + \varphi_z$. (1) and (2) describes the magnitude response of the individual filter stage programmed as either a pole or a zero, respectively. G_p (G_z) denotes the pole (zero) magnitude, and φ_p (φ_z) the pole or zero phase, while $f - f_c$ denotes the deviation from some given center frequency f_c , and FSR denotes the free spectral range of the pole or zero. A and B represent the gain or loss that the signal experiences going through each stage, but does not influence the relative filter shape. Given by the uncoupled nature of the structure, (3) shows how the overall magnitude transfer function for a filter array of N stages results from the product sequence of the individual filter stages (j).

$$|S_{21}^{\text{Total}}|^2 = \prod_j |S_{21}^j|^2. \quad (3)$$

Fig. 1 are simulated using (1)–(3), and demonstrates the flexible filter synthesis that can be achieved with a relatively simple filter array. Simulating only four filter stages using only zeros, only poles or a mix of zeros and poles, bandpass and bandstop filter are synthesized. The filter functions are displayed in normalized frequency for ease of comparison, and the programmed pole and zero locations for each filter case are shown in the pole-zero diagrams, inset in Fig. 1. The pole magnitudes were limited to <0.9 for the simulations to be realistic. We experimentally found that for pole values above ~ 0.9 mode competition becomes prominent. In essence, the gain (pole values) start to clamp for the majority of the mode spectrum while only one or a few modes experience higher pole values, i.e., the device approaches lasing.

In the next section, we describe the actual optical filter design, and explain how the pole and zero reconfigurability with

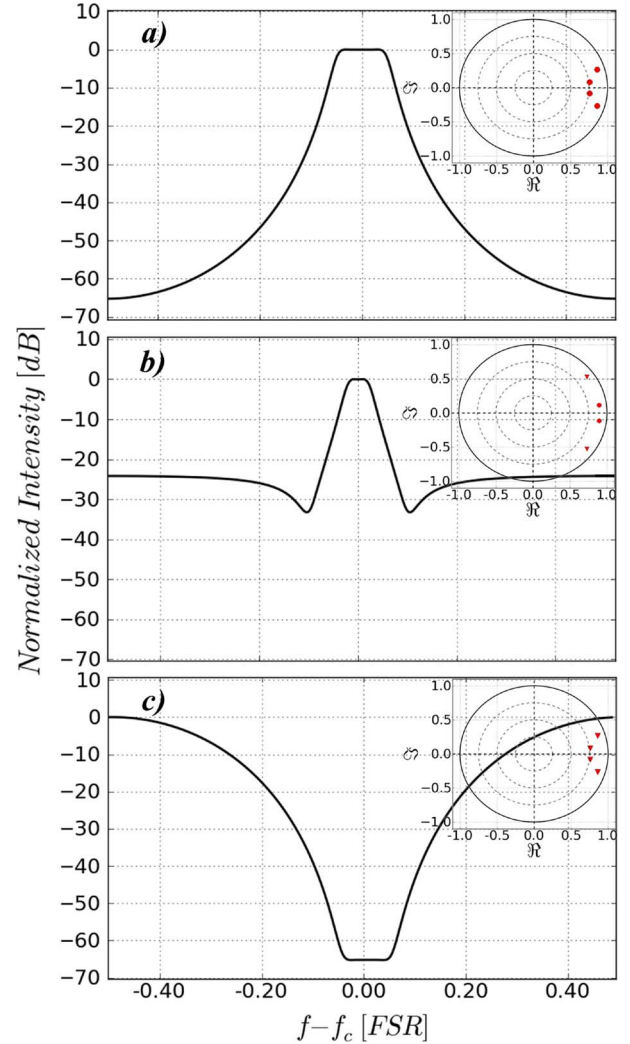


Fig. 1. Simulated 4th order reconfigurable filter responses. (a) Bandpass filter using only poles. (b) Bandpass filter using two poles and two zeros, yielding sharper filter roll-off but poorer stopband rejection. (c) Bandstop filter using only zeros. Inset show pole (circle) and zero (triangle) locations in each case.

arbitrary phase and magnitude are achieved in the single filter stage.

B. Optical Filter Design

For the coherent filtering in the previous section to be possible, the optical filter design is implemented on a single chip using monolithic integration. Still, in favor of control and stability as well as potential fabrication yield issues, we have in this work limited the filter array to five filter stages. A schematic of the optical filter chip is shown in Fig. 2(a), with the single filter stage highlighted in Fig. 2(b).

The single filter stage in Fig. 2(b) consists of an asymmetrical MZI with a feedback path connecting the output to the input, thus forming two resonator paths with different delay. Therefore, the single filter stage response really consists of two poles and one zero, however, the idea as outlined in the previous section is to utilize either only one pole or one zero per unit cell at any one time. The individual pole or zero is isolated by utilizing active semiconductor optical amplifier (SOA) elements

that provide gain or absorption. These SOAs are used to amplify or turn off different waveguide paths. If one of the lower waveguides is turned off, by reverse biasing SOA₁ ($G_1 = 0$) or SOA₂ ($G_2 = 0$), a single pole response is isolated, as shown in Fig. 2(c), and described by the optical scattering parameters in (4) and (5) respectively. If the top waveguide is turned off instead, a single zero through the remaining MZI path results, this is shown in Fig. 2(c) and described by the scattering parameters in (6). By designing the lengths of the different waveguide paths ($L_{1,2,3}$), desired FSR and filter bandwidths are achieved. In this work, the two resonators have a length of 1.750 or 3.500 mm, corresponding to time delays of 21.5 and 42.5 ps, or FSRs of 47 and 23.5 GHz respectively. The MZI was designed with a path difference of 21.5 ps (FSR of 47 GHz) as well.

$$\begin{aligned} & \left| S_{21}^{\text{pole2}} \right|_{G_1=0}^2 \\ &= \left| \frac{G_{ff} 0.5 \alpha_2 G_2}{1 - 0.5 \alpha_2 \alpha_3 G_2 G_3 e^{-j[\beta(L_2+L_3)+\varphi_2]}} \right|^2 \end{aligned} \quad (4)$$

$$\begin{aligned} & \left| S_{21}^{\text{pole1}} \right|_{G_2=0}^2 \\ &= \left| \frac{G_{ff} 0.5 \alpha_1 G_1}{1 + 0.5 \alpha_1 \alpha_3 G_1 G_3 e^{-j[\beta(L_1+L_3)+\varphi_1]}} \right|^2 \end{aligned} \quad (5)$$

$$\begin{aligned} & \left| S_{21}^{\text{zero}} \right|_{G_3=0}^2 \\ &= (0.5 G_{ff})^2 \left| 1 - \frac{\alpha_2}{\alpha_1} G_1 G_3 e^{-j[\beta(L_2-L_1)+\varphi_2-\varphi_1]} \right|^2. \end{aligned} \quad (6)$$

The optical scattering parameters shown in (4)–(6), includes all optical effects to first order. 0.5 appears in the equation assuming lossless 3 dB couplers throughout, L and α is the length and fractional loss of the different waveguide sections, G and φ represent the gain and phase added from the SOA and phase-modulators (PMs) respectively, and β is the propagation constant of the waveguide. Equation (4) and (5) are analog to (1), and (6) to (2). For example, comparing (6) and (2): it is clear from the phase condition that $L_z = L_2 - L_1$ and $\varphi_z = \varphi_2 - \varphi_1$. While the amplitude transmission gives $B = 0.5 G_{ff}$ and $G_z = \alpha_2 / \alpha_1 G_1 G_3$. Thus, we see that the pole and zero locations governed by G and φ in (1) and (2) are in the optical filter design simply controlled by adjusting the gain of the SOAs and phase of the phase modulators, since the waveguide losses and coupling ratios are fixed. We will for the sake of conciseness, in this paper, refer to G and φ in (1) and (2) when analyzing our measured filter functions. Finally, we note that if no phase ($\varphi_{2,3} = 0$) is applied, there is a π (half FSR) offset between the short and long resonator response, as shown in Fig. 2(c). This is also expressed in (5) compared to (4) with the + instead of in the denominator. For the longer resonator case described in (5), this discrepancy is caused by the $-\pi/2$ acquired phase from each MMI cross-couplings in one round trip.

III. DEVICE FABRICATION AND INTEGRATION PLATFORM

In order to utilize on-chip gain and fast phase modulation we have turned to the InP–InGaAsP material system. This mature photonic integration platform has the advantage of efficient

semiconductor amplifiers in the telecom C-band, and efficient and quick phase modulation using current injected phase modulators. The re-programming and tuning time constants of the filter is ultimately limited by the response time of the gain and phase controllers, which here is governed by the carrier lifetime on the ns time scale [14]. This ultimately allows for close to real-time tracking and sweeping in the RF domain, essential for many applications.

For long filter cascades with significant accumulated loss, on-chip gain is also necessary to avoid signal degradation and maintain a reasonable noise figure. However, when utilizing SOAs, careful consideration must be taken to minimizing the added amplifier noise and avoid gain saturation effects. These effects will degrade the noise figure and the third order intercept point (IP3), respectively, and lead to a SFDR. For this reason, we have utilized a high saturation and low gain offset quantum well (QW) integration platform. In this integration scheme, the quantum wells are placed on top of the waveguide for lowered active confinement factor and thus more linear amplifiers [15], compared to centered quantum wells. The SFDR performance of our programmable filters is characterized and discussed in Section IV.E of this paper.

Our programmable photonic filters are monolithically integrated, with all mask steps patterned by standard i-line stepper photolithography. Only a single blanket InP regrowth is needed to provide the p-cladding, after the quantum wells have been selectively removed to create passive waveguide sections. Attributed to the simple fabrication process, an overall yield of 96% (24 out of 25 tested) of fully operational single filter stages was achieved. Fig. 3 shows a fabricated photonic filter with five cascaded unit cells that has been wire-bonded to a carrier for interfacing with two 14-pin multi connector probe-cards. The overall dimension of this device is 4.5×1.5 mm. In order to avoid radiation loss from waveguide bends and keep the fabrication complexity to a minimum, deeply etched waveguides were used for the entire device; a cross section of the waveguide is shown in the inset of Fig. 3. For coupling, 3-dB restrictive multimode-interference (MMI) couplers, 100 μm in length, were utilized everywhere, as shown in the inset of Fig. 3. The couplers have a measured total insertion loss of ~ 1.0 dB/coupler. More details on the fabrication and integration platform have been published elsewhere [16].

IV. EXPERIMENTS AND DISCUSSION

A. Measurement Setup

In order to demonstrate the filtering function of our device, we characterize our filter in the optical as well as in the RF-electrical domain. The optical measurement is straight forward, as it only requires a broadband amplified spontaneous emission (ASE) spectrum input and an optical spectrum analyzer (OSA) to measure the output of the filter. The advantage of this technique is the wide bandwidth available, typically several tens of nm (several THz) using an erbium doped fiber amplifier (EDFA). Thus, this is useful for imaging more than one free spectral range (FSR) of our filter functions. However, the resolution of the OSA is limited to 0.01 nm (1.25 GHz), and will therefore not truthfully resolve the shape of any GHz

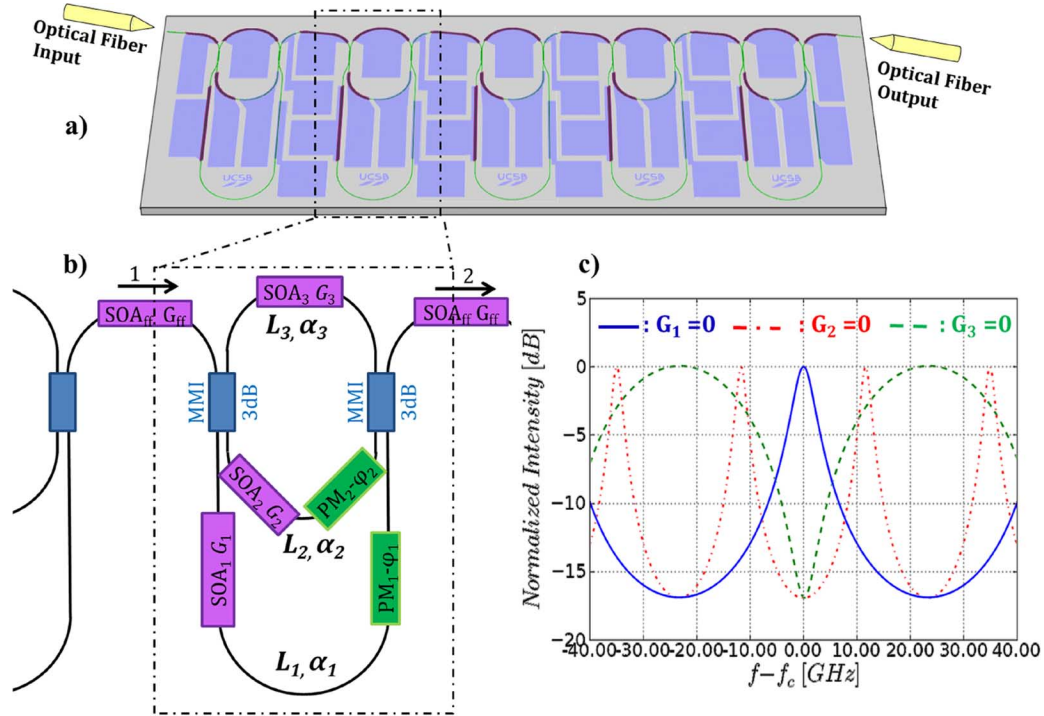


Fig. 2. (a) Illustration of programmable filter array chip. (b) A single filter stage and its functional components (SOAs, PMs and 3 dB MMI couplers) shown schematically. (c) Different filter responses generated by turning off different waveguide paths in the single filter stage ($G_{1/2/3} = 0$), isolated pole and zero responses results.

wide filter shapes, especially not the ripple magnitudes in the passband.

In order to increase the resolution, but also to more closely mimic the real photonic microwave application, we use a heterodyne detection scheme to image the filter in the electrical RF-domain. A schematic of the measurement is shown in Fig. 4. In this measurement, a band limited noise spectrum is input to the device under test (DUT). This input simulates a wide bandwidth single sideband (SSB) modulated microwave signal that has been carrier suppressed. The noise spectrum is generated by an amplified spontaneous emission (ASE) source and is amplified by an EDFA before being sent through a circulator connected to a fiber Bragg grating (FBG) to produce the band limited input signal. In the heterodyne detection, the filtered signal is down converted using a tunable local oscillator (LO) laser, placed just to the side of the initial noise spectrum, as shown in the inset of Fig. 4. A 40 GHz photodiode (PD), with a 38 GHz broadband amplifier and a 50 GHz electrum spectrum analyzer (ESA) is used to image the output of the filter device. All data are normalized to the throughput (w/o DUT) in order to remove ripples originated from the FBG spectrum. The added receiver noise is measured by turning off the LO laser, and is subtracted from the measured data. The resolution of this RF electrical measurement is limited by the relative frequency stability of the LO laser and the DUT, over the time scale of the ESA frequency sweep. An upper bound on this resolution was established by comparing many subsequent measurements of the filter function. The maximum frequency deviation and hence worse resolution was found to be ~ 50 MHz. The frequency drift is attributed to the DUT, as the frequency stability of the LO laser was characterized separately to ~ 10 MHz. The total band-

width of the RF electrical measurement is about 35 GHz, limited by the electrical components. Thus, the optical and electrical RF measurements are good compliments to each other, being able to characterize the DUT in both high resolution and over a wide bandwidth. All measurements were done continuous wave (CW) at room temperature.

B. Single Cell Filter Responses

We start by demonstrating the programmability of the single filter stage. The optical measurement was here used, to image a wide bandwidth and characterize the full frequency tunability. Also, for first order IIR and FIR filters there are no ripples or other details expected in the passband that would require the high-resolution measurement. However, we note that the measured stopband rejection for the MZI zero in Fig. 5(b) would possibly be slightly larger if a finer measurement resolution was used.

Fig. 5 demonstrates the reconfigurability and tunability of the single filter stage. In Fig. 5(a) the short resonator pole filter has been isolated by reverse biasing SOA₁ (see Fig. 2). By adjusting the currents on SOA₂ and SOA₃ the magnitude of the single pole is adjusted continuously. In order to keep the filter fixed in frequency (phase), the PM₂ is utilized to compensate for the parasitic phase shift induced by heating (positive added phase) and current injected (negative added phase), when changing the current on the SOAs. The pole-zero diagram of Fig. 5(a) shows the pole locations, as found by fitting the measured filter magnitude responses to (1). In Fig. 5(b) the arbitrary phase of the single filter stage is demonstrated using the MZI zero configuration. 2π of tunability is achieved by utilizing only the phase modulator of one MZI arm. Tuning more than 2π is never nec-

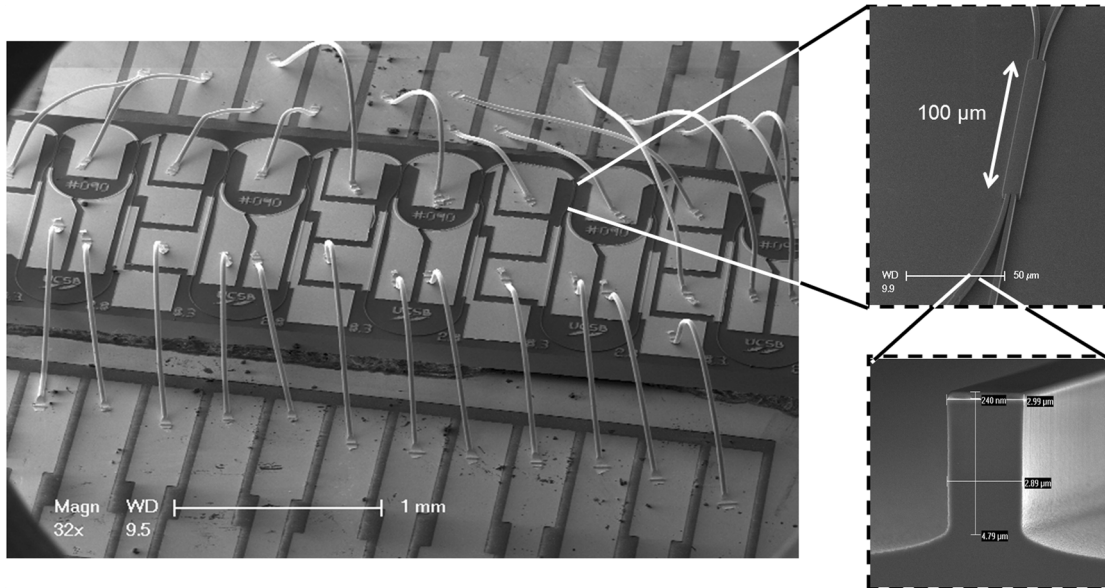


Fig. 3. Scanning electron microscopy (SEM) image of a programmable photonic filter device wire bonded to a carrier. Insets show deeply etched MMI coupler (upper) and a cross section of deeply etched waveguide (lower).

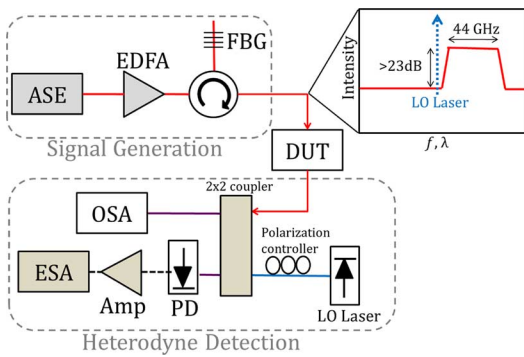


Fig. 4. Schematic illustration of the electrical RF-domain measurement setup.

essary, since this corresponds to the filter FSR where the pass-band is repeated. Although here showing ~ 47 GHz of tunability, in reality the zero (and poles) can be placed anywhere in the SOA gain bandwidth (typically around 5 THz wide, i.e., the optical C-band).

We note that there is a slight (< 2 dB) variation in stopband rejection as the zero is tuned around the unit circle (or over 47 GHz). This is due to the unbalancing of the MZI caused by the parasitic loss from free carrier absorption (FCA) when injecting current in the phase modulator, in only one of the MZI arms. This parasitic is easily compensated for by adjusting the SOA currents to balance the MZI path gains. However, to illustrate the point and quantify the magnitude of this parasitic, the SOA currents were kept unchanged in this demonstration.

In general, the pole and zero location can be tuned a full 2π . However, the MZI zero magnitude is limited to about 0.77 (assuming minimum phase zero), or ~ 18 dB of stopband rejection, as demonstrated in Fig. 5(b). The pole magnitude is not inherently limited in this fashion. But as the poles are tuned closer to the unit circle, the optical resonator approaches the lasing condition. This implies modal gain competition, which makes

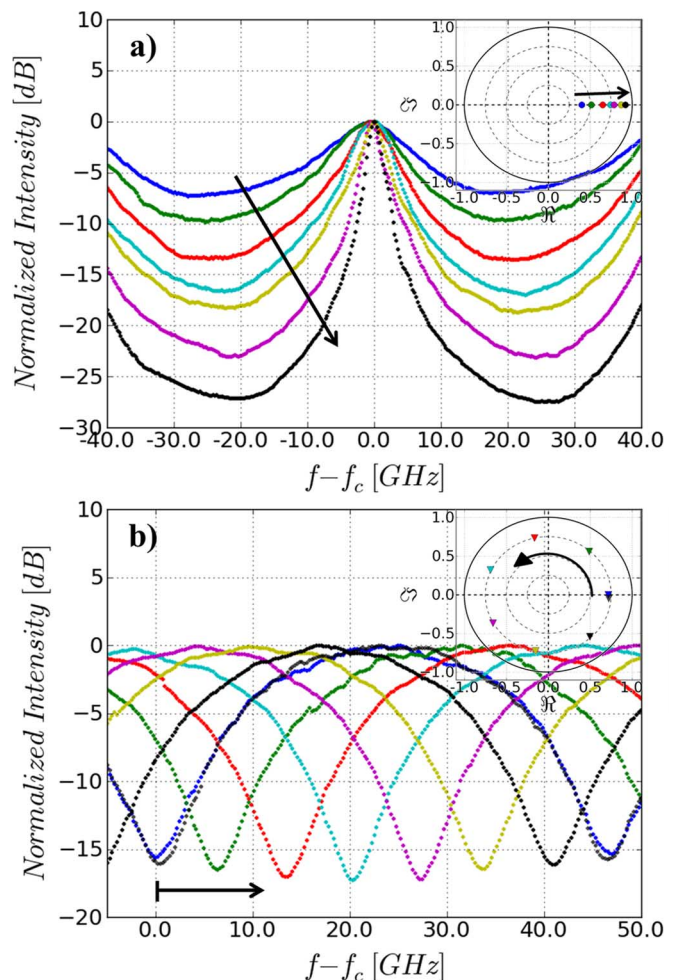


Fig. 5. Measured filter responses of a single filter stage reconfigured as a pole in (a) or zero in (b). Arbitrary placement of the pole/zero in the complex plane, demonstrated by independently adjusting the magnitude in (a) and phase in (b).

the filter synthesis non-linear, therefore compromising the linear filter synthesis and making the filter more difficult to control. In order to limit such negative effects, we decided to limit the pole magnitudes to <0.9 when synthesizing higher order filters in this work.

C. Higher Order Filters-Versatile Filter Synthesis

In order to demonstrate the versatile filter synthesis of our proposed cascaded filter structure, a variety of filter shapes are here demonstrated in Fig. 6. The filters are measured in the RF domain with higher resolution to accurately reveal the filter shapes, including quantifying in-band filter ripples. All filter responses have been centered at zero frequency for easy comparison. In the measurement the frequency offset between the filter center frequency and the LO ($f_c - f_{LO}$) is typically around 20 GHz, in order to best image the full filter FSR. Simulations have been superimposed on the measured data (dashed curves in Fig. 6), and shows a good theoretical agreement with the ideal linear filter functions, described by (1)–(3). The pole and zero locations for each filter response are thereby also extracted.

Utilizing the minimum of two poles, a bandpass filter is created in Fig. 6(a). This filter was created with the long resonator delay and identical pole values of 0.73, a ~ 3.5 GHz wide passband with 0.2 dB ripple and 23.5 GHz of filter FSR is demonstrated. By introducing an additional pole, larger stopband rejection and improved filter roll-off is achieved, as also shown Fig. 6(a). This third-order filter has a center pole magnitude of 0.74 with 0.83 magnitude poles on either side; the in-band ripple is 0.4 dB. Another way to improve rejection and roll-off is by introducing additional zeros instead of poles. This is illustrated in Fig. 6(b), where a total of four stages were utilized to create an elliptical filter with two poles and two zeros. The zeros are placed on either side of the passband. The π phase difference between the poles and zeros expected from the transfer functions (compare (5) and (6) and Fig. 2(c)), can also be seen in the pole-zero plot inset in Fig. 6(b).

The bandwidth over which the filter can operate is determined by the FSR, due to the repetition of the passband. For the longer resonator delay used to synthesize the filters in Fig. 6(a), (b), the FSR is 23.5 GHz. By using additional zeros, the FSR of the filters can be extended by placing zeros over neighboring passbands. This requires that the FSR of the zeros and poles are designed accordingly; in our single filter stage the FSR of the MZI zero is twice that of the long resonator delay (47 versus 23.5 GHz). In Fig. 6(c), two zeros are placed over the next filter order and thus enhancing the FSR from 23.5 to 47 GHz.

D. Passband and Center Frequency Tunability

In the previous sections we have demonstrated the programmability of the single filter stage, and how several cascaded stages can provide versatile filter synthesis of higher order filters. In this section, we investigate general bandpass filters that have both bandwidth and center frequency tunability. These are the key filter functionalities desired for the optical signal processing in microwave photonic links, as was described in the introduction.

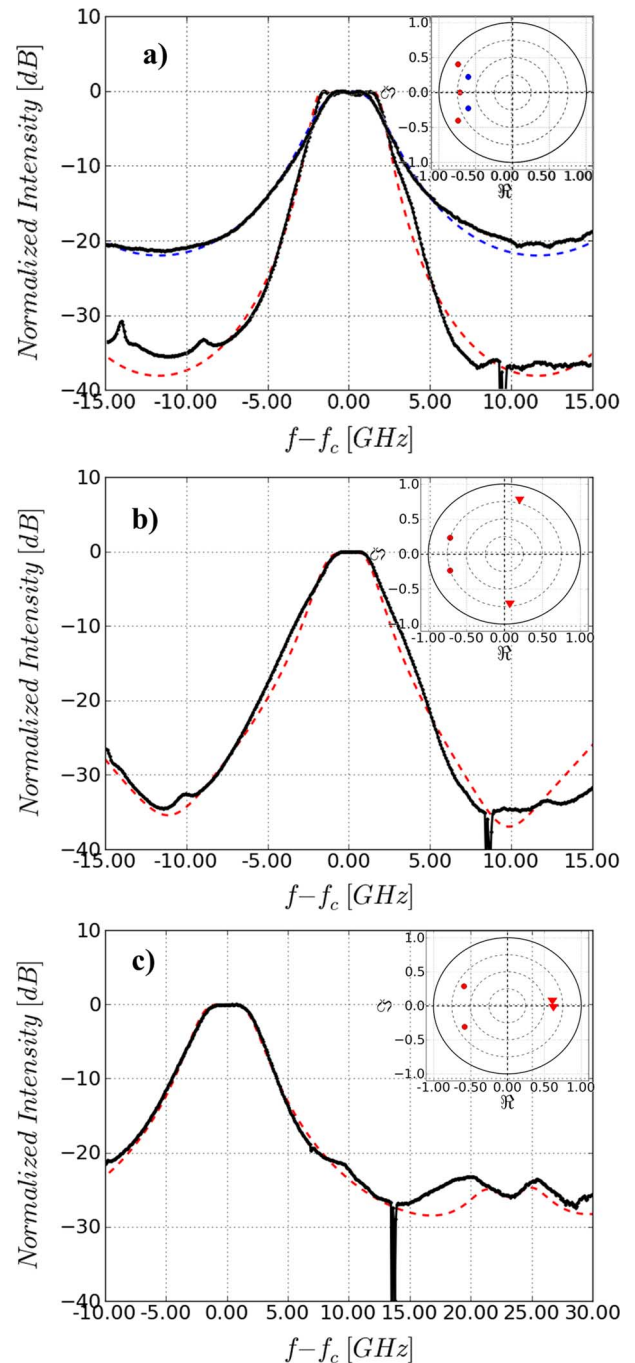


Fig. 6. Examples of higher order filters synthesized with our programmable filter device. Experimental data is represented with solid lines, theoretically fitted filter functions are superimposed with dashed lines. The fitted pole (circle) and zero (triangle) locations for each case are shown in the pole-zero diagram insets. The narrow notch feature evident in the experimental data (solid) is an artifact of the measurement, caused by a noise spike in the receiver resulting in the notch when the receiver noise is subtracted. (a) 2nd (red) and 3rd (blue) order bandpass filter using only poles. (b) Bandpass filter utilizing both zeros and poles. (c) 2nd order bandpass filter with zeros placed to eliminate the next filter order and thus double the FSR.

A family of filter functions have been programmed and superimposed in Figs. 7 and Fig. 8 to demonstrate the bandwidth and center frequency tuning capability of the filter device. The measured filter responses have again been fitted using (1)–(3) to find the pole locations. However, the actual simulation curves

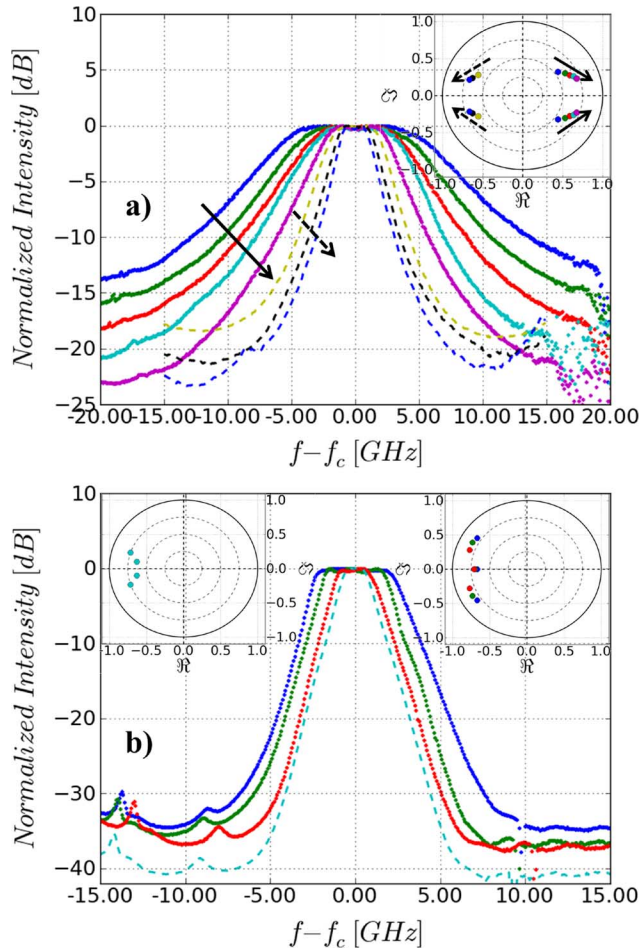


Fig. 7. (a) Bandwidth tunability for a 2nd order bandpass filter using the short (solid) and long (dashed) resonator. (b) Bandwidth tunability achieved with 3rd (dotted) and 4th order (dashed) bandpass filter.

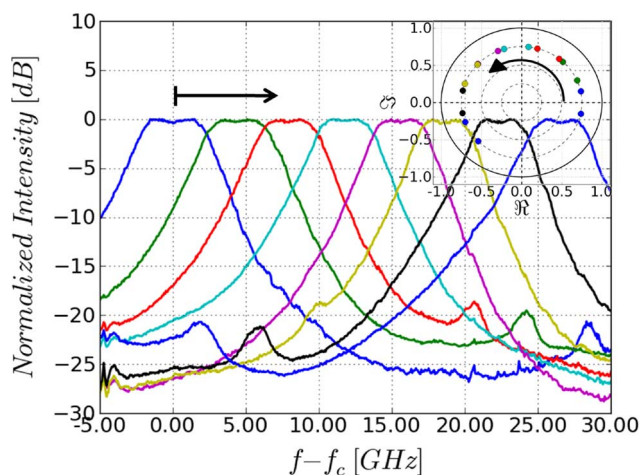


Fig. 8. Center frequency tunability demonstrated using a 2nd order bandpass filter.

have been left out from the figures to preserve the clarity of the measured filter responses.

Fig. 7(a) demonstrates the bandwidth tunability of a 2nd order bandpass filter, utilizing either the short or the long resonator

delay (solid and dashed line respectively). The passband tunability is achieved by introducing a phase difference between the poles that gives a desired bandwidth, and then adjusting the pole magnitude to get a preferred passband ripple; here, all ripples were kept < 0.3 dB. The arrows in the pole-zero diagram of Fig. 7(a) show how the poles move in the complex plane when the bandwidth is tuned. A total 3 dB bandwidth tunability from 14 down to 3 GHz is here demonstrated while keeping the stopband rejection > 13 dB. For the wider bandwidth filters, a low pole values must be utilized to achieve the flat passband; this unfortunately translates into slower filter roll-off and lower stop band rejection, as evident in Fig. 7(a). By introducing more filter stages (i.e., more zeros and/or poles), filter extinction and roll-off is improved. Fig. 7(b) shows the filter bandwidth tunability achieved using three (dotted) or four poles (dashed).

The stopband rejection is kept > 33 dB, while the bandwidth is adjusted from 1.9–5.4 GHz. The polar plots of Fig. 7(b) display the pole arrangement of these higher order filters. It shows that these filters are neither a classical Butterworth nor a Chebyshev Type I filter [17], but rather a combination of the two. Fig. 7(b) also demonstrates the limit of measurable passband rejection in the experimental setup; the spurious peaks showing up in the stopband are caused by the measurement setup.

The second important functionality of a photonic filter is center frequency tunability. This should ideally be achieved without changing the filter shape. The frequency tuning of our filter is achieved by tuning the individual poles and zeros (i.e., filter stages) by the same amount. Thus, every filter response demonstrated previously, can also be arbitrarily tuned in center frequency. Fig. 8 demonstrates the frequency tunability using a second order bandpass filter, where the shorter resonator delay is utilized. The filter shape is kept roughly constant with a passband bandwidth of ~ 5 GHz, while the center frequency is tuned from 0 to 27 GHz. The pole plot shows how the poles are tuned as a pair in the unit circle with a fixed phase difference and constant pole values of 0.75. The filter can be tuned a full 48 GHz (2π), but the tuning bandwidth is here limited by the measurement bandwidth to image the filter responses. We note that in a real application, the filtering domain is really $f_c - f_{lo}$ to $f_c - f_{lo} + 48$ GHz, based on the heterodyning receiver scheme. In this experiment, $f_c - f_{lo} = 10$ GHz, thus the filtering domain was in fact 10–58 GHz. This ability of signal filtering at arbitrary frequencies is a quality of photonic filtering unmatched in electronics.

E. Filter Linearity

For many real system applications, the requirement of a linear signal transfer function is very crucial. For microwave applications this is characterized by the spurious-free dynamic range (SFDR). Typical microwave applications, including radar, desire SFDR numbers in the range 105–120 dB·Hz $^{2/3}$ [18], [19]. A strength of our active filter device is the ability to compensate for inherent signal loss that would otherwise yield very large noise figures (NF) and degrade the SFDR. However, there is also a drawback in using active semiconductor material, in the introduction of excess noise and the potentially non-linear gain.

The noise figure is easily quantified by measuring the output spontaneous emission spectral density (S_{sp}) together with the signal gain (G). The NF is given by [20]:

$$NF = \frac{2S_{sp}}{h\nu G} + \frac{1}{G} \quad (7)$$

where the first term corresponds to the ASE noise and the second term is the enhancement in shot noise. The electrical noise current generated in the heterodyne detection, assuming ideal shot noise limited detection, is then given by

$$i_{noise} = \sqrt{2qR(P_{out} + P_{LO})NF} \quad (8)$$

P_{out} is the optical power output from the filter (signal together with the generated ASE noise power) and P_{LO} is the power of the LO.

The filter non-linearity can be characterized by passing two laser tones through the filter passband and examining the generated four-wave mixing (FWM) intermodulation distortion (IMD) terms. By varying the input laser power and recording the power in the fundamental and the third order intermodulation distortion (IMD3) terms, an equivalent optical output third order interception point (OIP3) is found. Again, the optical power is converted to an electrical current in the heterodyne detection scheme according to

$$i_{OIP3} = \sqrt{P_{OIP3}P_{LO}}R. \quad (9)$$

Utilizing a strong LO, $P_{LO} \gg P_{in}$ (in our measurement $P_{LO} = 10$ dBm $\gg P_{out} = -10$ dBm), the LO power cancels out in the expression for the SFDR

$$SFDR = \left(\frac{i_{OIP3}^2}{i_{noise}^2} \right)^{2/3} \approx \left(\frac{P_{OIP3}R}{2qNF} \right)^{2/3}. \quad (10)$$

This approach of characterizing the non-linearity of an optical device using two laser tones w/o modulators, has been investigated before [21], [22]. Compared to the more conventional approach of producing the input optical tones using optical modulators [23], this measurement eliminates the possibility of non-linearities originated from the optical modulators and being amplified in the SOAs [22].

We have characterized the SFDR of a two-stage filter device, while synthesizing a bandpass filter similar to those shown in Fig. 7. Two stable DFB lasers were used as the fundamental input tones, and were spaced by 110 MHz. In order to resolve the fundamental and generated IMD tones, the same receiver setup as in Fig. 4 was utilized, but without the electrical amplifier. The DC optical power was kept constant in the measurement by applying a third laser input to the filter, spaced far away from the two DFB lasers to avoid FWM with this laser. The OIP3 of the receiver (PD and ESA) was measured to be >30 dBm. A down converted filter output is shown in the inset of Fig. 9. Fig. 9 plots the powers of the fundamental and third order intermodulation tones versus the fundamental tone. The data is fitted to lines with slopes of 1 and 3 as predicted by theory; from this an extrapolated optical OIP3 point of -3.2 dBm is established.

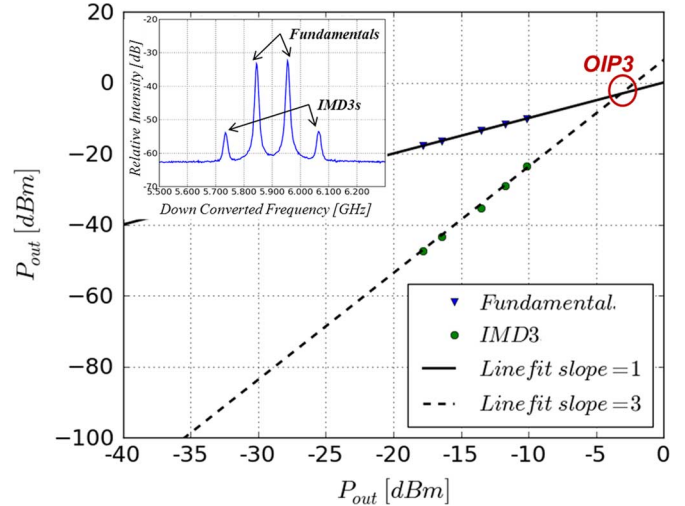


Fig. 9. Measured optical OIP3 for our active photonic filter structure. Inset shows a spectrum with the fundamental and generated IMD3 tones.

The NF was measured to be 23.2 dB, yielding an SFDR of 86.3 dB* Hz $^{2/3}$.

We believe that the SFDR number established here can be significantly improved upon, mostly by redesigning the amount of gain in the filter. In the current device design, there is a large overdesign in gain with around 16 dB excess gain in each resonator. Thus, the SOAs are currently biased close to transparency where they are very nonlinear and have worse NFs [15], [19]. Also by optimizing the actual SOA epitaxial design the linearity will improve significantly. The current SOA design have a maximum 3-dB saturation power (P_s) of 11.4 dBm, while we have previously demonstrated SOAs with $P_s > 20$ dBm on a similar integration platform [24], where the OIP3 scales with P_s^2 [21]. It is expected that scaling to more filter stages will not produce much worse NFs (and SFDR), since, when cascading amplifiers the overall NF can be limited if the gain is distributed correctly, similar to cascaded electronic amplifiers [20].

V. CONCLUSION AND FUTURE DIRECTION

We have investigated a novel programmable photonic filter architecture, consisting of an array of identical filter stages, each capable of producing a single zero or pole. We first demonstrated the reconfigurability of the single filter stage and the ability to arbitrary place zeros and poles in the complex plane. Next, versatile filter synthesis of various higher order filters was presented. Finally, we demonstrated a bandpass filter with tunable passband bandwidth of from 1.9–14 GHz, and center frequency over 27 GHz. Such filter characteristics could be valuable for real analog signal processing applications of wide bandwidth signals. For many RF-applications however, a sub-GHz filter is ultimately desired. The lower limit on passband bandwidth presented in this paper (1.9 GHz) is inherent to the resonator delays. In the future, the bandwidth could be narrowed, simply by making longer delays.

In this work, a total of five cascaded filter stages were monolithically cascaded, however, so far a maximum of four stages has simultaneously been utilized to synthesize filters. This

is attributed to the limited number of current/voltage control sources available in the testing setup and the complexity of manual control. Future work will include interfacing the filter with a computer or a field programmable gate array (FPGA). This will allow us to scale to larger filter structures and improve the ease of filter synthesis and control. We investigated the linearity of our active filter design, with a resulting SFDR of $86 \text{ dB} \cdot \text{Hz}^{2/3}$. This is unfortunately not enough for most practical RF-system applications, but we are confident that this number can be greatly improved by re-designing the amount of gain in the device and utilizing a more linear SOA epitaxial design. Hence, investigating the scalability and control together with improving the linearity of our filters is the focus of current research.

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Authors' biographies not included at authors request due to space constraints.

An InGaAsP/InP Integration Platform with Low Loss Deeply Etched Waveguides and Record SOA RF-linearity

Erik J. Norberg, Robert S. Guzzon, John S. Parker, Steven P. DenBaars, Larry A. Coldren

Department of Electrical and Computer Engineering and Department of Materials, University of California Santa Barbara, Santa Barbara, CA 93106
norberg@ece.ucsb.edu

Abstract: We present a novel InGaAsP/InP integration platform that simultaneously achieves high saturation power and low deeply etched waveguide loss, while requiring only a single blanket regrowth. RF-linearity of SOAs was characterized with record performance.

OCIS codes: (250.5300) Photonic integrated circuits; (250.4480) Optical amplifier; (130.3130) Integrated optics materials.

1. Introduction and Background

High saturation power (P_s) optical amplifiers find wide use in optical communication systems, mode-locked lasers and various RF-photonics applications [1-3]. For monolithic integration, low loss waveguides are advantageous in maintaining good signal integrity, and avoiding use of excess gain leading to worse overall noise figure and increased power consumption. In particular, integrated RF-photonics devices, demand both low passive loss and high P_s to achieve a high spur-free dynamic range (SFDR) [1,3].

For semiconductor optical amplifiers (SOAs), P_s is increased by reducing carrier lifetime, τ , or differential gain, a , or by reducing the photon density inside of the quantum wells. The former is reduced by operating the SOA at high current density, which is ultimately limited by device heating. The photon density can be decreased either by increasing the area of the active region (wd) or reducing Γ . Much has been reported on tapering the waveguide width to increase P_s . However, this typically only finds use as in laser amplifiers since integration with other components is difficult when using such wide waveguides. Also, using slab-coupled waveguides and also very large optical mode profiles, watt-class amplifiers have been successfully demonstrated [4]. However, neither the widely tapered waveguides nor the slab-coupled waveguides can be easily integrated with other functional chip components such as modulators, waveguide bends, lateral couplers or lasers. By reducing Γ , Raring *et al.* was able to integrate many functions on chip while achieving P_s in the 20 dBm range, by using a separate re-growth of low confinement quantum wells with a quantum well intermixing (QWI) integration platform [5].

For active InGaAsP/InP integration, free-carrier absorption (FCA) is typically the dominating contribution to propagation loss in passive sections. This can be eliminated by using additional butt-joint or complicated selective area re-growth schemes; however, either option significantly complicates the fabrication process.

In this work we have developed a modified single blanket re-growth offset quantum well (OQW) integration platform, which simultaneously achieves high P_s active regions and low-loss passive sections. Furthermore, by utilizing high confinement deeply etched waveguides, very compact integration and wide a variety of photonic integrated circuits (PICs) such as resonator structures are supported. We demonstrate excellent DC performance (G_o , P_s and passive loss) that matches well to theoretical simulations, and the SOAs are also characterized in terms of RF-linearity with state of the art results.

2. Epitaxial Design and Simulations

In order to increase P_s , we follow the general approach of Raring *et al.* [5], to reduce Γ by placing the quantum wells further out in the tail of the optical mode, increasing saturation power while decreasing the modal gain. Fig.1(a) illustrates our integration platform with a confinement tuning (CT)-layer inserted between the transverse waveguide and the active region. The waveguide consist of a 1.36Q:Si or 1.3Q:Si layer, and the active regions consists of five 65 Å thick 1.65Q material at 0.9% compressive strain surrounded by six 80 Å thick 1.22Q barriers at -0.2% tensile strain. A 170 Å 1.22Q -0.2% separate confinement heterostructure (SCH) layer is used on the p-side. We have investigated different thicknesses of the CT-layer to tune the Γ and achieve different levels of loss reduction.

P_s and the unsaturated gain, $G_o = e^{\Gamma g_o - \langle a_i \rangle}$ (g_o is unsaturated material gain and $\langle a_i \rangle$ is active loss), have been simulated in Fig.1(b), as a function of confinement factor and various numbers of quantum wells. The simulation uses the well-known equation for P_s , see e.g. [5], together with material parameters found from broad area laser measurements. It is clear that more quantum wells give a higher P_s for a constant confinement factor. This is of course due to the increased active region area (d). However, when lowering Γ (increasing CT-layer thickness), the first order transverse mode will eventually start guiding, a situation which cannot be tolerated. Thus, the P_s curves in

Fig. 1(b) are discontinuities where the design is no longer single mode, the point at which this occurs was separately established by calculating the optical mode spectrum for each design, using the finite-difference method (FDM).

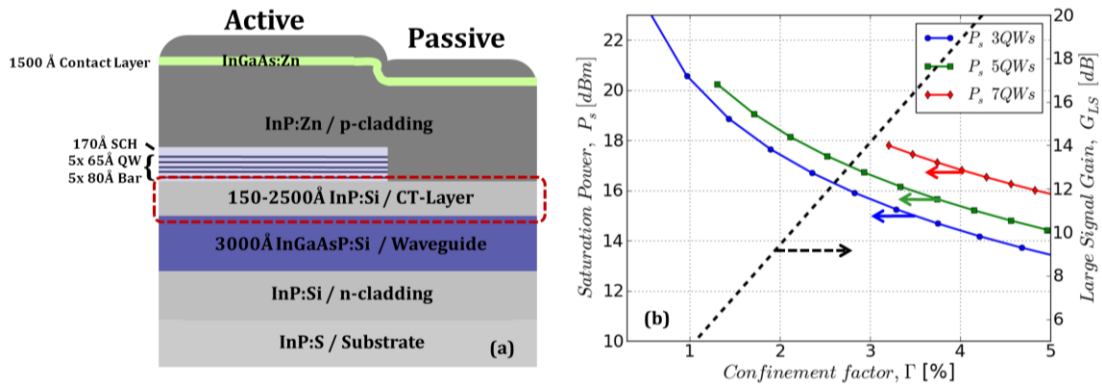


Fig. 1. (a) Schematic drawing of the integration platform, with the CT-layer highlighted. (b) P_s (solid lines) and G_{LS} (dashed line) simulated as a function of Γ and various numbers of quantum wells.

Passive waveguide sections are produced by patterning and selectively etching away the quantum wells in active regions, and a single blanket re-growth of InP:Zn p-cladding and InGaAs:Zn contact layer is then applied. The CT-layer of InP:Si is left in passive regions, in favor of the lower FCA of Si-doping compared with Zn-doping. We have simulated the reduction in passive loss using the CT-layer in Fig. 2(c). This was done by calculating the various modal overlaps with regions of different doping (again by solving the mode with FDM), and using absorption coefficients for Si- and Zn-doping of $9 \cdot (n/1e17) \text{ [cm}^{-1}\text{]}$ and $20 \cdot (p/1e18) \text{ [cm}^{-1}\text{]}$ [6], where n and p are the doping concentration in $\text{[cm}^{-3}\text{]}$.

3. Fabrication and Characterization of Deeply Etched Waveguides

The InGaAsP/InP epitaxial base structure as well as the p-cladding blanket regrowth was grown with metal organic chemical vapor deposition (MOCVD). Deeply etched waveguides were defined using standard i-line stepper lithography and a bi-layer $\text{SiO}_2\text{:Cr}$ hard mask, followed by an $\text{H}_2\text{:Cl}_2\text{:Ar}$ based inductively coupled plasma (ICP) etch [Parker]. Fig. 2(a) and (b) show a cross section of an active and passive deeply etched waveguide section, from the 250 nm CT-layer design; very anisotropic and fairly smooth sidewalls are evident. All the waveguides are kept $3.0 \mu\text{m}$ wide, and as we have previously shown when integrated with multi-mode interference (MMI) couplers single mode operation is still achieved [3].

The passive waveguide loss was found by fiber coupling amplified spontaneous emission (ASE) into 3 mm long waveguide cavities with cleaved mirror facets, then measuring the throughput extinction ratio with an optical spectrum analyzer (OSA), and using the standard Fabry-Pérot method with facet power reflection of 0.32 assumed. Deeply etched passive waveguides for three different CT-layer designs is compared in Fig 2(c). The loss is reduced by about a factor of two going from a standard OQW (15 nm CT-layer) to the 250 nm CT-layer design. The loss of the latter design is $\sim 3.5 \text{ dB/cm}$, which is low loss for deeply etched waveguides. The total simulated loss was fitted to measurement by adding a constant scattering (and/or interband absorption) loss contribution, we see a good fit for 0.25 cm^{-1} , thus the scattering loss is found to be 1.1 dB/cm .

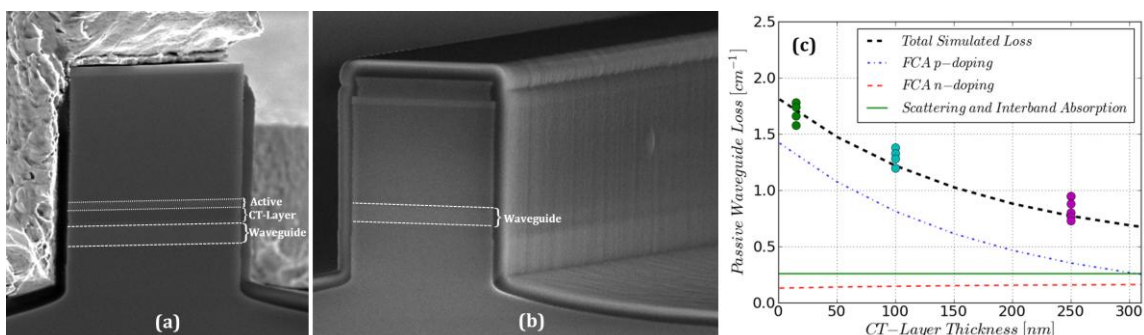


Fig. 2. Scanning electron microscopy (SEM) cross sectional image of (a) active and (b) passive waveguide sections of the 250 nm CT-layer design. (c) Passive waveguide loss simulated (lines) and measured (dots) for three different CT-layer thicknesses.

4. Characterization of Saturation Power and RF-linearity

The large signal gain, G_{LS} , and output saturation power, P_{so} , was determined by using two SOAs on the same waveguide. A continuous wave (CW) tunable laser at 1550 nm in-line with an EDFA and a variable attenuator was TE polarized and fiber coupled into the chip. First, the photocurrent in the front SOA is measured. Next, the front SOA is forward biased and the photocurrent in the back SOA is measured. Comparing the two photocurrents gives G_{LS} , while P_{so} is found by sweeping the input power and finding the 3dB G_{LS} roll off. Fig. 3(a) shows the measured results from a 1200 μm long SOA with $\Gamma=1.7\%$ (5 QWs, 1.36Q waveguide with 200 nm CT-layer thickness) at a terminal current density of 10 kA/cm². $P_{so}=19.1$ dBm and $G_{LS}= 78$ dB/cm fits very well with the theoretical simulation in Fig. 1(b).

RF-photonics applications provided a large motivation for the high saturation and low loss integration platform developed in this work. Accordingly, the RF-linearity should also be characterized. The 3rd order non-linearity in SOAs is caused by four-wave mixing (FWM), with the most severe contribution from closely spaced tones (difference frequency, $w < \tau \sim 1\text{GHz}$) that mix through the carrier population oscillation (CPO) effect [2]. Fig.3(b) shows a schematic for the measurement setup used to measure the optical 3rd order output intercept point (OIP3). Two stable DFB lasers centered at 1550.02nm and spaced by 300 MHz, are input into the device with equal powers. The output is heterodyned with a tunable laser acting as a local oscillator (LO) tunable laser placed at 1550.00 nm, and the spectrum is measured on an electrical spectrum analyzer. The tone powers are normalized to the output of the SOA. The OIP3 point is extrapolated from the measured output fundamental tone power and the 3rd order intermodulation distortion (IMD3) tone powers by fitting lines with slopes of 1 and 3 as theory predicts [2]. For the same SOA design as above ($\Gamma=1.7\%$), we measured $P_{OIP3}=17$ dBm (the photodiode linearity was measured to be >30 dBm, and so did not affect the measurement). Although the NF have yet to be measured experimentally, we theoretically predict a NF of about 4 dB on-chip (i.e. no fiber coupling loss including). Using this NF and calculating the SFDR in the limit of a strong LO ($P_{LO} \gg P_{signal}$) and assuming a shot-noise limited system, an SOA SFDR of 112.6 dB-Hz^{2/3} is calculated. This is to our knowledge the highest SOA SFDR reported to date and is promising for active integration of RF-photonics devices [1,3].

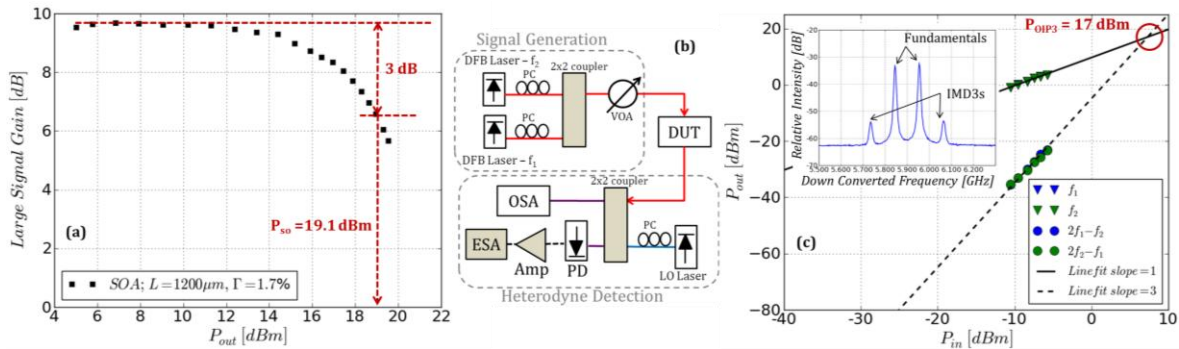


Fig.3. (a) Measurement of SOA DC characteristics, G_{LS} and P_{so} . (b) Schematic of measurement setup to characterize RF-linearity. (c) Optical fundamental and IMD3 tone powers extrapolated to find P_{OIP3} , inset show down-converted RF-spectrum.

5. Conclusion

We have presented an InGaAsP/InP integration platform capable of simultaneously achieving high P_s active regions and low loss passive regions. Using deeply etched waveguides, this platform is suitable for compact integration. We demonstrate deeply etched waveguides with passive loss as low as 3.5 dB/cm and P_s of 19.1 dBm while maintaining significant gain of 78 dB/cm. Finally we demonstrate state of the art RF-linearity results, with measured optical OIP3 power of 17 dBm suggesting SOA SFDR in the range of 112.6 dB-Hz^{2/3}.

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I. Photonic Integrated Circuits

*C. Coherent Receivers with Phase-locked
LOs*

A Widely-tunable Integrated Coherent Optical Receiver Using a Phase-Locked Loop

Mingzhi Lu¹, Ashish Bhardwaj¹, Abirami Sivananthan¹, Leif A. Johansson¹, *member*, IEEE, Hyunchul Park¹, Eli Bloch², Mark J. Rodwell¹, *Fellow*, IEEE, and Larry A. Coldren^{1,3}, *Fellow*, IEEE

¹Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA, 93106, USA.

²Technion university, Technion City, Haifa 32000, Israel.

³Department of Materials, University of California, Santa Barbara, CA, 93106, USA.

Email: mlu@ece.ucsb.edu

Abstract—A novel widely-tunable coherent receiver incorporating an optical phase-locked loop (OPLL) on two adjacent chips—a photonic IC and an electronic IC—is described. The design of both is novel, but the focus will be on the photonic IC in this paper. Results indicate a high degree of functionality.

Keywords—coherent; receiver; phase-locked loop

Digital coherent optical receivers have received a lot of interest lately because of their greater tolerance to noise, their compatibility with different modulation formats (such as multi-level phase shift keying), and their intrinsic ability to demultiplex wavelength-division multiplexed (WDM) channels without the use of optical filters.[1-3]

For the implementation of an optical coherent receiver, a free-running local oscillator (LO) is generally used. However, the high-speed digital signal processing is required to perform phase and frequency offset estimation and its correction. However, the high-speed digital signal processors used currently have high power consumption, latency, limited speed and cost considerations.

One solution to this problem is to implement an optical phase-lock loop (OPLL) [4,5], where a local oscillator tracks the frequency and phase of the transmitter laser. Although studies of optical phase-locked loops can be traced back almost fifty years, the OPLL has been proven hard to implement. The main difficulty is that it requires a short loop delay and generally narrow linewidth lasers. For example, to achieve a 1 GHz loop bandwidth, a loop delay less than 100 ps is normally required, which is not feasible using fiber pigtailed components. However, photonic integration can provide short loop delays and alleviate the linewidth issue to some extent.

In this work, we demonstrate a receiver that is realized using a highly integrated optical phase-locked loop that closely integrates a photonic integrated circuit (PIC) with an electronic integrated circuit (EIC) together with a loop filter, as illustrated in Fig.1. The PIC integrates a widely-tunable laser, a 90 degree hybrid and four waveguide detectors. The EIC includes limiting amplifiers, an XOR gate, and a single-sideband mixer. The phase error of the LO laser is detected and negatively fed back into the LO laser, which keeps both lasers phase-locked to

the incoming carrier. Since the two mixed signal have the same phase, no frequency or phase correction is needed.

The PIC uses a widely tunable sampled-grating distributed Bragg reflector (SG-DBR) laser [6] as the LO laser. Two variations 90 degree hybrid designs are realized. One uses four MMI multi-mode interference (MMI) couplers, and the other uses a star coupler.

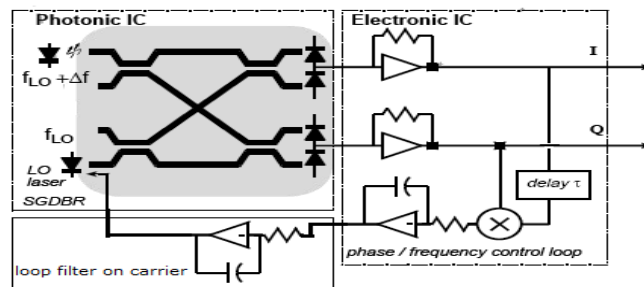


Fig. 1. The architecture of the coherent receiver showing three parts of this receiver: a photonic integrated circuit, an electrical integrated circuit and a loop filter.

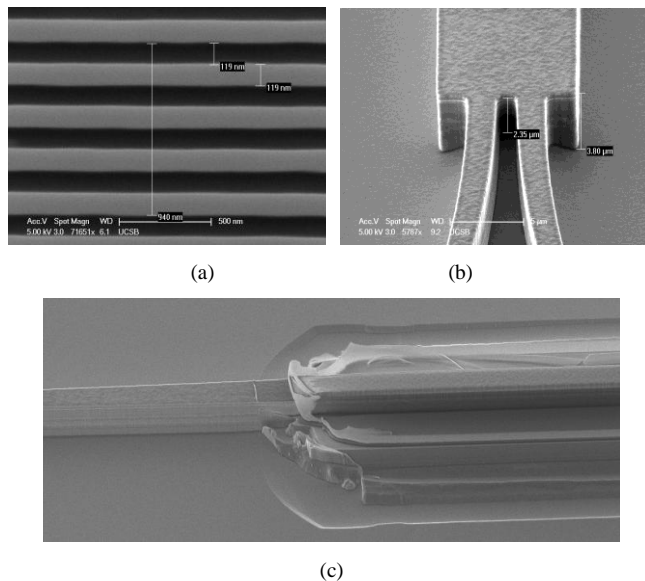


Fig. 2. SEM images of the fabricated PIC showing: (a) the gratings definition for SG-DBR lasers, (b) The vertical and smooth waveguide etch, (c) the waveguide transition from surface ridge to deeply etched waveguide.

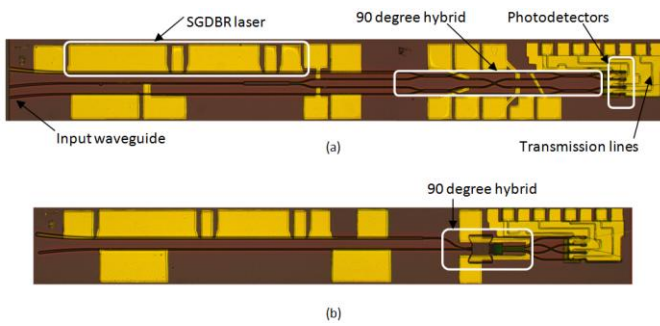


Fig. 3. Microscope images of the PIC showing (a) the PIC using MMI couplers as a 90 degree hybrid, (b) the PIC using star coupler as a 90 degree hybrid.

To monolithically integrate these optical components, we have chosen an InP/InGaAsP centered quantum well (CQW) platform. Quantum well intermixing (QWI) technology was used to define active and passive areas[7]. Sampled gratings, as shown in Fig. 2(a), are defined using electron beam lithography. This is followed by a p-cladding over-growth and waveguide definition using a $Cl_2/H_2/Ar$ based ICP-RIE etch. The results of the etching are shown in Fig. 2(b). Since both the surface ridge waveguide and deeply-etched waveguide are integrated on one PIC, a low loss transition is needed, as shown in Fig. 2(c). To achieve high-frequency on-chip photodetectors, microstrip transmission lines are fabricated on the PIC using bisbenzocyclobutene (BCB) as a dielectric layer. After the BCB definition step, the waveguide tops are opened for p-metal contacts using a ‘semi-self aligned’ process followed by the opening of direct vias for detectors. After deposition of P-metal, the wafer is thinned down, and back-side metallization is applied. Fig. 3 shows the microscope images of the final devices. Fig. 3(a) shows a PIC that is designed using MMI couplers as the 90 degree hybrid and Fig. 3(b) shows the PIC that is designed using a star coupler.

Fig. 4(a) shows the gain curve of a 200 μm long, 3 μm wide CQW SOA at 1550 nm. 68 mA (11.3 kA/cm²) of current gives a peak gain of 7dB (35 dB/mm). The performance of the SG-DBR laser is shown in Fig. 4(b). The SG-DBR laser is characterized using a 200 μm long SOA acting as a photodetector under reverse bias, assuming unity quantum efficiency. The threshold current is 40 mA with a differential efficiency of 0.37 W/A. The maximum output power is around 18mW.

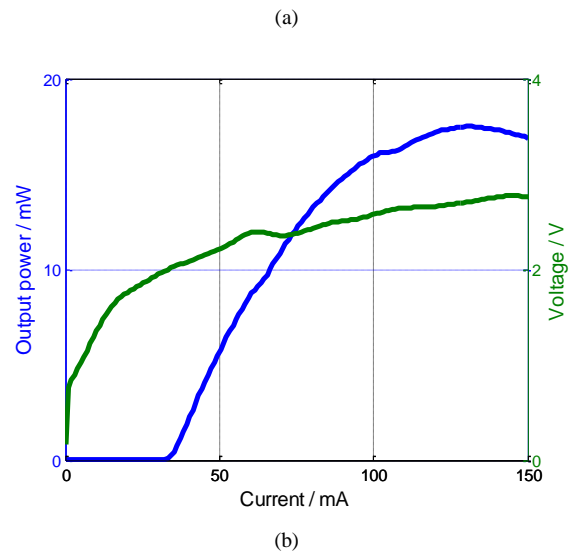
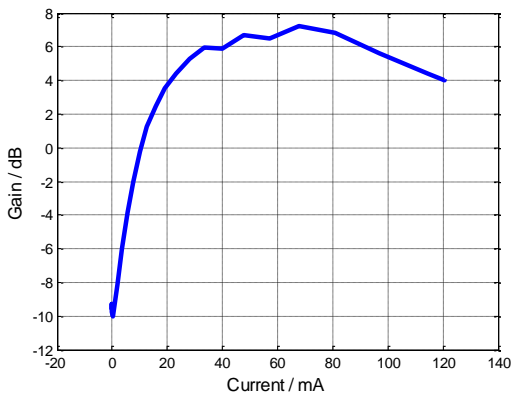


Fig. 4. Measurement result of the PIC. (a) The gain curve of the SOA at 1550nm. (b) The L-I-V curve of the SG-DBR laser

Data for the OPLL receiver will be presented at the meeting.

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I. Photonic Integrated Circuits

*D. Coherent RF Receivers using Tracking
Modulators*

ACP-OPLL Photonic Integrated Circuits for High Dynamic Range RF/Photonic links

^{a*}Yifei Li, ^bAshish Bhardwaj, ^bLarry Coldren, ^bJohn Bowers, and ^cPeter Herczfeld
^aECE Dept, UMass Dartmouth, 285 Old Westport RD, Dartmouth, MA, USA 02747;
^bECE Dept, The Univ. of California Santa Barbara, Santa Barbara, CA, USA 93106;
^cECE Dept, Drexel Univ, 3100 Market street, Philadelphia, PA USA 19104

ABSTRACT

Fiber-optic links are attractive for transmitting microwave/millimeter wave signals for applications such as radar, imaging and astronomy. However, current fiber-optic links that employ intensity modulation and direct detection suffer from limited spurious free dynamic range (SFDR). For solution, a new coherent fiber-optic link using linear phase modulation/demodulation has been proposed. The new link should be able to achieve an SFDR two orders of magnitude higher. The key for this link is an Optical Phase Locked Loop (OPLL) linear phase demodulator. In this paper we describe the design and preliminary measurements for the first generation ACP-OPLL photonic integrated circuits.

Keywords: optical phase locked loop, photonic integrated circuits, RF/Photonic link, and dynamic range

1. INTRODUCTION

Fiber-optic links are attractive for front-end applications due to their low loss, lightweight flexible cabling, immunity to electromagnetic interference, broad bandwidth, and low loss. Unlike conventional optical links for data communications, fiber-optic links in front-end applications require a large spurious free dynamic range (SFDR). Existing fiber-optic links employ intensity modulation and direct detection by a photodetector. Although simple, they have limited dynamic range due to the inherent nonlinearities in the optical intensity modulators. The state-of-the-art optical links manage to achieve an SFDR in the range of $115 \text{ dB}\cdot\text{Hz}^{2/3}$ through extensive linearization techniques [1]. However, many critical applications (such as channelized electronic warfare receivers) require an SFDR in excess of $140 \text{ dB}\cdot\text{Hz}^{2/3}$.

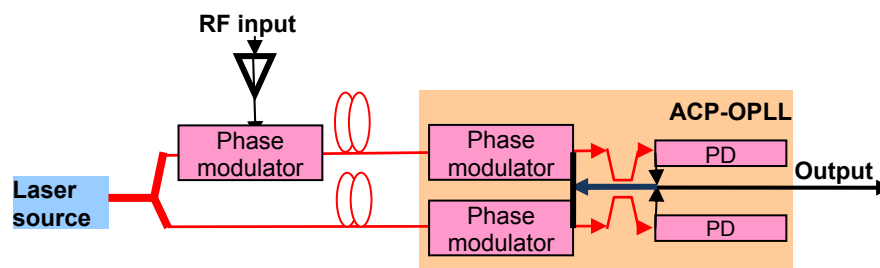


Fig. 1: RF/photonic link employing an ACP-OPLL phase demodulator

We have proposed a coherent, phase modulated RF/photonic link shown in Fig. 1 [2-3]. The most critical element in this approach is a linear optical phase locked loop (OPLL) linear phase demodulator. Through feedback, the OPLL forces the phase of a local phase modulator to mirror the phase of an incoming optical signal. Thus, the output from the photodetector is a scaled replica of the RF input. In order to tightly track the in-coming optical phase, the OPLL must have a high open loop gain ($\sim 20 \text{ dB}$) and a wide bandwidth ($> 0.5 \text{ GHz}$). Feedback stability requires that the OPLL has an extremely short feedback loop propagation delay ($< 8 \text{ ps}$). We have shown that an OPLL that is based on an attenuation counter-propagating (ACP) design [4] provides a lumped-element response to both the local optical phase modulators

and the photodetectors inside the OPLL. To further reduce the loop delay, the components of the ACP-OPLL should be integrated to form a photonic integrated circuit (PIC).

2. ACP-OPLL PIC DESIGN

A schematic view of an ACP-OPLL PIC is shown in Fig. 2. It contains a pair of balanced ACP local optical phase modulator, a pair of counter-propagating balanced photodetectors, a 3dB optical coupler and a feedback trace from the photodetector common electrode to the phase modulator common electrode. Through phase tracking the OPLL forces the optical phase of the local ACP phase modulator to mirror that of the incoming optical phase. Next, we discuss the design of the loop components that are used to fabricate an ACP-OPLL PIC.

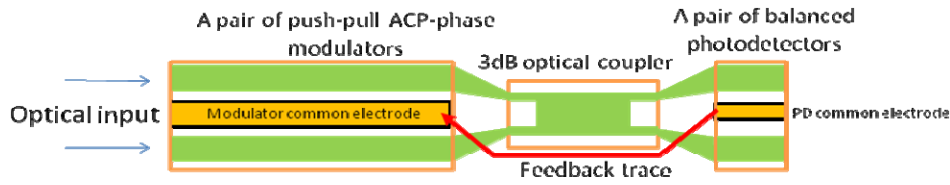


Fig. 2: Schematic of an ACP-OPLL PIC

2.1 MQW ACP optical phase modulator pair

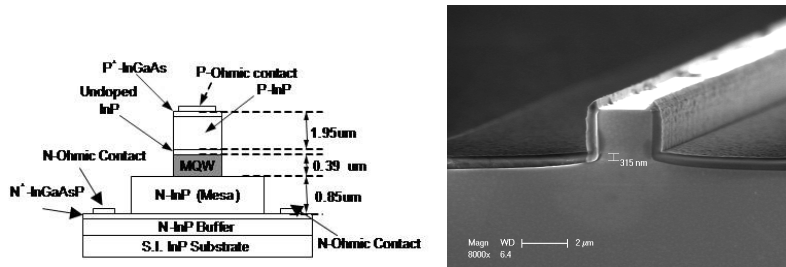


Fig. 3: Device structure for the InP MQW Phase modulator

The ACP-OPLL PIC employs InGaAsP-based multi-quantum wells (MQW) to realize optical phase modulators. However, in general the MQW phase modulators exhibit unwanted nonlinearities and electroabsorption, leading to high optical propagation losses. Both of these effects can limit the performance of the OPLL linear phase demodulator. To overcome this problem, we developed a detuned shallow quantum well optical phase modulator structure [5] (see Fig. 3). The quantum well region consists of lattice matched 9 nm thick $\text{In}_{0.65}\text{Ga}_{0.35}\text{As}_{0.76}\text{P}_{0.24}$ quantum wells and 6.5 nm thick $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}_{0.44}\text{P}_{0.56}$ barriers. To reduce the absorption in the quantum wells, the quantum well photoluminescence (PL) peak is designed to be ~ 170 nm away from the $1.55 \mu\text{m}$ operating wavelength. To reduce free carrier optical absorption, a low barrier height is used to help with sweeping out the photo-generated carriers. The low barrier height also reduces the quantum confinement at high reverse bias voltages. In general, the PM sensitivity of a quantum well phase modulator increases with the bias voltage. The reduction of the quantum confinement can diminish the PM sensitivity increase. Thus, near a certain reverse bias, this helps to create a plateau region where the PM sensitivity held constant against the bias voltage change. In this region, the phase modulator will behave more linear. The phase modulator device structure has a p-i-n diode configuration. To improve the lateral confinement, a deep ridge waveguide structure is used. The intrinsic region contains 25 periods of quantum wells, yielding a confinement factor of 0.63 when the quantum wells act as the guiding layer of the deep ridge waveguide structure. The width of the optical waveguide is $2 \mu\text{m}$. At a reverse bias of 6 V, a 1 mm long phase modulator device demonstrated:

- Large phase modulation linearity: $\phi_{IP3} \sim 4\pi$ @ 6 volt bias
- Low insertion loss: $\sim 0.9\text{dB}$ @ 6 volt bias
- V_{π} : $\sim 6\text{V}$ @ 6 volt bias

This quantum well design is used to implement the phase modulators in the ACP-OPLL PICs. To meet the SFDR goal of $140 \text{ dB}\cdot\text{Hz}^{2/3}$, the combined ϕ_{IP3} of the ACP phase modulator should be over 20π [x]. Therefore, 3 mm long phase modulator length were chosen. A pair of 3mm long phase modulators in a push-pull configuration should yields a combined ϕ_{IP3} of 24π .

The ACP configuration eliminates the phase delay from the phase modulators. The ACP phase modulators require that RF attenuation is applied to the modulator electrode. This is accomplished by employing high resistance electrodes ($\sim 150 \text{ ohm}$) to both the n and p contacts of the phase modulator pair. Fig. 3 shows the simulated response of the push-pull ACP-phase modulator pair. The simulated phase modulation sensitivity is $\sim 3.2 \text{ rad/volt}$, which corresponds to a V_{π} of $\sim 1 \text{ V}$. Its 3-dB bandwidth is $\sim 0.5 \text{ GHz}$. In addition, as shown in Fig. 4b, the phase response of the ACP phase modulator pair is bound between 0 and $\pi/2$. This suggests that a lumped element response that would result in the absence of phase delay in the feedback loop. The simulated ACP phase modulator load impedance is also shown in Fig. 5. To help increase the OPLL open loop gain, a high modulator load impedance is desired.

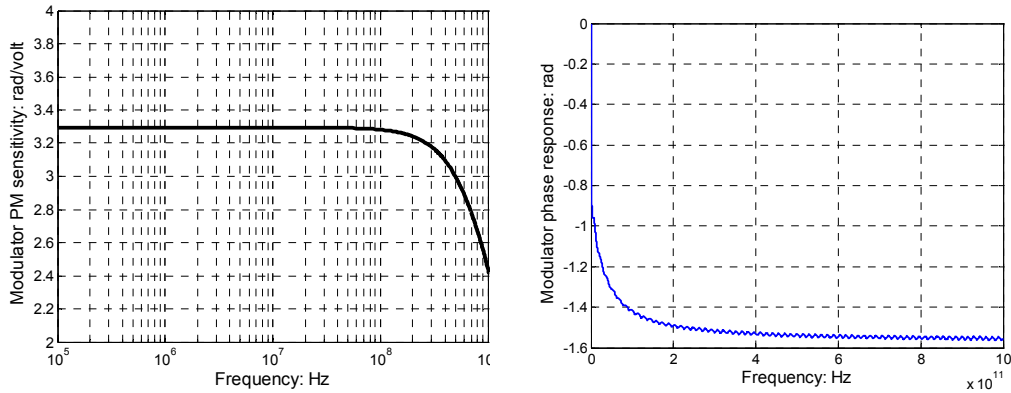


Fig. 4: Phase modulator frequency response.

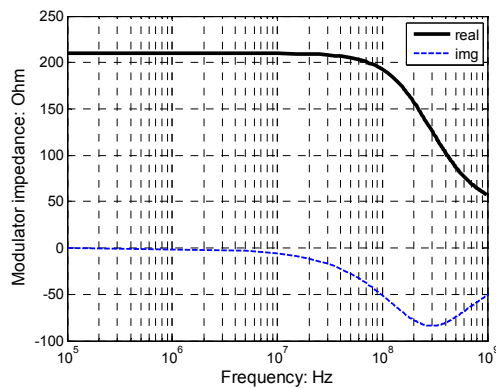


Fig. 5 Load impedance of the ACP-phase modulator pair

2.2 Balanced photodetector

We use the waveguide uni-traveling carrier waveguide photodiode (UTC) design developed by Klamkin et al [6] as the basis to implement the balanced photodetectors for the ACP-OPLL photonic integrated circuit. However, we employ a counter-propagating photodetection scheme to help mitigate the phase delay of the photodetectors[7]. In this configuration, the optical field counter-propagates with respect to the photo-generated feedback signal. The width and the total length of the photodetector waveguides are 10 microns and 200 microns, respectively. Fig. 5 shows the simulated response of the photodetector when the balanced photodetector is loaded by the ACP-phase modulator pair and an external load (50 ohm or 150 ohm). The frequency response is defined as the ratio between the photodetector output voltage and the optical input power. A lower load impedance will result in a larger photodetection bandwidth (~2GHz), whereas a higher impedance will result in a higher output voltage.

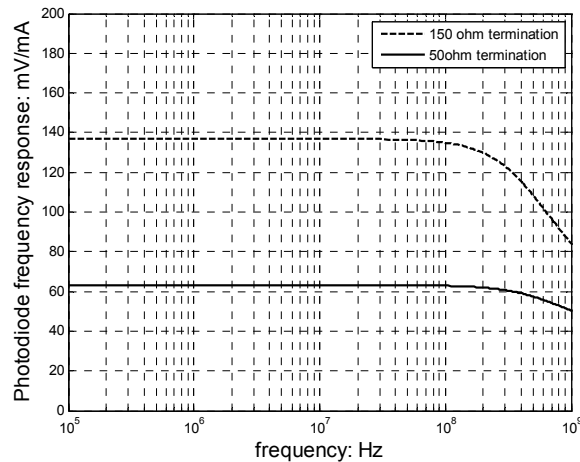


Fig. 6: Frequency response of counter propagating balanced UTC photodetector when loaded by a pair of 3mm long ACP local phase modulators in parallel with an external termination.

2.3 Optical 3dB coupler

In order to implement a compact 3-dB optical 2x2 coupler, a regular multi-mode interferometric (MMI) coupler is designed. The width of the MMI section is 7 microns and the length of the coupler is 219 microns.

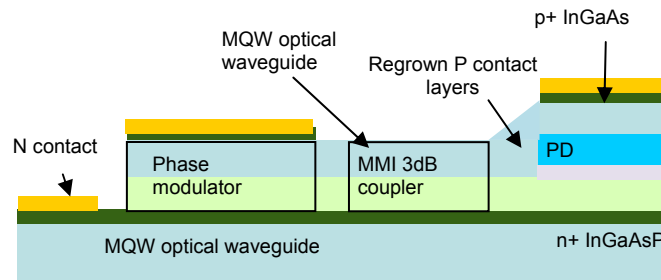


Fig. 7: Monolithic integration platform for the fabrication of the ACP-OPLL PIC

2.4 ACP-OPLL PIC designs

The monolithic integration platform used for the ACP local phase modulators, the UTC-photodetectors, and the 3-dB 2x2 coupler is shown in Fig. 7. The phase modulators and the photodetectors are connected by a regular multi-mode interferometric (MMI) 3dB optical coupler. The length of the MMI coupler and the electric feedback path results in the

total loop delay of the ACP-OPLL loop delay to be ~ 10 ps. The three variations of the ACP-OPLL PICs were designed and implemented (see Fig. 8). They are: the ACP-OPLL with 3 mm long modulators, the ACP-OPLL with 2.2 mm long modulators, and an optoelectronic ACP-OPLL. The optoelectronic ACP-OPLL, which also has 2.2 mm long ACP phase modulators, can be hybrid-integrated with an electronic amplifier circuit in order to increase the OPLL open loop gain.

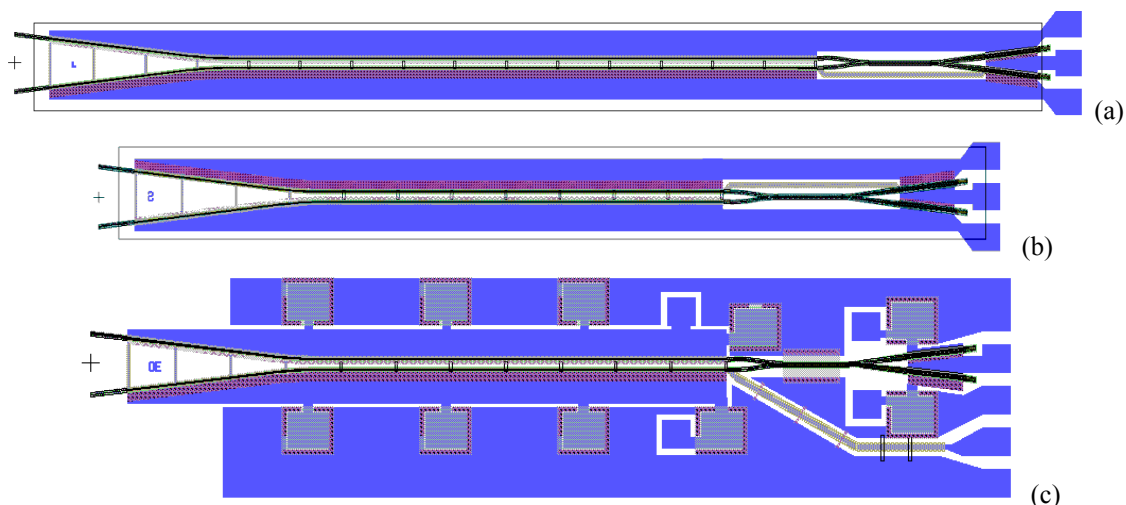


Fig. 8: Three designs of ACP-OPLL PICs. (a) ACP-OPLL with 3 mm phase modulator; (b) ACP-OPLL with 2.2 mm phase modulator; (c) optoelectronic ACP-OPLL with 2.5 mm long phase modulator

3. ACP-OPLL PIC CHARACTERIZATION- PRELIMINARY RESULTS

The ACP-OPLL PICs were fabricated using the nanofabrication facilities at UCSB. In this section, we present some preliminary experimental results from the ACP-OPLL PICs with the 3 mm long ACP-modulators. Fig. 9 shows a group of three ACP-OPLL PICs being probed. The experimental setup for characterizing the ACP-OPLL was depicted in Fig. 10.

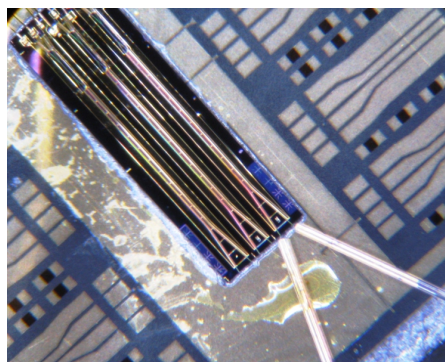


Fig. 9: ACP-OPLL PIC characterization

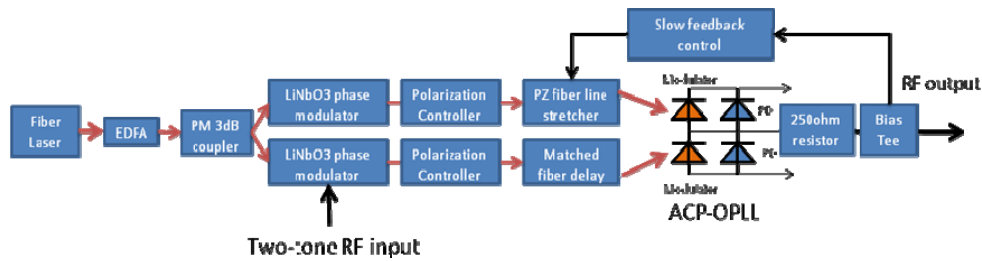


Fig. 10: PM link experimental setup

In this set of measurements, a 250ohm series resistor was placed between the ACP-OPLL output and the external 50 ohm load. This increases the ACP-OPLL open loop gain but it is at expense of the OPLL bandwidth, but ensures adequate voltage drop across the phase modulators. Phase tracking is clearly observed in the ACP-OPLL PIC. As shown in Fig. 11, with only 4mA photocurrent, we observed a **21dB** improvement in intermodulation distortion. Figure 12 shows the OPLL output and spurious distortion level when the RF input power is swept from 12 to 14dBm. The distortion level follows strictly 3:1 slope and the link input IP3 point is 39dBm.

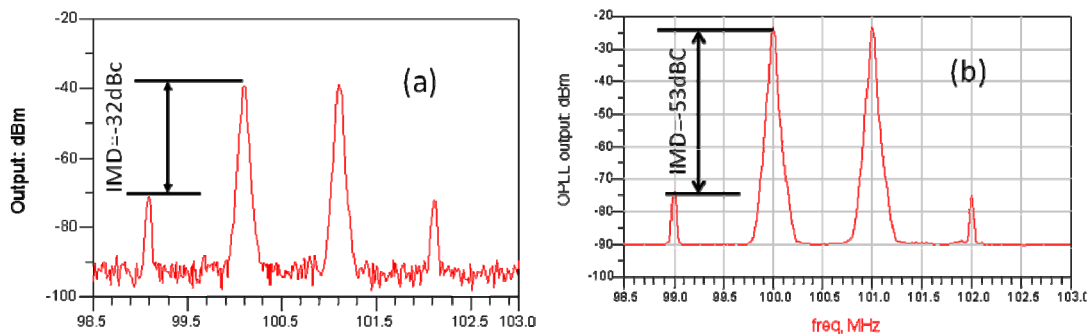


Fig. 11: Comparison of inter-modulation distortion levels between the ACP-OPLL (LW1) and an conventional homodyne phase detector. (a). Output spectrum of a conventional homodyne phase detector ; (b) Output spectrum of the ACP-OPLL. RF input is 14dBm/tone in both cases. The photocurrent of the ACP-OPLL is ~4mA and the bias is 6V.

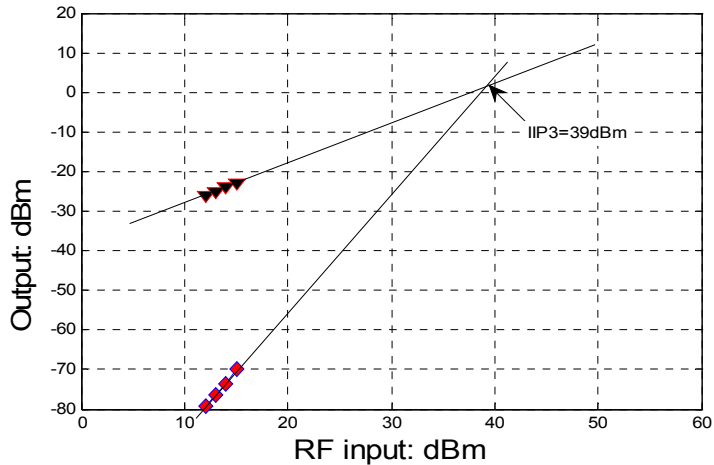


Fig. 12: Output vs RF input

4. CONCLUSION

In this paper we have described the design and preliminary experimental results for an ACP-OPLL photonic integrated circuit that can be used as a linear optical phase demodulator in high dynamic range RF/photonic links. Phase demodulation by phase tracking has been observed.

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All-Optical ACP-OPLL Photonic Integrated Circuit

Y. Li⁺, A. Bhardwaj[#], R. Wang⁺, S. Jin⁺, L. Coldren[#], J. Bowers[#], and P. Herczfeld^{*}

⁺University of Massachusetts at Dartmouth, MA 02747, USA

^{*}Drexel University, Philadelphia, PA 19104, USA

[#]The University of California, Santa Barbara, CA 93101, USA

Abstract — The optical-phase-locked-loop linear phase demodulator is the most critical component for a high dynamic range phase modulated RF/Photonic link. Due to the stringent loop latency requirement, the OPLL should be implemented as a photonic integrated circuit. In this paper we address the design and implementation of an all optical attenuation-counter-propagating (ACP) optical-phase-locked-loop photonic integrated circuit. The preliminary experimental results for this device are also presented.

Index Terms — Optical phase locked loop, photonic integrated circuits, dynamic range.

I. INTRODUCTION

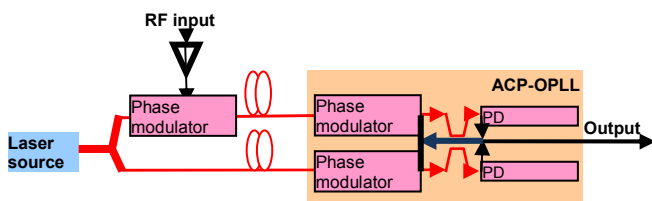


Fig. 1: Coherent RF/photonic link with OPLL phase demodulator

An RF/Photonic link for radar frontend applications requires a large Spurious-Free Dynamic Range (SFDR). However, conventional fiber-optic links that employ intensity modulation and direct detection (IM-DD) have limited SFDR due to the nonlinearities in the optical modulation process. As a solution, we have proposed a coherent phase modulated RF/photonic link shown in Fig. 1[1-2]. The most critical element in this link is an Optical Phase-Locked Loop (OPLL) linear phase demodulator. Through feedback, the OPLL forces the output phase of a local optical phase modulator to mirror the phase of an incoming optical signal. Thus, the output from the photodetectors of the OPLL is a scaled replica of the RF input at the link transmitter. In order to tightly track the phase optical carrier, the OPLL must have a high open loop gain (~ 20 dB) and a wide bandwidth (>0.5 GHz). Thus, feedback stability requires that the OPLL has an extremely short loop propagation delay (<10 ps). To realize the delay requirement, the attenuation counter-propagating (ACP) device design was proposed [3], which renders a lumped-element low-pass response to both the optical phase modulators and the photodetectors inside the OPLL. However, to further reduce the loop delay, the OPLL should also be integrated on a chip in order to minimize the propagation delays arising from signal routing and feedback. In this paper, we describe the

design and implementation of an ACP-OPLL Photonic Integrated Circuit (PIC) on an Indium Phosphide (InP)-based material platform, and present some preliminary experimental results.

II. ACP-OPLL PIC DESIGN

The first major problem facing the design of the ACP-OPLL PIC is the nonlinearity of the quantum well optical phase modulators. We have developed and experimentally verified a detuned shallow MQW phase modulator with record linearity and low optical propagation loss [4]. The quantum well design consists of lattice matched 9 nm thick $\text{In}_{0.65}\text{Ga}_{0.35}\text{As}_{0.76}\text{P}_{0.24}$ quantum wells and 6.5 nm thick $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}_{0.44}\text{P}_{0.56}$ barriers. We use this quantum well design to implement the ACP phase modulators inside the OPLL photonic integrated circuit.

As shown in Fig. 2, our ACP-OPLL photonic integrated circuit contains:

- 3 mm long push-pull balanced ACP-phase modulators
- 200 microns long balanced counter-propagating photodetectors
- A 217 microns long regular interference MMI coupler

Table 1 summarized the design of the ACP-OPLL PIC.

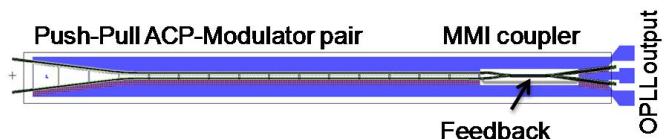


Fig. 2: ACP-OPLL Mask layout

Table 1 ACP-OPLL PIC design parameters

| | |
|-------------------------|-------------------|
| ACP modulator length | 3 mm |
| ACP modulator V_{π} | ~ 2 volt |
| ACP modulator loss | <3 dB |
| MMI coupler Length | 217 μm |
| Photodetector length | 200 μm |
| PD 95%absorption length | 168 μm |
| Loop delay | ~ 10 ps |

A. Push-pull ACP phase modulator

The key idea of the ACP phase modulator is to use the RF attenuation to synthesize a lumped element low-pass response [3]. We use a high resistance thin film electrode to introduce the desired RF attenuation to the phase modulator electrode.

However, this can create non-uniform bias voltage along the quantum well phase modulators. When under optical input, a substantial photocurrent ($>1\text{mA}$) is generated [4]. When this photocurrent flows through the lossy electrode, it can cause an unwanted bias voltage variation along the length of the electrode. A constant bias voltage is critical for the phase modulator's linearity. To mitigate this effect, we have developed a push-pull ACP phase modulator pair as illustrated in Fig. 3.

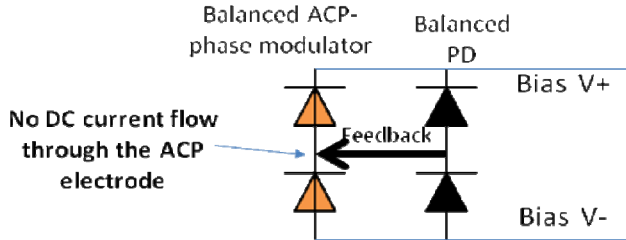


Fig. 3: Push-pull balanced ACP phase modulator and balanced PD

In this design the photocurrents generated in each ACP-phase modulator complement each other. Thereby, there is no net DC photocurrent flowing through the high resistance ACP thin film electrode. The optimum bias voltage is maintained throughout the ACP electrode. This push-pull modulator design also doubles the open-loop gain, which is very beneficial when the optical power that couples into the photodetector is low.

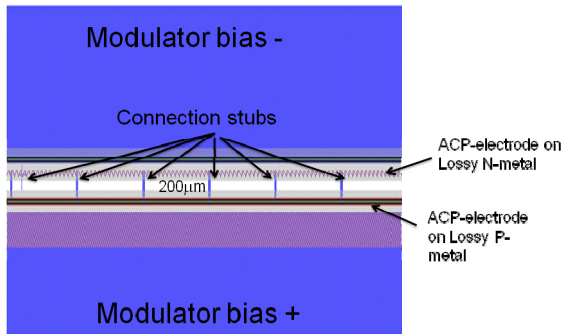


Fig. 4 A section of push-pull ACP phase modulator

A section of the photomask layout of the push-pull ACP phase modulator is shown in Fig. 4. The lossy electrodes of the upper and the lower ACP-modulators are implemented on modulator lossy-n-metal and lossy-p-metal layers, respectively. Both electrodes have a resistance of approximately 150ohm.

The lossy metal recipe tailors the RF loss to be small within the OPLL bandwidth and large beyond this bandwidth. This eliminates the modulator's propagation delay without sacrificing too much the modulation sensitivity and linearity within the OPLL bandwidth. The simulated effective V_{π} of the push-pull ACP phase modulator pair is ~ 1 volt. Also shown in Fig. 9, the two lossy electrodes are electrically connected by

an array of 3 micron wide metal stubs. The distance between the adjacent stubs is 200 microns. The unwanted RF reflection due to these stubs was carefully simulated using Ansoft HFSS. It was found to be small and does not reduce the OPLL phase margin.

B. Balanced counter propagating balanced UTC PD

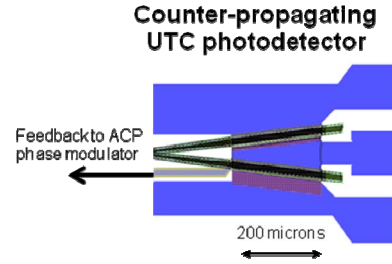


Fig. 5: Counter propagating balanced UTC photodetector

The photodetector (Fig 5) is based on a waveguide Uni-travelling Carrier Photodiode (UTC-photodetector) design [5]. In order to minimize the delay, we introduce a counter-propagating photodetector configuration. The detector width and length are 10 microns and 200 microns, respectively. The photodetector's absorption length is 168 microns. Each photodetector is capable of achieving a saturation photocurrent $>50\text{mA}$.

C. 3dB optical coupler

To mitigate risks, a regular multi-mode interferometric (MMI) coupler was used to implement the 3dB coupler (Fig. 6). The length of the coupler is 217 microns. Its loss was simulated to be less than 0.3dB. The MMI coupler sets the total OPLL loop delay to be $\sim 10\text{ps}$, which includes delays of the MMI coupler, waveguide bends, tapers and feedback electrode. By employing more compact couplers, much shorter delay can be achieved.



Fig. 6. Regular MMI 3dB coupler (217 micron long and 7 micron wide)

Table 2 Simulated ACP-OPLL performance

| | |
|--------------------------|---|
| Photocurrent | $\sim 45 \text{ mA/PD}$ |
| Load impedance | 50 ohm |
| SFDR in shot noise limit | $\sim 140 \text{ dB} \cdot \text{Hz}^{2/3}$ |
| Open loop gain | $\sim 22 \text{ dB}$ |
| Bandwidth | $\sim 0.7 \text{ GHz}$ |
| Phase Margin | 60 degrees |

D. ACP-OPLL PIC performance projection

The ACP-OPLL PIC design was simulated and its performance with 45 mA photocurrent is summarized in Table 3. In the calculation, we assume the shot-noise limit.

III. EXPERIMENTAL RESULTS

The ACP-OPLL PIC was fabricated using UCSB's nanofabrication facilities. The base epitaxially grown wafer for the fabrication of the ACP-OPLL PIC was provided by Landmark Inc. It contains the MQW layers for the phase modulators as well as the layers for the UTC-photodetector on a semi-insulating InP substrate. The layers that define the UTC photodetector were first removed selectively for the regions where the detector is not present. Then the p-contact layers were regrown. Deep ridge optical waveguides were defined, followed by n-metal deposition. Helium implantation and proton implantation were performed to introduce electric isolation between the loop components. Finally, the p-metal deposition was performed. The details on the fabrication steps will be addressed in a separate paper. Fig. 7 shows a group of three ACP-OPLL PICs mounted on a carrier chip.

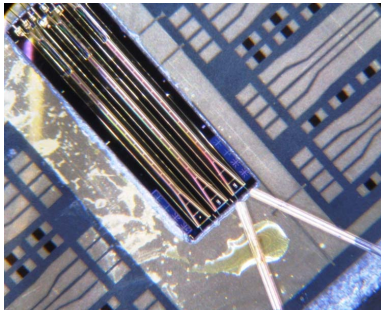


Fig. 7 Fabricated ACP-OPLL PICs

A. Phase modulator optical loss

To realize the full dynamic range potential of the ACP-OPLL PIC, it is critical to generate large photocurrents from the balanced photodetectors of the ACP-OPLL. This requires that the ACP phase modulators have low optical loss. A dual drive modulator test structure device (as shown Fig. 8) was co-fabricated with the ACP-OPLLs. It was used to determine the optical loss of the ACP phase modulators.

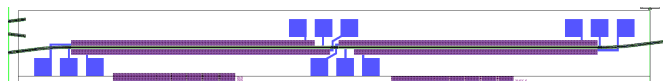


Fig. 8. Dual drive phase modulator test structure

The dual drive modulator contains two identical 1.5 mm long modulator sections, which are reverse biased and used as a photodetector instead. The modulator optical loss is determined by comparing the ratio between the photocurrents of the two modulator sections when illuminated by a small optical input. The measured optical loss (Fig. 9) for a 1.5 mm long modulator section is ~ 3 dB, suggesting an optical absorption of ~ 2 dB/mm. It does not show strong dependence on the modulator bias and optical input power.

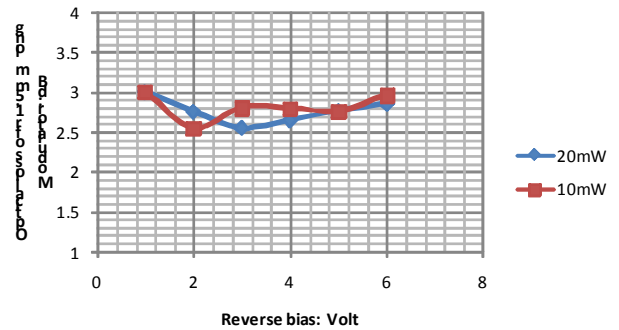


Fig. 9 Phase modulator optical loss measurement results

B. Preliminary ACP-OPLL PIC characterization

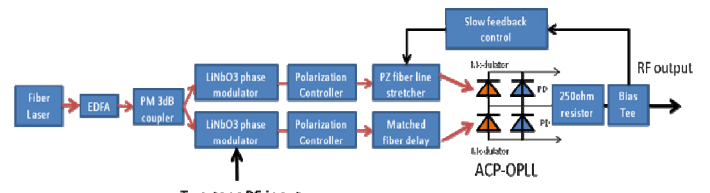


Fig. 10. PM link experimental setup

The ACP-OPLL PIC is characterized using the setup shown in Fig. 10. It is a phase modulated optical link. A 1.55micron CW low phase-noise fiber laser provides the optical carrier. The output of the fiber laser is amplified using a high power erbium doped fiber amplifier, and then split into two paths using a polarization maintaining 3 dB optical coupler. Each path contains a LiNbO₃ linear phase modulator ($V_{\pi} \sim 7$ volt), which is used as the link transmitter. After some fiber delay, the two paths are recombined at the ACP-OPLL PIC, in order to perform linear phase demodulation. In addition, to overcome the slow environmental fluctuations of the relative optical phase between the two optical paths, the low frequency portion (< 100 kHz) of the ACP-OPLL output is extracted via a microwave bias-Tee and is fed back to a Piezo-electric fiber line stretcher. This slow feedback allows long-term stable phase locking.

In this preliminary experiment we generate ~ 4 mA photocurrent in each photodetector of the ACP-OPLL PIC. To increase the ACP-OPLL open loop gain in presence of the low photocurrent, a 250 ohm series resistor was placed between the ACP-OPLL output and the external 50 ohm load. This elevates the load impedance of the ACP-OPLL output to 300 ohm.

To establish the baseline for comparison, we first "turn off" the optical feedback by intentionally reducing the photocurrent to a negligible level so that the OPLL open loop gain is close to zero. Thereby, the ACP-OPLL is reduced to a conventional homodyne phase detector. Fig. 11 shows the output captured by a microwave spectrum analyzer when the two-tone RF input is at 100 MHz and 12 dBm per tone. The measured inter-modulation distortion is ~ 29 dBc.

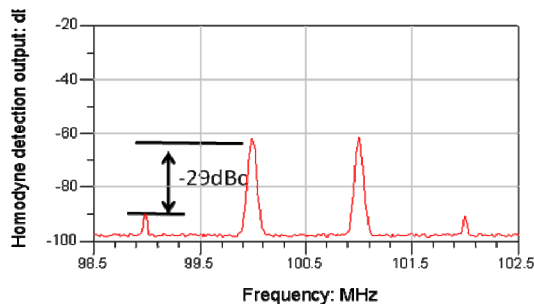


Fig. 11 Distortion level of homodyne phase detector without feedback

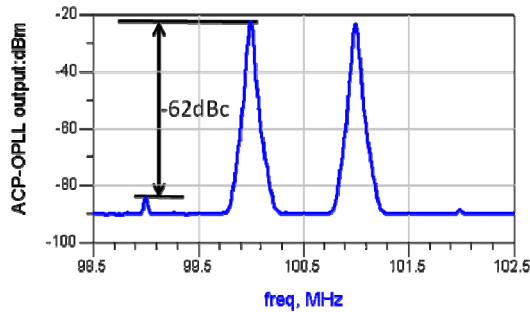


Fig. 12 Distortion of ACP-OPLL. 33dB improved in distortion level is observed. The photocurrent is 4mA and the rest input condition is similar to that of Fig.11.

Under the same RF input condition, we increased the optical input power to obtain ~ 4 mA photocurrent from each photodetector. With the OPLL feedback enabled, we observed a 33 dB reduction in the intermodulation distortion (IMD) levels as shown in Fig. 12. The distortion level in this measurement is very close to the spectrum analyzer's noise floor and the 12 dBm/tone RF input power is the power limit of the RF signal sources. Thus, we are unable to determine the distortion level as a function of the RF input power under these conditions.

IV. CONCLUSIONS

We have described the design, implementation of the ACP-OPLL PICs and have presented results from preliminary measurements. With only 4 mA photocurrent, we obtained 33 dB improvement in spurious distortion levels.

ACKNOWLEDGEMENT

The authors wish to acknowledge Dr. Leif Johansson, Dr. Arye Rosen, and Dr. Jonathan Klamkin for valuable suggestions.

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Optical PLLs can improve the dynamic range of coherent receivers

non-spurious reception*

Researchers in the US have demonstrated a monolithically integrated attenuated counter-propagating optical phase-locked loop photonic integrated circuit (ACP-OPLL PIC) as a highly linear coherent receiver. Their results show that such devices can realise a high dynamic range in future phase-modulated RF/photonic links.

Head narrow and noisy

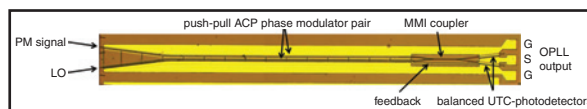
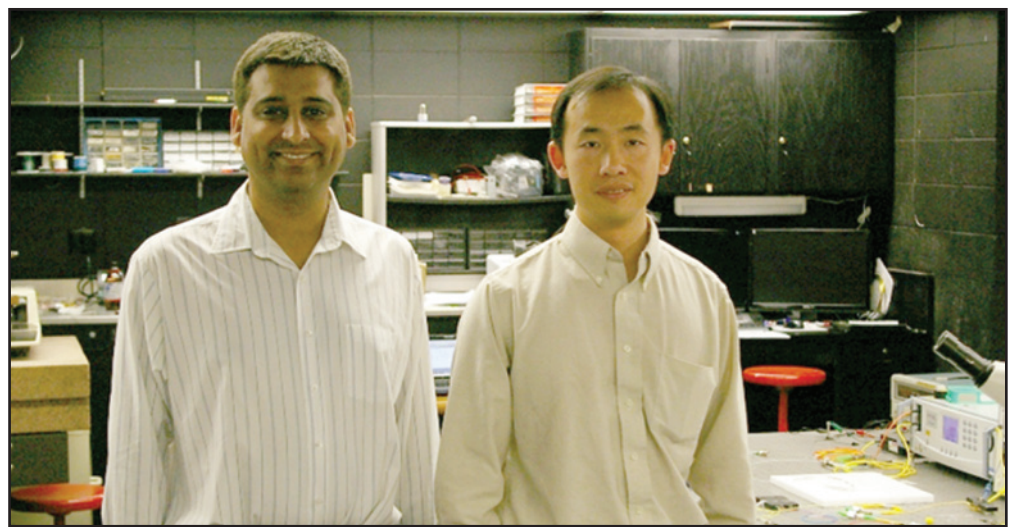
OPLLs are similar to conventional PLLs – familiar in electronics – but instead use optical phase modulators (or tuneable lasers) as local oscillators, with optical couplers and balanced photodetectors for phase detection. Using negative feedback, the OPLL forces the phase of the local optical phase modulator to track the phase of an incoming optical signal. Thus, the OPLL performs linear optical phase demodulation and can be used as a coherent receiver.

Although an OPLL-based coherent receiver can considerably increase the dynamic range of a phase-modulated RF/photonic link, current state-of-the-art coherent receivers using OPLLs require significant improvements – in particular, their frequency bandwidth and noise properties – before their widespread use becomes a reality.

Photonic complexity

One measure of the quality of these receivers is their spurious-free dynamic range (SFDR). This is defined as the ratio of the strength of the fundamental signal to the strongest spurious signal in the output. To increase this quantity, the team have developed a high-linearity optical phase modulator on an InP material platform using a detuned shallow multi-quantum well structure. These modulators were realised using a newly developed waveguide fabrication process allowing for very long deep ridge modulators with low optical propagation losses. "These low-loss high-linearity ACP-modulators were critical in achieving the record SFDR values reported in our Letter", said Dr Ashish Bhardwaj.

The team's main problems in developing their single-chip receivers was the sheer number of processes involved in making



them, as Bhardwaj explained: "The biggest challenge in realising the ACP-OPLL PIC was the development of a processing methodology that comprised a set of very complex fabrication steps to enable monolithic integration of the deep ridge modulators with other components of the OPLL." In fact, the fabrication required "over sixteen photolithography steps along with multiple dielectric material depositions, several different types of etching steps, one regrowth step, two ion implantation steps and seven separate metal depositions."

As well as increasing the SFDR, the team's techniques allow different active components such as tuneable lasers, optical amplifiers, high-speed modulators and photodetectors to be monolithically integrated with passive waveguides on a single InP chip. Compact multimode interference (MMI) couplers as well as signal routing with a tight bend radius were also realised using the deep ridge waveguides. As a result, they were able to realise a loop propagation delay of approximately 10 picoseconds.

ABOVE: Dr. Ashish Bhardwaj (left) from the University of California Santa Barbara and Dr. Yifei Li (right) from the University of Massachusetts Dartmouth have collaborated to develop a high-linearity single-chip coherent receiver.

RIGHT: Photograph of a fully fabricated high-linearity ACP-OPLL PIC coherent receiver.

A front-end future

While the team have reported a record SFDR, they feel that the technology can be improved. By further optimisation of component design and the fabrication process, Bhardwaj believes it should be possible to improve the bandwidth and dynamic range of such OPLL-based coherent receivers compared to those observed in current devices. This would include improvements in the design of the UTC photodetectors, further reduction in the optical propagation loss of the deep ridge waveguides, and improvement in the coupling efficiency between the input optical fibre and the deep ridge waveguides by using integrated spot-size converters.

Bhardwaj also explained that the possibilities of photonic integration go beyond the current industrial concerns of cost saving, reduced complexity and footprints. "There is a substantial interest in using photonic integration to realise optical functionality that is impossible using discrete optical components," said Bhardwaj. Furthermore, looking into the future, he says that "we envision PICs that perform complex optical signal processing, where more of the front-end processing is moved into the optical domain at high data rates, especially as equivalent electronic solutions become cumbersome or simply impractical."

Monolithic integration of high linearity attenuated counter-propagating optical phase-locked loop coherent receiver

A. Bhardwaj, Y. Li, R. Wang, S. Jin, P. Herczfeld, J.E. Bowers and L.A. Coldren

The first monolithically integrated attenuated counter-propagating optical phase-locked loop based coherent receiver is presented. A spurious-free dynamic range of $131.3 \text{ dB Hz}^{2/3}$ is measured in the detector shot-noise limit at 100 MHz, which is the highest reported for a single-chip device.

Introduction: Coherent phase modulated RF/photonic links have been proposed [1, 2] to realise high dynamic range analogue optical links, which require the use of an optical phase-locked loop (OPLL) as a linear phase demodulator. Through feedback, the OPLL forces the output phase response of a local optical phase modulator to mirror the phase of an incoming optical signal. Since high loop gain and wide bandwidth are required for efficient phase tracking, the OPLL must have an extremely short loop delay to ensure feedback stability. This can be realised using an attenuated counter-propagating (ACP) configuration [2], which eliminates the phase delays from the optical phase modulators and photodetectors in the OPLL. Integration of the ACP-OPLL on a single chip is necessary so that the propagation delays arising from optical signal routing and the electrical feedback are minimised.

In this Letter, we describe the first monolithically integrated ACP-OPLL PIC on an indium phosphide (InP) material platform. We present preliminary results that demonstrate the highest spurious-free dynamic range (SFDR) reported for a single-chip OPLL coherent receiver.

ACP-OPLL PIC fabrication: The ACP-OPLL PIC uses shallow multi-quantum wells (MQWs) as highly linear phase modulators with low optical propagation loss. The MQW structure consists of 25 lattice-matched 9 nm-thick $\text{In}_{0.65}\text{Ga}_{0.35}\text{As}_{0.76}\text{P}_{0.24}$ wells and 6.5 nm-thick $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}_{0.44}\text{P}_{0.56}$ barriers [3]. A 2.5 μm -wide deep ridge waveguide is used, where the MQW layers provide waveguiding of the optical mode. High-resistance electrodes ($\sim 150 \Omega$) provide RF attenuation in the 3 mm-long ACP phase modulators that operate in a push-pull configuration. The balanced photodetector pair uses waveguide uni-travelling carrier photodetectors (UTC-PD). A compact 3 dB 2×2 multimode interference (MMI) coupler routes light from the ACP phase modulators into the balanced photodetector pair. A feedback path connecting the balanced photodetector pair to the ACP-phase modulator pair is also monolithically integrated on the ACP-OPLL PIC. The total feedback loop delay is ~ 10 ps. A detailed design of the ACP-OPLL PIC is presented in [4].

The base epitaxial wafer used in the fabrication is designed on a semi-insulating InP substrate, where the layers defining the UTC-photodetectors are grown on top of the phase modulator MQW structure with a 15 nm InP stop-etch layer in between. The modulator MQW structure is grown on top of a 0.85 μm -thick n -doped InP layer. Below the n -doped InP, a 100 nm-thick n -doped quaternary layer is used to make top-side n -metal contacts.

Photodetector regions are formed by selectively wet-etching the UTC-PD layers everywhere except in areas that define the UTC-PDs using an SiN_x hard mask. This is followed by regrowth of a 1.9 μm -thick p^+ -InP cladding, where the Zn-doping gradually increases from 5×10^{17} to $1 \times 10^{18} \text{ cm}^{-3}$, a 150 nm-thick p^{++} -InGaAs contact layer and a 400 nm-thick InP sacrificial cap layer. The waveguide pattern is first transferred to a 70 nm-thick Cr hard mask, which in turn is used to pattern a 600 nm-thick SiO_2 hard mask. The Cr hard mask is removed and the SiO_2 hard mask is used to etch deep ridge waveguides using $\text{Cl}_2:\text{H}_2:\text{Ar}$ chemistry in an inductively-coupled plasma reactive ion etching (ICP-RIE) system. The etch depth is controlled so that the etch stops $\sim 0.5 \mu\text{m}$ below the modulator MQW layers and at least 200–300 nm above the n -contact layer. The SiO_2 hard mask is removed and a mesa is defined using a SiN_x hard mask that covers the ridge. The remaining n -doped InP outside of the mesa is selectively wet-etched to expose the underlying quaternary n -contact layer. A scanning electron microscope (SEM) image of a cross-section of the phase modulator waveguide is shown in Fig. 1. This is followed by a

deposition and annealing of n -metal contacts, which consists of Ni/AuGe/Ni/Au (5 nm/80 nm/20 nm/120 nm) to provide RF loss in the n -ACP electrodes.

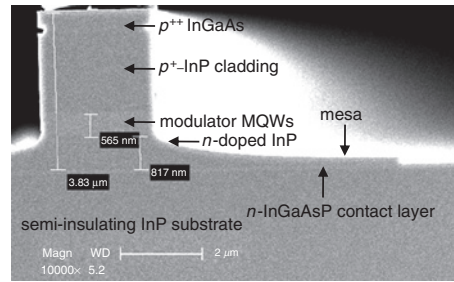


Fig. 1 SEM image of cross-section of phase modulator waveguide after deep ridge and mesa etch

Helium implantation is performed to electrically isolate the n -contact layers under the different active elements of the ACP-OPLL PIC using a 4.6 μm -thick Ti/Au mask that is defined in two stages using angled electron beam evaporation to prevent voids that would otherwise allow the He^+ ions to reach the semiconductor and block the lateral conduction from the ridge to the n -metal contacts. After helium implantation, the Ti/Au mask is removed and a deposition of 200 nm of SiN_x is performed. Proton implantation and subsequent removal of the p^{++} -InGaAs contact layer is performed between the active elements of the ACP-OPLL PIC to increase the electrical isolation in the p -doped top cladding layers between them. Proton implantation also reduces the free-carrier-induced optical loss. Photosensitive benzocyclobutene (BCB) is patterned and then hard-cured at 250°C in an N_2 atmosphere. The BCB is patterned on both sides of the ridge waveguides to reduce parasitic capacitance and enable high-speed operation of the 3 mm-long ACP phase modulators. Since the BCB does not planarise equally over the deep ridge waveguides ($\sim 3.7 \mu\text{m}$ tall) with different widths, BCB vias are opened separately over the 2.5 μm -wide ACP modulators and the $> 10 \mu\text{m}$ -wide UTC-photodetectors to remove the BCB on top of the ridge waveguides and expose the SiN_x where the p -contact vias can be etched later. A deposition of 150 nm-thick SiN_x is done to fill any voids that may have formed between the waveguide sidewalls and BCB. n -contact vias are opened over the n -contact and n -ACP electrodes to enable contact with interconnect metal pads. The SiN_x on top of the ridge is etched using a p -contact via, which is designed to be narrower than the waveguide ridge. The sacrificial InP cap layer is selectively wet-etched to expose the p^{++} -InGaAs contact layer. This is followed by deposition and annealing of p -metal contacts, which consists of Ti/Pt/Au (20 nm/40 nm/70 nm) to provide the RF loss in the p -ACP electrode. A final deposition of Ti/Au (20 nm/1.5 μm) forms pads for electrical contacts and the feedback trace of the OPLL. The wafer is thinned to $\sim 150 \mu\text{m}$ and back-side metallisation of Ti/Au (20 nm/0.5 μm) is applied. Devices are cleaved and mounted on carriers for testing. Each ACP-OPLL PIC is 4.25 mm long and 350 μm wide and a photograph is shown in Fig. 2.

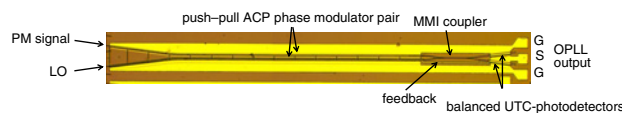


Fig. 2 Photograph of fully fabricated ACP-OPLL PIC coherent receiver PM: phase-modulated

Experiment and results: The phase demodulation linearity of the ACP-OPLL PIC is characterised in a phase modulated optical link at 1550 nm using a low phase noise CW fibre-laser and a LiNbO_3 linear phase modulator at the link transmitter. A 250 Ω series resistor is placed between the output of the ACP-OPLL PIC and the external 50 Ω load. This increases the OPLL open-loop gain ensuring adequate voltage drop across the ACP phase modulators. A standard two-tone intermodulation test was performed at 100 MHz. For 12 mA of photocurrent generated in each photodetector, the ACP-OPLL PIC demonstrates a 44.5 dB reduction in the relative nonlinear distortion level with respect to that observed when it operates as a conventional homodyne phase detector without feedback, as shown in Fig. 3.

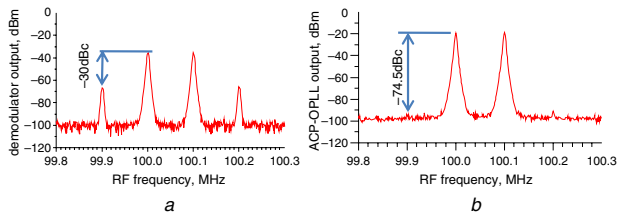


Fig. 3 Output spectrum showing distortion levels from ACP-OPLL
a Operating as conventional homodyne phase detector without feedback
b Operating with 12 mA of photocurrent generated in each photodetector
 Input RF power is +7 dBm/tone in both cases

The measured fundamental and the nonlinear distortion from the ACP-OPLL PIC are plotted against input RF power in Fig. 4. The distortion level follows a 3:1 slope, indicating that the distortion is due to the third-order nonlinearity. The third-order intermodulation intercept point at the input (IIP3) is +44 dBm. This corresponds to a phase IP3, Φ_{IP3} , of $\sim 7.8\pi$ as the V_{π} of the phase modulator at the transmitter is 4.5 V. The shot-noise limited link input noise floor (with 12 mA of photocurrent) is -152.6 dBm/Hz. Thus, the measured SFDR is 131.3 dB Hz^{2/3} in the detector shot-noise limit, which is 14 dB higher than the SFDR reported previously in a single-chip OPLL coherent receiver [5].

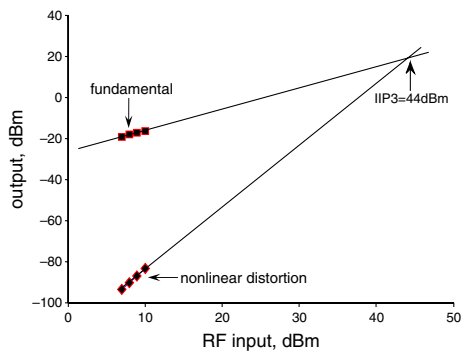


Fig. 4 Output from ACP-OPLL PIC showing measured fundamental and third-order nonlinear distortion against two-tone RF input power at 100 MHz

Conclusions: We have presented the first monolithically integrated ACP-OPLL coherent receiver. For 12 mA of photocurrent generated in each photodetector, an SFDR of 131.3 dB Hz^{2/3} is measured in the detector shot-noise limit at 100 MHz, which is the highest SFDR reported in a single-chip OPLL coherent receiver.

Acknowledgment: This work was supported by DARPA under the United States Air Force Contract FA8750-05-C-0265.

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 25 May 2011

doi: 10.1049/el.2011.1507

One or more of the Figures in this Letter are available in colour online.

A. Bhardwaj, J.E. Bowers and L.A. Coldren (*Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106, USA*)

E-mail: ashish.bhardwaj@jdsu.com

Y. Li, R. Wang and S. Jin (*Department of Electrical and Computer Engineering, University of Massachusetts, Dartmouth, MA 02747, USA*)

P. Herczfeld (*Department of Electrical and Computer Engineering, Drexel University, Philadelphia, PA 19104, USA*)

A. Bhardwaj: Also with JDSU Corporation, 80 Rose Orchard Way, San Jose, CA, 95134, USA

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A Monolithically Integrated ACP-OPLL Receiver for RF/Photonic Links

Yifei Li, Ashish Bhardwaj, Renyuan Wang, Sheilei Jin, Larry A. Coldren, *Fellow, IEEE*, John E. Bowers, *Fellow, IEEE*, and Peter Herczfeld, *Fellow, IEEE*

Abstract—The first monolithically integrated optical phase-locked loop (OPLL) employing attenuating-counter-propagating waves is presented. It demonstrates the highest dynamic range among monolithically integrated OPLLs. Its performance is limited by the bandwidth and linearity of the photodetectors used in the OPLL.

Index Terms—Dynamic range, optical phase-locked loop (OPLL), phase demodulation, photonic integrated circuit.

I. INTRODUCTION

It is desirable to replace bulky coaxial cables by fiber-optic links in advanced radar systems. However, the adaptation of fiber-optic links is still limited by their small Spurious Free Dynamic Range (SFDR). Many critical radar applications (such as channelized EW receivers) require an SFDR larger than $140 \text{ dB} \cdot \text{Hz}^{2/3}$, which is orders of magnitude higher than what is available with current state of the art. As a solution, a new phase modulated (PM) fiber-optic link employing an Optical Phase-Locked-Loop (OPLL) linear phase demodulator has been proposed [1], [2]. The OPLL demodulates the optical phase by tight phase tracking. It requires a large open loop gain over a wide bandwidth. Thus, its feedback stability only tolerates a very short loop delay ($< 10 \text{ ps}$). To realize such a short delay requirement, a novel Attenuation Counter-Propagating (ACP) OPLL has been proposed [2]. The ACP approach eliminates the phase delays arising from the phase modulators and the photodetectors within the OPLL. The ACP-concept has been validated in a hybrid integrated OPLL that consists of an ACP LiNbO_3 local phase modulator and a pair of bulk photodetectors [2]. In this letter, we present the first monolithically integrated ACP-OPLL Photonic Integrated Circuit (PIC) on an

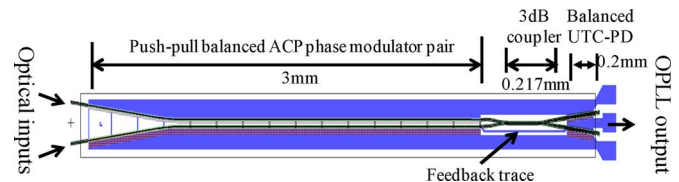


Fig. 1. ACP-OPLL photonic integrated circuit.

Indium Phosphide (InP)-based material platform. Details regarding its fabrication are reported in [3].

II. ACP-OPLL PHOTONIC INTEGRATED CIRCUIT

A mask layout of the ACP-OPLL PIC is shown in Fig. 1. It consists of a pair of push-pull ACP optical phase modulators, a pair of balanced uni-traveling carrier (UTC) waveguide photodetectors, a 3-dB optical coupler and a feedback trace that connects the balanced photodetectors to the phase modulators. Similar to previous OPLL PICs [1], the ACP-OPLL loop components share a multi-quantum well (MQW) optical waveguide to facilitate photonic integration. The MQW region contains 25 periods of lattice-matched $\text{In}_{0.65}\text{Ga}_{0.35}\text{As}_{0.76}\text{P}_{0.24}$ wells (9 nm thick) and $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}_{0.44}\text{P}_{0.56}$ barriers (6.5 nm thick). Stand-alone phase modulators using this quantum well design showed excellent linear phase modulation range (ϕ_{IP3}) per unit length ($\sim 4 \pi/\text{mm}$) and low optical loss ($< 1 \text{ dB/mm}$) [4].

To improve lateral confinement, the phase modulators inside the ACP-OPLL PIC are realized as deep ridge optical waveguides with a width of $2.5 \mu\text{m}$. The push-pull modulator pair is 3 mm long providing a combined ϕ_{IP3} of 24π , which is sufficient to enable an OPLL with an SFDR $\sim 140 \text{ dB} \cdot \text{Hz}^{2/3}$. To eliminate the latency, the phase modulator pair uses counter-propagating optical and RF modulation fields, where the RF modulation field is attenuated by the n- and the p-lossy electrodes of the push-pull modulator pair (see Fig. 2). Both lossy electrodes have a series resistance of $\sim 150 \Omega$. Fig. 3 shows the simulated response of the phase modulator pair. The simulated phase modulation sensitivity is 2.5 rad/volt , which corresponds to a V_π of 1.26 V . Its 3-dB bandwidth is 1.15 GHz . The phase response of the ACP phase modulator pair is bound between 0 and $\pi/2$, suggesting a lumped-element response that is free of propagation delay.

The layers that define the UTC-waveguide photodetector were developed by Klamkin *et al.* [5], and are grown on top of the phase modulator MQWs in the base-epitaxial wafer used in the fabrication of the ACP-OPLL PIC. This UTC-waveguide photodetector design can generate a large photocurrent ($> 50 \text{ mA}$) with high photodetection linearity

Manuscript received May 19, 2011; revised June 23, 2011; accepted July 16, 2011. Date of publication August 22, 2011; date of current version September 23, 2011. This work was supported DARPA via the PHOR-FRONT Program under the United States Air Force Contract FA8750-05-C-0265. A portion of this work was done in the UCSB nanofabrication facility, part of the NSF funded NNIN network.

Y. Li, R. Wang, and S. Jin are with the Department of Electrical and Computer Engineering, University of Mass, Dartmouth, MA 02747 USA (e-mail: yli2@umassd.edu).

A. Bhardwaj, L. A. Coldren, and J. E. Bowers are with the Department of Electrical and Computer Engineering, the University of California Santa Barbara, CA 93106, USA (e-mail: ashishb@ece.ucsb.edu).

P. Herczfeld is with the Department of Electrical and Computer Engineering, Drexel University, Philadelphia, PA 19104, USA (e-mail: herczfeld@ece.drexel.edu).

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Digital Object Identifier 10.1109/LPT.2011.2163184

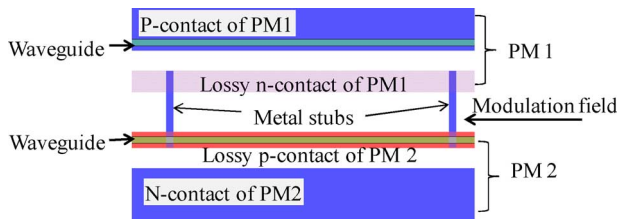


Fig. 2. A section of push-pull ACP phase modulator.

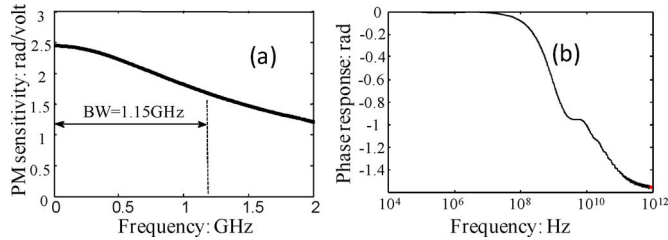


Fig. 3. Phase modulator response. (a) Magnitude response. (b) Phase response.

TABLE I
LOOP COMPONENT MEASUREMENTS

| Component | Measurement | Design goal |
|--------------------------------|-----------------|----------------|
| Push-pull phase modulator pair | Optical loss | ~ 2 dB/mm |
| | V_{π} | ~ 1.2 V |
| 3-dB coupler | Insertion loss | ~ 1 dB |
| | Splitting ratio | 50.7:49.3 |
| Single waveguide UTC-PD | Bandwidth * | < 200 MHz |
| | Quantum eff.* | $< 50\%$ |
| | OIP3* | ~ 13 dBm |

*The PD measurements were taken with 5 mA photocurrent, 6 V reverse bias, and a 50- Ω termination. The performance improves at a higher bias voltage but deteriorates with a larger photocurrent (or higher input power).

(OIP3 > 40 dBm) [5]. To eliminate its latency, the photodetector also employs the counter-propagating optical and RF fields. The width and the length of the photodetector are 10 μm and 200 μm , respectively. Based on the dimensions, a single photodetector should exhibit an RC time limited bandwidth of 2.76 GHz.

The photodetectors and the phase modulators are connected by a Multi-Mode Interference (MMI) 3-dB coupler to form the ACP-OPLL PIC. The coupler is 7 μm wide and 217 μm long. The complete loop delay of the ACP-OPLL, which is determined by the coupler and the feedback path, is ~ 10 ps.

III. EXPERIMENTAL RESULTS

The loop components of the ACP-OPLL PIC were first characterized using discrete components that were co-fabricated with the ACP-OPLL PIC on the same epitaxial wafer. The measurement results are summarized in Table I. The 3-dB coupler showed low insertion loss and ideal splitting ratio. The modulator pair also showed good V_{π} . However, the photodetector showed narrow bandwidth, small responsivity, and poor linearity (OIP3) compared to the design goals that were based on the photodetectors in [5].

Next, the ACP-OPLL receiver was characterized within a phase modulated optical link (see Fig. 4). The output of a fiber

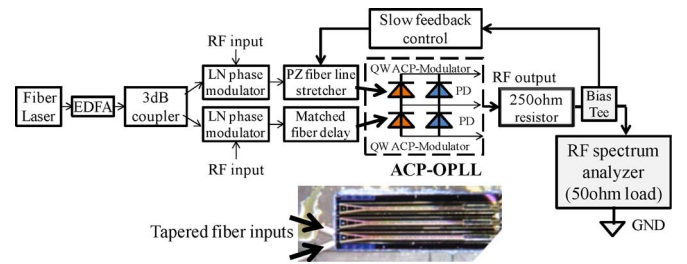


Fig. 4. PM link experimental setup.

laser operating at 1.55 μm was amplified using an erbium doped fiber amplifier (EDFA) unit, and then split into two paths using a polarization maintaining 3-dB optical coupler. Each path contains a transmitter (Tx) LiNbO₃ optical phase modulator with V_{π} of 4.5 V. The RF inputs are applied to the LiNbO₃ phase modulators. Phase modulated optical signals are launched into the waveguide inputs of the ACP-OPLL using a tapered fiber with a 2.5 μm spot diameter. The coupling loss between the tapered fiber and the optical waveguide was measured to be ~ 2.5 dB. To ensure a sufficient open loop gain in presence of poor photodetector responsivity, a 300 Ω load impedance was used at the ACP-OPLL output. Ideally, this should be accomplished using an impedance transformer. However, a simpler approach was taken by inserting a 250 Ω series resistor between the output of the ACP-OPLL and the external 50 Ω load. Due to this arrangement, the power captured at the RF spectrum analyzer is 7.78 dB lower than the RF power at the ACP-OPLL output. To overcome environmental perturbations, the slow varying portion of the ACP-OPLL's output was extracted through the DC port of an RF bias-Tee and fed back to a piezo-electric fiber-optic line stretcher to correct for phase errors. This ensures long-term stable phase locking.

The feedback stability of the ACP-OPLL PIC was verified while gradually increasing the optical input power. To avoid facet damage, the optical power launched from each tapered fiber was limited to 200 mW. During this process, no oscillation or other forms of instabilities were observed.

The linearity of the ACP-OPLL PIC was determined using a two-tone inter-modulation test. The optical power launched into each input waveguide was 200 mW. The reverse bias voltage was initially set at 6 V, where the MQW ACP-phase modulators showed good linearity [4]. Each photodetector generated a photocurrent of 12 mA. The ACP-OPLL PIC showed good phase demodulation linearity below 170 MHz. A sample of the 150 MHz output captured at the 50 Ω load is shown in Fig. 5(a). With 7 dBm RF input, the measured inter-modulation distortion (IMD) level was -71 dBc. The link input third order inter-modulation intercept point (IIP3) was measured to be 42.5 dBm (see Fig. 5(b)). Since the LiNbO₃ phase modulator at the link input has a V_{π} of 4.5 V, the IIP3 corresponds to a demodulation ϕ_{IP3} (i.e., the maximum linear phase demodulation range) [4] of 6.9π . In addition, the third order intercept point at the output of the ACP-OPLL (OIP3) is ~ 23.68 dBm. At 150 MHz, the noise power delivered to the 50 Ω external load was measured to be ~ -171 dBm/Hz, from which the ACP-OPLL output noise floor was determined to be ~ -163 dBm/Hz. Thus, the SFDR is ~ 124.5 dB \cdot Hz^{2/3} at 150 MHz.

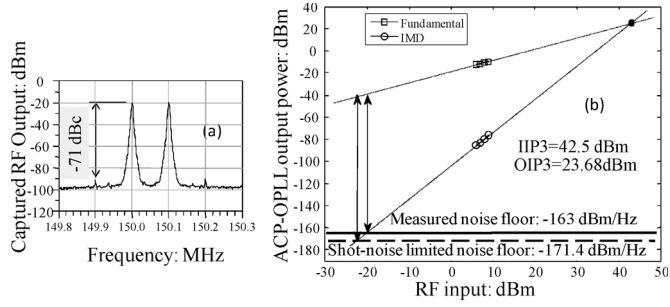


Fig. 5. Distortion measurements at 150 MHz. (a). Captured RF spectrum with 7 dBm RF input. (b) The third order intercept point measurement. The ACP-OPLL output is 7.78 dB higher than the spectrum analyzer reading.

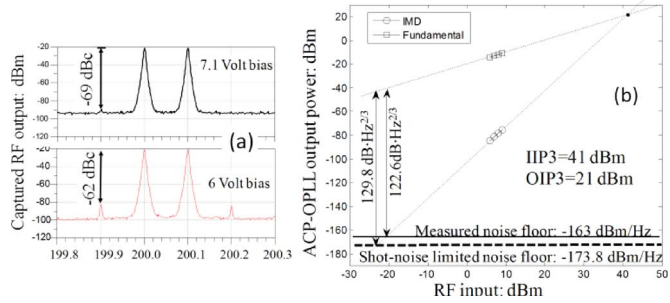


Fig. 6. Distortion measurements at 200 MHz. (a). Captured RF spectrum with 7 dBm RF input. (b) The third order intercept point measurement at 7.1 V bias. The ACP-OPLL output is 7.78 dB higher than the spectrum analyzer reading.

Since this letter is focused on the ACP-OPLL receiver, we also determined the SFDR in the photodetector shot-noise limit. This represents the performance of the ACP-OPLL receiver when the noise from the link transmitter is negligible. The link output noise floor in the shot-noise limit is given by:

$$N_{\text{out_shot_noise_limit}} = G_{\text{link}} \cdot \left(\frac{e}{I_{PD}} \right) \cdot \left(\frac{V_{\pi}}{\pi} \right)^2 \quad (1)$$

where G_{link} is the link gain, I_{PD} is the photocurrent generated in each photodetector, V_{π} and Z_{term} are the half wave voltage and the termination resistance of the Tx LiNbO₃ phase modulator, respectively. G_{link} was measured to be -18.82 dB. With 12 mA of photocurrent, the output noise floor in the shot-noise limit was calculated to be -171.4 dBm/Hz. Thus, the SFDR in the shot-noise limit is 130.1 dB \cdot Hz^{2/3} at 150 MHz.

The performance of the ACP-OPLL PIC degraded significantly beyond 170 MHz at a reverse bias of 6 V due to the narrow bandwidth observed in the photodetectors. But a higher reverse bias voltage helped to extend the operating bandwidth of the ACP-OPLL PIC. As shown in Fig. 6(a), when the reverse bias voltage was increased to 7.1 V, the distortion level at 200 MHz improved by 7 dB. The IIP3 and OIP3 in this case were 41 dBm and 21 dBm, respectively (see Fig. 6(b)). The measured SFDR was 122.6 dB \cdot Hz^{2/3}. The link gain was -20 dB. With a higher reverse bias voltage the photocurrent also increased to 15 mA. The shot-noise limited output noise floor was -173.8 dBm/Hz. Thus, at 200 MHz, the SFDR in the photodetector shot-noise limit was 129.8 dB \cdot Hz^{2/3}. Increasing the

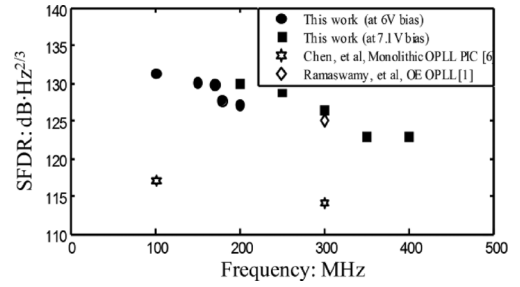


Fig. 7. SFDR in the photodetector shot-noise limit versus RF frequency.

reverse bias voltage further did not enhance the performance of the ACP-OPLL receiver.

The SFDR (in the shot-noise limit) of the ACP-OPLL PIC as a function of RF frequency is summarized in Fig. 7, and the results are compared with the best reported SFDRs (also in the shot-noise limit) of other OPLL PIC devices. Despite the non-ideal photodetectors, the SFDR of the ACP-OPLL PIC is 10 dB higher compared to that observed in earlier monolithically integrated OPLL PICs [6]. At 300 MHz, its SFDR is comparable (~ 1 dB better) to an optoelectronic (OE) OPLL [1] that requires an external electronic amplifier.

IV. CONCLUSION

The design and characterization of the first monolithically integrated ACP-OPLL PIC have been presented. This device demonstrates the highest SFDR (in shot-noise limit) among monolithically integrated OPLL PICs. Its performance is limited by the bandwidth and the linearity of the photodetectors.

ACKNOWLEDGMENT

The authors would like to thank Dr. J. Klamkin, Dr. S. Ristic, U. Krishnamachari, and Dr. L. Johansson for helpful discussions.

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I. Photonic Integrated Circuits

E. Coherent Beam Sweeping

Two-dimensional free-space beam steering with an optical phased array on silicon-on-insulator

J. K. Doylend*, M. J. R. Heck, J. T. Bovington, J. D. Peters, L. A. Coldren, and J. E. Bowers

Dept. of Electrical and Computer Engineering, University of California, Santa Barbara, California 93106, USA
*doylend@ece.ucsb.edu

Abstract: We demonstrate a 16-channel, independently tuned waveguide surface grating optical phased array in silicon for two dimensional beam steering with a total field of view of $20^\circ \times 14^\circ$, beam width of $0.6^\circ \times 1.6^\circ$, and full-window background peak suppression of 10 dB.

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OCIS codes: (130.3120) Integrated optics devices; (250.5300) Photonic integrated circuits.

References and links

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1. Introduction

Optical phased arrays enable free-space beam steering without moving parts, making them desirable for robust point-to-point free-space communications, Light Detection and Ranging (LIDAR), and optical memory. Chip-scale optical phased arrays have been demonstrated using tunable gain elements [1] and phase tuning [2], and phased arrays composed of waveguide surface gratings in silicon-on-insulator (SOI) have also been demonstrated with a steering range of $2.3^\circ \times 14^\circ$ using a single thermo-optic phase tuner together with wavelength tuning [3,4]. While the approach demonstrated by Acoleyen *et al.* is both CMOS-compatible and elegant in its simplicity, there is no means of actively compensating for accumulated phase errors between individual channels due to on-chip propagation and thermal cross-talk, thus resulting in undesirable off-axis peaks and limited tuning range. Phase tuning of the

individual channels provides a solution to these problems; such an approach has been used to demonstrate 1-dimensional beam steering in a silicon slab [5]. Also of note is an alternate technique in which an entirely passive device was used to raster a beam across the far field using wavelength alone [6], thus avoiding phase tuning elements altogether at the cost of a relatively wide beam in the far field (4°) and no means of arbitrarily shaping the wavefront. The use of SOI is significant because it is compatible with standard CMOS fabrication techniques; furthermore, with the advent of tunable optical sources [7, 8] and amplifiers [9, 10] using hybrid integration of III-V gain materials with silicon rib waveguides, the prospect of a self-contained steerable free-space optical source becomes possible.

In this work we demonstrate a 16-channel optical phased array in SOI in which the phase of each channel is individually controlled to achieve free-space beam steering in two dimensions across a $20^\circ \times 14^\circ$ field of view, far field beam width of $0.6^\circ \times 1.6^\circ$, and 10 dB background peak suppression. The phase tuning was accomplished thermo-optically using resistive heaters in the vicinity of the waveguides. Phase errors and background peaks were minimized by an optimization algorithm using feedback from an infrared camera which recorded the far field image in real time; a lookup table of solved phase settings was then used to steer the beam arbitrarily without the need for real-time feedback. In this manner thermal crosstalk and phase errors were circumvented so as to achieve arbitrary two dimensional beam pointing within the field of view.

2. Design and fabrication

Rib waveguides of $1 \mu\text{m}$ width were patterned via photolithography in SOI and dry-etched to a depth of $280 \pm 20 \text{ nm}$. The SOI has 500 nm top silicon thickness and $1 \mu\text{m}$ buried oxide. Multi-mode interferometer (MMI) 1×2 couplers were used to split the beam into 16 channels. Surface gratings were defined via e-beam lithography and etched to a depth of 75 nm . Resistive heaters of $470 \mu\text{m}$ length for thermo-optic tuning were fabricated by e-beam deposition and lift-off of a $72 \text{ nm} / 75 \text{ nm}$ nickel-chrome-gold metal stack directly on the silicon surface. The heaters were offset $6.5 \mu\text{m}$ from the rib waveguides so as to avoid excess loss due to metal optical absorption at the expense of thermal tuning efficiency. The waveguides in this phase-tuning region of the device were spaced $100 \mu\text{m}$ apart, of which $79 \mu\text{m}$ was etched entirely to the buried oxide to enhance thermal isolation. The grating array had 50% duty cycle, $3.5 \mu\text{m}$ lateral waveguide spacing, $200 \mu\text{m}$ length, and full width (i.e. the grating grooves completely spanned each waveguide). The propagation length from the input to the grating was approximately 4 mm . A schematic picture of the device is shown in Fig. 1.

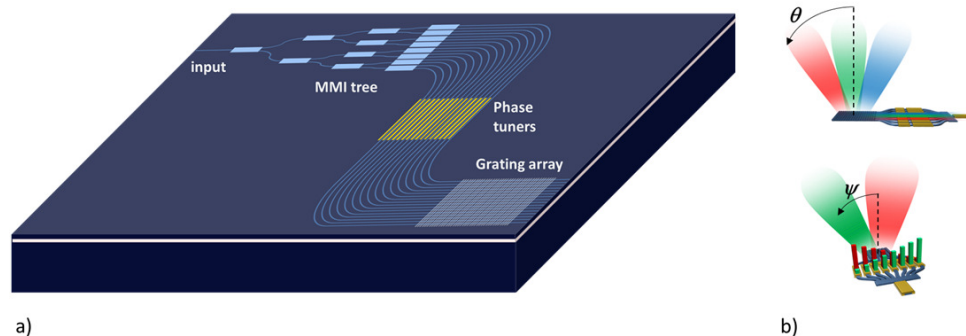


Fig. 1. a) Schematic diagram of the 16-channel grating array with independently tuned channels for 2-dimensional beam steering. A multi-mode interferometer (MMI) tree split the input into 16 channels which were then independently phase tuned and coupled to a grating array. Beam steering in the longitudinal axis θ was accomplished via wavelength tuning while beam steering in the lateral axis ψ was accomplished by phase tuning. b) Schematic diagrams illustrating the respective orientations of the longitudinal axis θ and the lateral axis ψ .

The small grating etch depth relative to the overall rib waveguide dimensions was chosen to reduce the grating strength, thus increasing the propagation length over which the guided mode was outcoupled in order to maintain a narrow beam in the far field along the longitudinal axis. Solitary waveguide surface grating test structures with a variety of duty cycles and grating widths (i.e. width of the grating groove within the rib waveguide) were fabricated alongside the 16-channel device in order to evaluate the feasibility of incorporating chirp/apodization into future grating array devices. Scanning electron microscope images of the grating array, a grating test structure, and an optical microscope image of the phase tuners are shown in Fig. 2.

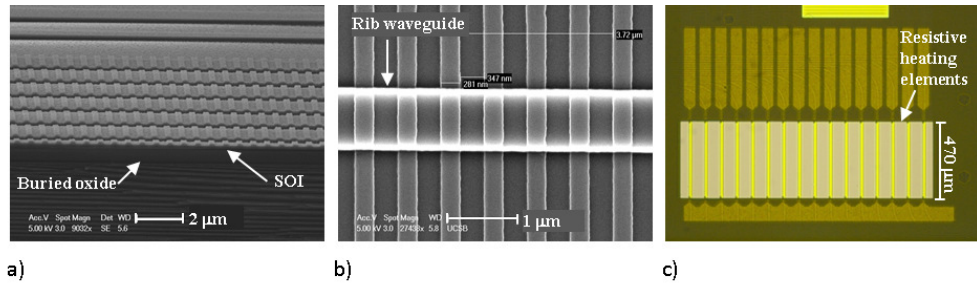


Fig. 2. Scanning electron microscope images of (a) the grating array cross-section, (b) a single surface waveguide grating test structure, and (c) optical microscope images of the thermo-optic phase tuners.

3. Passive grating characterization

The far field output was characterized using a high-numerical-aperture aspheric lens ($NA = 0.83$, effective focal length = 15 mm) to image the far field into the Fourier plane and two additional lenses (effective focal lengths 180 mm and 60 mm) to magnify and focus the beam onto an infrared camera (320x256 pixels, 25 μm pitch); this system has far field resolution of 0.3° at normal outcoupling. The maximum longitudinal outcoupling angle measurable by the system (without tilting the lens tube relative to the chip surface) is 39° ; the maximum measurable angle in the lateral direction is 33° . A polarization controller was used to align the polarization along the TE axis and a polarizer mounted in front of the camera was used to filter out any remaining TM polarized scattering; all measurements described in this work are for TE polarized input light. The 180 mm focal length lens was attached via a rotating mount such that near field images of the grating could be collected and then the lens could be reinserted for far field images. This characterization technique follows the approach presented by Thomas *et al.* [11] and enabled the system to be focused on the grating array (using the near field image for guidance) prior to collecting far field data. This system will henceforth be referred to as the “Fourier imaging system”.

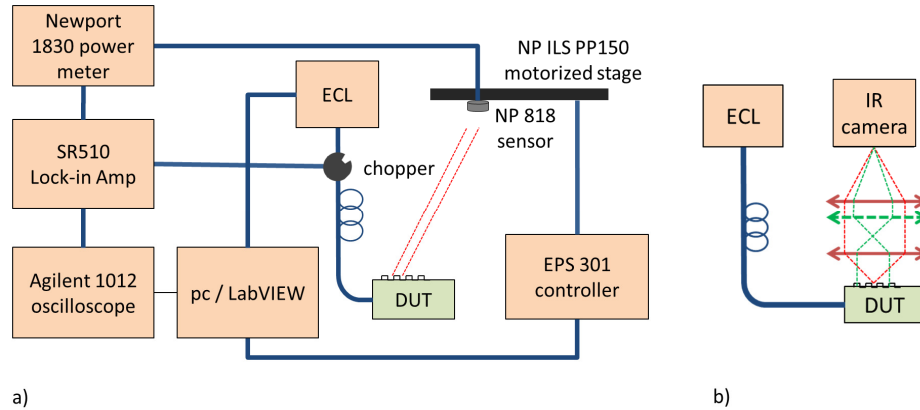


Fig. 3. a) Beam profiler measurement system, and b) Fourier imaging system with removable lens for near field imaging. The removable lens is shown in green together with the associated far field ray traces, while the non-removable lenses are shown in red with the associated near field ray traces. ECL = external cavity laser; DUT = device under test.

A second characterization system consisting of a Newport 818 photodetector mounted on a Newport ILS PP150 motorized stage at a distance of 14.7 cm from the chip surface and translated across the far field was used to profile the beam and calibrate the Fourier imaging system. A schematic of each characterization system is shown in Fig. 3.

Test structures consisting of individual gratings fabricated on isolated waveguides were characterized to assess wavelength tuning and longitudinal beam width. The longitudinal emission angle θ is given by Eq. (1):

$$\sin \theta = \frac{n_{eff} \Lambda - \lambda_0}{\Lambda} \quad (1)$$

where n_{eff} is the effective index of the waveguide within the grating for λ_0 , Λ is the grating pitch, and λ_0 is the free-space wavelength.

The longitudinal optical far field emission profile of a test grating with 600 nm pitch measured using the beam profiler is shown in Fig. 4 together with corresponding far field images captured using the Fourier imaging system and a plot of the longitudinal emission angle as a function of wavelength both for the 16-channel grating array and a corresponding test structure. The simulated output was obtained from Eq. (1) using the calculated effective index of the waveguide within the grating. For wavelengths from 1525 nm – 1625 nm, the tuning efficiency was measured to be 0.14 ± 0.01 °/nm, matching the value calculated from RSoft BeamPROP simulations. An offset of 4° between the measured and simulated outcoupling was observed and attributed to the effects of trenching, non-vertical sidewalls, and etch depth variation. The results of the Fourier imaging measurement matched those of the beam profile measurement, thus experimentally validating the former.

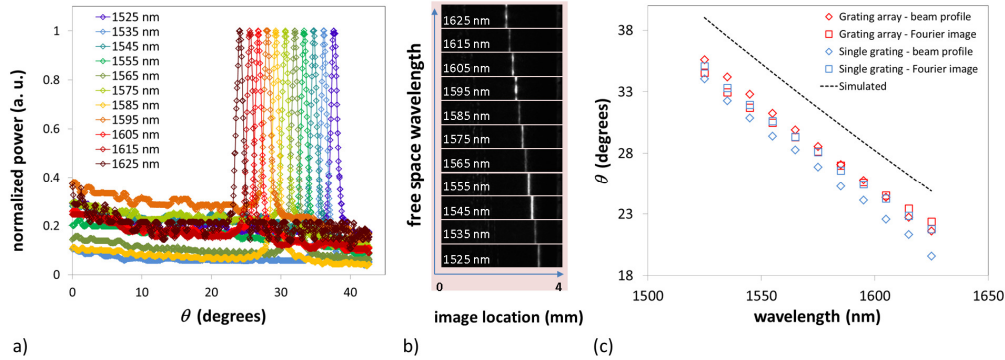


Fig. 4. (a) Normalized optical output profile in the far field measured using the beam profiler; (b) Far field images captured using the Fourier imager for wavelengths from 1625 nm (top) to 1525 nm (bottom); (c) Plot of the longitudinal beam angle in the far field measured for an individual grating (blue) and a 16-channel grating array (red) using both the Fourier imaging system (square markers) and beam profiler (diamond markers), with the simulated output calculated from the Bragg equation shown for comparison.

The ability to chirp individual gratings or to apodize the grating array can be a valuable means of optimizing efficiency and beam shape; grating width and duty cycle are parameters which can be adjusted for this purpose. However, since the far field emission angle is affected not only by wavelength but also by variation in the effective index according to Eq. (1), the variation in output angle as a function of grating duty cycle and width (i.e. the width of the grating grooves relative to the rib waveguide – see Fig. 5b) can be a concern since it necessarily introduces a spread of outcoupling angles in the far field. Accordingly the angular variation of the output as a function of duty cycle and grating width was characterized using single-grating test structures. A plot of the angular deviation with respect to each parameter is shown in Fig. 5 together with SEM images of gratings with varying width and duty cycle. As expected, $\Delta\theta$ decreased with duty cycle due to the decreasing effective index of the mode with a larger fraction of the rib etched away and decreased for wider etched grating trenches. Total variation of $>2^\circ$ in the outcoupling angle was observed for duty cycles ranging from 20% - 80%, and $> 1.5^\circ$ variation was observed for grating widths ranging from 100 nm – 900 nm. Accordingly, using these parameters as a means of chirping and/or apodizing would involve a significant tradeoff due to concomitant increases in beam width.

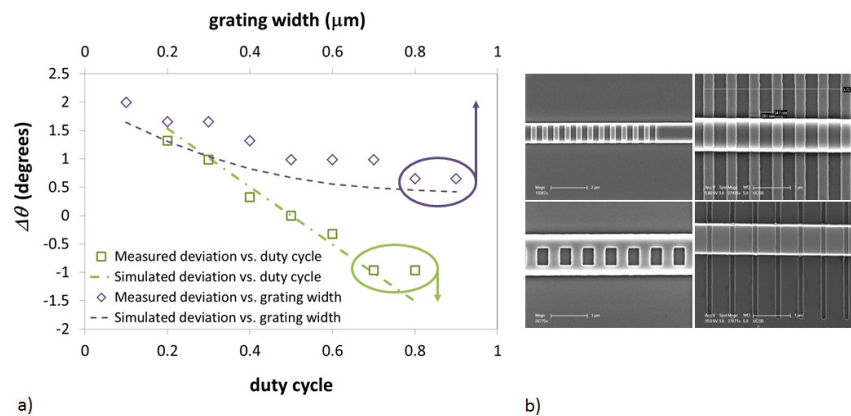


Fig. 5. Plot of the longitudinal angular deviation in the far field (calculated relative to the output for 50% duty cycle and full width (i.e. width extending across the entire array of test structures) measured and simulated as a function of grating width and duty cycle. Shown to the right are SEM images of a 50% duty cycle grating with 0.9 μm width (upper left), 400 nm width (lower left), 50% duty cycle full width (upper right), and 20% duty cycle full width (lower right).

For a uniform grating the longitudinal beam width in the far field is determined by the propagation length over which power is emitted. The scattering profile of each single-grating test structure was measured from near field images of the optical emission, fitted to an exponential decay, and used to calculate beam width (full-width half-maximum, or FWHM) in the far field by numerically integrating the associated Fourier transform. These calculated results are plotted for a selection of duty cycles and grating widths in Fig. 6 together with the beam width directly measured in the far field using the Fourier imaging system. Theoretical values calculated from the propagation loss simulated using RSoft FullWAVE are shown for comparison.

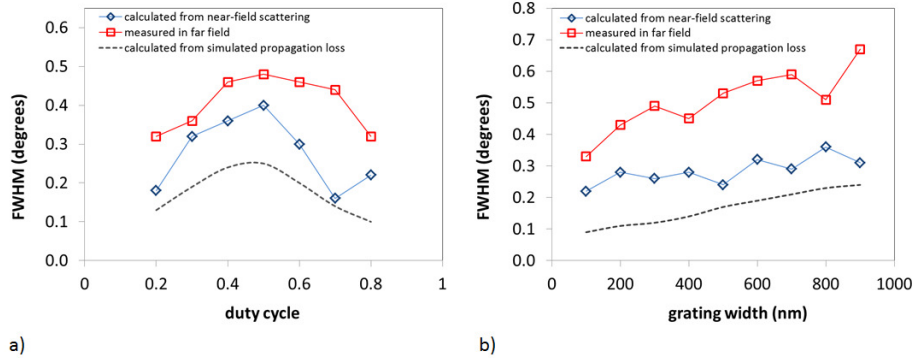


Fig. 6. Plots as a function of grating duty cycle (a) and width (b) of the longitudinal beam width (FWHM) in the far field calculated from the scattered power distribution in the near field (blue) and measured directly from the far field image (red) at 1555 nm.

The grating strength increased as duty cycle approached 50%, yielding a smaller effective grating length and thus a larger beam width in the far field. Similarly, the grating strength increased with grating width, reducing the effective grating length and thus spreading the beam in the far field. The discrepancy between FWHM calculated from the near field images and measured directly in the far field was attributed to mode evolution within the grating, resulting in a spread of output emission angles and hence a larger than expected beam width. It should be noted that the measured far field beam width is also limited by the angular measurement resolution of the system (0.2° per pixel at $\theta = 31^\circ$). The disparity between the simulated and actual beam width also suggests additional scattering mechanisms within the grating (e.g. sidewall roughness).

3. Phase tuned grating array characterization

While beam control in the longitudinal axis θ was controlled with wavelength, control in the lateral direction was accomplished with a phased array. For a regular emitter array, the lateral direction ψ of the beam is determined according to Eq. (2):

$$\sin \psi = \frac{\lambda_0 \phi}{2\pi d} \quad (2)$$

where ϕ is the uniform phase increment between emitters, and d is the emitter spacing. In practice, however, phase errors are introduced by differences in effective path length between channels due to wavelength bends and process variation across the chip. To correct for these phase errors, a resistive heater was added in the vicinity of each waveguide so as to permit individual thermo-optic phase tuning of each channel.

The phase tuning efficiency of a single element was measured using a Mach-Zehnder interferometer (MZI) test structure with the same waveguide profile and phase tuners used in the 16-channel grating array. The efficiency was found to be (215 ± 15) mW/ π . In order to

provide 430 mW per channel as required to reach a full 2π tuning range, an ILX 3916 laser driver array with modulation inputs driven by a National Instruments analogue output data acquisition card via a custom-built buffer array was used. The thermo-optic tuners were fabricated with a resistance of $(65 \pm 5) \Omega$ such that each could be driven past 500 mW without exceeding the laser driver voltage limit of 7.5 V.

Thermal crosstalk between channels was measured by recording the resistance of each tuning electrode in the array at steady state while a single channel was subjected to high thermal power. The dependence of tuner resistance on temperature was determined separately by fabricating identical tuners on bulk silicon and measuring their resistance and the temperature of the substrate while slowly heating the substrate. A plot of the relative temperature thus measured across the tuning array with 15 of the 16 channels each driven to 30 mW while a single channel near the center (channel 9) was driven at higher thermal power is shown in Fig. 7.

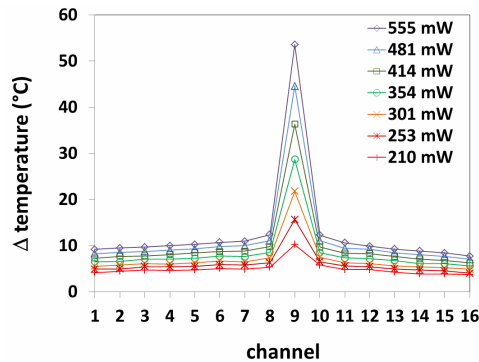


Fig. 7. Relative thermal gradient across the 16-channel array when 15 channels were driven at 30 mW and a single central channel was driven at higher thermal powers. Temperatures (relative to the corresponding values when all channels were driven at 30 mW) were calculated from the change in resistance of each tuner; the relationship between resistance and temperature for the tuners was calibrated separately using a thermocouple to record the temperature of a bulk silicon substrate on which identical tuners had been fabricated.

It is apparent from Fig. 7 that crosstalk between channels is significant, with all channels heated by several degrees in response to power injected on a single channel. Since individual channels were separated by $79 \mu\text{m}$ wide trenches etched through the top silicon to the buried oxide, this suggests that injected thermal power heats the whole top silicon layer above the buried oxide as well as affecting adjacent channels via heat transfer along the axis of the waveguide particularly around the beginning and end of the thermal isolation trenches. This problem may be alleviated in future by using a thinner buried oxide and by etching holes through the buried oxide and depositing metal at each end to form thermal shunts between the top silicon layer and the substrate.

While phase errors might be eliminated for a given beam angle using a particular phase vector applied to the thermo-optic tuners for each wavelength, a different beam angle requires a new tuning vector determined not only by Eq. (2) but also by the thermal crosstalk. It was therefore impractical, within this configuration, to control the beam output using Eq. (2) to predict the 16-element thermal tuning vector required for a given beam angle. Instead a brute-force hill-climber algorithm implemented in NI LabVIEW code was used to solve for the optimal tuning vector along each desired beam direction, with the Fourier imaging system providing far field feedback. The algorithm operated by setting five closely spaced drive currents on a given channel and comparing the far field distribution for each by parsing the image from the infrared camera to calculate R , where R is the ratio of the power $P(\psi_0, \theta_0)$ (i.e. power measured in the vicinity of the desired angles ψ_0 and θ_0) to the overall power $\int P(\psi, \theta_0) d\psi$ collected within the total field of view near longitudinal angle θ_0 . The algorithm

calculated $R(i, \psi_0, \theta_0)$, $\partial R / \partial i$, and $\partial^2 R / \partial i^2$ using a polynomial fit, evaluated a truth table to decide in which direction and how far to step the drive current on the given channel, and then proceeded to the next channel. A flowchart illustrating these steps is shown in Fig. 8.

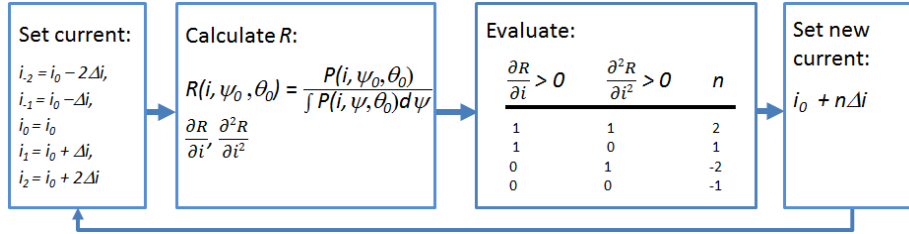


Fig. 8. Hill-climber algorithm implemented in NI LabVIEW and used to optimize the phase tuning of the 16-channel grating array for beam outcoupling at a given lateral angle ψ using feedback from the Fourier imaging system.

Using this automated optimization routine together with real-time feedback from the Fourier imaging system, phase tuning solution sets with background suppression of 10 dB were obtained for points at 1 degree spacing in each axis across a 14° (θ axis) by 20° (ψ axis) field of view. The algorithm generally required less than 100 iterations of the full tuning array to reach a solution; the iterative speed was limited by the 60 Hz refresh rate of the infrared camera such that 1.3 seconds was required to evaluate and adjust the full 16-element phase vector at 5 points per channel. Total solution time for each point was therefore typically less than 2.5 minutes although certain locations within the field of view required considerably longer to converge.

Representative plots of the beam profile at $\psi = 0^\circ$, $\theta = 31^\circ$ (i.e. 1555 nm) as seen without phase tuning and as solved by this system are shown in Fig. 9 along with theoretical profiles and the corresponding sections of the far field images.

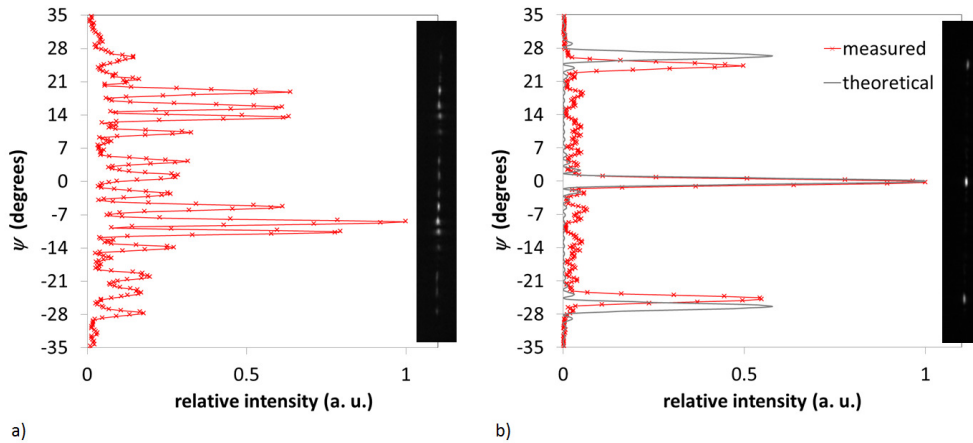


Fig. 9. Beam profile in ψ axis and corresponding sections of the far field image for a wavelength of 1555 nm (a) without phase tuning and (b) with phase tuning after applying the optimization algorithm. The 2° discrepancy between measured and theoretical side lobe location is attributed to lens Seidel aberrations.

The theoretical profile was attained by summing the far field contributions from each emitter assuming an emission amplitude function corresponding to the calculated mode profile at the grating etch depth. The measured beam width (FWHM) along ψ was 1.6° . It should be noted that the location of the secondary peaks at $\psi = \pm 26^\circ$ was determined by the spacing between array elements while their height was determined by the width of each array element. For beam pointing applications where the ability to collect the output at a single

emission angle is required, the total field of view over which a solitary beam can be swept is limited by the secondary peak spacing; for the device described here, the maximum total field of view was $\pm 10^\circ$ in order to prevent secondary peaks from encroaching on the field of view. It is therefore apparent that for a given number of channels there is a tradeoff in the ψ axis between beam width (ideally as small as possible) and total field of view (ideally as large as possible) since increased spacing between adjacent gratings reduces both the beam width and the secondary peak spacing.

The phase solution set obtained for the entire field of view using the algorithm/feedback technique described above was then used to generate a look-up table (LUT) such that the beam could be pointed arbitrarily without further need for real-time feedback. Profiles of the beam in the ψ axis for alignment at 1° increments across the field of view are shown in Fig. 10, and 3D plots of the beam measured at the corners and center of the field of view are shown in Fig. 11.

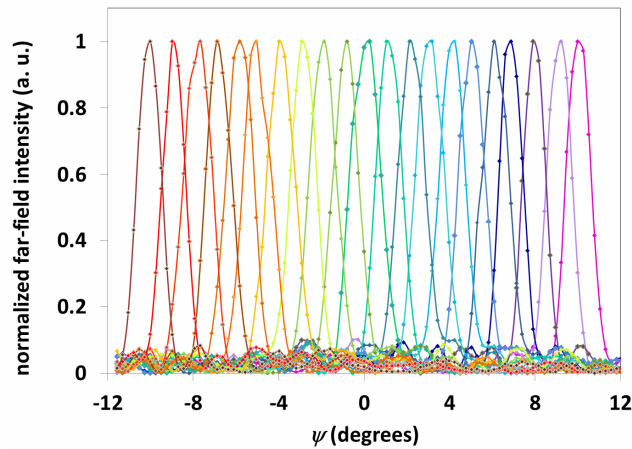


Fig. 10. Measured beam profiles at 1555 nm wavelength as the beam was swept across the field of view in the ψ axis at 1° increments.

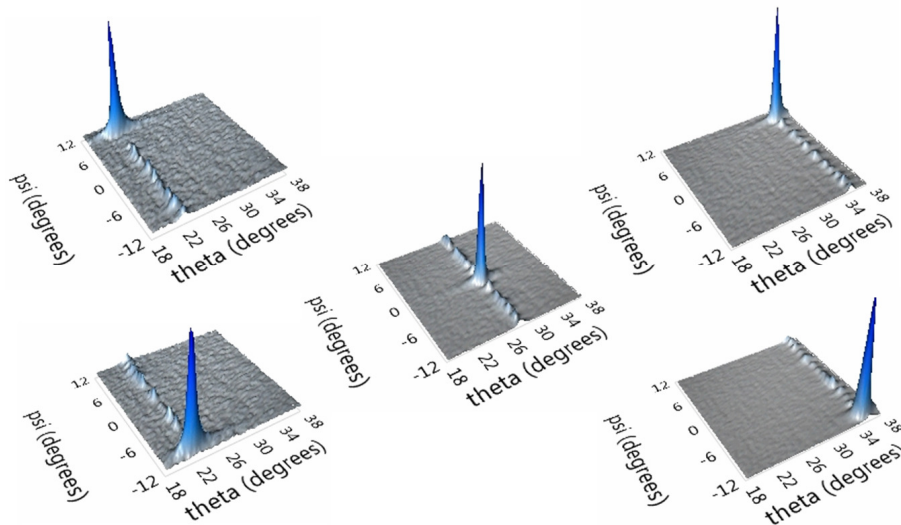


Fig. 11. Plots of the 2D beam profiles at the corners and centre of the field of view located using the LUT. The field of view was chosen so as to exclude the secondary peaks.

The optical efficiency of the device was measured by using the lookup table to point the beam at the Newport 818 photodetector in the far field. The Newport 818 photodiode has a 3 mm diameter aperture - corresponding to 0.8° at a distance of 147 mm and $\theta = 35^\circ$; the photodiode aperture therefore limited the portion of the beam collected in the ψ axis. However a comparison of the measured peak power (-41.2 dBm for fiber launch power of -13 dBm) with the known photodiode aperture and measured beam width of 1.6° in the ψ axis suggests total beam power of -38.4 dBm (beam width in the θ axis was 0.7° , and therefore not significantly apertured by the photodiode). On-chip waveguide propagation loss and fiber-to-chip facet coupling loss were measured via the Fabry-Pérot transmission fringes of a straight waveguide test structure and found to be 3.0 ± 0.2 dB/cm and 10.1 ± 0.2 dB respectively using $1.7 \mu\text{m}$ spot size lensed fiber. Since on-chip propagation length prior to the grating array was 4 mm, the grating efficiency (defined as the quotient of total power in the desired far field beam and on-chip waveguide-coupled power) was calculated to be -14.1 ± 0.2 dB. Of this, theoretical coupling to the side lobes was calculated to account for 6.4 dB and downward emission into the substrate was calculated to account for 5.8 dB. The former can be addressed in future devices by increasing the rib waveguide width in order to suppress side lobes; the latter may be improved by optimizing the buried oxide thickness [12]. The remaining 1.9 dB was therefore due to excess loss within the 16-channel MMI tree and the grating array.

4. Conclusion

A 16-channel optical phased array fabricated in SOI with independently phase-tuned channels has been fabricated and shown to achieve free-space beam steering across a $20^\circ \times 14^\circ$ field of view with far-field resolution of less than 1° , and background suppression of more than 10 dB. The effect of duty cycle and grating width on far field beam direction and size were characterized and shown to introduce significant alteration in regard to both.

An algorithm using feedback from far field images of the beam was applied to the 16-channel device to solve for phased array solutions at each beam direction in the field of view, and these solutions were then incorporated into a lookup table such that the beam was steerable in two dimensions without feedback. This approach shows promise as a means of achieving rapidly scanned beams in two dimensions for applications such as LIDAR, free space communications and optical memory.

Acknowledgements

The authors thank Pietro Binetti, Weihua Guo, Chad Althouse, Ben Curtin, Bill Mitchell, and Scott Rodgers for useful discussions. This research was supported by the DARPA Sweeper program, grant #HR0011-10-2-0003. Jonathan Doyle's work was supported in part by a Natural Sciences and Engineering Research Council of Canada Post-doctoral Fellowship.

InP Photonic Integrated Circuit for 2D Optical Beam Steering

Weihua Guo¹, Pietro R. A. Binetti¹, Chad Althouse¹, Ashish Bhardwaj¹, Jonathan Doylend¹, Huub P.M.M. Ambrosius², Leif A. Johansson¹, member, IEEE and Larry A. Coldren^{1,3}, Fellow, IEEE

¹Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA, 93106, USA.

²Electrical Engineering Department, Eindhoven University of Technology, Eindhoven, NL.

³Department of Materials, University of California, Santa Barbara, CA, 93106, USA.

Email: guow@ece.ucsb.edu

Abstract—InP photonic integrated circuit for 2D ($5^\circ \times 10^\circ$) optical beam steering has been demonstrated for the first time. Design, fabrication, and preliminary results are presented.

Keywords—Lidar; optical beam steering; photonic integrated circuit

I. INTRODUCTION

Electronically controlled 2D optical beam steering will become very useful for light detection and ranging (LIDAR) [1, 2]. In this work we demonstrate an InP based photonic integrated circuit (PIC) for this purpose. The critical component of the PIC is an optical phased array with embedded second-order gratings which function as out-of-plane vertical emitters, as schematically shown in Fig. 1. Wavelength tuning is employed to steer the beam in the direction along the grating (longitudinal direction θ) because the emission angle of the grating is dependent on the wavelength. Phase tuning across the phased array is used to steer the beam perpendicular to the grating (lateral direction ϕ). 2D beam steering is thus achieved by controlling both the wavelength and the phase across the phased array.

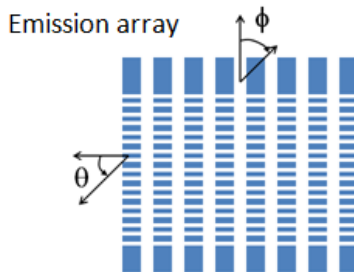


Fig. 1 Schematic structure of the emission array

II. STRUCTURE AND FABRICATION

As shown in Fig. 2, the PIC consists of an input semiconductor optical amplifier (SOA), a 1×8 beam splitter composed of cascaded 1×2 MMI beam splitters, a phase shifter (PS) array, an SOA array, the emission array composed of SOAs with embedded 2nd order gratings for out-of-plane light emission, and monitors composed of MMI splitters and

photodiodes (PD) to provide feedback for the electronic control of the photonic circuit.

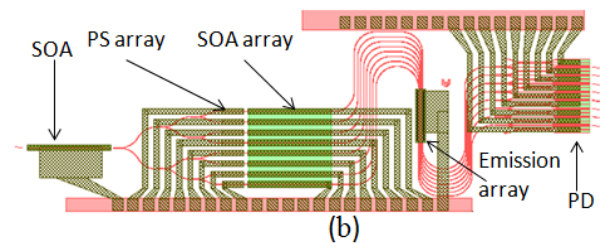


Fig. 2 Mask layout of the InP PIC

The emission array has eight channels. To make the two controls, wavelength and phase, independent of each other equal path length has to be ensured for each channel, so additional bends are added between the SOA array and the emission array. The preamplifier SOA, the phase shifters and the SOAs in the SOA array have independent contact pads as seen in Fig. 2. The SOAs in the emission array are $500\mu\text{m}$ long and $2.7\mu\text{m}$ wide and are contacted together because they are narrowly spaced ($2.8\mu\text{m}$ gap). Deeply etched ridge waveguides are used to form all the waveguides in the PIC. The PIC has an overall size of about $2\text{mm} \times 6\text{mm}$. The waveguide core consists of ten compressively strained InGaAsP quantum wells with the emission peak around 1550nm and separate optical confinement layers [3]. Quantum well intermixing technique is employed to increase the bandgap of the quantum wells to 1450nm in the regions intended for passive waveguides [4]. The 2nd order gratings are etched into the upper optical confinement layer above the quantum wells. The Bragg wavelength is designed to be 1550nm . Because of quantum well intermixing and also the grating, regrowth of the P doped upper cladding layer and the contact layer is used to finish the whole wafer structure. The emission is through the InP substrate and through a window opened in the bottom N contact metal.

III. MEASUREMENT AND RESULTS

The output from an external tunable laser is fibre coupled into the input waveguide of the PIC and preamplified by the input SOA biased at 200mA , then split into eight equal channels. They then pass through the phase shifters and the SOAs and enter into the emission array and emit perpendicular

to the PIC. Although the SOAs in the SOA array have independent contacts, they are connected together and have current injected through a single source meter for the ease of these preliminary measurements. A total current of 800mA was injected into the SOA array. The emission array has a total current injection of 500mA. The phase shifters are individually controlled by source meters. The far field of the emission is monitored by an infrared imaging system which has the ability to resolve an angle range of $(\pm 17.5^\circ) \times (\pm 13.9^\circ)$ with the resolution of $\sim 0.1^\circ$. The current injection into each phase shifter was varied to maximize the side lobe suppression in the angle range from -10° to 10° through the Particle Swarm Optimization (PSO) algorithm [5]. The inset of Fig. 3 (a) shows the far field pattern for 1550nm captured by the infrared camera after the PSO optimization. The field distribution along the longitudinal and lateral direction across the peak is shown in Fig. 3(a). As expected, the beam is very narrow in the longitudinal direction because of the long emission length of the active grating while is broad in the lateral direction because the whole emission array is just about $40\mu\text{m}$ wide. The backside surface of the PIC is not polished, which causes scattering as seen from the inset. The peak position in the longitudinal direction versus wavelength is shown in Fig. 3(b). A slope of $5^\circ/40\text{nm}$ is in good agreement with the design. The emission angle for 1550nm is -2° which means that the effective index is overestimated by about 1.3% in the design. This level of overestimation is reasonable for active waveguides with current injections, where the injected carriers reduce the effective index.

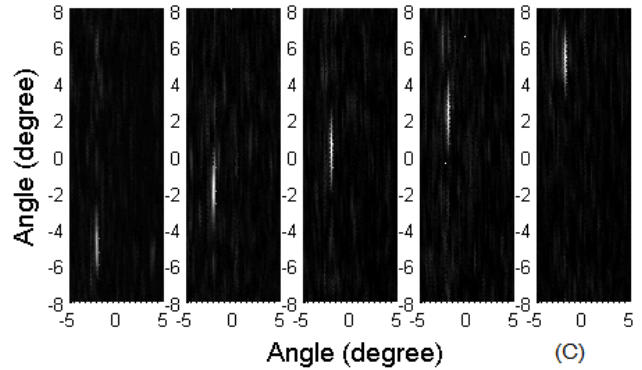
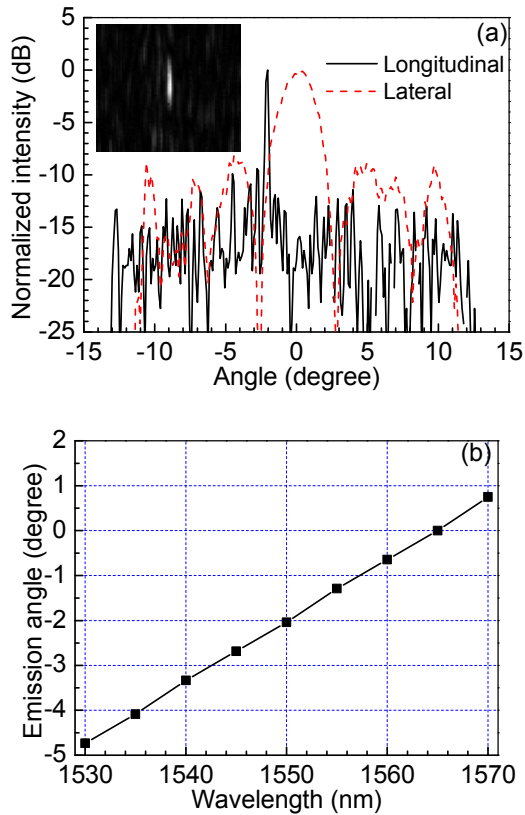


Fig. 3(a) Far field distribution in the longitudinal and lateral direction. The inset shows the picture captured by the camera. (b) Peak position in the longitudinal direction versus wavelength. (c) Beam steering with phase shifter current variations.

For each wavelength in the range from 1530 to 1570nm, the phase shifter currents can be varied to make the beam steer to any angle in the range from -5° to 5° in the lateral direction. Fig. 3(c) shows the result for the 1550nm wavelength steered to the angle of -5° , -2° , 0° , 2° and 5° .

IV. SUMMARY

Electronically controlled 2D optical beam steering has been demonstrated for the first time on a monolithically integrated active/passive InP PIC. Preliminary measurements demonstrated 5° longitudinal beam steering and 10° lateral beam steering by wavelength and phase tuning, respectively.

Acknowledgement

This work is supported by DARPA SWEEPER project.

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II. Fabrication and Component Development

Etched beam splitters in InP/InGaAsP

Erik J. Norberg,^{1,*} John S. Parker,¹ Steven C. Nicholes,² Byungchae Kim,¹
Uppiliappan Krishnamachari,¹ and Larry A. Coldren¹

¹Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA, USA

²Department of Materials, University of California, Santa Barbara, CA, USA

*norberg@ece.ucsb.edu

Abstract: An etched beam splitter (EBS) photonic coupler based on frustrated total internal reflection (FTIR) is designed, fabricated and characterized in the InP/InGaAsP material system. The EBS offers an ultra compact footprint (8x11 μm) and a complete range of bar/cross coupling ratio designs. A novel pre-etching process is developed to achieve sufficient depth of the etched coupling gaps. Fabricated EBS couplers demonstrate insertion loss between 1 and 2.6 dB with transmission (cross-coupling) \leq 10%. The results show excellent agreement with 3D finite-difference time-domain (FDTD) modeling. The coupling of EBS has weak wavelength dependence in the C-band, making it suitable for wavelength division multiplexing (WDM) or other wide bandwidth applications. Finally, the EBS is integrated with active semiconductor optical amplifier (SOA) and phase-modulator components; using a flattened ring resonator structure, a channelizing filter tunable in both amplitude and center frequency is demonstrated, as well as an EBS coupled ring laser.

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OCIS codes: (130.0130) Integrated optics; (230.1360) Beam splitters; (250.5300) Photonic integrated circuits; (230.5750) Resonators

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1. Introduction

The optical coupler is a key component for photonic integration. Desirably the coupler should have: low loss, variable bar/cross splitting ratio designs, a compact footprint and be easily integrated with other photonic components on-chip. Traditional coupler designs are the y-branch, multi-mode interference (MMI), and directional coupler. For many applications a small foot-print directly translates into higher performance; this includes: short optical delays for linear RF-receivers [1], large free-spectral range (FSR) of micro resonators used as add/drop filters in wavelength division multiplexing (WDM) applications [2], and high sensitivity for micro-rings used in biosensing [3]. The y-branch and MMI coupler is typically limited in compactness, where the smallest MMI coupler to date is 20 μm long, but also very sensitive to fabrication variations [4]. Thus, for compact integration, the directional couplers are most commonly utilized [2,5]. However, when the length of the direction coupler is decreased the coupling gap must be made extremely small in order to obtain any significant coupling. For lateral directional couplers this implies the use of electron beam lithography (EBL) and very small processing tolerances. While the coupling gap can be controlled precisely in vertical directional couplers, this design has the disadvantage of multiple waveguide stacks, thus demanding complicated fabrication often with additional material growths [6]. Ultimately, for compact coupler designs, the cross coupling of direction couplers is still limited to a few percent. On the contrary, the etched beam splitter (EBS) has been proposed and investigated as an ultra compact coupler that offers a complete range of power splitting ratios independent of size [7–10]. The EBS is the monolithic version of a conventional bulk prism beam splitter, with the coupling mechanism based on the same physical phenomena of evanescent coupling through frustrated total internal reflection (FTIR) [11]. The first EBS was realized over two decades ago [7], but with very limited success due to immature fabrication technology. More recently, the EBS has demonstrated better performance with silicon-on-insulator (SOI) [12], AlGaAs [13] and polymer based waveguide

platforms [8]. We have extended to the InP/InGaAsP material system in order to integrate the EBS coupler with an active gain platform [14,15]. Here, we report on the modeling, fabrication and characterization of such EBS couplers in InP/InGaAsP. Furthermore, taking advantage of the active gain and phase modulation provided by the InP/InGaAsP material system, we have integrated the EBS in a novel flattened ring resonator structure to create a channelizing filter tunable in both center wavelength and extinction ratio.

2. EBS design and modeling

The general design of the EBS is two intersecting waveguides with a narrow lower index gap at the crossing point, making it a symmetric 2x2 coupler, as shown in Fig. 1(a). For total internal reflection (TIR) to take place, the incident angle of the waveguides (Θ_i) needs to be greater than the critical angle (Θ_c). The power coupling across the EBS gap is facilitated by the evanescent wave present during TIR. In this work we used a 300 nm thick InGaAsP 1.3Q waveguide layer surrounded by InP cladding. For the lateral optical confinement we utilize air cladding by etching through the waveguide layer, as shown Fig. 1(c). For this waveguide design and using an air filled EBS gap, Θ_c is approx. 18° . The deeply etched waveguides provide strong lateral optical confinement and robust fabrication in any crystallographic direction due to the sole use of dry etching. For smaller resonator sizes with reduced ring radii, the strong optical confinement is crucial to avoid excess radiation loss from waveguide bends.

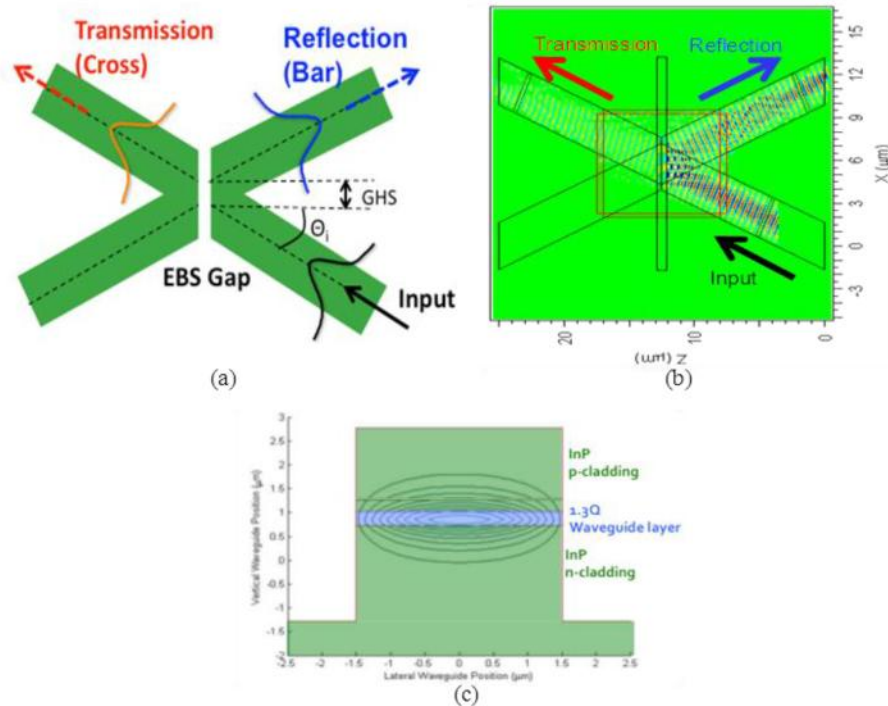


Fig. 1. (a) Schematic of the EBS coupler illustrating the basic design parameters, incident angle (Θ_i) of the input and output waveguides, EBS air gap for evanescent coupling and the Goos-Hanchen shift (GHS) between input and output waveguides. (b) FDTD simulation showing the magnetic field intensity $|H_y|$. (c) Deeply etched InP/InGaAsP waveguide, with the calculated fundamental mode superimposed.

Qualitatively the evanescent coupling behavior of the EBS can be described with a simple analytical plane-wave model derived from the Fresnel equations [10]. Quantitatively however,

this method is only valid in the limiting cases of very weakly guided modes, i.e. when the modal plane wave spectrum is narrow and can be approximated with a single plane wave. For integrated optics this is seldom the case, thus, a more rigorous approach is needed. So far, most predictions on EBS performance has been done using numerical 2D-FDTD simulations [8–10,14]. Some full 3D-FDTD treatment of EBS structure has recently been reported [12,13]. The trade-off in the 2D versus 3D treatment is the computational intensity in the full 3D case versus the fact that the 2D simulations do not account for any transverse effects, such as transverse modal diffraction or slanted EBS mirrors. Here, we make use of and compare the 2D- and 3D-FDTD simulations when designing InP/InGaAsP based EBS couplers. For the 2D-FDTD simulations, the effective index of the waveguide is calculated to be 3.24 using the effective index method, with the surrounding lateral cladding and the EBS air gap being 1. For the 2D simulations, a 10 nm mesh size was used with a time step of 2.3×10^{-17} s, while in the 3D simulations a slightly larger 20 nm mesh size with a 3.3×10^{-17} s time step was used, to reduce computation time. The 20 nm is still much smaller than the minimum feature size of the 300 nm EBS air gap. Hence, numerical errors from the mesh generation should be insignificant. Figure 1(c) shows the FDTD simulation with the evanescent coupling across the air gap.

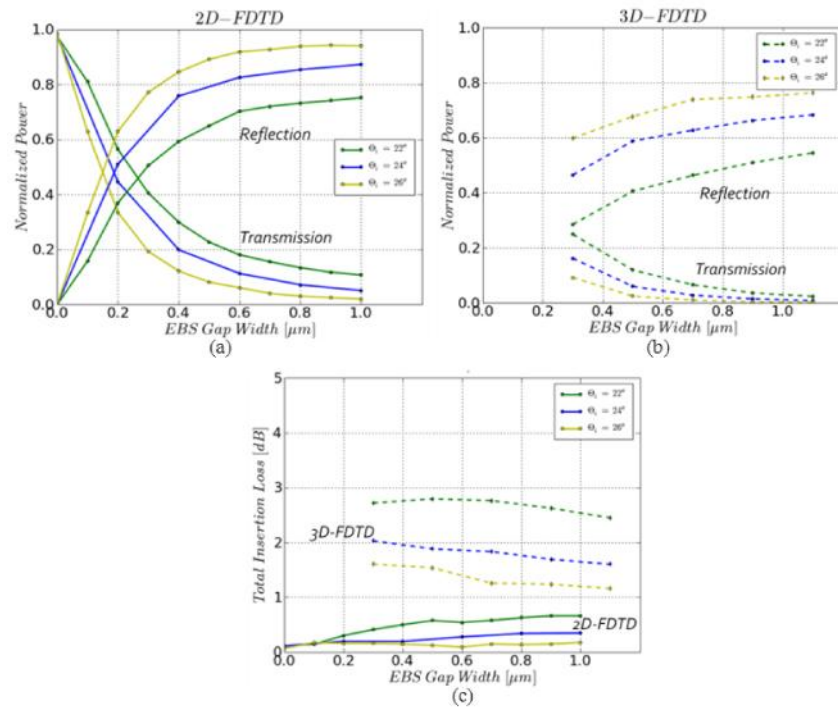


Fig. 2. Power coupling ratios as a function of EBS gap width for different incident angles (Θ_i), (a) 2D- and (b) 3D-FDTD simulations. (c) Total insertion loss of the EBS coupler as a function of gap width for different incident angles, 2D- (solid) and 3D-FDTD simulations (dashed).

The EBS power splitting for different incident angles and air gap widths are shown in Fig. 2(a,b). The trends for the 2D and 3D simulations are consistent; the reflection (bar) component is reduced in favor of a larger transmission (cross) component when the incident angle or gap width is decreased. This is also intuitively expected from the FTIR evanescent field behavior; i.e., the rate of exponential power decay in the EBS gap decreases as the incident angle approaches the critical angle, and a narrower gap corresponding to a shorter decay distance. The obvious discrepancy between the 2D and 3D simulations is seen in the absolute powers, in other words, the insertion loss, shown in Fig. 2(c). The 3D case indicates

a much more severe insertion loss compared to the 2D case. This discrepancy can be attributed to transverse modal effects, not accounted for in the 2D simulations. This includes the fact that for the relatively narrow transverse mode profile (i.e. wide transverse plane wave spectrum), as shown in Fig. 1(c), a part of the transverse mode does not obey TIR at the EBS gap. Also, for the transmitted (cross) component, transverse diffraction in the EBS gap results in additional loss. Thus, the insertion loss found in the 3D simulations is rather inherent to our InGaAsP waveguide design. Comparably, using a less confined waveguide mode, lower EBS insertion loss can be achieved [8,12]. The drawback of a wider transverse modal waveguide design lies in that it requires a deeper etched EBS gap, which in this work is the limiting factor of the fabrication process, as will be shown in the following section (EBS fabrication). While the 3D simulations will provide more reliable predictions about the absolute power coupling, the 2D-FDTD is still a good compliment when investigating effects in the lateral plane due to the much shorter simulation time. 2D simulations were thus utilized in optimizing the Goos-Hänchen shift (GHS) [16]. The GHS was accounted for by slightly displacing the reflected waveguide relative to the incident waveguide, as shown in Fig. 1(a). When designing the EBS coupling ratio we note that larger incident angles predict lower insertion loss, as shown in Fig. 2(c). This can be qualitatively explained by the modal profile, where a greater part of the lateral mode profile (or equivalent plane wave spectrum) will not experience the TIR when the waveguide incident angle approaches the critical angle. Also, with narrower incident angles, there is a greater portion of the transmission (cross) coupling component, which has inherently more loss compared to the reflection component, in the 3D versus 2D simulations. In order to maintain transmission (cross) coupling, the EBS gap must also be made narrower, which makes the fabrication more difficult. The narrower gaps suffer increasingly from fabrication imperfections, such as rough and sloped etch sidewalls and insufficient etch depth. Hence, there is a tradeoff between the simulated low insertion loss with larger incident angles and narrow gaps versus the insertion loss added from non-ideal fabrication. Here, we limited the inherent insertion loss to a maximum of ~2 dB by utilizing incident angles of 24° and 26°, 6° and 8° away from the critical angle respectively. The gap width was varied between 0.35 and 1.0 μm , with the narrowest gap limited by the fabrication process. The overall foot-print of the designed EBS coupler is 8x11 μm .

3. EBS fabrication

The main difficulty of realizing the proposed beam splitter lies in the definition and etching of the narrow high aspect ratio EBS gap with good quality. This implies no slanted or rough sidewalls and a sufficient etch depth that reaches through the waveguide layer. In addition, the fabrication complexity of the EBS should ideally be kept to a minimum to allow for easy integration with standard photonic integrated circuit (PIC) fabrication. For our deeply etched EBS coupler design, the EBS is simply patterned and etched together with all the other waveguide structures. This eliminates any alignment errors and adds minimal process steps. A standard i-line photolithographic process was used to pattern waveguides and all EBS gaps 400 nm and wider. However, due to this resolution limitation in our photolithographic capabilities the 350 nm EBS gaps were in this work defined using electron beam lithography (EBL). For the hard mask we use a bi-layer of 50 nm Cr on top of 500nm SiO₂. The EBL and photolithographic patterns are first etched separately into the Cr layer. The complete mask pattern is then transferred into the SiO₂, which acts as the hard mask for etching the semiconductor. In order to achieve anisotropic waveguides and EBS gaps, it is crucial that the SiO₂ hard mask has straight sidewalls, since any slope will subsequently transfer into the semiconductor due to mask degradation. We have developed a SF₆-Ar based inductively coupled plasma (ICP) etch that has good Cr to SiO₂ selectivity (30:1) and produces very straight SiO₂ sidewalls [17]. The ICP etching of InP/InGaAsP uses a Cl:H₂:Ar chemistry [17–19]. We have previously optimized conditions to yield very anisotropic and smooth deeply etched waveguides that demonstrate low propagation loss [20]. In order for the optical mode

to experience FTIR in the EBS coupler, the etch must reach through the transverse waveguide layer inside of the EBS gap. However, like most reactive ion etching (RIE), there is an aspect ratio dependent etch rate (ARDE) that limits the etch depth inside of the narrow EBS gap. At the same time, for device integration, the upper waveguide cladding thickness is restricted by the layer structure in active regions. A $\sim 1.6 \mu\text{m}$ cladding layer is necessary between the waveguide and the top InGaAs contact layer, to avoid absorption. Thus the etching of narrow and deep EBS gaps is especially difficult for active material integration platforms. In this work we solved this problem by implementing a novel pre-etching technique to counteract the ARDE effect of the EBS gaps. An area around the EBS coupler is etched prior to the waveguide and EBS patterning, decreasing the required etch depth of the EBS gaps, as shown in Fig. 3(a). The depth of this pre-etch is limited by two factors: first, the EBS and waveguides must be able to be patterned over the induced step height, and second, optical loss due to the change in optical mode profile at the interface must be avoided. Using a 950 nm thick photo-resist with contrast enhancer (SPR950CM with CEM365i) we found that the lithographic patterning is not compromised for step heights up to about 1 μm . Treating the waveguide discontinuity as a modal excitation problem, the interface loss is calculated to be small (-0.027 dB) for the 1.0 μm step. Still, in order to avoid detrimental back reflections, this interface is angled with respect to the propagation direction. The pre-etched region with successful patterning is demonstrated in Fig. 3(b). With this $\sim 0.9 \mu\text{m}$ pre-etch, a reduced etch depth of 1.55 μm inside the EBS gap is required, in order to reach 300 nm below the waveguide layer.

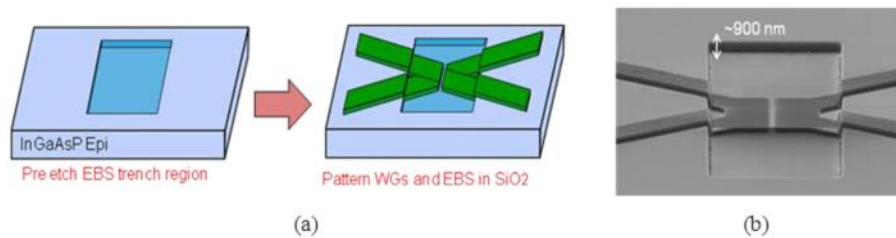


Fig. 3. (a) Schematic of pre-etching process. (b) Scanning electron microscopy (SEM) image of the hardmask illustrating the successful patterning over the pre-etched region.

The fabricated EBS coupler is shown in Fig. 4, the EBS gaps demonstrate smooth anisotropic sidewalls with a satisfactory etch depth even for the narrowest gaps. However, all EBS gaps are widened by about 70 nm in the ICP process. This is attributed to minor mask degradation together with a slow lateral etch rate.

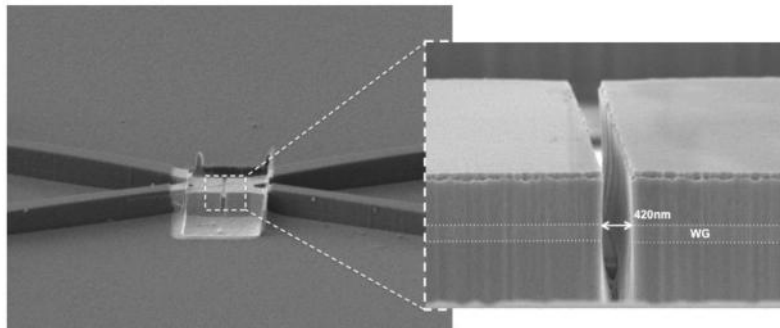


Fig. 4. SEM image of the EBS coupler. The lighter region shows where the SiN_x insulation layer was selectively removed to achieve a semiconductor-air interface in the EBS gap. The highlighted EBS gap demonstrates anisotropic and smooth sidewalls and a sufficient etch through the waveguide layer.

For integration of the EBS coupler with standard InP/InGaAsP PICs, there is only a single added process step, besides the pre-thinning process described above. The nitride layer used for isolating metal contacts from the substrate needs to be selectively removed inside of the EBS gap in order to achieve FTIR. This was done by using a 7 μm thick resist (SPR220-7) to cover deep waveguides and metal contacts. Then selectively opening a region around the EBS coupler and using a high pressure (300 torr) CF_4 plasma etch to isotropically remove SiN_x around and inside the EBS gap, see Fig. 4.

In this work we incorporated: active gain, phase modulation and low loss passive waveguides, by utilizing an active/passive InP/InGaAsP offset quantum wells (OQW) integration platform [21]. Passive waveguide sections and phase modulator regions are here defined by selectively etching away the quantum wells. This is followed by a single blanket re-growth to provide p-cladding everywhere.

3. EBS characterization

The EBS coupler was characterized using a symmetric 4-port test structure shown in Fig. 5. Each of the waveguide arms around the EBS incorporates a semiconductor optical amplifier (SOA), used as an on-chip detector. The absolute power transmission and reflection components and the overall insertion loss of the EBS coupler can be accurately determined by fiber coupling an external tunable laser source and measuring the photocurrents on-chip. The input SOA is first used to measure the input light intensity. This input SOA is then biased at transparency and the light transmitted and reflected in the EBS coupler is measured by the SOAs in each waveguide arm. Since all the SOAs are identical, the measurement becomes insensitive to the responsivity of the SOAs. However, a separate test structure was however used to determine the wavelength dependent transparency current of the SOAs. Because of the small transmission components for some of the EBS designs, a lock-in approach was utilized to enhance signal-to-noise ratio (SNR) and separate the signal from the DC diode leakage current in the SOAs ($\sim 10\mu\text{A}$). All measurements were done at room temperature and with TE-polarized light in order to interact with the compressively strained InGaAsP quantum wells [21]. Finally, to account for the passive waveguide sections around the EBS coupler, a 0.22 dB insertion loss was subtracted from the measured coupling powers. This number was determined from previous measurements of 2.1 cm^{-1} propagation loss in our deeply etched waveguides [20].

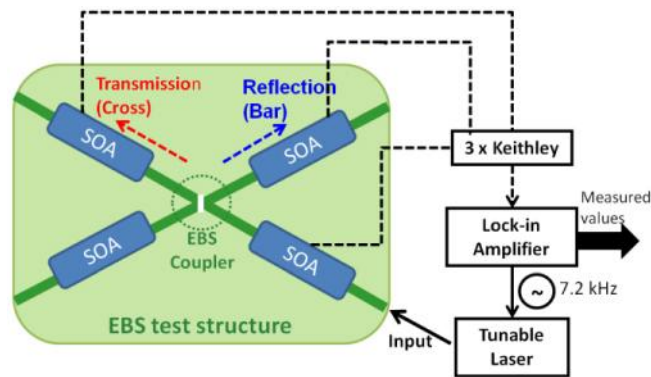


Fig. 5. Schematic of the test structure used for characterizing power coupling and insertion loss of the different EBS coupler designs. Lock-in at 7.2 kHz issued to improve sensitivity. On-chip SOAs are reversed biased to detect coupled light.

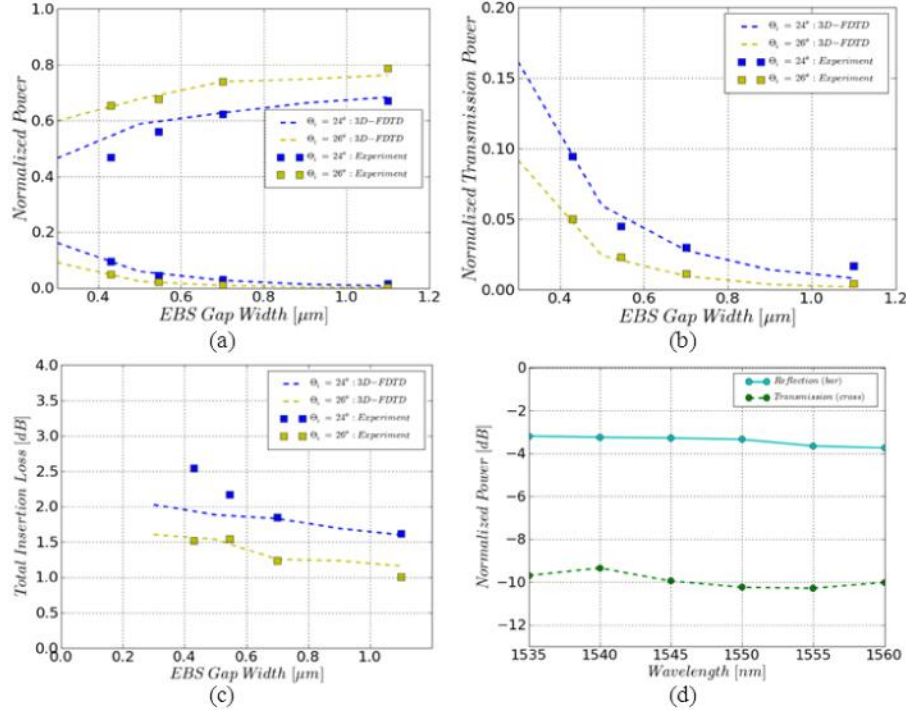


Fig. 6. (a),(b) EBS power coupling and (c) insertion loss as a function of gap width for incident angles (Θ_i) of 24° and 26° at 1550 nm, for measured EBS coupler designs (squares) and 3D-FDTD simulations (dashed lines). (d) Measured power coupling as a function of wavelength for the 80/20 (bar/cross) EBS design.

The experimentally measured coupling values and insertion loss of the EBS matches very well with the 3D-FDTD simulations, as demonstrated in Fig. 6(a,b,c). The largest transmission (cross) coupling design was the $\Theta_i = 24^\circ$ with 0.42 μm air gap, which demonstrates an relative bar/cross coupling ratio of 80/20 and an overall insertion loss of 2.6 dB. The lowest insertion loss coupler design was the $\Theta_i = 26^\circ$ with 1.1 μm air gap. This design demonstrates only 1.0 dB insertion loss, but has at the same time a very unequal bar/cross coupling ratio of 99.5/0.5. For WDM or other applications where a wide range of bandwidth is utilized, it is important that the coupling ratio and insertion loss does not change significantly with wavelength. We confirmed that the EBS coupler has a relatively weak wavelength dependence, as shown in Fig. 6(d). The reflection (bar) and transmission (cross) component for this 80/20 coupler varies only by <0.6 dB and <1.0 dB respectively over a 25 nm wavelength span in the C-band.

4. EBS couplers integrated with PICs

In order to further demonstrate the integration of the EBS coupler with the InP/InGaAsP integration platform, we designed and fabricated novel flattened ring resonator devices [13]. Figure 7 highlights the flattened ring design and how it offers a larger bending radius for a fixed resonator delay compared to a conventional circular design. An increased bending radius translates into a lower roundtrip loss, through reduced scattering and radiation loss. This becomes especially advantageous for micro-ring resonators where the bending radius needs to be very small. The resonator length (L) is defined by the incident angle (Θ_i) (in degrees) at the EBS coupler together with the bend radius (R) of the waveguides: $L = \Theta_i R \pi / 45$. The fabricated device in Fig. 7 utilizes the flattened ring resonator with a $\Theta_i = 24^\circ / 0.5 \mu\text{m}$ EBS coupler design and a bending radius of 500 μm , giving a resonator

circumference of 838 μm . The resonator incorporates a 375 μm SOA and two phase modulators (PM). In addition to the flattened resonator, the device also includes a Mach-Zehnder interferometer (MZI). Such a device could be used as the basic building block for higher order lattice filters [22].

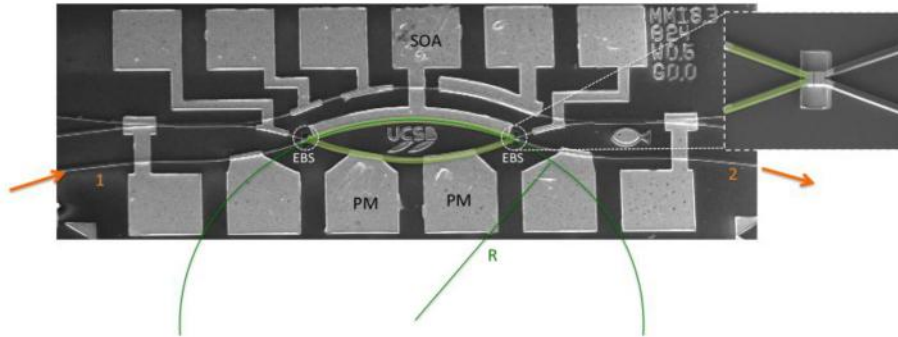


Fig. 7. SEM image of a PIC filter device that utilize the flattened ring resonator design with EBS couplers. Highlighted waveguides shows the flattened ring and illustrates the reduction in resonator length versus a circular resonator design. Port 1 and 2 shows the input and output waveguide filter responses.

Here we use the single resonator to demonstrate a tunable channelizing filter device. The filter function is measured by sweeping the wavelength of an external tunable laser and locking in the signal using an on-chip reversed biased phase modulator after the resonator. Figure 8 shows the measured filter responses. Adjusting the current to the SOA the pole-magnitude (G) of the filter response is tuned, this is demonstrated in Fig. 8(a) for $G=0.5$ and 0.75 for SOA biases of 15 and 20 mA respectively. The filter function fits well with the theoretical S_{21} parameter of an ideal resonator shown in the inset of Fig. 8(a). By utilizing the phase modulators, the filter can easily be shifted in wavelength, as verified in Fig. 8(b). Hence, using the SOA and PMs together the resonator poles can be placed anywhere in the complex plane. This demonstrates the basis of a very versatile channelizing filter. For better stopband rejections and flat-topped passbands, several stages should be cascaded to produce higher order filters [22]. For this application, the small cross-coupling provided by the EBS is ideal, as it allows for high finesse filters with large stopband rejections [23]

The flattened ring resonator can naturally also works as a laser if the SOA is biased at higher currents. The CW threshold for this device is 23 mA with single mode lasing and a side mode suppression ratio (SMSR) of ~ 32 dB demonstrated in Fig. 9.

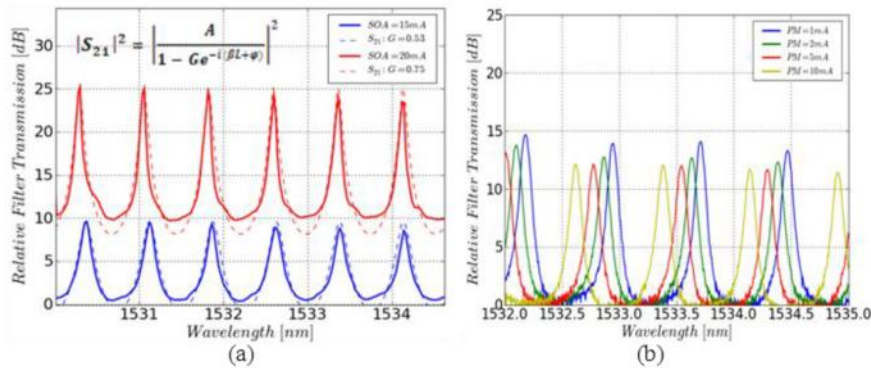


Fig. 8. Measured filter responses of the flattened ring resonator. (a) Tuning of pole-magnitude (G) by changing bias on the SOA (solid), with ideal simulated S_{21} filter function superimposed (dashed). (b) Tuning of the filter center frequency by current injection in the phase modulators (PM).

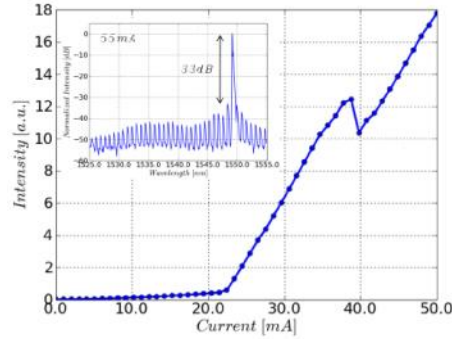


Fig. 9. Light-current characteristic of the flattened ring resonator demonstrating onset of lasing at ~23 mA, inset shows the lasing spectrum at 55mA, single mode operation with ~32 dB of SMSR.

5. Conclusion

We have reported on the design, integration and characterization of etched beam splitter (EBS) couplers in the InP/InGaAsP material system. For the design, 2D- and 3D-FDTD simulations were investigated and compared. It was concluded that the 2D case is useful for predicting trends although inaccurately predicting low insertion loss due to the ignoring of the transverse modal effects. EBS couplers with relatively low transmission components ($\leq 10\%$) were preferred in order to limit inherent insertion loss (incident angles $\geq 24^\circ$) and provide realistic fabrication (EBS gaps $\geq 0.35 \mu\text{m}$). Using a novel pre-thinning process and optimized ICP etching conditions for the InP/InGaAsP material system, EBS couplers were successfully realized. We note that the EBS does not add significant fabrication complexity to standard InP/InGaAsP PIC fabrication, grating EBL can be avoided. The EBS couplers were characterized using a robust test structure utilizing on-chip detectors, thus, eliminating any uncertainty in fiber-coupling. Measured power coupling ratios showed very close agreement with 3D-FDTD simulations. EBS couplers with transmission (cross) and reflection (bar) components of 0.5-10% and 44-80% respectively, were demonstrated. The foot-print of the coupler is $8 \times 11 \mu\text{m}$. Such couplers are useful for applications requiring compact foot-print and relatively large bar/cross coupling ratios including, low threshold ring lasers, and coupled ring filters, where in order to achieve a narrow passband the inter-ring coupling must be small. In this work we utilized the EBS coupler in a novel flattened ring resonator geometry. This resonator design offers an increased bending radius for a given resonator circumference, compared to conventional circular resonators; this translates into a lower bending loss. Utilizing the active gain and phase modulation offered by the InP/InGaAsP material system, a tunable channelizing filter as well as a ring laser was demonstrated.

Acknowledgements

This work was supported by DARPA under the PhASER program, a portion of this work was done in the UCSB nanofabrication facility, part of the NSF funded NNIN network.

High verticality InP/InGaAsP etching in Cl₂/H₂/Ar inductively coupled plasma for photonic integrated circuits

John S. Parker,^{a)} Erik J. Norberg, Robert S. Guzzon,
Steven C. Nicholes, and Larry A. Coldren

Department of Electrical and Computer Engineering, University of California, Santa Barbara,
California 93106

(Received 1 September 2010; accepted 3 November 2010; published 5 January 2011)

High verticality and reduced sidewall deterioration of InP/InGaAsP in Cl₂/H₂/Ar inductively coupled plasma etching is demonstrated for a hydrogen dominant gas mixture. Selectivity >20:1, an etch rate of 24 nm/s, and a sidewall slope angle of >89° have been measured for etch depths >7 μm. The Ar flow is minimized to reduce surface etch damage while increased Cl₂ and H₂ gas flow is shown to increase etch rate and selectivity. The high chamber pressure required for plasma ignition causes isotropic etching at the start and creates an undercut beneath the masking layer. A novel ignition scheme using a hydrogen gas “flood” is suggested and results are presented. © 2011 American Vacuum Society. [DOI: 10.1116/1.3522659]

I. INTRODUCTION

In photonics, deeply etched waveguides provide high confinement to the optical mode allowing for tight bends with low radiation losses. Dry etching can achieve such high-aspect ratio structures in InP/InGaAs,^{1,2} InP/InGaAlAs,¹ and InP/InGaAsP² with vertical sidewalls and minimal discontinuities between the various layers. These structures can be made with a single etch-step and typical etch rates >20 nm/s.³ Recently, an 8×8 monolithic tunable router with more than 200 functional elements has been demonstrated, which combined deeply etched, surface ridge, and buried rib waveguides.⁴ As future applications continue to increase the number of components on photonic integrated circuits (PICs), the component size will need to be further reduced and more of them will rely upon the deeply etched platform to achieve compact structures with tight bends.

To realize high yield on large PICs, the dry-etch process must produce uniform and vertical structures to ensure that waveguide and component widths are conserved from the lithography, which is critical to minimize insertion loss. One functional element that is highly sensitive to waveguide width variations is the four-port restricted multimode interference (MMI) coupler⁵ used heavily for integrated power splitters, combiners, and Mach-Zehnder interferometers (MZIs). For example, from three-dimensional beam propagation method (BPM) simulations using Rsoft BEAMPROP software, the acceptable width tolerance is <120 nm to achieve <1 dB insertion loss on a typical 8.1 μm wide, 100 μm long, restricted MMI as shown in Fig. 1. This requires a sidewall slope angle >88.6° to match the average waveguide width to the mask dimensions within 120 nm, assuming the middle of the waveguide is 2.5 μm below the mask layer (300 nm height waveguide, 1.8 μm p-InP cladding, 150 nm contact layer, and 400 nm InP cap). If reproducible coupling and low insertion loss cannot be obtained in MMI couplers,

the extinction ratio in Mach-Zehnder interferometers will be decreased, and the performance of MZI modulators and balanced detectors will be degraded.

As an additional requirement, the sidewall surface of the waveguide must be smooth to reduce scattering losses that have significant effect for tight bending radii <100 μm. A variety of photonic components have been previously demonstrated with a deeply etched process including ring resonators,⁶ slot couplers,⁷ MMI couplers,⁸ distributed Bragg reflector gratings,⁹ and photonic crystals.¹⁰

Inductively coupled plasma (ICP) reactive ion etching (RIE) has become widespread for etching InP based structures. Elevated electrode temperatures (>150 °C) are commonly used to increase the volatility of the InCl_x byproducts and reduce micromasking.¹¹ Etching with only Cl₂ gas has been shown to produce smooth sidewalls with selectivity of 20:1 for a SiN_x or SiO₂ mask.⁹ While Berg and Pang¹² has shown a much higher selectivity for InP of >300:1 using a less common Ti/Ni mask, their feature sizes and etch depths were relatively large (i.e., >10 and >69 μm, respectively), and their process required long etch times of 110 min. However, the Cl₂ chemistry generally suffers from a large undercut or slow anisotropic etch rates.² Dry-etch Cl₂-based chemistries with additive gas including Cl₂/Ar,^{2,13} Cl₂/H₂,^{3,14–16} Cl₂/H₂/Ar,^{2,9–11,17,18} Cl₂/O₂,¹⁹ Cl₂/N₂,^{20,21} and Cl₂/BCl₃/N₂,²² have been studied previously to improve anisotropy and etch rate.

Adding Ar to the Cl₂ based chemistry benefits etch anisotropy due to an increased physical etch component from Ar ion bombardment. Gatilova *et al.*¹⁴ and Bouchoule *et al.*¹⁵ showed that when using a Si carrier with Cl₂-based chemistry, a SiO_x passivation layer forms on the semiconductor sidewall and is enhanced by H₂ gas, further improving anisotropic etching. Selectivity of 30:1 has been found etching with Cl₂/H₂ chemistry,³ while Cl₂/H₂/Ar selectivity remains around 14:1 using a SiO₂ mask.⁹ The downside of Cl₂/H₂ etching is that good verticality has only been demonstrated for chamber pressures ≤1 mT,³ which is not available on all

^{a)}Electronic mail: jparker@ece.ucsb.edu

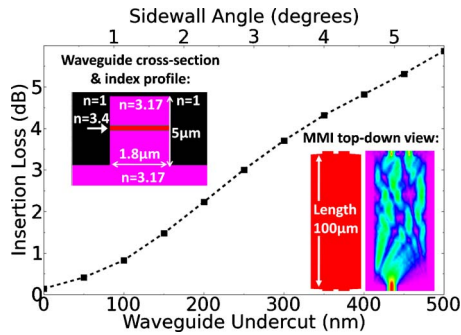


FIG. 1. (Color online) Rsoft BPM simulation of MMI coupler insertion loss vs waveguide undercut due to nonvertical etching. The reduction of the waveguide width greatly increases the insertion loss. The restricted MMI design is $100\ \mu\text{m}$ in length and has an optimal width of $8.1\ \mu\text{m}$ for $1.8\ \mu\text{m}$ input waveguides.

systems, while $\text{Cl}_2/\text{H}_2/\text{Ar}$ provides anisotropic etches at pressures as high as 4 mTorr with a greater process tolerance.^{9–11} In studies with other additive gas besides Ar or H_2 , Cl_2/O_2 based chemistry shows higher verticality than with only Cl_2 due to O_2 surface passivation. Selectivity of $>13:1$ was observed with a SiN_x mask; however, micro-masking at high O_2 ratios remains a limitation of this chemistry.¹⁹ In etch studies on high-aspect ratio holes for photonic crystals, N_2 is commonly used as a passivation gas added to Cl_2 based chemistry providing higher verticality and reduced sidewall deterioration.^{20,21} BCl_3 has been reported to form more reactive chlorine ions than Cl_2 , and the investigation of BCl_3 added to the Cl_2/N_2 based chemistry has shown a further improved verticality while causing increased sidewall roughness.²² Selectivity for Cl_2/N_2 based chemistry with a SiN_x mask is reported to be quite low compared to other chemistries at $>8:1$.^{20–22} However, these measurements are taken on photonic crystals, which have a large RIE lag effect reducing the InP etch rate in small sub-micrometer features, and therefore this etch selectivity cannot be directly compared to etches on waveguides or electronic components.

Starting from previous work by Rommel *et al.*² using 2/2.5/3 SCCM (SCCM denotes cubic centimeter per minute at STP) ($\text{Cl}_2/\text{H}_2/\text{Ar}$) and Docter *et al.*⁹ using 7/11/4 SCCM ($\text{Cl}_2/\text{H}_2/\text{Ar}$), we show that a higher H_2 gas ratio improves verticality, and that increased total gas flow improves selectivity and etch rates while maintaining extremely vertical sidewalls. One predominant form of etching damage observed for Cl_2/H_2 based chemistry is an undercut notch directly beneath the mask layer.¹ In functional InP/InGaAsP PICs, the undercut notch can damage the contact layer, typically InGaAs, which is near the top of the layer stack and close to the etch mask. Extensive plasma damage to the contact layer can produce surface traps and an increased contact resistance. In this article, we present an optimized high gas flow recipe for $\text{Cl}_2/\text{H}_2/\text{Ar}$ ICP that has the highest selectivity, etch rates, and verticality yet reported. In addition, we demonstrate that a hydrogen gas “flood” can reduce the undercut notch, and that compensation of total etch area is necessary when etching small InP pieces.

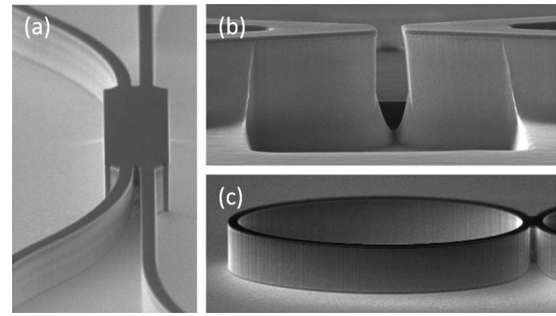


FIG. 2. SEM images of various dry etched photonic components including (a) multimode interference coupler, (b) etched beam splitter coupler, and (c) ring resonator with a compact two-mode coupler.

II. EXPERIMENTAL SET UP

Etching studies were performed on InP:S wafers with a metalorganic chemical vapor deposition grown 350 nm thick 1.4Q InGaAsP waveguide, seven InGaAsP quantum wells and barriers, and an InGaAs:Zn contact layer. A three-level mask is used to define the deeply etched photonic patterns that include the following: 550 nm of plasma-enhanced chemical vapor deposition SiO_2 on the InP/InGaAsP sample, followed by 50 nm Cr, and 900 nm photoresist (PR) SPR955CM-0.9 defined by stepper lithography. The Cr is etched in a Panasonic E640 ICP with a nonheated low power Cl_2 based recipe with a PR-to-Cr selectivity of 1:1. The PR is removed and the SiO_2 mask is defined in the Panasonic E640 ICP with a nonheated low power SF_6 -based dry-etch recipe with SiO_2 -to-Cr selectivity of 30:1. The Cr mask is removed by repeating the same low power Cl_2 based Cr etch recipe. No InP damage was observed in scanning electron microscope (SEM) images after this etch. The resulting SiO_2 mask is nearly vertical ($\sim 86^\circ$ sidewall slope) compared to a typical SiO_2 masked etched with CHF_3 chemistry ($\sim 66^\circ$ sidewall slope). The more vertical mask profile reduces InP sidewall deterioration during the etch, which is common on sloped mask profiles as the tapered edges of the mask layer break down.

The InP etching was done in a Unaxis Versalock (VLR) ICP RIE chamber with a $200\ ^\circ\text{C}$ heated chuck and backside He cooling to regulate the temperature. Samples are loaded on a 4 in. Si carrier wafer that is necessary to avoid micromasking¹¹ and to develop the SiO_x passivation layer needed for anisotropic etching;¹⁵ no thermal grease is used to adhere the samples to the carrier. Figure 2 shows several InP components deeply etched on this tool including the following: a ring resonator with a compact two-mode coupler, a MMI coupler, and a slot coupler. During the fabrication of these components, we found high etch rates and smooth sidewalls around 800–850 W ICP/125 W RIE, and we used these power conditions for this gas flow study. A series of tests was conducted on $\sim 1\ \text{cm}^2$ InP/InGaAsP pieces cleaved from two larger samples (sample A used for 850 W ICP experiments and sample B for 800 W ICP experiments). In order to avoid edge effects and improve the etch uniformity across the sample, InP pieces with a total area of $4\ \text{cm}^2$ (i.e.,

TABLE I. H₂ and Cl₂ gas flow variations at 800 and 850 W ICP power. All etches done on 1 cm² InP/InGaAsP sample with 4 cm² chamber loading and 300 min etch time. Sidewall angle measurements taken at the maximum waveguide undercut.

| ICP/RIE (W) | Gas flows (SCCM) | | | | Cl ₂ /H ₂ (%) | Etch rate (nm/s) | Selectivity (InP:SiO ₂) | Sidewall |
|----------------|---------------------|-----------------|----------------|----|--|---------------------|--|--------------------------------|
| | Total | Cl ₂ | H ₂ | Ar | | | | Angle off Vertical (deg) |
| 800/125 | 30 | 7 | 21 | 2 | 33 | 19 | 16 | 0.4–0.7 |
| 800/125 | 30 | 8 | 20 | 2 | 40 | 20.5 | 18 | 0.5–0.8 |
| 800/125 | 30 | 9 | 19 | 2 | 47 | 24 | 20.5 | 0.5–0.8 |
| 800/125 | 29 | 9 | 18 | 2 | 50 | 22.5 | 19 | 0.4–0.7 |
| 800/125 | 27 | 10 | 15 | 2 | 67 | 21.5 | 18 | 0.4–0.7 |
| 850/125 | 21 | 4.75 | 14.25 | 2 | 33 | 18 | 16 | 1–1.3 |
| 850/125 | 21 | 6.3 | 12.6 | 2 | 50 | 17 | 15 | 3–3.3 |
| 850/125 | 29 | 9 | 18 | 2 | 50 | 21.5 | 18.5 | 0.8–1.1 |
| 850/125 | 40 | 12.6 | 25.2 | 2 | 50 | 27 | 23 | 0.9–1.2 |
| 850/125 | 78 | 25.2 | 50.4 | 2 | 50 | 39 | 24 | ~33 ^a |
| 850/125 | 21 | 7.6 | 11.4 | 2 | 67 | 20 | 17 | 4.5–4.8 |

^aFeatures greatly undercut and damaged due to high chamber pressure. Angle measurement was made at the upper undercut.

“chamber loading” samples) are placed evenly around the sample and are reused for each 300 min etch test.

III. RESULTS AND DISCUSSION

A. Etch rates, selectivity, and verticality

The most optimal etch conditions were found to be 800 W ICP, 125 W RIE with gas flows of 9 SCCM Cl₂, 19 SCCM H₂, and 2 SCCM Ar for a chamber pressure of 1.5 mTorr. Table I shows the results of the gas composition study for the 850 W ICP and 800 W ICP tests. SEM images of the corresponding waveguide cross-sections are shown in Figs. 3 and 4. As listed in Table I, the reduction in ICP power from 850 to 800 W shows only a minor improvement in the verticality, which is already >89° for the 9/18/2 (Cl₂/H₂/Ar) test at 850/125 W (ICP/RIE). The 2 SCCM Ar flow used in all of the experiments was found to be necessary for creating stable plasma ignition; increased Ar ratio in the gas chemistry results in reduced selectivity and deeper vertical striations on the sidewalls due to the increased physical etch caused by Ar ion bombardment. The optimal H₂ gas fraction found on the Unaxis VLR for vertical sidewalls is 62%–66% of the total flow, which is a different operating regime than previously studied by Rommel *et al.*² using 23%–33% H₂ on a PlasmaTherm SLR 770 and Docter *et al.*⁹ using 50% H₂ on an Oxford Plasma Technology 100, indicating that the ideal gas ratios are reactor specific. This is further supported by the different dc-bias voltages used by Rommel (–215 V), Docter (–150 to –420 V), and in this study (–115 V at 800 W ICP and –111 V at 850 W ICP). For a fixed distance between electrodes, a higher dc-bias produces a greater electric field causing ions to reach a higher velocity. Thus, at lower dc-biases, etching becomes more chemically dependent as physical bombardment is reduced.

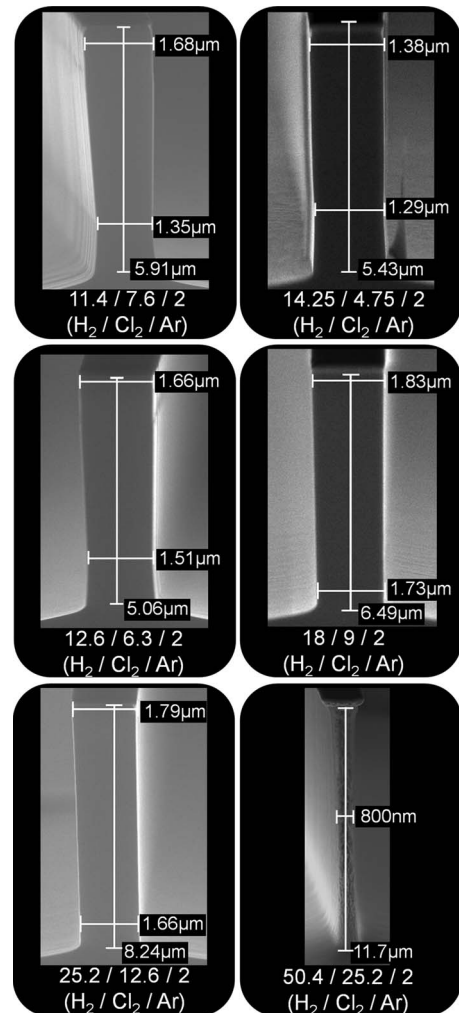


FIG. 3. SEM images of waveguide cross-sections for etch gas composition variations at 850/125 W (ICP/RIE).

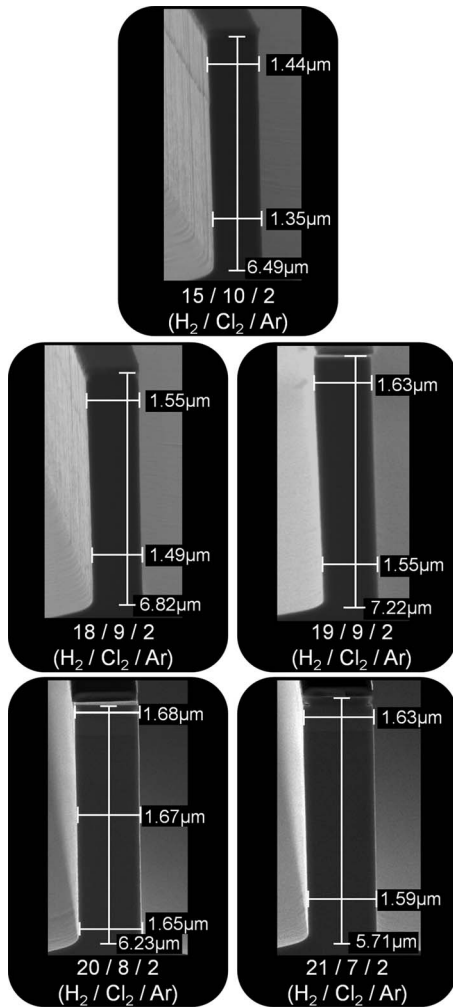


FIG. 4. SEM images of waveguide cross-sections for etch gas composition variations at 800/125 W (ICP/RIE).

Higher Cl₂/H₂ gas flow is found to increase etch rate and improve selectivity as shown in Table I. For 850/125 W (ICP/RIE) with 6.3/12.6/2 SCCM (Cl₂/H₂/Ar), the etch rate is 17 nm/s and selectivity of 15:1, whereas at double the hydrogen and chlorine 12.6/25.2/2 SCCM (Cl₂/H₂/Ar), the etch rate has increased to 27 nm/s and selectivity to 23:1. However, above 30 SCCM total gas flow, the pump on our system cannot maintain the 1.5 mTorr set-point. This occurs in the run 12.6/25.2/2 SCCM (Cl₂/H₂/Ar) in which the chamber pressure is set at 1.5 mTorr, but the turbo-vacuum maintained \sim 2 mTorr during the etch. Even with this chamber pressure increase, the sidewall verticality was still quite good indicating that 2 mTorr is still a sufficiently low pressure for vertical etching. Eventually, the verticality is reduced as increased gas flow causes the chamber pressure to rise above 2 mTorr. For instance, with 25.2/50.4/2 SCCM (Cl₂/H₂/Ar), the chamber pressure rose to \sim 6 mTorr during the etch and significant undercut occurred causing the thin 12 μm tall waveguide to break in many places. All systems will have an upper limit to their selectivity and total

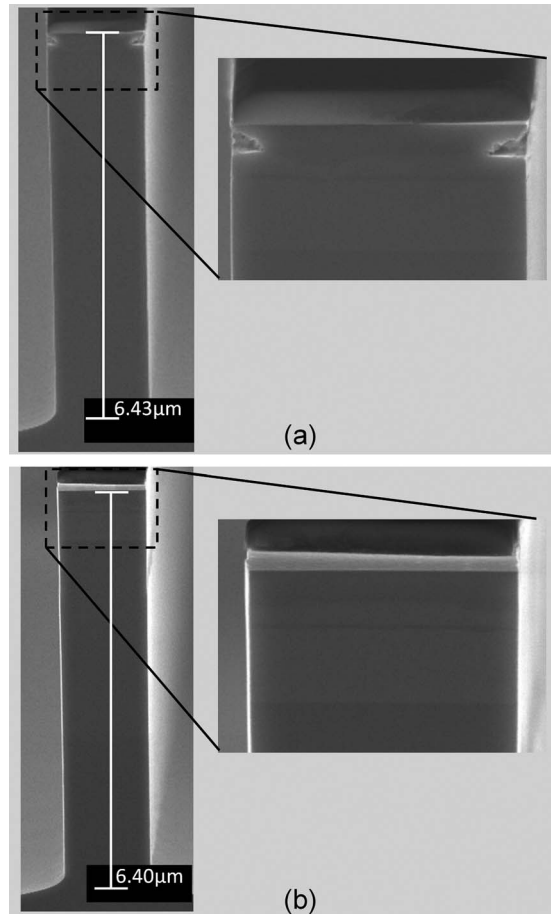


FIG. 5. SEM images of the waveguide cross-section (a) with the standard high pressure ignition process causing isotropic etching, and (b) with the improved ignition process using a hydrogen gas flood before ignition to passivate the InP and followed by hydrogen gas reduction after ignition to speed up the transition to low chamber pressure.

etch rate determined by the pump. In this series of experiments, sidewall slopes $>89^\circ$ were obtained only for pressures \leq 2 mTorr during the etch.

B. Reduction of sidewall damage

An undercut notch >100 nm deep is visible directly below the SiO₂ mask in Fig. 5(a), which has appeared in most of our etches regardless of chemistry and has been found in other InP etch studies.¹ This undercut notch is especially troublesome as most active InP devices have a *p*-contact layer beneath the mask which would be damaged by such a notch. The notch is caused by the inability of the vacuum system to open the throttle-valve and reduce the chamber pressure rapidly after the high pressure ignition at 20 mTorr and 500/15 W (ICP/RIE). High pressure ignition above 10 mTorr is common on ICP systems. While additional rf electrodes, magnetic fields, and ultraviolet ion excitation could improve ignition at lower pressure, these capabilities are rarely found in ICP tools. At such high ignition pressures, the etch is isotropic and etches underneath the mask during the 10–20 s, the vacuum controller takes to stabilize the pressure

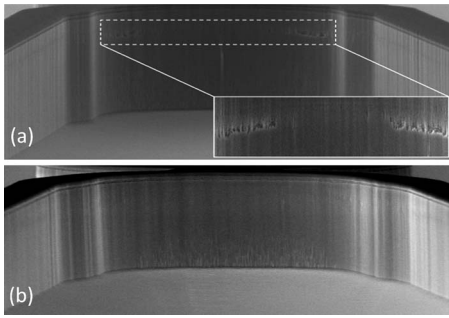


FIG. 6. SEM image of (a) sidewall pitting on small etch area of $\sim 5 \text{ cm}^2$ and (b) smooth sidewalls without pitting after 4 cm^2 of added chamber loading.

below 2 mTorr for high verticality anisotropic etching. The notch is further enhanced without the protective SiO_x passivation layer at the etch start.

In order to address the notch, we start the Cl_2 and H_2 flows at 4/20 SCCM, respectively. This “hydrogen flood” causes the turbovac throttle-valve to open, and after ignition, the high-hydrogen ratio helps to promote the formation of the SiO_x passivation layer.¹⁴ After ignition occurs, the hydrogen gas flow is reduced to 8 SCCM, which helps the chamber pressure to drop rapidly to 1.5 mTorr for anisotropic etching. Once the pressure is stabilized at 1.5 mTorr, a gas ramp brings the Cl_2 and H_2 flows up to 9/19 SCCM over 20 s while maintaining their flow ratio. An etched sample with the modified gas ignition steps shows no notch as seen in Fig. 5(b).

Pitting defects have also been observed on various features on small etch samples with area $< 5 \text{ cm}^2$. These defects contribute to scattering loss and occur often on waveguide bends with very small radii. The cause of this pitting is unknown, but might be due to localized build-up of excess gas reactants. Since the samples being etched are much smaller than the Si carrier wafer, nonuniform gas concentrations may be formed over the sample. Increasing the etch area with the addition of chamber loading pieces was found to alleviate the occurrence of pitting. Figure 6(a) shows waveguide pitting in small bending radius structures for initial test etches with an area $\sim 5 \text{ cm}^2$. Chamber loading samples were added in $\sim 2 \text{ cm}^2$ increments until pitting was no longer observed. This occurred with $\sim 9 \text{ cm}^2$ of total etch area as shown in Fig. 6(b).

IV. CONCLUSION

The etch verticality was improved by optimizing the gas ratios for 800–850 W ICP power. For maximum selectivity and etch rate, the total Cl_2 and H_2 gas flow should be set as high as possible for a given ratio while maintaining a constant chamber pressure ≤ 2 mTorr. The Ar flow should be set as low as possible while maintaining stable plasma conditions. The optimal flows of 9/19/2 SCCM ($\text{Cl}_2/\text{H}_2/\text{Ar}$) produced selectivity $> 20:1$, an etch rate of 24 nm/s, and a sidewall angle of 89.2° – 89.5° . High pressure conditions at plasma ignition often result in a notch beneath the etch mask.

Plasma ignition using a hydrogen flood scheme was shown to prevent these undercut notches. Pitting of the InP/InGaAsP sidewalls has been observed when etching small pieces with area $\leq 5 \text{ cm}^2$ and can be corrected by adding chamber loading samples to increase the amount of etched material in the chamber.

ACKNOWLEDGMENTS

The authors wish to thank Demis John for assistance with the SF_6 etch of SiO_2 . This work was supported by the Office of Naval Research. A portion of this work was done in the UCSB nanofabrication facility, part of the NSF funded NNIN network.

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InP/InGaAsP-Based Integrated 3-dB Trench Couplers for Ultra-Compact Coherent Receivers

Uppiliappan Krishnamachari, Sasa Ristic, Chin-Hui Chen, Leif Johansson, Anand Ramaswamy, Jonathan Klamkin, Erik Norberg, John E. Bowers, *Fellow, IEEE*, and Larry A. Coldren, *Fellow, IEEE*

Abstract—We present the design, fabrication, and test results for ultra-compact 3-dB frustrated total internal reflection-based trench couplers in an InP/InGaAsP monolithic integration platform. The trench coupler is integrated with phase modulators and a balanced photodiode (BPD) pair to enable a 180°-hybrid ultra-compact coherent receiver. Several trench splitter designs exhibit near 3-dB splitting with a loss of ~3 dB. The BPD pair is used to characterize coherent mixing of two input optical signals into the trench splitter, and coherence efficiency of 75% is achieved.

Index Terms—Beam splitter, coherent mixing, etched slot, frustrated total internal reflection (FTIR), 3-dB coupler, trench.

I. INTRODUCTION

WAVEGUIDE couplers are important components in the realization of compact, integrated optical circuits due to their ability to split the light beam or change its direction in a short distance [1]. A compact optical mixing element is required to minimize the footprint and optical path length. The most commonly used beam splitter for photonic integrated circuits is the multimode interference (MMI) coupler, and although recent advances in MMI design have yielded lengths as short as 50 μm , the devices are still limited in geometry due to radiation loss suffered in sharp bends [2]. In contrast, an etched trench that cuts the optical waveguide can perform 3-dB splitting within a submicrometer length. This is achieved by using the trench as a frustrated total internal reflection (FTIR) mirror, where the angle of the input waveguide incident on the trench is greater than the critical angle [3]. In a process analogous to quantum mechanical tunneling, the incident wave creates an evanescent field that penetrates into the lower index medium of the trench. If the gap width is small enough, this evanescent wave can couple across the gap to the waveguide on the other side and form the transmitted wave. The reflected wave still behaves as a totally internally reflected wave, exhibiting a small lateral Goos–Hanchen shift from the incident wave. The reflected and transmitted waves are complementary, behaving

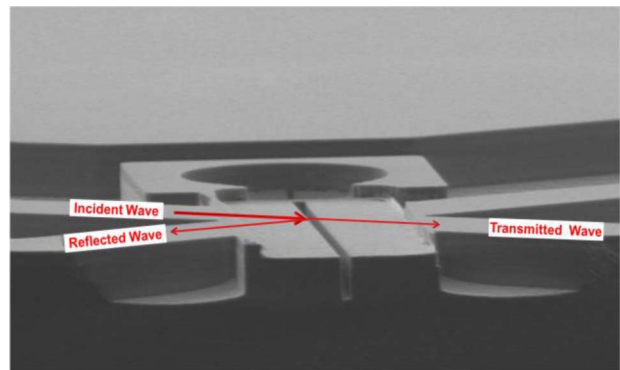


Fig. 1. SEM image of trench coupler illustrating reflection and transmission of a wave incident on the trench coupler.

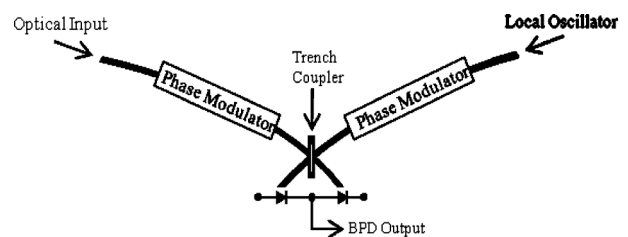


Fig. 2. Schematic of trench splitter-based coherent receiver.

as a 180° hybrid [4]. The splitting of the incident wave into reflected and transmitted signals is shown in Fig. 1.

The theoretical framework for an FTIR based 3-dB coupler design has been explained elsewhere [5]. Demonstration of FTIR trench beam splitters has been reported in both AlGaAs and InGaAsP material systems [6], [7]. In this letter we present a coherent receiver structure with a trench beam splitter integrated with phase modulators and a balanced uni-traveling-carrier photodiode (UTC-PD) for use in an ultra-compact coherent optical receiver with feedback [8]. A schematic of the coherent receiver can be seen in Fig. 2.

II. DESIGN AND SIMULATION

In this design, we use benzocyclobutene (BCB) with a refractive index of 1.57 to fill the trench. With a calculated effective index of 3.265 for the InGaAsP optical waveguide, the critical angle for the semiconductor/BCB interface is 28.5°. We fabricated waveguides with values of crossing angle, θ , that range from 27°–32° to account for any error in the index of the semiconductor or the BCB. Two-dimensional finite-difference time-domain (FDTD) simulations were carried out for each of these angles in order to find the gap width corresponding to

Manuscript received August 30, 2010; revised October 27, 2010; accepted November 27, 2010. Date of publication December 17, 2010; date of current version February 24, 2011.

The authors are with the University of California, Santa Barbara Engineering Science Building, Electrical and Computer Engineering, Santa Barbara, CA 93106-9560 USA (e-mail: ukrishna@ece.ucsb.edu; ristic@ece.ucsb.edu; janet@ece.ucsb.edu; leif@ece.ucsb.edu; anand@ece.ucsb.edu; klamkin@engineering.ucsb.edu; norberg@ece.ucsb.edu; bowers@ece.ucsb.edu; coldren@ece.ucsb.edu).

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Digital Object Identifier 10.1109/LPT.2010.2100376

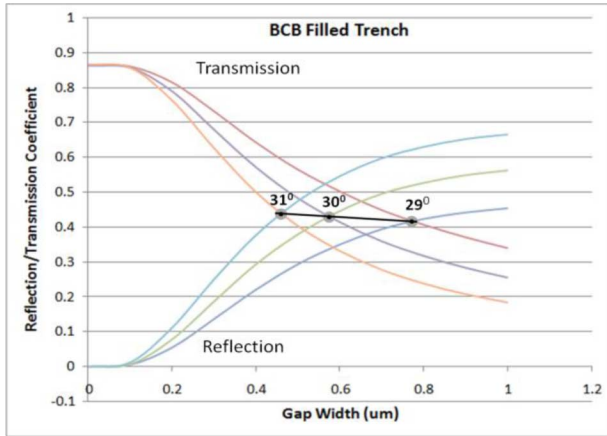


Fig. 3. Two-dimensional FDTD simulations of trench coupler splitting for TE polarized light.

3-dB splitting. There are many assumptions in using a two dimensional structure for numerical simulation. For one, we assume that the trench etch is deep enough to encompass the optical mode. In practice, the aspect ratio of the etch is limited. More importantly, the 2-D simulations significantly underestimate loss and do not take into account beam divergence due to nonidealities of fabrication such as tilted sidewalls, which is a significant problem in high aspect ratio etching [9]. However, we can still see many trends that help guide the design.

Simulated reflection and transmission of transverse electric (TE) polarized light for different trench widths are shown in Fig. 3. For ease of interpretation, only crossing angles 29° , 30° , and 31° are shown. The point where the reflection and transmission curves intersect is the 3-dB splitting point. The trend from these simulations is that the design width decreases as the crossing angle is increased above the critical angle. The simulated widths for angles 29° – 31° were found to be in the range of $0.4\ \mu\text{m}$ – $0.8\ \mu\text{m}$. However, considering that 2-D simulations overestimate the trench width needed for 3-dB splitting [6], we select a width range of $0.15\ \mu\text{m}$ – $0.55\ \mu\text{m}$ for our crossing angle range of 27° – 32° . Simulations for transverse magnetic (TM) polarization yield a 3-dB gap width of less than $0.1\ \mu\text{m}$. Because this is impractically small for fabrication, we design 3-dB splitters for TE polarized light.

The device epitaxial structure has roughly $1.8\ \mu\text{m}$ of p-InP cladding on top of $0.4\ \mu\text{m}$ of an InGaAsP multiple quantum well (MQW) optical waveguide core. The optical waveguide consists of a multiple quantum well (MQW) stack of 15 compressively strained wells and 16 tensile strained barriers. The QW width is $65\ \text{\AA}$ and the barrier width is $80\ \text{\AA}$.

Ideally, the etch depth should be below the MQW core and have smooth and vertical sidewalls. We aim for a target etch depth of $3.2\ \mu\text{m}$ which corresponds to an aspect ratio of larger than 10:1 for our design widths, presenting a serious challenge in realizing a straight sidewall trench of sufficient depth. In high aspect ratio etching, an RIE-lag effect limits the etch rate of small features with greater than 10:1 aspect ratios [10]. However, simulations show that we can etch a wider area around the trench by as much as $1\ \mu\text{m}$ without causing significant reflection of the mode at the etched interface. Pre-etching of the

trench area prior to the actual trench etch can reduce our target etch depth to $\sim 2.2\ \mu\text{m}$, bringing the aspect ratio of most of our design widths down to 7:1.

III. FABRICATION

In order to fabricate the coherent receiver, integrated UTC-PDs are first defined by selective removal of photodiode layers in nondetector regions. Waveguides are deeply etched to a depth of $\sim 3\ \mu\text{m}$ using $\text{Cl}_2 : \text{H}_2 : \text{Ar} = 7.6 : 11.4 : 2\ \text{sccm}$, 800 W ICP power, 125 W RIE power, $p = 8\ \text{mT}$ and $t = 120\ \text{s}$. Contact metal is deposited and high energy Helium implants are used to electrically isolate the PDs in the balanced photodiode pair. As mentioned above, windows over the trench areas are opened and pre-etched by $\sim 0.8\ \mu\text{m}$. Topography of the waveguide is planarized using reflowed polymethylglutarimide (PMGI) with openings over the pre-etched window in order to write the trench features using electron beam lithography.

The trench etch was carried out on an inductively coupled plasma—reactive ion etching (ICP-RIE) system employing $\text{Cl}_2/\text{H}_2/\text{Ar}$ chemistry. Cl_2 is generally known to contribute to chemical etching while Ar acts as a physical milling process. The addition of H_2 acts to balance these two processes [11]. As a starting point, we used the chemistry of the waveguide etch. To find optimal etch conditions for a deep trench, we varied etch time, pressure, RIE and ICP powers, and the relative flows of Cl_2 , H_2 and Ar. The optimized trench etch condition was $\text{Cl}_2 : \text{H}_2 : \text{Ar} :: 7 : 12 : 8\ \text{sccm}$, 250 W RIE power, 800 W ICP power, $p = 8\ \text{mT}$, $t = 350\ \text{s}$, which is very close to the waveguide etch process except for an increased Ar flow and much longer etch time. The Ar presumably continues physical milling of the trench even after the trench gets too deep for Cl_2 chemical etching to occur, thus achieving the necessary sidewall straightness. The longer etch time is necessitated by the RIE lag effect and requires a very thick dielectric mask of $\sim 6000\ \text{\AA}$ SiO_2 to withstand the etch to $\sim 2.5\ \mu\text{m}$ depth. After etching, BCB 4022-35 is used to fill the trench features. Thick pad metal is deposited for the metal traces, and lastly the devices are thinned and cleaved for characterization.

IV. TRENCH COUPLER CHARACTERIZATION

Trench devices were tested for splitting ratio and loss using a laser source emitting at $1548.5\ \text{nm}$ with 10 dBm at the facet. Splitting ratio was determined simply by taking the detected photocurrent in a given detector over the sum of the photocurrent in both detectors. The trench loss was determined by comparing current in one input modulator with the total current in the detectors. First, current in a modulator is measured at high reverse bias voltage so that the modulator absorbs practically all input light. Assuming modulator responsivity to be 100% under this condition, the measured modulator photocurrent represents the optical power at the input of the modulator. Second, the total current in the two detectors is measured for an unbiased input modulator. Assuming a detector responsivity of 100%, the measured detector photocurrent represents the total optical power at the input of the photodetectors. Dividing the modulator current over the total detector current represents the optical power lost in the trench, overestimated by the fraction of optical power lost in the modulator due to scattering, free-carrier absorption, and

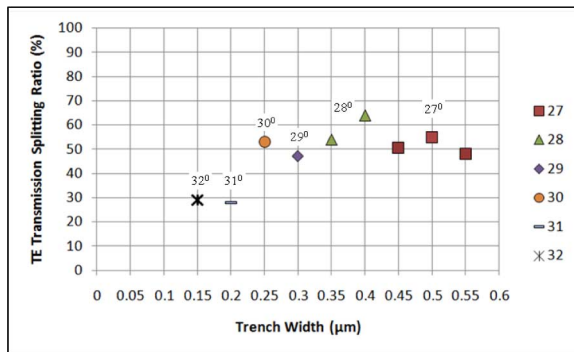


Fig. 4. TE splitting ratios of several crossing angles.

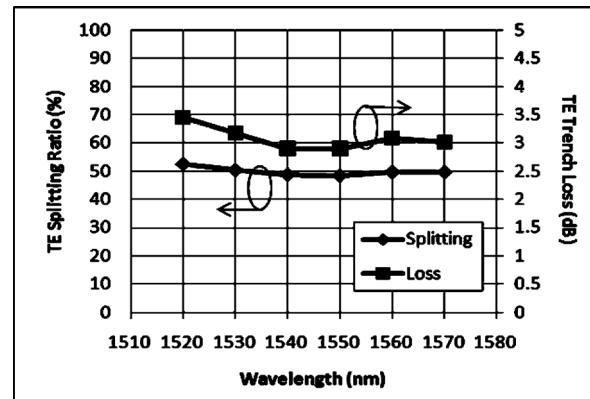


Fig. 5. Wavelength insensitivity of TE splitting ratio and loss.

other mechanisms that do not contribute to photocurrent. The maximum power transmitted through the trench occurs for TE polarized light, which also corresponds to the optimized splitting ratio for these devices. TM polarized light typically had a very low transmission and very high reflection, which is in agreement with simulations. Optical loss of an unbiased modulator is measured to be 2 dB/mm by comparing devices with 300 μm and 500 μm modulator lengths. Subtracting this from the measured loss using the above method, trench coupler losses for TE polarized light fell in the range of 2.5–3.5 dB, which is very close to the AlGaAs trench coupler losses reported in [6].

Many device designs throughout the range of crossing angles (and corresponding trench widths) exhibited $\sim 50 : 50$ splitting for TE polarized light. Fig. 4 shows several devices that achieved 3-dB splitting at different crossing angles/trench widths. The crossing angles 31° and 32° did not achieve 3-dB splitting most likely because the RIE-lag effect limited the etch depth of the corresponding small trench widths. For trench widths greater than 200 nm, the trench depth seems to have been large enough to extend over most of the optical mode, and the crossing angles of 27° – 30° achieved ~ 3 -dB splitting. The measured values cannot be directly correlated to the 2-D FDTD simulations, but the trend of smaller 3-dB trench width for higher crossing angles is clearly observed. The trench couplers were tested with a Tunics tunable external cavity laser source over the *C*-band wavelength range. Splitting and loss for both polarizations are seen to be relatively wavelength insensitive. The wavelength dependence of the TE transmission splitting ratio and trench loss are plotted in Fig. 5.

Lastly, the integrated BPD pair was used to observe the coherence efficiency of the coupler. A signal was split in two and input into both sides of the coherent receiver, with one of the arms being phase modulated. The envelope of the balanced signal corresponds to the constructive and destructive mixing of the two signals. Comparing this envelope to the maximum envelope theoretically obtainable for the detected photocurrent levels [12], we observed a coherence efficiency of 75%. We suspect that the coherence efficiency suffers penalties due to modal and polarization mismatch between the two arms of the interferometer.

V. CONCLUSION

We have designed, fabricated, and characterized 3-dB FTIR-based trench couplers. Splitting ratio is optimized for TE polarization and shows little wavelength dependence over the *C*-band. The small footprint of the 3-dB trench couplers makes them an enabling technology for ultra-compact InP PICs.

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RIE Lag Directional Coupler based Integrated InGaAsP/InP Ring Mode-locked Laser

John S. Parker,¹ Pietro R.A. Binetti,¹ Yung-Jr Hung,² Erik J. Norberg,¹ Larry A. Coldren¹

¹Electrical and Computer Engineering Department, University of California, Santa Barbara, CA 93106

²Dept. of Electronic Engineering, National Taiwan University of Science and Technology, 43 Keelung Rd., Sec. 4, Taipei 106, Taiwan

E-mail: JParker@ece.ucsb.edu, Phone: (805)893-5955

We have demonstrated the first integrated ring mode-locked laser (MLL) with a reactive ion etch (RIE) lag coupler. The RIE lag directional coupler (RL-DC) is highly advantageous for integrated MLLs as it has an insertion loss <1 dB and can be designed to provide any coupling value. This provides the RL-DC with a much needed flexibility in large photonic systems unlike standard multimode interference (MMI) couplers, which typically provide only 3 dB power splitting.

InGaAsP/InP MLLs operating at a 1.55 μm wavelength are very stable pulsed sources, which makes them attractive components for high-speed optical fiber communication with optical-time-division-multiplexing (OTDM) [1], multi-wavelength sources for wavelength-division-multiplexing (WDM) [2], and clock distribution systems [3]. MLLs built on a highly versatile InGaAsP/InP material platform provide the capability to create monolithically integrated systems-on-chip. Previously, Y. Shi has demonstrated a single RIE lag directional coupler defined by electron-beam lithography [4]. To allow ease of fabrication of the current MLL device in large photonic integrated circuits (PICs), we have defined the entire structure using i-line stepper lithography and a single etch.

A standard offset quantum well (QW) InGaAsP/InP integrated platform was used with 7 QWs positioned above a 300 nm tall 1.3Q waveguide with a confinement factor of 7.1%. A wet-etch removes the QWs for low loss passive waveguides followed by a single blanket p-cladding regrowth. Waveguides were defined by stepper lithography on a photoresist/Cr/SiO₂ three-layer mask. The patterned SiO₂ mask was used to mask the InGaAsP/InP in Cl₂/H₂/Ar etch chemistry with Inductively Coupled Plasma (ICP) Reactive Ion Etching (RIE). The RIE lag effect, which acts to slow the etch rate of smaller features, was used to define a 300 μm long 700 nm wide directional coupler on a deeply etched 4400 μm ring with a single etch-step, as shown in Fig. 1. The directional coupler has an etch depth of ~ 2.65 μm (100 nm from the bottom of the waveguide), while the deeply etched waveguides have an etch depth of 3.6 μm (below the waveguide layer by 850 nm), as shown in Fig. 2. A deeply etched directional coupler requires an extremely narrow gap <200 nm to have appreciable coupling. This typically requires more complicated Electron-Beam-Lithography (EBL), while the severe RIE lag effect from the narrow feature necessitates long etch times. This etch is difficult to make vertical and smooth, which increases scattering losses. We overcome these issues by adopting the single-etch process, which uses the RIE lag to our advantage and allows more streamlined processing of directional couplers without the need for a separate surface ridge waveguide defined by wet-etching and deeply etched waveguide defined by dry-etching.

As shown in Fig. 3, the measured cross coupling of the RIE lag directional coupler varies from 7-to-10% over the telecom C-band. The measured peak power off-chip was $\sim 200\mu\text{W}$ (-7 dBm). The RF spectra of the fundamental and second harmonic from ESA measurements is shown in Fig. 4. The raised plateau on the RF spectra at 3 GHz is due to distortion from a low noise amplifier in the ESA and appears regardless of signal. The MLL shows stable operation over a wide range of SA biases -8 to -3 V and Semiconductor Optical Amplifier (SOA) drive currents of 170-290 mA. The mode-locked regime with RF power >25 dB above the noise is shown in Fig. 5. The pulse width variation measured by an Inrad SHG autocorrelator (AC) is shown in Fig. 6. The minimum pulse width is 1.1 ps with a spectral width of ~ 6 nm.

This work was supported by the Office of Naval Research (ONR). A portion of this work was done in the UCSB nanofabrication facility, part of the National Science Foundation (NSF) funded NNIN network.

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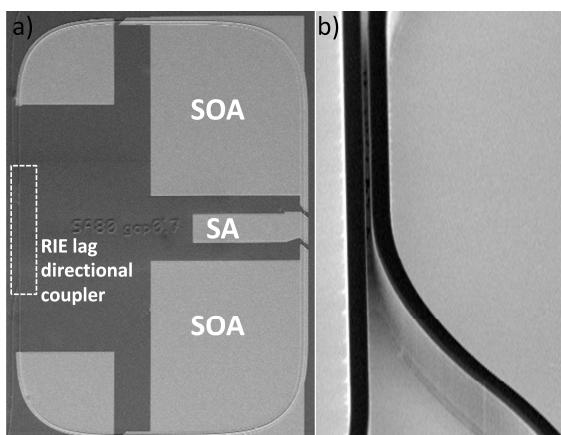


Fig. 1. Top-down SEM image of a) fabricated ring mode-locked laser and b) RIE lag directional coupler.

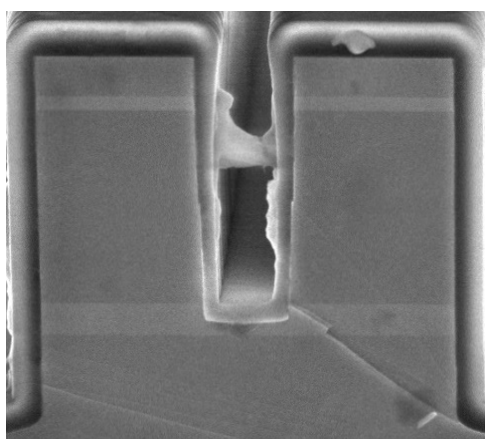


Fig. 2. SEM image of RIE lag directional coupler cross-section. The center etch depth is 200 nm into the waveguide layer.

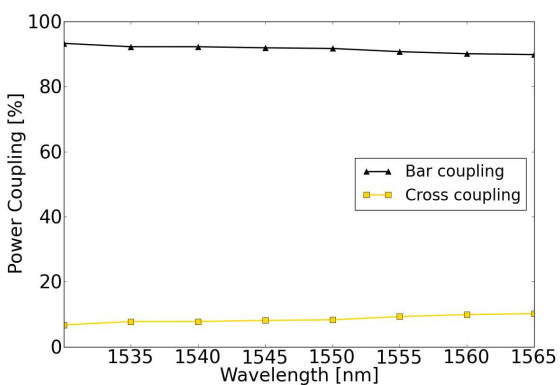


Fig. 3. Measured bar and cross coupling of 300 μm long RIE lag directional coupler. Insertion loss was measured at <1 dB.

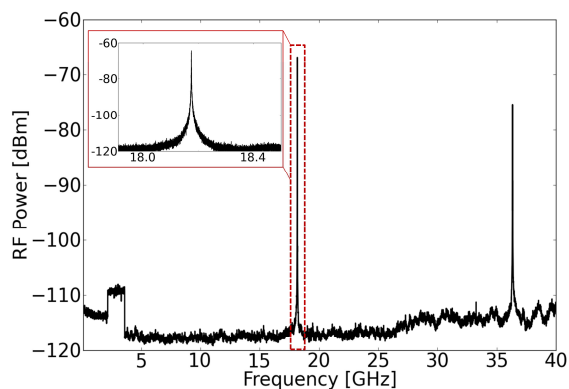


Fig. 4. ESA RF power spectrum at mode-locking showing first and second harmonic. Due to the low input power, the input electrical signal passes through a 30 dB low noise amplifier (LNA). The pedestal seen at 3 GHz is an artifact due to the LNA.

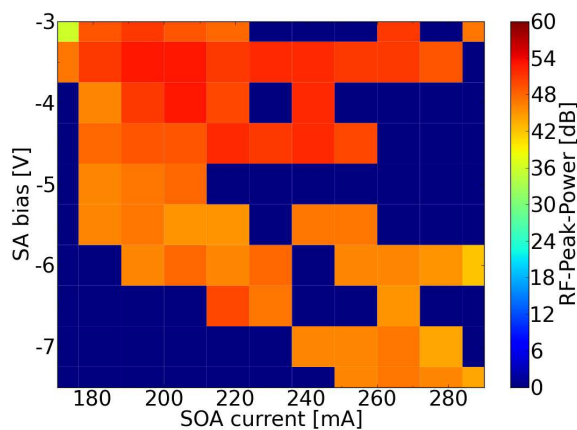


Fig. 5. Measured RF power of the MLL over the operating regime.

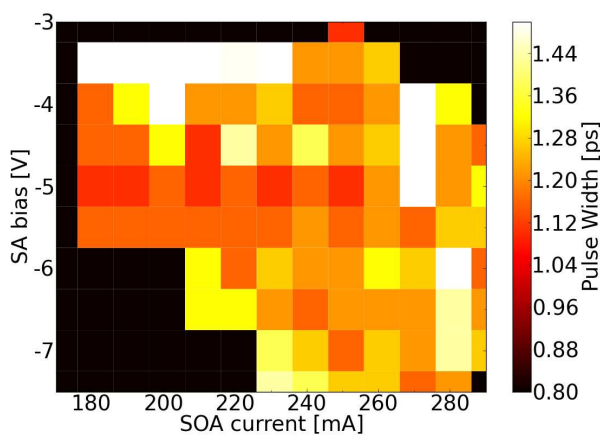


Fig. 6. Measured pulse width of the MLL over the operating regime.

Fabrication of Highly Ordered Silicon Nanowire Arrays With Controllable Sidewall Profiles for Achieving Low-Surface Reflection

Yung-Jr Hung, *Student Member, IEEE*, San-Liang Lee, *Senior Member, IEEE*,
 Brian J. Thibeault, *Senior Member, IEEE*,
 and Larry A. Coldren, *Fellow, IEEE*

Abstract—A novel and simple approach is demonstrated for fabricating silicon nanowire arrays (SNWAs) with controllable sidewall profiles. A single-step deep-reactive-ion etching (SDRIE) is used to transfer the holography patterned photoresist template to silicon or silicon-on-insulator substrates. With the SDRIE etching process, scalloping of the sidewalls can be avoided while reserving the high-mask selectivity over resist and high-etching rate. The sidewall angle of resultant patterns can be adjusted by tuning the composition of the gas mixture of the process. A modified-SDRIE process with a linearly changed gas flow is further developed to extend its capability. A post-high-energy argon plasma treatment is used to create sharp tips on the top of SNWAs and to increase the filling factor. Broadband antireflective (AR) window with a low reflectivity can be realized from tall SNWAs with high-filling factor. Depositing silicon dioxide over SNWAs can further enhance the AR performance. The position and bandwidth of the AR window can be controlled by tuning the SNWA parameters.

Index Terms—Antireflection (AR), holography lithography, silicon nanowire array (SNWA), single-step deep-reactive-ion etching (SDRIE).

I. INTRODUCTION

SILICON nanowire arrays (SNWAs) have been extensively used in many emerging technologies, including biomedical sensing [1], chemical sensing [2], electronic field emission [3], optical waveguiding [4], [5], field-effect transistors [6], and photovoltaic devices [7]–[9]. Except for bottom-growth techniques, a sequence of patterning and etching processes are usually required to realize nanostructures in semiconductors. Most of nanostructures are patterned using electron-beam lithography, which has the disadvantages of being time consuming and

low throughput. However, holographic lithography is an attractive method for periodic pattern generation with high uniformity over a large area. For transferring the SNWA patterns to semiconductor structures, numerous etching schemes have been reported for attaining high-aspect-ratio nanostructures. Most of them require a metal hard mask for the following deep etching [10]–[13]. The metal hard mask may require an additional liftoff step that will degrade the profile resolution and increase process complexity. Recently, self-masked dry etching technique is proposed by depositing nanoclusters formed by reactive gas mixtures [14], [15]. However, the resultant nanostructure arrays are lack of regularity. Deep-reactive-ion etching (DRIE) is mainly used for microelectromechanical systems (MEMS) and microfluidic device fabrication. Multiple cycles of the two-step Bosch process enable anisotropic etching of silicon with high-mask selectivity [$>200:1$ for silicon oxide and $>75:1$ for photoresist (PR)] and high-etching rate (several micrometer per minute) [16]. The major concern for using this technique to etch nanostructures is the scalloping of the sidewalls, where the peak-to-valley height can be in the scale of several hundred nanometers. Recently, researchers have demonstrated the use of Bosch etching to realize submicrometer structures [17], [18] and silicon nanopillar arrays with a high-aspect ratio and reduced scalloping of the sidewalls [19]. However, the scalloping effect is still a critical issue for etching deeper nanowires.

In this paper, we have realized 2-D resist templates by using the holography lithography [20]. We developed a single-step DRIE (SDRIE) scheme using $\text{Ar/SF}_6/\text{C}_4\text{F}_8$ chemistry to directly transfer the PR patterns into silicon-based structures. The effects of various process parameters are investigated in order to control the resultant profile. A modified-SDRIE process is developed for obtaining tall SNWAs. A tip-sharpening scheme is also developed to realize tapered nanowires with large filling factor. The antireflection (AR) characteristics of the SNWAs realized with the new fabrication schemes are then measured and discussed.

II. SINGLE-STEP DEEP-REACTIVE-ION ETCHING

We developed a novel SDRIE technique for fabricating SNWAs by simply using the PR template as the mask. For the etching of silicon nanowires, we use a Plasma-Therm 770 SLR series system with a loadlock for deep-etching silicon pillars. The system has an inductively coupled plasma (ICP) coil

Manuscript received July 1, 2010; revised August 12, 2010; accepted August 12, 2010. Date of publication October 18, 2010; date of current version August 5, 2011. This work was supported in part by the National Science Council, Taiwan under Grant NSC97-2221-E-011-077-MY3 and Grant NSC97-2917-I-011-103, in part by the Ministry of Education, Taiwan under the Top University Program, in part by the University of California at Santa Barbara nanofabrication facility, and in part by the National Science of Foundation for National Nanotechnology Infrastructure Network.

Y.-J. Hung and S.-L. Lee are with the Department of Electronic Engineering, National Taiwan University of Science and Technology, Taipei 106, Taiwan (e-mail: yungjrhung@gmail.com; silee@mail.ntust.edu.tw).

B. J. Thibeault and L. A. Coldren are with the Department of Electrical and Computer Engineering, University of California at Santa Barbara, Santa Barbara, CA 93117 USA (e-mail: thibeault@ece.ucsb.edu; coldren@ece.ucsb.edu).

Digital Object Identifier 10.1109/JSTQE.2010.2068540

and a capacitively coupled substrate RF supply to independently control the plasma density and ion energy in the system. This system can be used to deeply etch silicon by means of the conventional Bosch process, which cycles between a polymer deposition cycle using C_4F_8 gas without substrate bias and an etching cycle using a SF_6 mixture with substrate bias. Due to the isotropic etching nature of SF_6 dry etching, it causes scalloping on the sidewalls. We developed a SDRIE process with a controlled mixture of $Ar/SF_6/C_4F_8$ gas to avoid this scalloping issue, while simultaneously achieve high-etching rate and high-mask selectivity. Polymer deposition for protecting lateral sidewalls and deep silicon etching proceed simultaneously in the SDRIE process.

The difference in the etched profiles between the conventional Bosch process and SDRIE can be clearly observed from Fig. 1 for etching a $2\text{-}\mu\text{m}$ -wide waveguide. Detailed information of the process condition is listed in Table I. Although higher etching rate ($\sim 2.3\ \mu\text{m}/\text{min}$) and higher selectivity (~ 88.46) can be obtained in the Bosch process, serious scalloping occurs on the sidewalls ($\sim 265\ \text{nm}$) of the resultant profile. On the contrary, patterns with smooth and vertical sidewalls become possible by using the SDRIE process. Although the elimination of the scalloping sidewall profile is achieved at the expense of reduction in etching rate, around $300\text{--}400\ \mu\text{m}/\text{min}$ of etching rate is still comparable with the existing single-step approaches [21]–[24]. Table II shows the comparison of the proposed SDRIE with other state-of-art single-step etching approaches. $Cl_2/HBr/N_2$ -based etching technique has been widely used in IC manufacturing and known to have a good controllability over the sidewall slope [21], [22]. $SF_6/O_2/HBr$ -based etching technique has shown the ability to realize high-aspect-ratio features in silicon because silicon etching by F radical is a lot faster than Cl and Br ones [23], [24]. However, both approaches require oxide or nitride hard mask and relatively complicated control of gas composition (three different gases involved) for deep silicon etching. On the contrary, $Ar/SF_6/C_4F_8$ -based SDRIE technique provides high-etching selectivity over both resist (~ 16) and silicon nitride (~ 32) materials. Directly pattern transfer from resist template into silicon becomes possible by SDRIE process, which is particularly useful for etching high-aspect-ratio silicon nanostructures, since it is difficult to define nanometer-scale patterns in very thick resist layers or thick oxide/nitride layers. Unlike $Cl_2/HBr/N_2$ and $SF_6/O_2/HBr$ approaches, which create SiO_x or SiN_x layers for sidewall protection, sidewall passivation in $Ar/SF_6/C_4F_8$ -based SDRIE is achieved by directly depositing polymers on the surfaces, allowing higher etching selectivity. Besides, SDRIE only requires the control of gas composition between two reactive gases (SF_6 for etching and C_4F_8 for passivation, the effect of Ar flow is neglectable).

Fabrication of SNWAs includes two steps: pattern formation by holography lithography and silicon etching by SDRIE. 2-D SNWA resist patterns are realized by means of two-beam interference principle with double exposure and sample rotation steps. The sample is exposed to a 1-D interfered stripe with a sinusoidal intensity profile at 0° and 90° of sample rotation for obtaining square-oriented 2-D periodic patterns. With an optimized process procedure, the width of the resultant patterns can

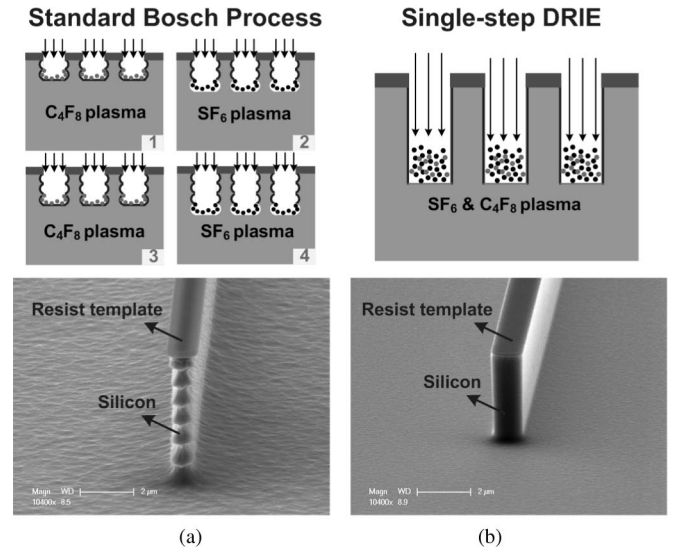


Fig. 1. Schematic of etching process and the resultant profiles for (a) Bosch and (b) SDRIE process.

be adjusted and fine-tuned by controlling the total exposure energy and development time [20]. In this paper, a 270-nm -thick PR template (OHKA THMR-M100) rather than a thin one [18] is used as the mask for deep etching. The SNWAs have a square lattice with a lattice constant of $350\ \text{nm}$. High uniformity can be achieved over a large area with the help of an AR coating (ARC). Transferring PR patterns into the bottom ARC layer is carried out by using the anisotropic O_2 plasma using a conventional RIE machine with an O_2 flow of $10\ \text{sccm}$, a pressure of $10\ \text{mTorr}$, and a RF voltage of $250\ \text{V}$. The substrate is then etched by SDRIE using the PR/ARC pattern as a mask. After SDRIE, the remaining PR/ARC is removed by the isotropic O_2 plasma with an O_2 flow of $20\ \text{sccm}$, a pressure of $80\ \text{mTorr}$, and a RF voltage of $250\ \text{V}$. Finally, the substrate is cleaned with a Piranha solution ($H_2SO_4:H_2O_2 = 3.75:1$ by volume) at a lifted temperature of 100°C . The resultant structures are then characterized using a SEM.

In order to control the SNWA profile, we will report the effects on the resultant profile by varying the process conditions. For comparisons, the reference process condition is set as the flow rate of Ar, SF_6 , and C_4F_8 being 20 , 26 , and $54\ \text{sccm}$, respectively, the dc-bias power of $9\ \text{W}$, ICP power of $800\ \text{W}$, and the chamber pressure of $19\ \text{mTorr}$.

A. Effect of $Ar/SF_6/C_4F_8$ Gas Mixture

The gas mixtures will affect the etching rate and slope of nanowire sidewalls. The incorporation of Ar gas during the SDRIE process is to stabilize the helium gas in the system. The contribution of additional physical bombardment by Ar gas to the silicon etching rate in the SDRIE process is relatively small. Therefore, in this experiment, we vary only the relative flow rate of SF_6 and C_4F_8 from the reference condition. The total flow rate of SF_6 and C_4F_8 is fixed at $80\ \text{sccm}$. Fig. 2(a) shows the silicon etching rate and the corresponding sidewall angle against the gas flow rate of C_4F_8 . The C_4F_8 -dominated

TABLE I
ETCHING CONDITIONS OF BOSCH PROCESS AND SDRIE, AND THE CORRESPONDING RESULTANT PROFILES

| Dry etching | Time (min) | C ₄ F ₈ /SF ₆ /Ar (sccm) | Pressure (mTorr) | ICP/Bias (W) | Height (μm) | Scalloping (nm) | Selectivity over resist |
|---------------|------------|---|------------------|--------------|-------------|-----------------|-------------------------|
| Bosch process | 2 | 0/100/40 70/0/40 | 23 | 825/13 | 4.6 | 265.5 | 88.46 |
| SDRIE | 10 | 52/28/20 | 19 | 850/9 | 3.15 | 0 | 16.52 |

TABLE II
COMPARISON OF THE PROPOSED SDRIE WITH OTHER STATE-OF-ART SINGLE-STEP ETCHING APPROACHES

| Technique/Chemistry | Mechanism | | Etching rate (nm/min) | Mask material | Selectivity | Reference |
|--|-----------------|--------------------------------|-----------------------|-----------------------|-------------|-----------|
| | Silicon etching | Sidewall protection | | | | |
| SF ₆ /C ₄ F ₈ /Ar (SDRIE) | F ⁻ | CF ₂ (main product) | 300~400 | PR Silicon nitride | ~16 ~32 | This work |
| Cl ₂ /HBr/N ₂ | Cl ⁻ | SiNx and SiBr | 450~530 | Silicon nitride | ~15 | [21, 22] |
| SF ₆ /O ₂ /HBr | F ⁻ | SiOx and SiBr | 500~800 | Silicon oxide | ~15 | [23, 24] |

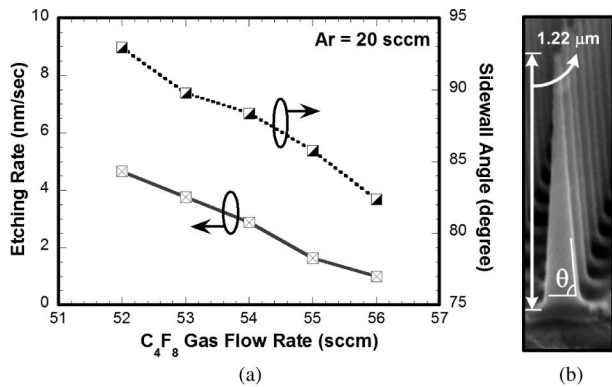


Fig. 2. Etching rate and sidewall angle, as defined in (b), for different C₄F₈ gas flow rate.

(SF₆-dominated) process condition has lower (higher) silicon etching rate and smaller (larger) sidewall angle. Here, the sidewall angle is defined as the inner angle of the pillar, as shown in Fig. 2(b). When the etching and deposition processes are balanced, high-aspect-ratio patterns with vertical sidewalls can be obtained. However, pillars with a tapered profile and a sharp tip can be realized by increasing the flow rate of C₄F₈. Undercut can appear in the pillars as the SF₆ flow rate rises, which may lead to the collapse of patterns. In our previous report, we have demonstrated hexagonal-oriented SNWAs with almost the same height, but different sidewall angles by tuning the gas mixture and etching time [25]. Here, the etching time is fixed at 3 min for obtaining the variation of etching rate and SNWA profile under different gas mixture. Lower C₄F₈ (SF₆) flow rate results in lower (higher) silicon etching rate and smaller (larger) sidewall angles. Around 10° sidewall tunable angle is achieved, verifying that tall SNWAs with controlled profiles can be realized by adjusting the gas mixture.

B. Effect of Chamber Pressure

The chamber pressure can also affect the etching rate and slope of nanowire sidewalls. SNWA samples are fabricated by varying only the chamber pressure from the reference condition.

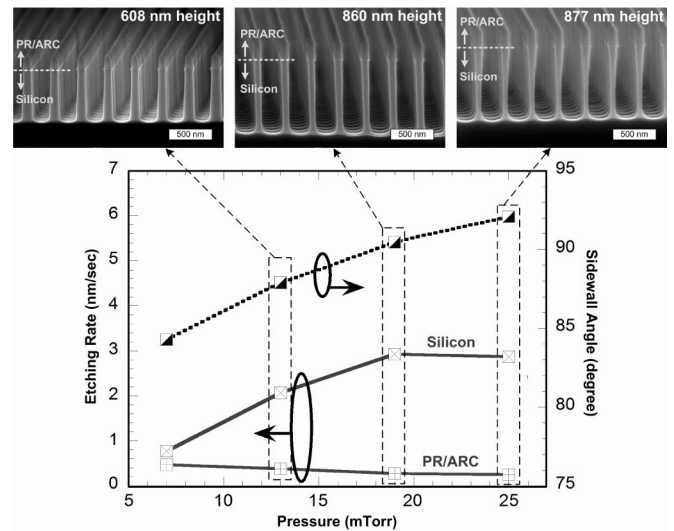


Fig. 3. Silicon etching rate and SNWA sidewall angle against the chamber pressure.

The etching time is fixed at 5 min. Fig. 3 shows the silicon etching rate and the SNWA sidewall angle against the chamber pressure. The silicon etching rate is increased with the chamber pressure due to the increased fluorine radical density [26], [27]. However, the increased fluorine radical density also causes the undercut-etching problem. The saturation of silicon etching rate happens as the pressure is higher than 19 mTorr.

C. Effect of DC-Bias and ICP Power

The degree of dissociation of fluorine is of primary importance in determining etching rate and profile shapes. As the electromagnetic field induced by the ICP source power, a low-source power process can lead to neutral-driven etching rather than ion-driven etching. From our experimental results, the etching rate is relatively insensitive to the ICP source power.

To study the influence of dc-bias power on the SDRIE process, SNWA samples are fabricated by SDRIE with the reference process condition except that the dc-bias power is set as

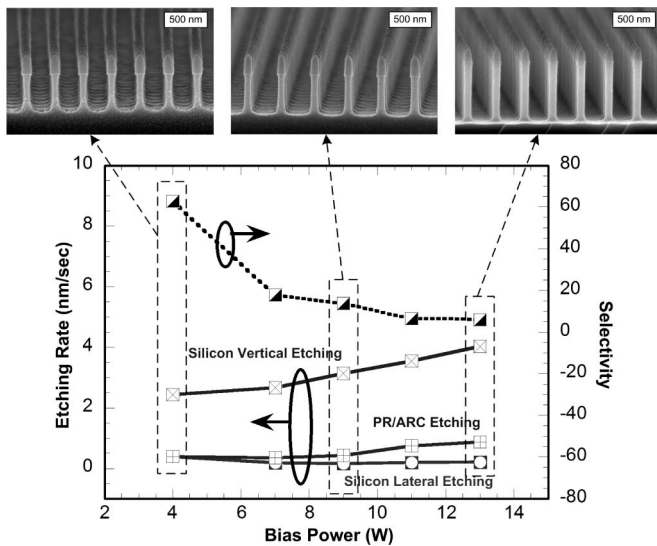


Fig. 4. Etching rate of SDRIE and etching selectivity to resist template under different dc-bias power.

4, 7, 9, 11, and 13 W, respectively. The etching time is fixed at 3 min. Fig. 4 shows the etching rate and selectivity of SDRIE under different dc-bias power. Lowering the physical bombardment on the wafer surface induced by the ion acceleration leads to isotropic etching with undercut etching. By increasing the dc-bias power, the addition of physical etching enhances the etching rate of silicon and PR/ARC and minimizes the silicon lateral etching rate, which will eliminate the pattern shrinkage. However, in case that the physical etching process dominates, the etching selectivity decreases as the dc-bias power rises. Besides, the sidewalls become rough as a high-dc-bias power is applied in the SDRIE process. The compromised value for the dc-bias power of SDRIE is around 9 to 11 W, which will provide an etching rate of around 3 nm/s, a selectivity of around 16, and smooth sidewalls.

III. MODIFIED SDRIE AND TIP SHARPENING

A. Modified SDRIE With Linearly Changed Gas Flow

Low-silicon surface reflection can be realized with the help of tall nanostructure arrays [29]. Tapered profile of nanostructures could further improve the AR properties [30]. The goal of this paper is to realize tall silicon wire arrays with tapered rods and moderate filling factor (radius to lattice-constant ratio). Although the SDRIE process is good for making silicon nanopillar arrays with a high-aspect ratio and smooth sidewalls, the issues of pattern shrinkage, RIE-lag [26], and undercut etching may limit the process flexibility. We can realize tall nanostructures by increasing the etching time of SDRIE. However, as the etching proceeds deeper, the etching rate in the vertical direction will be decreased due to the RIE-lag effect. Thus, it will require a longer etching time to achieve taller pillar structure. However, the pattern shrinkage becomes serious for a long etching process due to the lateral etching of the PR and silicon. For example, the SDRIE A and B processes, as listed in Table III, result in very narrow pillars as the height exceeds 900 nm. Thus, it is

difficult to realize tall nanowire structures, while maintaining a large filling factor by using the SDRIE process. It can be clearly seen from Fig. 3 that the lateral undercut is serious in tall nanostructures, since it is hard for both the etching (SF_6) and protection (C_4F_8) gases to flow into the high-aspect-ratio nanostructures. From Fig. 2, more C_4F_8 gas flow for sidewall passivation is needed to achieve vertical sidewalls. The reduced total gas flow inside tall nanostructures will result in the SF_6 -dominated etching process, thus cause lateral undercut etching in the bottom of pillars. Serious lateral undercut may lead to the collapse of patterns.

From Fig. 4, the pattern shrinkage problem can be reduced by increasing the physical bombardment (increase the dc-bias power) and decreasing the chemical etching (decrease/increase the $\text{SF}_6/\text{C}_4\text{F}_8$ gas flow). To verify this point, we change the bias power from 9 to 13 W and the $\text{SF}_6/\text{C}_4\text{F}_8$ gas mixture from 26/54 to 25/55 sccm. The process condition and resultant profile is listed as “SDRIE C” process in Table III. After 5 min etching, a 906-nm-tall silicon array can be realized to have an improved filling factor of 0.13 and vertical sidewalls.

In order to obtain silicon wire arrays with larger filling factors, we demonstrate here a “modified SDRIE” process, as listed in Table III, by linearly changing the gas flow. During the process, the flow rate of C_4F_8 (SF_6) changes linearly from 55 (25) to 55.8 (24.2) sccm in five steps. Silicon nitride (SiN_x) is used as the hard mask for deep silicon etching. A stronger hard mask is also good for maintaining the width of the resultant patterns. Pattern transfer from PR/ARC into SiN_x is carried out by anisotropic CHF_3 plasma etching. The etching time in each step is set to 1.5 min. Higher bias power (13 W) is used to eliminate the pattern shrinkage. The resultant profile after each step of the process is shown in Fig. 5 and the corresponding parameters are summarized in Table III. The pillar height can reach 632 nm after 3 min etching (after step 2). A 1340-nm tall and tapered silicon wire array with an aspect ratio of 10.89 and a filling factor of 0.18 is obtained with a total etching time of 7.5 min (after step 5).

B. Tip-Sharpening Process

Another approach for making nanotip array is to utilize the post-tip-sharpening process. Tip sharpening can be performed by using high-energy argon plasma treatment after the SDRIE etching. In the experiment, two set of samples with almost the same sample area are fabricated by the SDRIE process to have a height of 464 nm (Sample A) and 880 nm (Sample B), respectively. These samples are then exposed to the plasma atmosphere for 20 min with an argon gas flow of 20 sccm, a chamber pressure of 80 mTorr. The RF-bias voltage is varied from 50 to 500 V for observing the tip-sharpening process.

Fig. 6 shows the SEM photos of resultant profiles after post-argon plasma treatment for different RF-bias voltages. It can be found that a bias voltage of 50 V for the tip-sharpening process has little effect on the resultant pattern profiles. The top of the pillars become rounded as the bias voltage is raised to 200 V. The tip sharpening of Si pillars happens with a bias voltage of 350 V or larger. We believe that the tip-sharpening effect is due

TABLE III
COMPARISON BETWEEN THE ORIGINAL AND MODIFIED-SDRIE PROCESS

| Etching processes | SDRIE process conditions | | | | Resultant profiles | | |
|-------------------|--------------------------|--------------------------------------|------------------------|----------------|--------------------|----------------|-------------------------|
| | Time (min) | C ₄ F ₈ (sccm) | SF ₆ (sccm) | Bias power (W) | Height/Width (nm) | Filling Factor | Sidewall Angle (degree) |
| SDRIE A | 5 | 54 | 26 | 9 | 978/30.2 | 0.04 | 90.6 |
| SDRIE B | 7 | 54 | 26 | 9 | 1390/24 | 0.03 | 90.3 |
| SDRIE C | 5 | 55 | 25 | 13 | 906/93.5 | 0.13 | 90 |
| Modified SDRIE | Step 2 | | | | 632/150 | 0.21 | 90.5 |
| | Step 3 | 55 | 25 | | 849/139 | 0.20 | 89.6 |
| | Step 4 | ↓ | ↓ | 13 | 1110/130 | 0.19 | 89.1 |
| | Step 5 | 55.8 | 24.2 | | 1340/123 | 0.18 | 88.4 |

* The pressure, ICP power and Ar gas flow are fixed at 19 mTorr, 800 W and 20 sccm, respectively. Original SDRIE process uses PR/ARC as the mask. Modified SDRIE process uses silicon nitride as the hard mask.

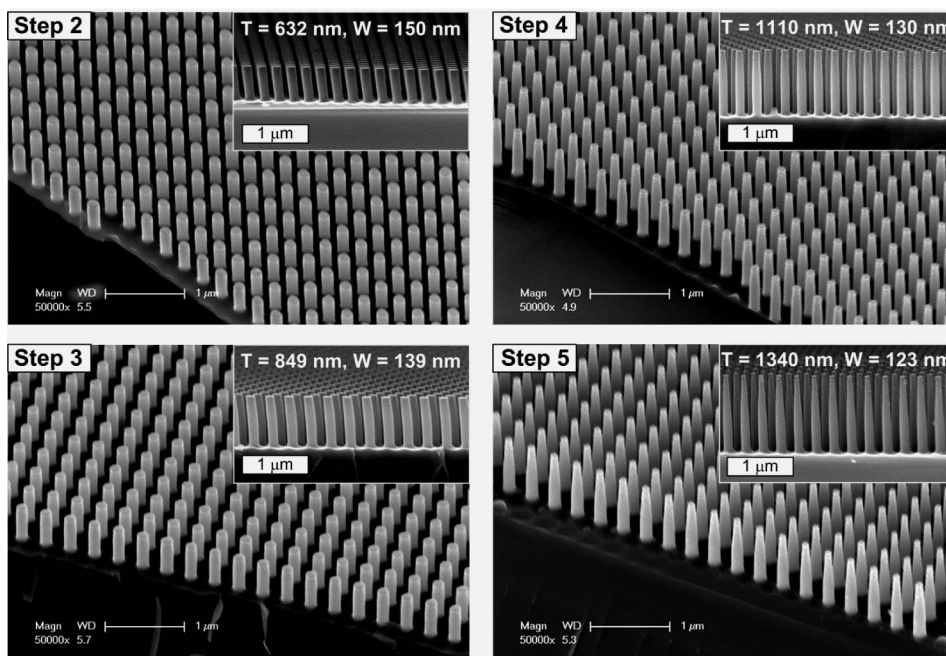


Fig. 5. SEM views of resultant profiles after each step of the modified SDRIE with linearly changed C₄F₈/SF₆ gas flow.

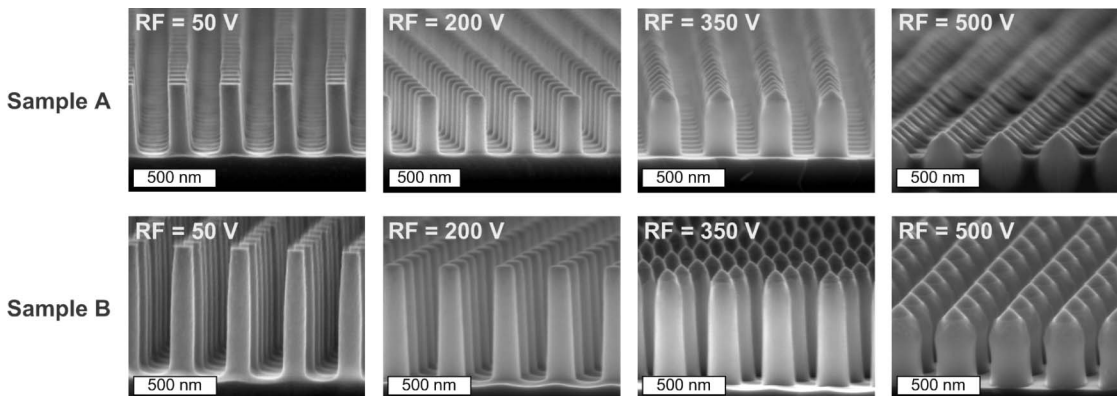


Fig. 6. SEM views of resultant profiles (Samples A and B) after postargon plasma treatment with different RF-bias voltages.

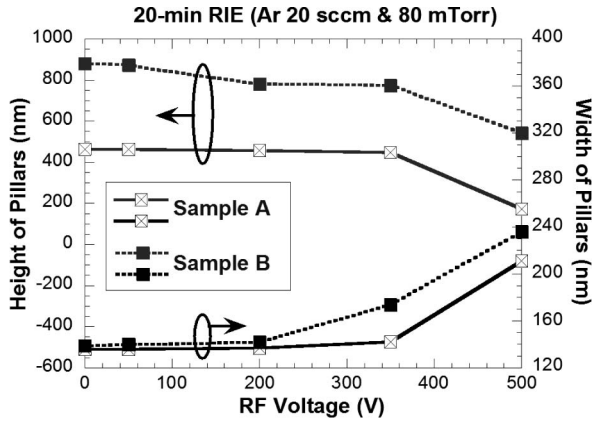


Fig. 7. Height and width of resultant profiles (Samples A and B) after postargon plasma treatment with different RF-bias voltages.

to the existence of higher electric field at the pillar edges, resulting in an enhanced sputtering rate there. However, the height of resultant patterns decreases as the bias voltage increases because of the enhanced physical bombardment, as shown in Fig. 7. It is interesting to find that the width of resultant patterns increases with the bias voltage. This might be due to the fact that the silicon material of pillar arrays is sputtered out and attached on the sidewalls, resulting in an increase in the filling factor of silicon wire arrays.

IV. OPTICAL REFLECTION

A. Modified-SDRIE Realized SNWAs

We have fabricated tall SNWAs with moderate filling factor by using the modified-SDRIE process. Optical reflection spectra of the resultant SNWA samples are characterized using a spectrophotometer (Filmetrics F20-UV). Fig. 8 shows the reflection spectra of the SNWAs after each step of the modified-SDRIE process. Since the resultant SNWAs are not tall enough after step 2 of the modified SDRIE, the reflection can be as high as 25% in the visible region. The AR effect is improved as the SNWAs become taller and tapered. The reflectivity between 550 and 700 nm of wavelength can be as low as 0.2% for the SNWAs after step 5 of the modified SDRIE. The reflectivity can be less than 7% over the whole visible region.

B. SNWAs After Argon Plasma Treatment

The argon plasma treatment after SDRIE etching can be used to sharpen the tips of SNWAs and to increase their filling factor. Fig. 9 shows the reflection spectra of the SNWAs after argon plasma treatment with different RF-bias voltages for Sample A and B in Figs. 6 and 7. Since the original SNWAs of Sample A are relatively short, low reflectivity can only be obtained over a narrow wavelength range. The lowest reflectivity for the original Sample A is around 3% at 625-nm wavelength. The reflection spectrum of Sample A after 200 V argon treatment is slightly improved to be around 2.4%. For Sample A, after 500 V argon treatment, the height and width of the resultant SNWAs change to 173 and 211 nm, respectively, with sharp tips on the top. Due

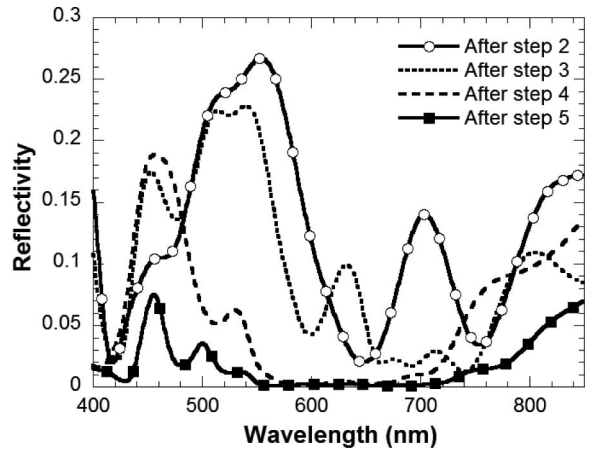


Fig. 8. Measured reflection spectra of SNWAs after each step of the modified SDRIE with linearly changed C₄F₈/SF₆ gas flow, as listed in Table III.

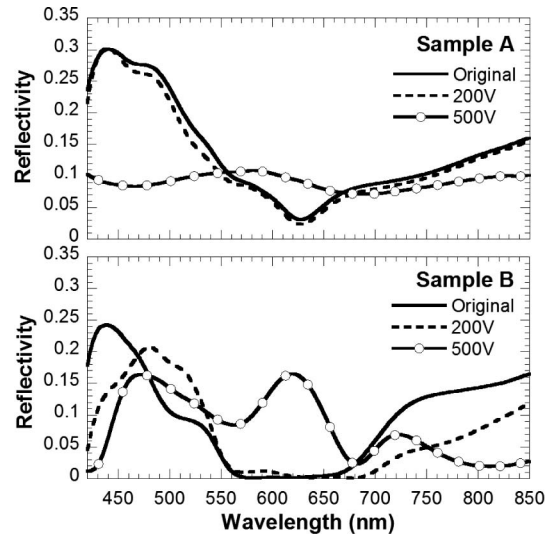


Fig. 9. Measured reflection spectra of Samples A and B in Fig. 6 after postargon plasma treatment with different RF-bias voltage.

to the shallow nanostructures, the resultant SNWAs lose the photonic crystal property, but provide surface roughness effect, resulting in an around 10% reflectivity throughout the visible region.

For the taller Sample B, the minimum reflectivity is around 1.2% in the visible region. The reflectivity is slightly reduced to be around 1% after 200 V argon treatment. The height and width of resultant SNWAs change dramatically to 543 and 236 nm, respectively, after 500 V argon bombardment. With sharp tips on the top and enlarged filling factor, 33.7%, the low-reflectivity window is red-shifted. The reflectivity is increased for shorter SNWAs.

C. SiO₂ Coated SNWAs on Silicon-on-Insulator Substrate

The SNWAs reported in previous sections are fabricated on bare silicon substrate. In this section, we address the properties of SNWAs on silicon-on-insulator (SOI) wafers, which are often used for fabricating optical ICs or thin-film optoelectronic

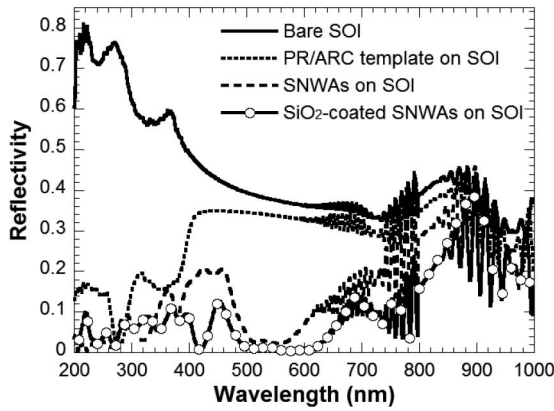


Fig. 10. Measured reflection spectra of bare SOI, 250-nm-tall PR/ARC templates on SOI, 700-nm-tall square SNWAs on SOI, and the 700-nm-tall SNWAs coated with a 186-nm-thick SiO₂ film.

devices. The SOI wafer contains a 2- μm -thick silicon dioxide as the intermediate layer and a 6- μm -thick silicon layer on the top. SNWA samples are fabricated using the SDRIE process. Fig. 10 shows the reflection spectra of the bare SOI, 250-nm-tall PR/ARC templates on SOI, 700-nm-tall SNWAs on SOI, and the 700-nm-tall SNWAs coated with a 186-nm-thick SiO₂ film. The SiO₂ film is deposited by plasma-enhanced CVD (PECVD) over the tall SNWAs to serve as a buffer layer between SNWAs and air.

Lower reflectivity of PR/ARC templates on SOI is due to its lower effective index, which serves as a buffer layer between air and silicon substrate. Reduced reflectivity over the UV wavelengths is due to the absorption characteristic of the ARC film. SNWAs on the SOI substrate can provide lower reflectivity than the bare SOI wafer over a wide wavelength range due to its deeper subwavelength structure. The overall reflectivity of this nanostructure is below 20% in the entire UV to visible region and is around 2.5% in the wavelengths between 500 and 550 nm. The reflectivity is further reduced by depositing a SiO₂ film on top of the SNWAs. The reflectivity is below 10% over the entire UV to visible region and below 1% for the wavelengths between 500 and 600 nm. It verifies that SNWAs coated with a SiO₂ film of right thickness can also improve the AR performance. Since SOI wafer contains Si-SiO₂-Si structures, multicavity resonance can be observed in the longer wavelength side of the reflection spectra.

D. Change of AR Spectra With SNWA Parameters

To figure out how the SNWA parameters affect the characteristic of AR window, we fabricated several SNWA samples on SOI substrate to have different widths, lattice constants, and heights. Fig. 11(a) shows the reflection spectra for SNWAs with different holography exposure time that leads to different pillar widths. The SNWAs with smaller pillar width have blue-shifted reflection spectrum and reduced bandwidth of AR windows. Fig. 11(b) compares the reflection spectra for SNWAs with different lattice constants. Again, the low-reflectivity window becomes narrower and moves to shorter wavelengths for the SNWAs with a smaller lattice constant. The trend shown

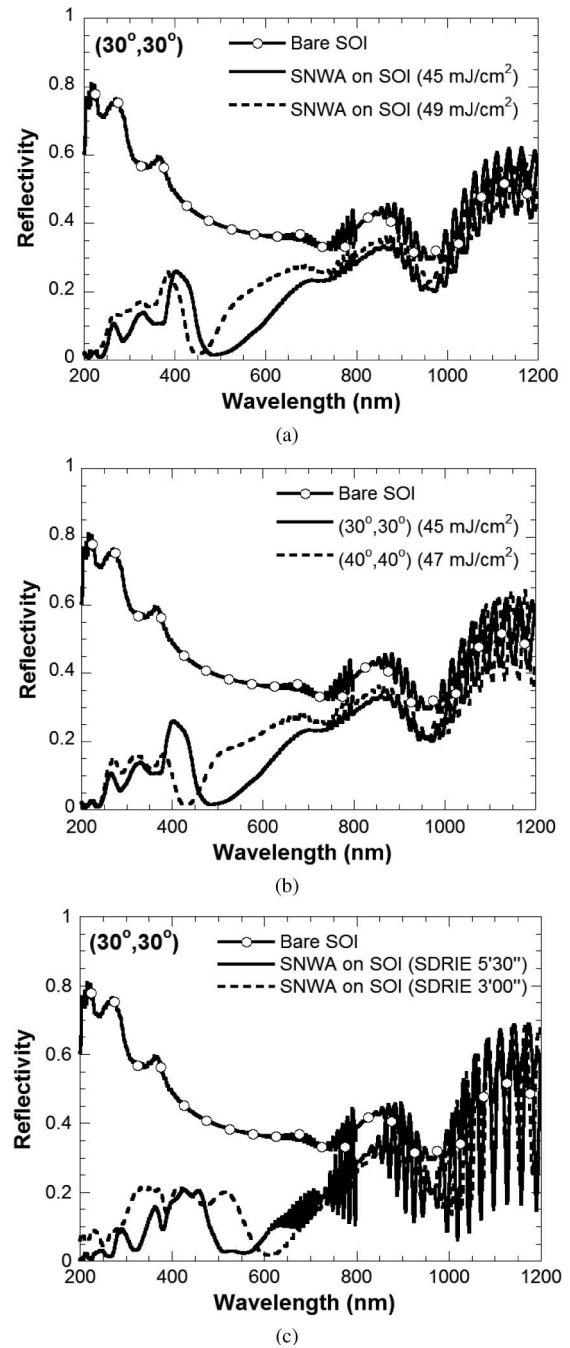


Fig. 11. (a) Measured reflection spectra of 330 nm spaced square SNWAs on SOI substrate with different exposure time during holography for obtaining different pillar widths. (b) Measured reflection spectra of SNWAs on SOI substrate with different lattice constants. (c) Measured reflection spectra of square SNWAs on SOI substrate with different SDRIE etching time for obtaining different pillar heights.

in Fig. 11(a) and (b) agrees with the rigorous coupled-wave analysis (RCWA) simulation results. Fig. 11(c) shows the reflection spectra for the SNWAs with different SDRIE etching time that result in different pillar heights. The RCWA simulation indicates that taller SNWA results in the broadening and red-shifting of the AR spectrum. However, for SNWAs realized by the SDRIE process, pattern shrinkage in taller SNWAs leads to

TABLE IV
OPTICAL PROPERTY VARIATION FOR DIFFERENT SNWA PARAMETERS

| SNWA parameters | Simulated AR spectrum | Measured AR spectrum | AR bandwidth |
|--------------------|-----------------------|----------------------|----------------|
| Pillar height ↑ | Red shift | Blue shift | Increased (↑↑) |
| Pillar width ↑ | Red shift | Red shift | Increased (↑) |
| Lattice constant ↑ | Red shift | Red shift | Increased (↑) |

smaller pillar width because of the lateral silicon etching. Thus, the overall reflection spectrum is broadened, but blue-shifted, as shown in Fig. 11(c). The effects of the SNWA parameters on the AR property of SNWAs are summarized in Table IV.

V. CONCLUSION

A novel and simple approach for fabricating tall SNWAs with high uniformity is demonstrated. PR templates realized by the holographic lithography can be used directly as the mask for the SDRIE etching. The SDRIE process with a controlled mixture of Ar/SF₆/C₄F₈ gas can be used to attain smooth and controllable sidewalls on the resultant SNWA patterns, while simultaneously keeping the advantages of high-mask selectivity and high-etching rate. The sidewall angle of resultant patterns can be adjusted by adjusting the composition of the gas mixture of SDRIE process. A modified-SDRIE process with a linearly changed gas flow is developed to solve the undercut-etching issue, to eliminate the pattern shrinkage by using a higher dc-bias power and a stronger hard mask. The high-energy argon plasma treatment after SDRIE etching can be used to increase the filling factor and create sharp tips on SNWAs. This postetching process can be used to amend the reflection spectra of SNWAs.

We also demonstrate that SNWAs coated with a SiO₂ film can be used to obtain good AR performance, which is comparable to what we have achieved from tapered SNWAs [8]. How the SNWA parameters affect the characteristic of AR window is also investigated. With increased height, width, and lattice constant of SNWAs, the AR window will be widened and red-shifted. The highly ordered SNWAs fabricated with the SDRIE process and the postetching treatment can be used for reducing surface reflection with high controllability.

ACKNOWLEDGMENT

The authors would like to thank Prof. K.-Y. Lee and Dr. C.-A. Chen in National Taiwan University of Science and Technology for their discussion and help.

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Yung-Jr Hung (S'07) received the B.S. and Ph.D. degrees in electrical engineering from the National Taiwan University of Science and Technology (NTUST), Taipei, Taiwan, in 2005 and 2010, respectively.

In 2009, he was a Visiting Scholar in the Department of Electrical and Computer Engineering, University of California at Santa Barbara, partly supported by the National Science Council, Taiwan. He is currently a Postdoctoral Fellow in the Department of Electronic Engineering, NTUST. His research interests include holographic photonic crystals, semiconductor lasers, solar cells, and photonic integrated circuits.



San-Liang Lee (SM'07) received the B.S. degree in electronics engineering from the National Chiao Tung University, Hsinchu, Taiwan, in 1984, the M.S. degree in electrical engineering from the National Taiwan University, Taipei, Taiwan, in 1986, and the Ph.D. degree in electrical and computer engineering from the University of California, Santa Barbara, in 1995.

In 1988, he joined the faculty of the Department of Electronic Engineering, National Taiwan University of Science and Technology (NTUST), Taipei, and became an Associate Professor in 1995 and a Professor in 2002. From 2002 to 2005, he was the Director of the Center for Optoelectronic Science and Technology, College of Electrical and Computer Engineering, NTUST. He is currently the Dean of the Academic Affairs of NTUST, where he was the Chairman from 2005 to 2008. From 2005 to 2009, he was also the Director of the program office for the National Innovative Education Program on Image Display Technology, sponsored by the Ministry of Education, Taiwan. He has authored or coauthored more than 150 referred papers in international journals and conferences. He holds 22 patents. His research interests include semiconductor optoelectronic components, photonic integrated circuits, nanophotonics, and optical switching technologies.



Brian J. Thibeault (S'89–M'97–SM'05) received the B.S. degree in electrical engineering from the University of California, Irvine, CA, in 1990, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Santa Barbara (UCSB), in 1991 and 1997, respectively.

In 1996, he started WideGap Technologies, LLC, where he was engaged as a Principal Investigator and a member of the Technical Staff in GaN-based high-electron mobility transistor technologies, and ultraviolet and visible light emitting diodes, which was later merged with Cree, Inc. in 2000. In December 2000, he joined the staff at the UCSB nanofabrication facility as a Principal Development Engineer, where he is currently a Project Scientist. He has authored or coauthored more than 115 journal and conference papers. He has also coauthored one book chapter. He is also an Inventor in ten U.S. patents. His research interests include the area of fabrication of electronic and optoelectronic devices.



Larry A. Coldren (S'67–M'72–SM'77–F'82) received the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, in 1972.

In 1984, he joined University of California, Santa Barbara (UCSB), where he is currently the Fred Kavli Professor of optoelectronics and sensors and the Director of the Optoelectronics Technology Center, and also engaged with materials, and electrical and computer engineering. At UCSB, he continued work on multiple-section tunable lasers; in 1988, he invented the widely tunable multielement mirror concept, which is now used in some JDSU products. During the late 1980s, he also developed efficient vertical-cavity multiple-quantum-well modulators, which led to novel vertical-cavity surface-emitting laser (VCSEL) designs that provided unparalleled levels of performance. He is engaged in developing new photonic IC (PIC) and VCSEL technology, including the underlying materials growth and fabrication techniques. In 1990, he was the Co-Founder of Optical Concepts, later acquired as Gore Photonics, to develop novel VCSEL technology. In 1998, he was the Co-Founder of Agility Communications, later acquired by JDS Uniphase Corporation (JDSU), to develop widely tunable integrated transmitters. At Bell Labs, he was involved in waveguided-surface-acoustic-wave signal processing devices and coupled-resonator filters, and then, developed tunable coupled-cavity lasers using novel reactive-ion etching technology that he created for the new InP-based materials. He has authored or coauthored more than 1000 journal and conference papers, seven book chapters, one textbook, and has issued 63 patents. His research interests include the creation of efficient all-epitaxial InP-based and high-modulation speed GaAs-based VCSELs as well as a variety of InP-based PICs incorporating numerous optical elements for widely tunable integrated transmitters, receivers, and wavelength converters operating up to 40 Gb/s.

Prof. Coldren has presented dozens of invited and plenary talks at major conferences. He was the recipient of the 2004 John Tyndall and 2009 Aron Kressel Awards. He is the Fellow of the Optical Society of America and Institution of Electrical Engineers. He is also a member of the National Academy of Engineering.

III. Vertical-Cavity Surface-Emitting Lasers (VCSELs)

Control of Polarization Phase Offset in Low Threshold Polarization Switching VCSELs

Yan Zheng, Chin-Han Lin, *Student Member, IEEE*, and Larry A. Coldren, *Fellow, IEEE*

Abstract—Both polarization switching and control over the angle between polarization states is demonstrated. A novel dual intracavity contacted vertical-cavity surface-emitting laser utilizing asymmetric current injection is tested. Large extinction ratios >21 dB and a record-low threshold current of 0.19 mA is achieved for such devices. Control over the phase offset between two polarization states is accomplished by rotating current injection direction relative to the $\langle 110 \rangle$ axis. The phase offset between two polarization states is shown to follow a trigonometric function with maximum offsets along the $\langle 110 \rangle$ and $\langle \bar{1}\bar{1}0 \rangle$ directions and minimum offsets along the $\langle 100 \rangle$ and $\langle 010 \rangle$ directions.

Index Terms—Asymmetric current injection (ACI), molecular beam epitaxy, polarization, vertical-cavity surface-emitting lasers (VCSELs).

I. INTRODUCTION

VERTICAL-CAVITY surface-emitting lasers (VCSELs) have become key components in next-generation optical interconnects [1]. This is in part because VCSELs have shown many advantages such as higher reliability, yield, and their ability to be put into arrays. If the output polarization could be controlled, further opportunities in medical imaging [2], environmental monitoring [3], and military applications [4] could be explored. Although output polarization of VCSELs does not exhibit fundamental selection rules [5], several methods have been used to stabilize output polarization such as utilizing various mesa geometries [6], off-axis crystal surfaces [7], and surface gratings [8]. Several groups have also demonstrated asymmetric current injection (ACI) as a way to introduce gain anisotropies to control output polarization [9]–[11]. Although the carrier k -vectors are necessarily aligned with the substrate-normal (z -direction) at the absorption edge energy in quantum-wells, at lasing threshold and above, there is sufficient state filling to provide a significant lateral carrier momentum component which modifies the overall electron k -vector. Since there is a transition strength dependence between the electron k -vector and the incident electric field, a change in current direction can potentially control output polarization by influencing the transition strength (and thus gain) of specific polarizations.

Manuscript received October 07, 2010; revised November 11, 2010; accepted November 27, 2010. Date of publication December 10, 2010; date of current version February 24, 2011. This work was supported by the Defense Advanced Research Projects Agency (DARPA) through an STTR with ZIVA Corp.

The authors are with the University of California, Santa Barbara, Santa Barbara, CA 93106 USA (e-mail: yazheng@umail.ucsb.edu).

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Digital Object Identifier 10.1109/LPT.2010.2098026

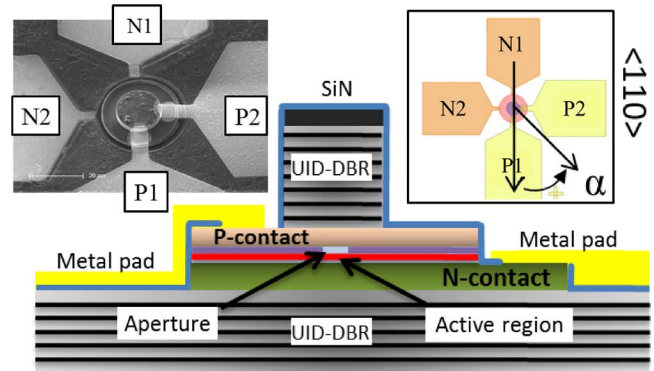


Fig. 1. Schematic of VCSEL epitaxial structure. Insets show top view of VCSEL contact-pads and its rotation angle α relative to the $\langle 110 \rangle$ axis and a corresponding SEM image.

In this letter we demonstrate switching between two orthogonal polarization states via asymmetric current injection utilizing a novel dual intracavity contacted circular mesa design. Control over polarization phase offset, or, the angle between polarization states, will also be shown by rotating current injection direction.

II. GROWTH AND FABRICATION

A dual intracavity design was used to avoid having to contact through a p-doped Distributed Bragg Reflector (p-DBR) top mirror which would have increased the current path length and decreased the carrier momentum lifetime through scattering events [12]. Moreover, traveling through the p-DBR unnecessarily adds more z -component to the carrier momentum vector that is isotropic with current direction. The p- and n-contact layers were thus grown close together to increase current directionality shown in Fig. 1. Molecular Beam Epitaxy (MBE) growth on (001)-cut undoped GaAs starts with 18 periods of unintentionally doped (UID) GaAs/AlAs to form the bottom DBR mirror followed by 420 nm of Si doped GaAs for the n-contact layer. The active region consists of three 8 nm thick $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}$ quantum wells separated by 8 nm GaAs barriers. The active region was surrounded by a 30% AlGaAs separate confinement heterostructure (SCH). A linearly graded AlGaAs region then forms the oxide aperture. The free carrier absorption associated with the overlap between the optical field and the hole concentration is an important issue since the p-contact layer is placed so close to the active region. A modulation doping scheme was employed using multiple doping levels to minimize this overlap. In order to quickly and accurately supply all the doping levels, a custom Carbon Tetrabromide (CBr_4) carbon doping system was used [13]. The doping ranged from $1 \times 10^{18} \text{ cm}^{-3}$ to $4 \times 10^{18} \text{ cm}^{-3}$.

with the highly doped regions occurring at the optical nulls. The top mirror was composed of 32 periods of 85% AlGaAs/GaAs.

Circular mesas were created in a two-step dry-etching process that stops in the intracavity contact layers using a laser etch-monitor. The devices are then placed in a wet oxidation furnace to form the oxide aperture. A third etch removes the n-contact layer except from where the n-metal pads will be to help isolate orthogonal electron paths. A blanket SiN layer is then deposited and four equally spaced vias are opened around the mesa for metal contacts. Devices were rotated in various increments on the mask so that the output polarization can be studied as a function of current injection direction.

III. POLARIZATION SWITCHING

A linear polarizing lens is used to measure output polarization. The polarizer transmission axis is aligned to the 0° marker on the rotational lens mount. The $\langle 1\bar{1}0 \rangle$ axis of the wafer is then aligned to this marker. Output light intensity (LI) first passes through a microscope objective then the rotating polarizing lens and finally is measured by a Si photodetector.

Light-current-voltage (LIV) curves for a device with a mesa diameter of $13 \mu\text{m}$ and an aperture of $6 \mu\text{m}$ is shown in Fig. 2 for two polarization states. Asymmetric current injection was achieved by directing current between pads that face each other i.e. P1N1 or P2N2. The threshold current is 0.19 mA for both current configurations which is the lowest threshold reported for ACI polarization switching VCSEL. Output wavelength was 971 nm and the near field pattern uniformly filled the aperture with a diameter of roughly $13 \mu\text{m}$. When injecting current between the P1N1 pads, light output was found to be polarized close to 40° from the $\langle 110 \rangle$ axis. Probing the orthogonal P2N2 pads first showed lasing in the same polarization but quickly switches to the orthogonal polarization. This initial switching could be related to temperature effects [14]. At a polarizer angle of 120° shown in Fig. 2(b), the P2N2 direction initially lases aligned to 40° but switches to the orthogonal polarization after 0.37 mA. The preferred polarization angle is offset from the crystal axis due to misalignment of the polarizer to the current path. The ripples in the LI curves are a result of feedback from the substrate-air interface due to no anti-reflection (AR) coating. Small differences in wavelength between polarization states and thermal impedances of the two current paths slightly offset the oscillations in P1N1 to P2N2. The intensity and frequency of ripples in light output increases with decreasing device size and ultimately disappear under $1 \mu\text{s}$ pulsed conditions.

IV. POLARIZATION PHASE OFFSET

The phase offset between two polarization states was also investigated. Here we have defined the polarization state as the output polarization for a given current injection direction. The phase offset between two polarization states is the difference in polarizer angle between output power peaks.

LI curves were taken for every 20° rotation of the polarizer with either the P1N1 or P2N2 configuration probed. Light output of the device at a bias of 2 mA is plotted against the polarizer rotation angle to generate the polarization resolved output shown in Fig. 3. The measured data for the two orthogonal current injection configurations is fitted to a sine wave that has a R^2

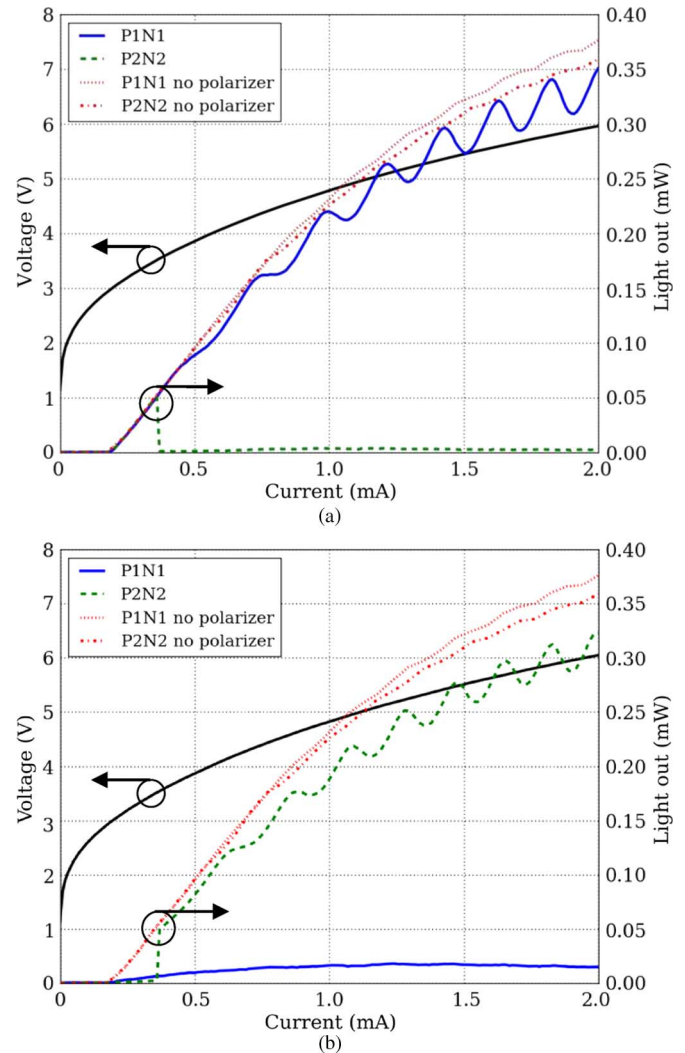


Fig. 2. L - I - V curve with polarizer transmission axis (a) 40° to the $\langle 1\bar{1}0 \rangle$ axis and (b) 120° to the $\langle 1\bar{1}0 \rangle$ axis.

value >0.999 . From the fit, the polarization rotational frequency was determined to be 2 rad^{-1} for both current directions. These two polarization states also showed a phase offset of approximately 90° .

From the good fit, extrapolated extinction ratios were obtained. The (P1N1)/(P2N2) state had an extinction ratio $>21 \text{ dB}$ at a polarizer angle of 38° and the (P2N2)/(P1N1) state had an extinction ratio $>25 \text{ dB}$ at a polarizer angle of 131° . These are one of the largest extinction ratios reported for a polarization switching VCSEL using ACI.

The circular structure of our VCSEL is a good platform to study the polarization dependence on current direction because its infinite rotational symmetry might allow one to see current injection effects independent of certain geometrical effects.

When injecting current along either the $\langle 110 \rangle$ or $\langle 1\bar{1}0 \rangle$ axis, past work with square VCSELs have reported phase offsets that vary randomly between 25° - 90° [9] or aligned to only the $\langle 110 \rangle$ or $\langle 1\bar{1}0 \rangle$ axes [15]. To test if our structure could better control the phase offset, VCSELs were rotated in the following angles (α), relative to the $\langle 110 \rangle$ direction: $[0^\circ, 22.5^\circ, 45^\circ, 90^\circ, 135^\circ,$

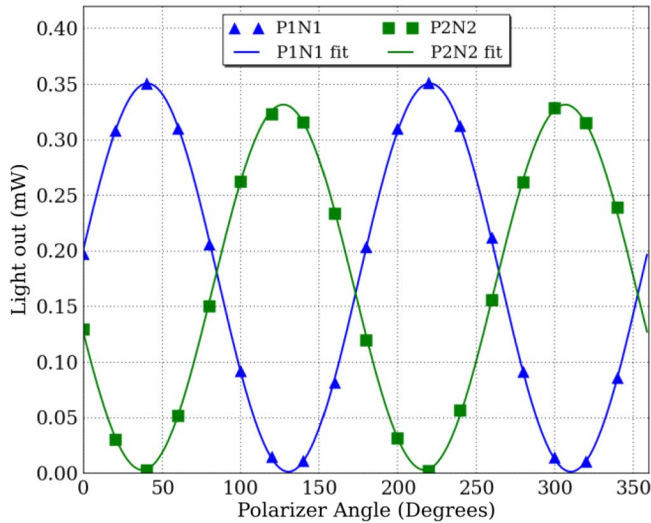


Fig. 3. Output power at 2.0 mA showing sinusoidal dependence to polarizer angle.

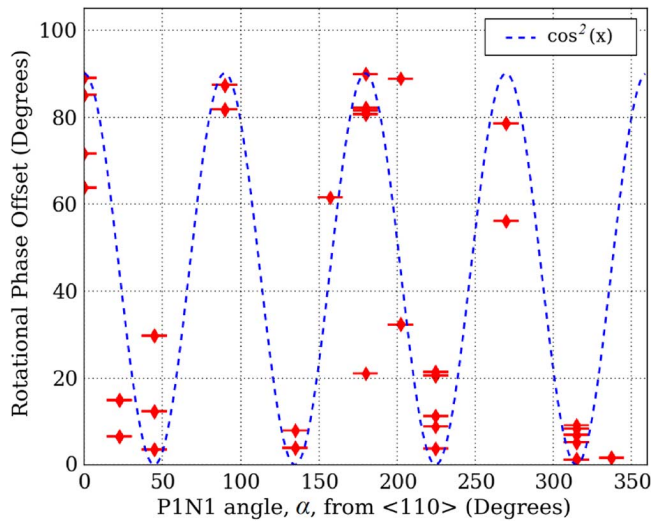


Fig. 4. Phase offsets between two polarization states measured as the current injection angle α is rotated.

157.5°, 180°, 202.5°, 225°, 270°, 315°, 337.5°] and phase offsets were calculated. These calculations were performed at biases that showed the best polarization switching performance.

We demonstrate in Fig. 4 control of polarization phase offset by rotating the current injection angle α . The measured data follows a $\cos^2(\alpha)$ dependence. The largest offsets between polarization states occurred every 90° with respect to the $\langle 110 \rangle$ axis. Minimal polarization phase offsets were found to occur when current was aligned to the $\langle 010 \rangle$ and $\langle 100 \rangle$ directions. This is related to the angle-dependent nature of the transition matrix element. Sopra *et al.* looked at birefringence in VCSELS [16] and showed that birefringence followed a similar trend. It is possible that other effects play complimentary roles in controlling polarization switching.

V. CONCLUSION

In this letter we have demonstrated a novel dual intracavity VCSEL capable of controlled switching between polarization

states by utilizing asymmetric current injection. Additional control over the offset between polarization states was also demonstrated. A reported threshold current of 0.19 mA is the lowest reported for a asymmetric current injection controlled polarization switching VCSEL. A high extinction ratio of >21 dB was also achieved between orthogonal polarization states. The output polarization was shown to fit a sinusoidal function with a polarization rotational frequency of 2 rad^{-1} .

ACKNOWLEDGMENT

The authors would like to thank Dr. M. Gross for his contributions.

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High-Speed Potential of Field-Induced Charge-Separation Lasers for Short-link Applications

Chin-Han Lin¹, Yan Zheng¹, Matthias Gross³, Mark J. W. Rodwell¹, and Larry A. Coldren^{1,2}

¹Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106, USA

²Department of Materials, University of California, Santa Barbara, CA 93106, USA

³Ziva Corporation, San Diego, CA 92121, USA

Phone: 1-805-893-7065 Fax: 1-805-893-4500 Email: chinhan@ece.ucsb.edu

Abstract – Novel three-terminal FICSLs in VCSEL form were designed and fabricated for direct gain modulation, which by analysis introduces an additional zero to the modulation transfer function and promises modulation bandwidth enhancement.

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OCIS codes: (140.7260) Vertical cavity surface emitting lasers; (140.3430) Laser theory; (060.4080) Modulation

I. Introduction

As the microprocessor performance scales and the number of cores in supercomputers increases, high-speed, high-efficiency VCSELs have become more and more attractive for applications ranging from chip-to-chip to box-to-box optical links. Over the recent years, state-of-the-art diode VCSELs have demonstrated above 35 Gbit/s operation and above 20 GHz bandwidth at different lasing wavelengths [1-3]. These breakthroughs were made possible by enhancing the modulation bandwidth, which is limited by the double-pole roll-off of the relaxation resonance response as well as carrier transport effects [4].

II. Modulation Bandwidth Enhancement via Direct Gain Modulation

Arising from the interaction between carrier and photon rate equations, relaxation resonance frequency plays an important role in laser performance. As illustrated in Fig. 1, the modulation transfer function can be characterized with the relaxation resonance frequency ω_R and the damping factor γ . Hence, all diode lasers have a 40 dB/decade roll-off when operated at the high frequencies. According to the expression for relaxation resonance frequency, there are several possible ways to increase the relaxation resonance frequency.

$$\text{Modulation transfer function } \frac{P_{ac}(\omega)}{P_{ac}(0)} = H(\omega) = \left(\frac{\omega_R^2}{\omega_R^2 - \omega^2 + j\omega\gamma} \right)$$

$$\text{Relaxation resonance frequency } f_R = \frac{\omega_R}{2\pi} = \frac{1}{2\pi} \sqrt{\frac{v_s a}{qV_p} \eta_i (I - I_{th})}$$

| | |
|----------|----------------------|
| v_s | Group velocity |
| a | Differential gain |
| η_i | Injection efficiency |
| V_p | Optical volume |
| I_{th} | Threshold current |

Fig. 1. Modulation transfer function and relaxation resonance frequency of lasers.

Firstly, we can increase the differential gain a . Common ways to increase the differential gain include introducing delta or modulation p-doping into the quantum well barriers, and increasing the strain in the quantum wells, such as adding more indium in the InGaAs/GaAs quantum well system [5]. In addition, active region composed of quantum dots can be an alternative candidate to provide high differential gain [6].

Secondly, we can reduce the optical mode volume V_p . Selective oxidation is a common way to confine the optical mode laterally, and tapered oxide apertures have been shown to reduce the mode volume effectively without introducing extra loss [7]. It is also possible to further reduce the optical mode volume in the longitudinal direction by utilizing high-reflectance mirrors such as high-contrast grating (HCG) reflectors [8].

Last and perhaps the easiest way is just increasing the bias current I , as the modulation bandwidth can be steadily enhanced by increasing the current above threshold. However, there will be a point that the damping effect and thermal limitations start to dominate. Also, operating VCSELs at high current densities can be detrimental to the device lifetime.

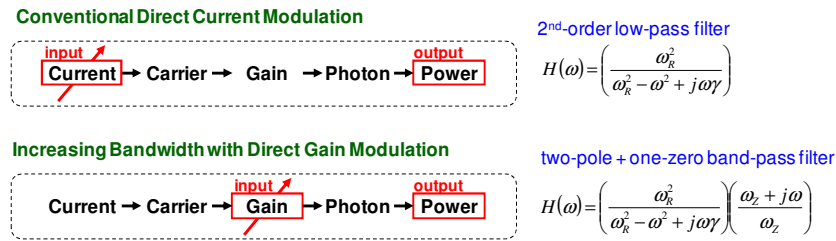


Fig. 2. Modulation chain effects and transfer functions of conventional current-modulated lasers (upper) and gain-modulated lasers (lower).

The conventional current-modulation can be characterized with a “C2GP2” chain, as shown in upper part of Fig. 2. The laser driver modulates the current, which populates the active region with carriers. Carriers provide gain to the optical mode and generate photons, part of which comes out of the cavity as the output power. The result is the double-pole or 2nd-order low-pass filter type of frequency response. If we can find a way modulate the gain directly, this chain effect will be shortened, as shown in the lower part of Fig. 2. From our analysis, the shortened chain effect adds an additional zero, which we defined as ω_z , to the original two-pole transfer function. The result is a two-pole, one-zero band-pass filter type of frequency response for the gain-modulated lasers. As we are going to show in the next section of this paper, ω_z plays an interesting role for modulation bandwidth enhancement.

III. Field-Induced Charge-Separation Laser (FICSL)

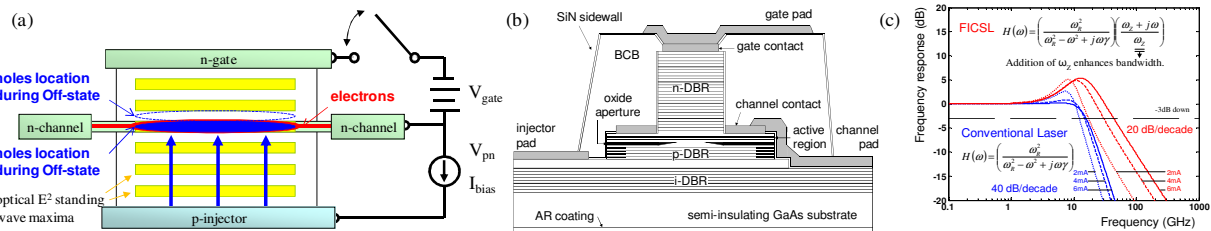


Fig. 3. (a) FICSL operation mechanism. (b) Cross-sectional schematic of a FICSL. (c) Modeled small-signal response comparison of a conventional laser and a FICSL with the same parameters and reduced carrier lifetime. Bias current I_{bias} was 2mA, 4mA and 6mA.

To realize direct gain modulation, the field-induced charge-separation laser (FICSL) was built by adding a third terminal to a convention dual-intracavity-contacted diode VCSEL, as shown in Fig. 3a. Electrons are injected laterally into the active region from the upper intracavity n-contact, which we also defined as the **n-channel**. Holes are injected from the bottom intracavity p-contact, which we defined as the **p-injector**. Electrons and holes overlap and recombine radiatively at one of the optical standing wave maxima. The modal gain is maximized and the carriers can recombine radiatively and provide gain to the optical mode. This is the On-state of the FICSL.

To turn off the laser, a negative bias is applied to the third terminal, which we defined as the **n-gate**. Driven by the external electric field, the holes will be pulled toward the gate, and the electrons will be pushed away from the gate. The two types of charges are separated and the modal gain is reduced, therefore the laser output is also reduced. One can clearly see that with the application of gate voltage, the gain can be modulated directly without changing the bias current. Devices were designed and fabricated with details described in ref. [9] and the schematic is illustrated in Fig. 3b.

Fig 3c compares the frequency response of FICSLs versus conventional diode lasers. Unlike the 2nd-order low-pass filter response of conventional diode lasers, the FICSL response ramps up around the additional zero frequency ω_z , peaks around the relaxation resonance ω_R , and then features a 20dB roll-off at the high-frequencies. Consequently, with the same relaxation resonance frequency and damping factor, FICSLs will have a much higher 3dB cutoff frequency than conventional diode lasers.

Furthermore, the 3dB cutoff frequency of FICSLs scales with the bias current almost linearly, while the 3dB cutoff frequency of a conventional diode laser saturates regardless of bias current increase, as shown in Fig 4a. For more accurate modeling, thermal limitations and parasitic effects have to be considered. In this case, the 3dB cutoff frequency of FICSLs will be lower than what Fig 4a predicts but still higher than that of conventional diode lasers.

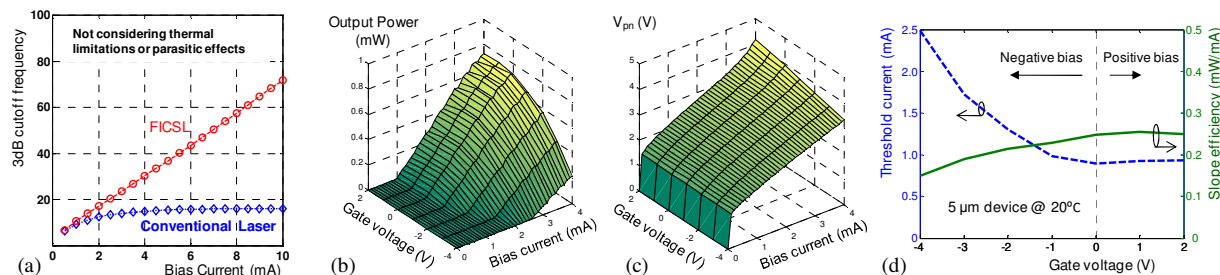


Fig. 4. (a) Modeled 3dB cutoff frequency comparison a conventional laser and a FICSL assuming no thermal limitations or parasitic effects. (b) L - I_{bias} - V_{gate} plot. (c) I_{bias} - V_{pn} - V_{gate} plot. (d) Threshold current and slope efficiency as a function of gate voltage.

IV. Experimental Results

To verify the gain modulation effect, the device was tested by DC L-I-V setup with different gate voltage applied. The results are summarized in Fig. 4b-4d. When there was a positive voltage on the n-gate, the threshold current and the slope efficiency did not change significantly. If we put a negative bias on the n-gate, an increase of the threshold current, a reduction of the slope efficiency and a reduction of the output power could be observed. Direct modulation with the gate voltage was demonstrated. However, the required voltage swing was around 4V peak-to-peak, much higher than expected. This indicated that the fabricated FICSLs had very large resistance in the n-DBR which consumed a large voltage drop. The large n-DBR resistance also limited the small-signal bandwidth to be around 11GHz [9]. The parasitic time constant determined by the n-DBR resistance and the junction capacitance became a limiting factor to prevent good observation of the high frequency roll-off.

V. Conclusion

We have demonstrated the novel theory of direct modulation via field-induced charge-separation in FICSLs. Analysis showed an addition of zero to the conventional two-pole transfer function. Simulation showed that due to the additional zero, FICSLs were promised to have much higher modulation bandwidth than conventional diode VCSELs. Experimental results verified the physics of field-induced modulation, but the high resistance in the n-DBR increased the voltage required for modulation, and limited the RF performance.

Acknowledgement

This work was supported by DARPA through a STTR with Ziva Corp. and by NSF through a GOALI program. A portion of this work was done in the UCSB nanofabrication facility, part of the NSF funded NNIN network.

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Implant Enhanced Dual Intracavity Polarization Switching Asymmetric Current Injected VCSEL

Yan Zheng[†], Chin-Han Lin[†] and, Larry A. Coldren^{†*}
[†]*Department of Electrical and Computer Engineering*
^{*}*Department of Materials*
 University of California, Santa Barbara 93106

Abstract

Output polarization is controlled by injecting current along crystalline directions. VCSELs with record-low threshold current of 0.19 mA and extinction ratio >21dB from fit is achieved. Polarization switching is shown to be enhanced by implantation.

OCIS codes: 140.7260 Vertical cavity surface emitting lasers, 130.5440 Polarization-selective devices

I. Introduction

Meeting the needs of next-generation computational systems and data centers will require a concerted effort on many different fronts. Vertical-cavity surface-emitting lasers (VCSELs) have emerged in this effort as a valuable platform because of their reliability, high speed characteristics, and their ability for onchip integration of components such as microlenses. Recently our group has demonstrated 980 nm VCSELs capable of 35Gb/s error-free operation with a very low-threshold of only 0.144 mA [1]. Still, other avenues such as polarization control can be explored for other innovative approaches. For instance, output polarization control can increase the bit/symbol density by additionally embedding polarization information. Other work has also demonstrated 40Gb/s NRZ optical memory using a polarization bistable VCSEL [2].

Although polarization stability has been demonstrated using various geometries, off-axis crystal surfaces, and surface gratings [3]-[5], these devices lose the functionality that comes with complete output polarization control. Recently several groups have investigated asymmetric current injection (ACI) as a way to introduce gain anisotropy to control output polarization [6]-[7]. We demonstrate switching between two orthogonal polarization states via asymmetric current injection utilizing a novel dual intracavity contacted circular mesa design. A record-low threshold current of 0.19 mA was achieved. Deuterium (D^+) implantation in the p-contact layer was also investigated to reduce lateral current spreading.

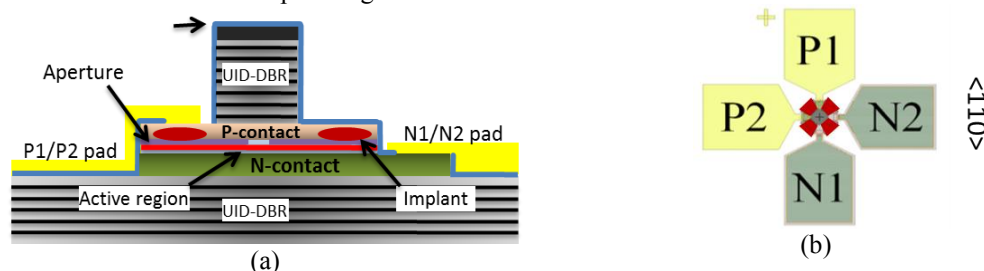


Fig. 1 a) Polarization switching VCSEL schematic. b) Top view showing contact pads relative to $\langle 110 \rangle$. Ion implant locations shown in red.

II. Growth and Fabrication

Devices were grown using molecular beam epitaxy (MBE) on undoped (001) GaAs starting with 18 periods of GaAs/AlAs to form the bottom DBR mirror followed by 420nm of Si doped GaAs for the n-contact layer. The p- and n-contact layers were grown close together to increase current directionality. The active region consists of three 8nm thick $In_{0.2}Ga_{0.8}As$ quantum wells separated by 8nm GaAs barriers surrounded by a 30% AlGaAs separate confinement heterostructure (SCH). A linearly graded AlGaAs region then forms the oxide aperture. A modulation carbon doped GaAs p-contact layer is grown followed by 32 periods of 85% AlGaAs/GaAs to form the top mirror.

Circular mesas were created in a two-step dry-etch process that stops in the intracavity contact layers using a laser etch-monitor. An oxide aperture was created and a third etch removes the n-contact layer except from where the n-metal pads will be to help isolate orthogonal electron paths. A blanket SiN layer is deposited and four equally

spaced vias are opened around the mesa for metal contacts. The pad layout, shown in Fig. 1b is designed to break the conventional current injection symmetry and increase current directionality. Above threshold where there is sufficient state filling, current direction is used to provide a significant lateral carrier momentum component to control output polarization. Deuterium was also implanted into the p-contact layer in areas that straddle current injection paths shown in Fig. 1.

III. Experimental Results

Light output (LI) first passes through a rotating polarizing lens and then is measured by a Si photodetector. The polarizer transmission axis is aligned to the 0° marker on the rotational mount which is then aligned, by eye, to the <110> axis of the wafer.

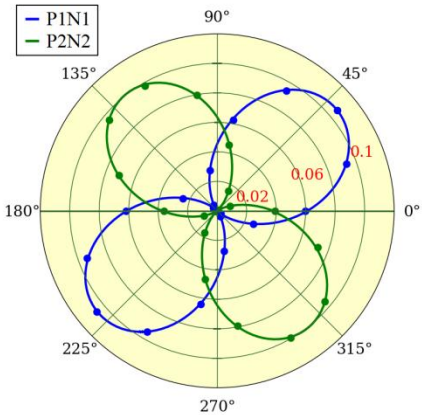


Fig. 2 Output power (radii-a.u.) and polarizer angle at 2.0 mA for the P1N1 and P2N2 current directions. 0° is aligned to the <110> axis.

LI curves were taken for every 20° rotation of the polarizer with either the P1N1 or P2N2 configuration probed. Light output of the device at a bias of 2 mA is plotted against the polarizer rotation angle to generate the polarization resolved polar plot shown in Fig. 2. Two polarization states are clearly shown with a phase offset of approximately 90°. The measured data fit very well to a sine wave with a R² value >0.999 and both showing a polarization rotational frequency of 2rad⁻¹. From the fit, record extinction ratios >21dB between polarization states were achieved at a bias of 2 mA.

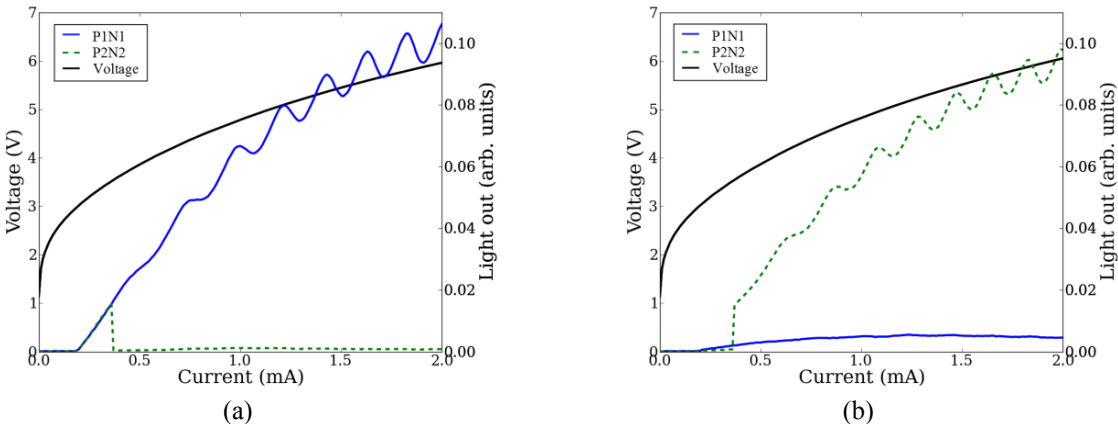


Fig. 3 LIV curves for orthogonal current directions with polarizer transmission axis a) 40° to the <110> axis b) and 120° to the <110> axis.

CW LIV curves for two polarization states under asymmetric current injection conditions are shown in Fig. 3. A typical IV curve shows a turn-on voltage of 1.7 V and is smooth when the polarization switches and throughout the rest of the current range. The threshold current of 0.19 mA is the lowest reported for an ACI VCSEL. Light output was found to be polarized close to 40° from the <110> axis when biasing the P1N1 pads. The output from biasing the P2N2 pads has the same polarization up until 0.37 mA where it then switches polarization and is almost completely extinguishing. At a polarizer angle of 120°, LI curves taken for both the P1N1 and P2N2 current injection directions are mirror opposites of that seen at 40°, shown in Fig. 3(b). The P2N2 output is slightly higher

because the data was not taken at the optimal polarization splitting angle. Ripples in the light output are believed to be from local heating and which disappear under 1 μ s pulsed conditions.

The enhancement of polarization switching from implantation is illustrated in Fig. 4. For a device that did not show polarization splitting from ACI, when implanted with D^+ , the output polarization showed a polarization phase offset of approximately 90° . The P2N2 polarization state slightly rotates clock-wise while the P1N1 state rotates in the counter clock-wise direction. Increased loss from the implant is suspected to be the cause of the slight reduction in output power.

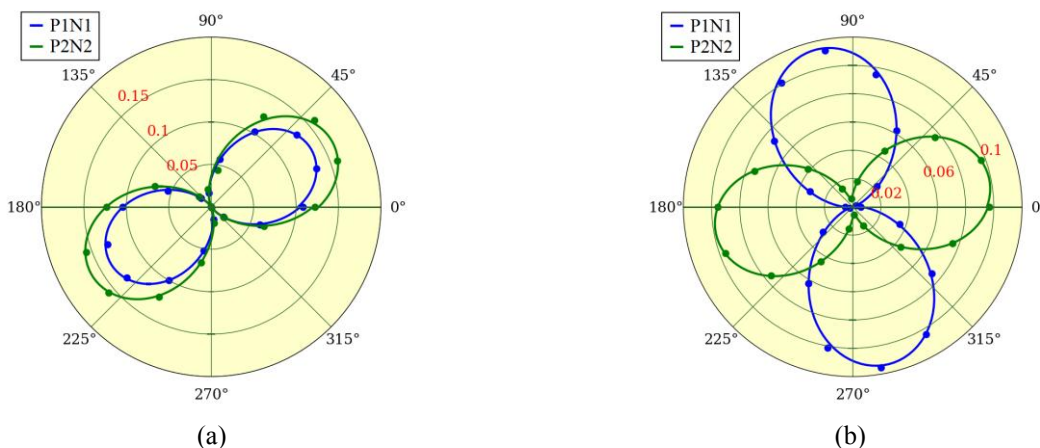


Fig. 4 Output power (radii-a.u.) and polarizer angle for the P1N1 and P2N2 current directions of a device a) before D^+ implantation and b) after D^+ implant. The 0° horizontal axis is aligned to the crystalline $\langle 1\bar{1}0 \rangle$ axis.

V. Conclusion

A VCSEL capable of controlled switching between polarization states by changing the direction of current injection was demonstrated. The measured threshold current of 0.19 mA is the lowest reported for an asymmetric current injection polarization switching VCSEL. Output polarization profile was fit to a sine wave where a record high extinction ratio of >21 dB was obtained between orthogonal polarization states. Deuterium implantation was also shown to enhance polarization splitting.

VI. Acknowledgements

This work was supported by DARPA through a STTR with Ziva Corporation.

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Lateral Carrier Injection with n-type Modulation-doped Quantum Wells in VCSELs

Chin-Han Lin¹, Yan Zheng¹, Matthias Gross³, Mark J. W. Rodwell¹, and Larry A. Coldren^{1,2}

¹Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106, USA

²Department of Materials, University of California, Santa Barbara, CA 93106, USA

³Ziva Corporation, San Diego, CA 92121, USA

Phone: 1-805-893-7065 Fax: 1-805-893-4500 Email: chinhan@ece.ucsb.edu

We have demonstrated a novel Field-Induced Charge-Separation Laser (FICSL) in a Vertical-Cavity Surface-Emitting Laser (VCSEL) embodiment. In addition to the initial optical modulation results that have been presented [1], we here for the first time present details on the novel lateral charge injection structure as well as the advanced bandgap engineering involved in the gate structure. These features together permit high-speed light modulation with a nearly constant injection current. The result is an entirely new concept for high-speed directly-modulated semiconductor lasers.

In conventional diode VCSELs, carriers are typically injected into the quantum wells from the perpendicular direction (Fig. 3a-b). The common epitaxial design is a SCH (Separate Confinement Heterostructure) with p-type and n-type DBR mirrors on the opposite side of the active region. On the other hand, to realize direct modulation via a gate voltage, any highly doped intra-cavity contact layer above the quantum wells such as in Fig. 3b would pin the Fermi level, screening the driving force from the gate. Hence, carriers have to be injected laterally into the active region (Fig 3c). To allow only hole movement and isolate the electrons between the active channel and the off-state well, the first period of the n-DBR has to be band-gap engineered to form a quantum barrier (Fig. 4).

Lateral injection of carriers into quantum wells has been demonstrated on lateral current injection (LCI) lasers. However, the sheet resistance in LCI lasers is typically 2-3 times higher than a vertically-injected ridge laser with the same dimensions [2]. In a VCSEL structure, the comparatively small dimensions makes the sheet resistance even more detrimental, especially when there has to be a finite setback distance d between the current aperture edge and the metal ring contact to avoid absorption loss (Fig. 1). To enhance the conductivity of lateral injection, delta-doping can be applied to the quantum well barriers to provide free carriers.

Early research showed that modulation doping was promising for quantum well performance [3]. Furthermore, both n-type and p-type doped quantum wells have been incorporated into diode lasers and demonstrated the reduction of threshold current density [4, 5]. However, doping near the optical standing wave E^2 peaks has to be treated carefully since the increase in absorption loss and dopant scattering may compromise overall performance, rendering the delta-doping benefit marginal.

To examine lateral injection with two-dimensional electron gas (2DEG) and two-dimensional hole gas (2DHG), three $\text{In}_{0.2}\text{Ga}_{0.8}\text{As}/\text{GaAs}$ quantum well samples were grown by Molecular Beam Epitaxy with different delta-doping level in the barriers; silicon was used for n-doping, and carbon via a CBr_4 source was used for p-doping. The sheet charge density and the carrier mobility of these samples were acquired by room temperature Hall measurement, and the overall sheet conductivity was calculated (Fig. 5). It is clear that due to the large difference in mobility, the conductivity of 2DEG is more than one order of magnitude higher than a 2DHG with the same sheet charge density. Material gain of the modulation-doped quantum wells was characterized by fabricating broad area lasers. It was confirmed that both n-type and p-type modulation-doping reduced the transparency current density, while p-type doping also increased the differential gain, dg/dJ (Fig. 6).

Due to the large difference in conductivity, n-type modulation-doped quantum wells are chosen to form the active channels. FICSLs were fabricated and the measurement results are shown in Fig. 7. The required gate voltage swing was higher than expected, indicating that the fabricated FICSLs had very large resistance in the n-DBR, causing a large voltage drop. The large n-DBR resistance also limited the small-signal bandwidth to be around 11GHz [1]. The differential series resistance between injector and channel was measured to be 550Ω in a $5\mu\text{m}$ (aperture diameter) device.

This work was supported by DARPA through a STTR with Ziva Corp. and by NSF through a GOALI program. A portion of this work was done in the UCSB nanofabrication facility, part of the NSF funded NNIN network.

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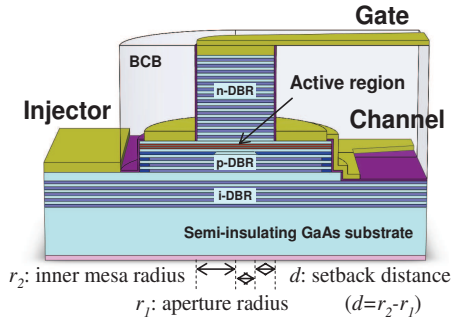


Fig. 1. Schematic of a FICSL. The injector-channel junction is DC biased, while the gate is the modulation terminal.

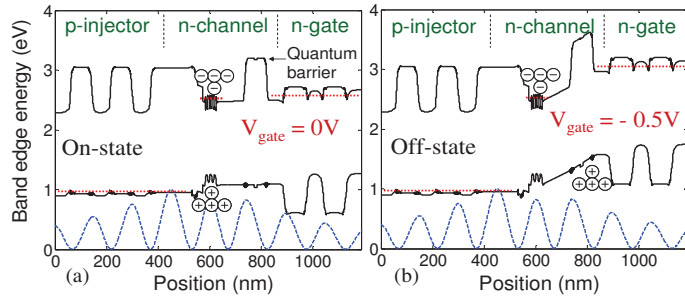


Fig. 2. Band diagrams of a FICSL (a) on-state: electrons and holes are aligned with a standing wave E^2 peak to provide gain. (b) off-state: a negative bias is applied to the gate, driving holes away from electrons and reducing output power.

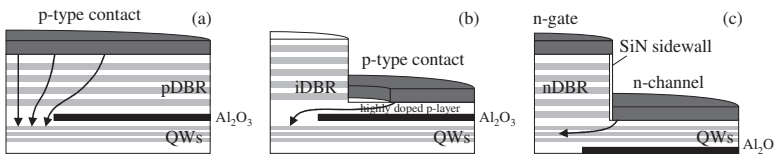


Fig. 3. Structural comparison of oxide-confined VCSELs: (a) top-contacted (b) intra-cavity contacted (c) laterally injected FICSL with top gate for modulation (this work). Arrows depict carrier injection flows. Oxide aperture layers are typically placed on the p-side due to the low spreading characteristics of holes compared to electrons.

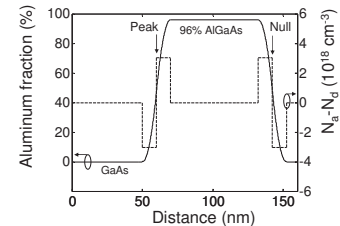


Fig. 4. Quantum barrier design to isolate electron transport.

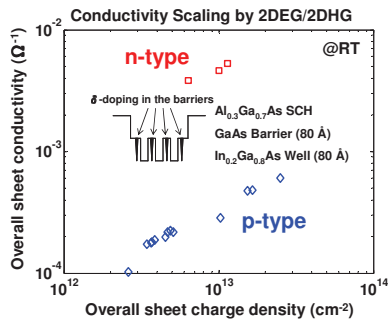


Fig. 5. Sheet charge conductivity of 2DEG and 2DHG in three modulation δ -doped quantum wells.

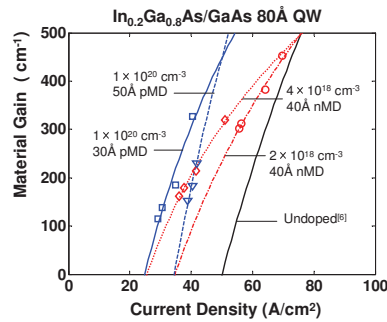


Fig. 6. Gain characteristics of modulation-doped QWs. Both n-doping and p-doping reduce transparency current density.

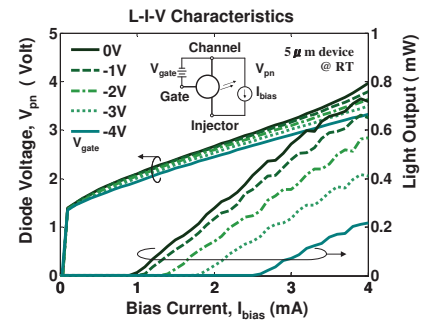


Fig. 7. DC performance of FICSL. Above threshold, negatively biasing the gate would reduce the light output given the same bias current to the injector-channel junction.

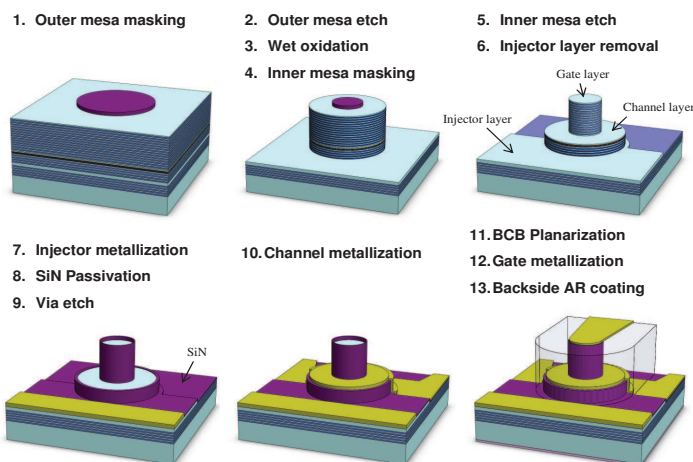


Fig. 8. Process flow for FICSLs. All steps are done with i-line lithography.

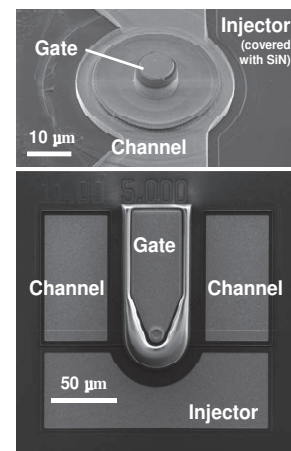


Fig. 9. SEM images of a fabricated FICSL before BCB planarization (upper) and after the completion of process (lower).

Output Polarization Dependence of Asymmetric Current Injection VCSELs on Crystalline Direction and Ion Implantation

Yan Zheng[†], Chin-Han Lin[†], Matthias Gross[‡], and Larry A. Coldren^{†*}

[‡]*Ziva Corporation, San Diego, CA 92121*

[†]*Department of Electrical and Computer Engineering*

^{*}*Department of Materials*

University of California, Santa Barbara 93106

Vertical-cavity surface-emitting lasers (VCSELs) have emerged as a valuable platform because of their reliability, high-speed characteristics, and ability for on-chip integration [1]. Recent work has also demonstrated the possibility of output polarization control [2]. By leveraging the advantages of the VCSEL platform, innovative solutions in imaging, sensing and military applications are possible. We demonstrate control between two orthogonal polarization states via asymmetric current injection (ACI) utilizing a novel dual intracavity contacted circular mesa design. Modulation doping is used in the contact layer to reduce optical loss. Deuterium (D^+) isolation implantation in the p-contact layer was also investigated to reduce lateral current spreading.

Devices were grown using molecular beam epitaxy (MBE) on undoped (001) GaAs starting with 18 periods of GaAs/AlAs for the bottom DBR mirror 420nm of Si doped GaAs for the n-contact layer. The p- and n-contact layers were grown close together to increase current directionality. The active region consists of three 8nm thick $In_{0.2}Ga_{0.8}As$ quantum wells separated by 8nm GaAs barriers surrounded by a $Al_{0.3}Ga_{0.7}As$ separate confinement heterostructure (SCH). Due to the large optical field in the p-contact region, only the standing wave nulls were doped to reduce free carrier absorption. Carbon was used in this modulation doping scheme because of its low diffusivity. The top mirror consists of 32 periods of 85% AlGaAs/GaAs. A wedding cake structure is created using standard lithographic procedures and an oxide aperture is created through a wet oxidation process. Metal contacts are laid out in a cross pattern to separately inject current in two orthogonal directions. The whole cross layout is also rotated relative to the crystal axis to investigate its effect on output polarization. Deuterium was also implanted into the p-contact layer in areas that straddle current injection paths to reduce lateral current spreading.

Light output (LI) first passes through a focusing lens/rotating polarizer combination and is then measured by a Si photodetector. Each arm of the diode is biased separately and the output polarization is measured. A measured phase difference of 90° means that the two outputs are orthogonally polarized relative to each other. By rotating the current injection directions relative to the crystal axes it was found that the amount of splitting between the two polarization states follows a $\cos^2(\alpha)$ dependence. The largest offsets between polarization states occurred every 90° with respect to the $\langle 110 \rangle$ axis. Minimal polarization phase offsets were found to occur when current was aligned to the $\langle 010 \rangle$ and $\langle 100 \rangle$ directions. For one device that did not display polarization splitting from ACI as grown, after D^+ implantation the output polarization showed a polarization phase offset of approximately 90° , demonstrating the ability to suppress crosstalk between polarization paths with ion implantation.

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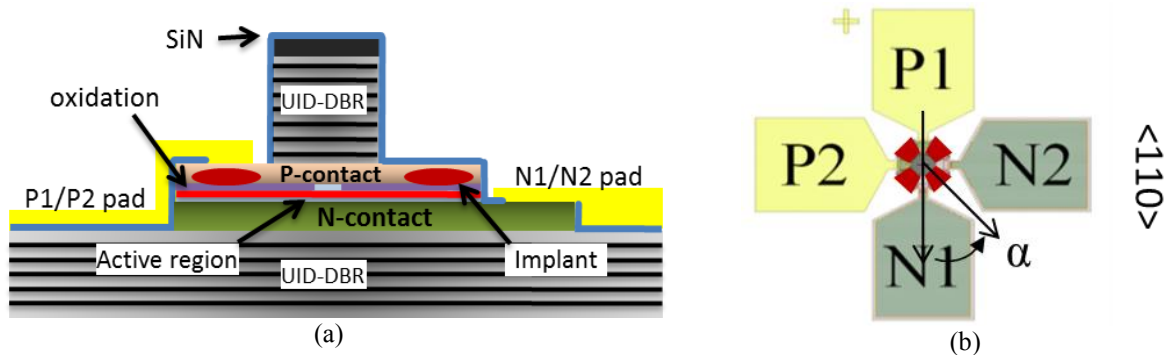


Fig. 1 a) Polarization switching VCSEL schematic. b) Top view showing contact pads relative to $\langle 110 \rangle$. Ion implant locations shown in red.

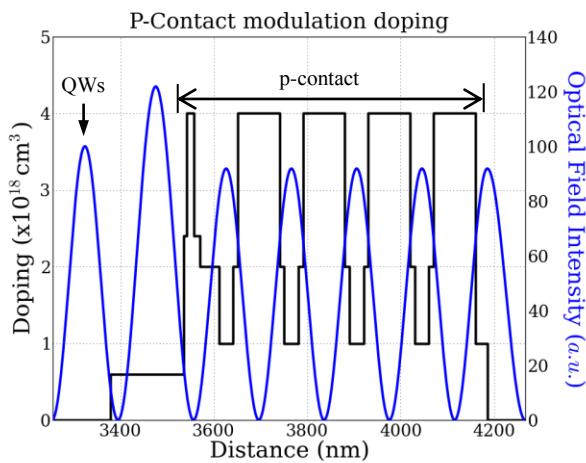


Fig. 2 Low optical loss modulation Carbon-doping of the p-contact region overlaid with optical standing wave in the laser cavity.

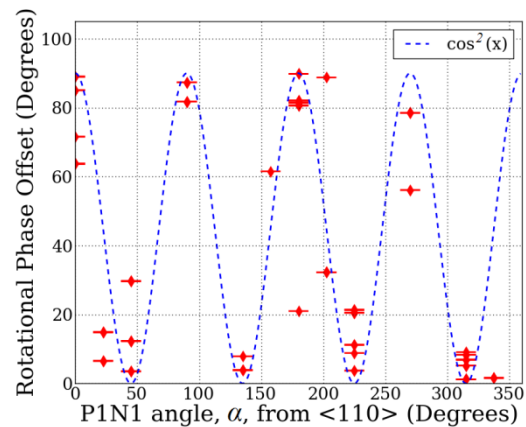


Fig. 3 Phase offsets between two polarization states measured as the current injection angle, α , is rotated.

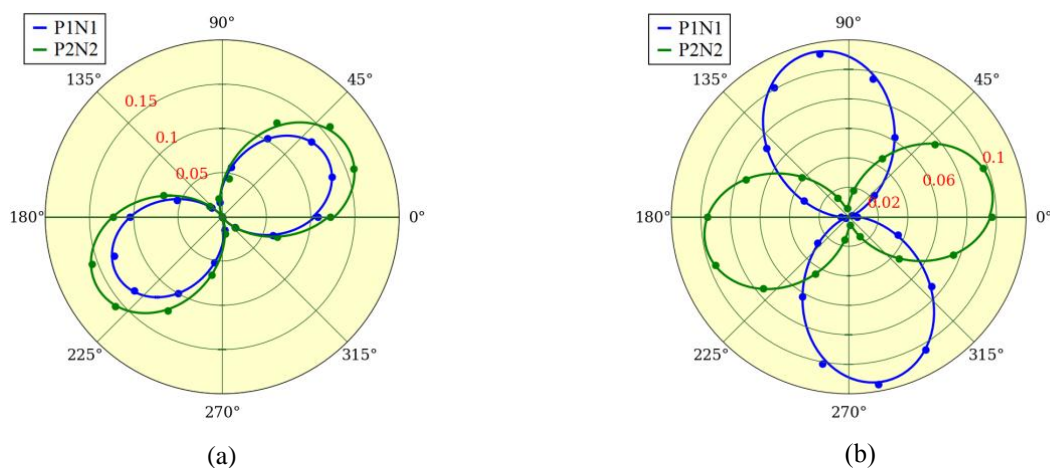


Fig. 4 Output power (radii-a.u.) and polarizer angle for the PIN1 and P2N2 current directions of a device a) before D^+ implantation and b) after D^+ implant. The 0° horizontal axis is aligned to the crystalline $\langle 1\bar{1}0 \rangle$ axis.

Efficient, High-Speed VCSELs for Optical Interconnects

Larry A. Coldren^{†*}, Chin-Han Lin[†], Yan Zheng[†]

Departments of [†]Electrical and Computer Engineering and ^{*}Materials, University of California, Santa Barbara, CA 93106
Phone: 1-805-893-4486; Fax: 1-805-893-4500; Email: coldren@ece.ucsb.edu

Abstract: The demand for efficient optical sources at high data rates is growing as the need for more interconnects and interconnect density grows in both data centers and high-performance computers. Novel vertical-cavity surface-emitting lasers (VCSELs) continue to be investigated for these applications. We conclude that more highly-strained, higher In-content devices on GaAs are a good choice because of their higher inherent efficiency, modulation speed, and reliability. A new three-terminal configuration is also being studied with some unique characteristics.

As the performance of microprocessors scales and the capacity of data centers increases, optical interconnects are recognized as superior to conventional electrical interconnects due to their low-power consumption, small size, weight, and superior bandwidth over significant path lengths [1]. Driven by this demand, high-speed, high-efficiency, high-reliability VCSELs are gaining increasing interest in such applications worldwide, and performance breakthroughs continue to occur. In fact, these new markets may eclipse existing markets for VCSELs and change the rules (standards) in the future. For example, Fig. 1 illustrates the growth of optical interconnect channels within single high-performance computers, showing that a single machine now has as many interconnects as the total worldwide volume of parallel optical channels in other applications.

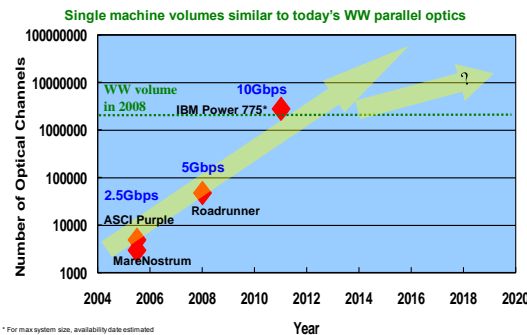


Figure 1. Number of optical interconnect channels within a single computer vs. time[1].

Highly-strained quantum-well gain regions are now well known to provide nearly all of the characteristics needed to advance VCSELs to the next level of performance and quality to meet the new challenges[2-5]. As indicated in Fig. 2 they provide high-gain, high-differential gain (high speed), and hold the promise of high reliability.

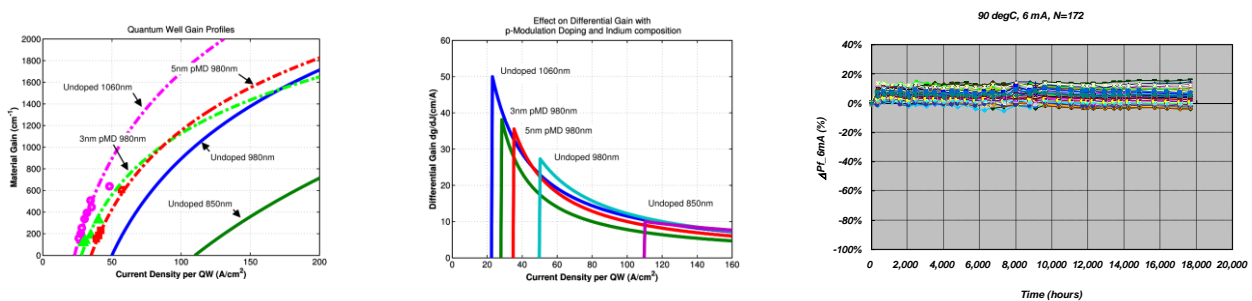


Figure 2. Material gain and differential gain, dg/dJ , versus current density per quantum well[3] together with accelerated aging data for 1060 nm VCSELs from Furukawa via IBM[1]

Co-incident to these improvements with the addition of In to the GaAs quantum wells is an increase in the emission wavelength from 850 nm to the 950 – 1100 nm range. Unfortunately, this has caused some heartburn amongst both users and suppliers as the old standards for datacom fixed the wavelength at 850 nm. Many would like to continue to stay at 850 nm to be compatible with existing applications. However, because the new data center and next generation computing applications will probably dwarf the volume of all of the prior VCSEL datacom applications [1], past standards as well as the desire to have a common product architecture may not be as relevant for these new markets.

Furthermore, it should be noted that there are a few advantages of having the longer wavelength emitters as outlined in Fig. 3: a) The GaAs substrate becomes transparent—this enables backside emission and simpler assembly/packaging techniques, including backside collimating microlenses on the chip; b) The eye-safe power threshold is approximately doubled; and c) The inherent fiber dispersion can be reduced to less than half [3].

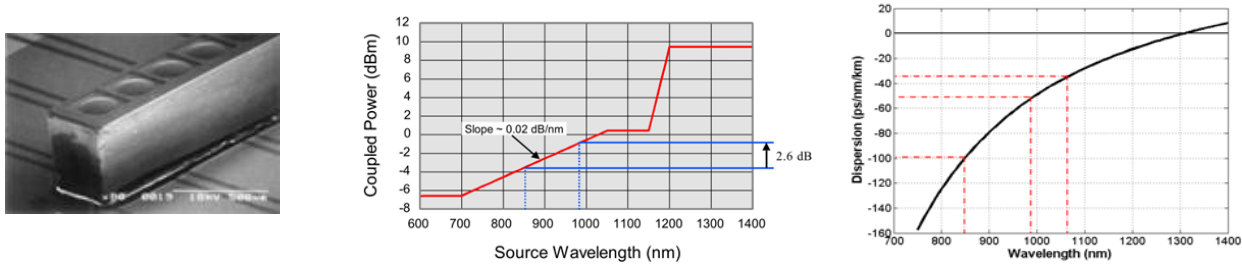


Figure 3. a) Flip-chip mounted 980 nm VCSEL with etched backside microlenses; b) eyesafe allowable optical power levels; c) fiber material dispersion[3]

As illustrated in Fig. 4, we have designed and fabricated 980nm diode VCSELs, which utilized an optimized p-DBR mirror design and deep oxidation layers to minimize parasitic effects [6]. These devices had >20GHz small-signal bandwidth and operated above 35Gb/s error-free with 10 mW of power dissipation (or 286 fJ/bit). They also were incorporated within record-efficiency IBM optical interconnect links [1].

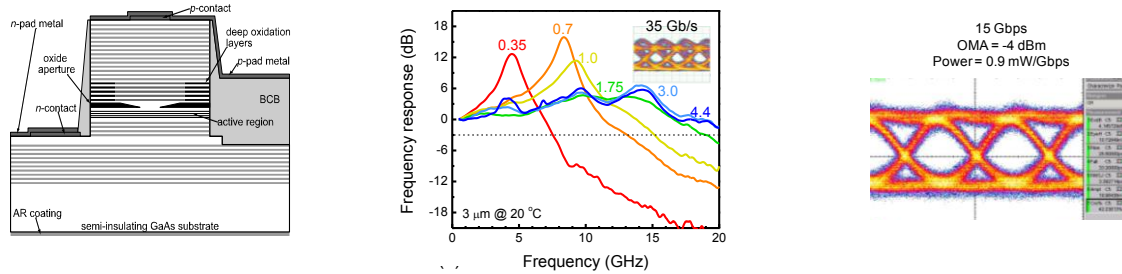


Figure 4. 980 nm VCSEL; frequency response & eye diagram @ 35 Gb/s; transmitter eye with CMOS driver (IBM)

Based on the same design rules, we further developed Field-Induced Charge-Separation Lasers (FICSLs), which introduce an extra-terminal to the diode VCSEL to be a new modulation lever (Fig. 5) [7]. By varying the bias voltage on the gate terminal, the overlap of electrons and holes in the quantum well can be modulated without changing the bias current of the p-n junction. Simulations have shown that this novel direct gain-modulation mechanism enhances the bandwidth, and the static as well as the rf characteristics of 1st generation FICSLs have been measured experimentally.

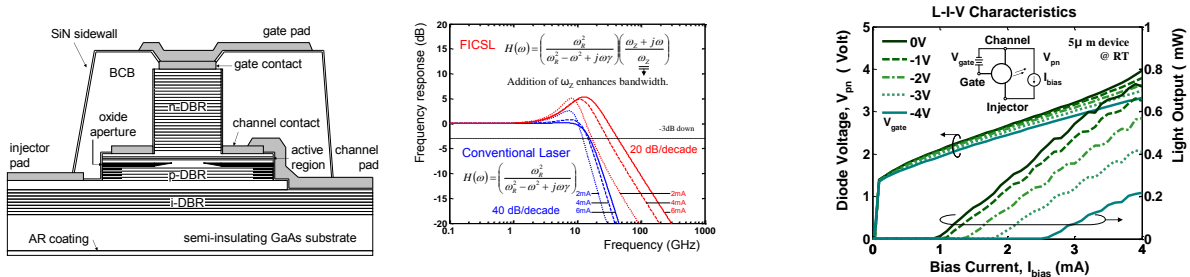


Figure 5. Field-Induced-Charge-Modulation VCSEL; theoretical frequency response compared to conventional laser; experimental gate voltage modulation[7].

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IV. MOCVD Growth

Coalescence Phenomena in Narrow-Angle Stripe Epitaxial Lateral Overgrown InP by MOCVD

Nicholas H Julian¹; Philip A Mages¹; Steven P DenBaars¹; Larry A Coldren¹; Pierre Petroff¹;
John E Bowers¹;
(1) University of California, Santa Barbara

The primary goals in Epitaxial Lateral Overgrowth (ELO) of one material over another are a) defect reduction and b) maximizing the amount of lateral growth vs. vertical growth. However, unless the material is very insensitive to defect concentrations, the usable size of even the largest field of ELO material will be cut in half by a coalescence front that creates defects when the two lateral growth wings converge. Work by Olsson et.al. has shown promising Photoluminescence (PL) results where HVPE-grown ELO InP on Si appears to have coalesced with a reduced number of recombination center defects¹. One aspect of their approach involves using the so-called zipper effect² which relies on the idea that the coalescence defects can be eliminated if the convergence of two lateral growth fronts can be arranged to occur at certain optimal angles. This is intended to avoid simultaneous convergence at multiple points along the convergence front, as experienced by parallel lines. We have investigated the zipper effect in ELO InP by MOCVD using various growth conditions on paired ELO stripes with very narrow opening angles of 5.6° along 32 different stripe directions ranging from $[-110]$ to $[1-10]$. This is in contrast to the usual approach of using large opening angles that maximize the amount of lateral ELO material per length of coalescence front. We observe multipoint coalescence as forming dimples or voids along the coalescence front and find that their formation occurs most often in the orientations with the highest overall coalescence rate. Our results illustrate the balance between mixed-plane sidewall formation and lateral sidewall growth rate, allowing optimization of multipoint coalescence and the resultant dimples. We present SEM images showing that slight deviations from high rate/high void orientations and tuning of growth parameters, especially Phosphorus overpressure, allow for the elimination of these voids by changing the sidewall faceting at the moment of coalescence. Further information from ongoing Atomic Force Microscopy, Luminescence and Transmission Electron Microscopy characterization of the resulting coalescence fronts will be presented as well.

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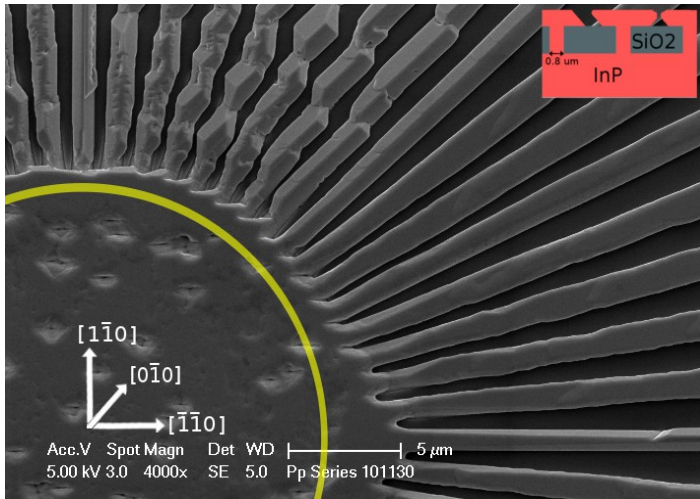


Figure 1: Morphological dependence on stripe direction. Notice the stripes above the [0-10] direction are highly faceted while those below have smoother growth fronts.

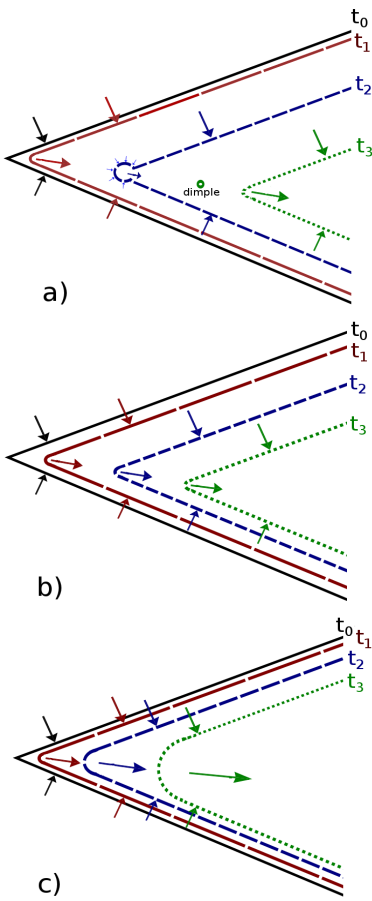


Figure 2: Illustration of the convergence of two directional growth fronts yields a third of dissimilar growth rate. This drawing illustrates the result when this third growth direction is a) slower than, b) equal to, and c) faster than the sum of the two merging growth front vectors. When this direction is too slow, dimples form. When this direction is fast, the neighboring sidewalls tend to be too slow.

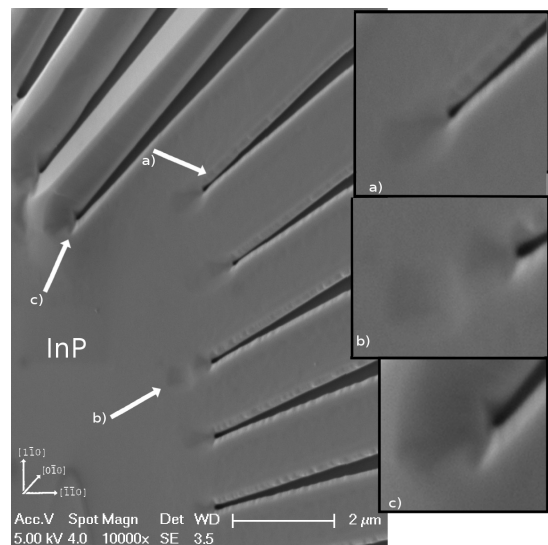


Figure 3: A variety of convergent growth directions and sidewall morphologies, illustrating a) near convergence of sidewalls, b) a resultant dimple, c) lowest rate of convergence for the most dissimilar sidewall morphologies.

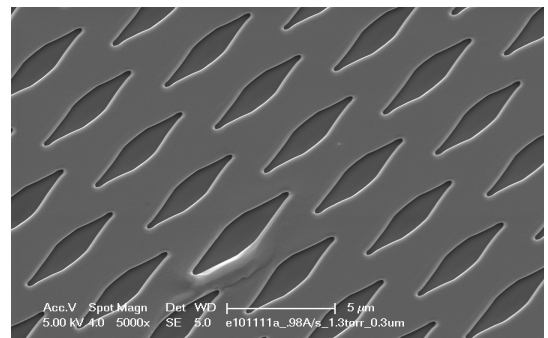


Figure 4: Islands over which opposing growth fronts move faster than their common intersection points, a prelude to dimple formation.

Growth Habit Control of Epitaxial Lateral Overgrown InP on Si Substrates by MOCVD

Phil Mages, Nick Julian, Chong Zhang, Larry Coldren, Steve Denbaars,
John Bowers *ECE & Material Science Departments, UCSB*

In this work we revisited the oft-attempted idea of Epitaxial Lateral Overgrowth (ELO) of InP on Si. Owing to the large number of failed attempts at this goal in the past, we have refocused our efforts on a few key growth and geometric relationships that seem to be held in common between InP-on-Si and the more successful c-plane III-Nitrides on sapphire ELO system. In contrast to most past attempts we do not focus initially on the all-important lateral/vertical growth ratio. Instead we consider the creation of an ELO film from the perspective of four key phases: Nucleation within the windows; Cresting of the III-V to the height of the dielectric; steady-state Lateral Propagation; and Film Coalescence. Each phase has different requirements for the sake of reducing defects, propagating laterally and producing a smooth film. Throughout this whole process we focus most closely on the detailed crystal habit of the growing films. We do this because in the past it has been found that lateral growth is easily stalled at some point during attempts to extend growth laterally until coalescence[1]. It has been found that the growth habit or cross-sectional faceting of the ELO material is strongly correlated to the orientation of the stripe opening [2]. We find that both of these results are due to the tendency of certain growth-limiting facets to form and have located parameter windows in which we can control the growth habits of the films during each phase of the ELO process. Namely, we present the results of varying stripe/mask geometry and orientation and discuss the most significant growth condition effects on the morphology of the films prior to and during coalescence. The result is the controllable production of stripes having sidewall geometries ranging from linear and smooth through strongly faceted and weakly roughened. We control profiles showing variation between the natural preference for (111)A and B planes and mixed plane circumstances of differing value for continued lateral propagation and coalescence. Primarily we show that the cross-sectional growth habit of the ELO material is extremely sensitive to stripe orientation with misalignments as small as 5° being very significant. Secondly we demonstrate that the effective local overpressure of Phosphorous (TBP) at the lateral growth front is most important to the sidewall formation and faceting at any growth rate or mask geometry.

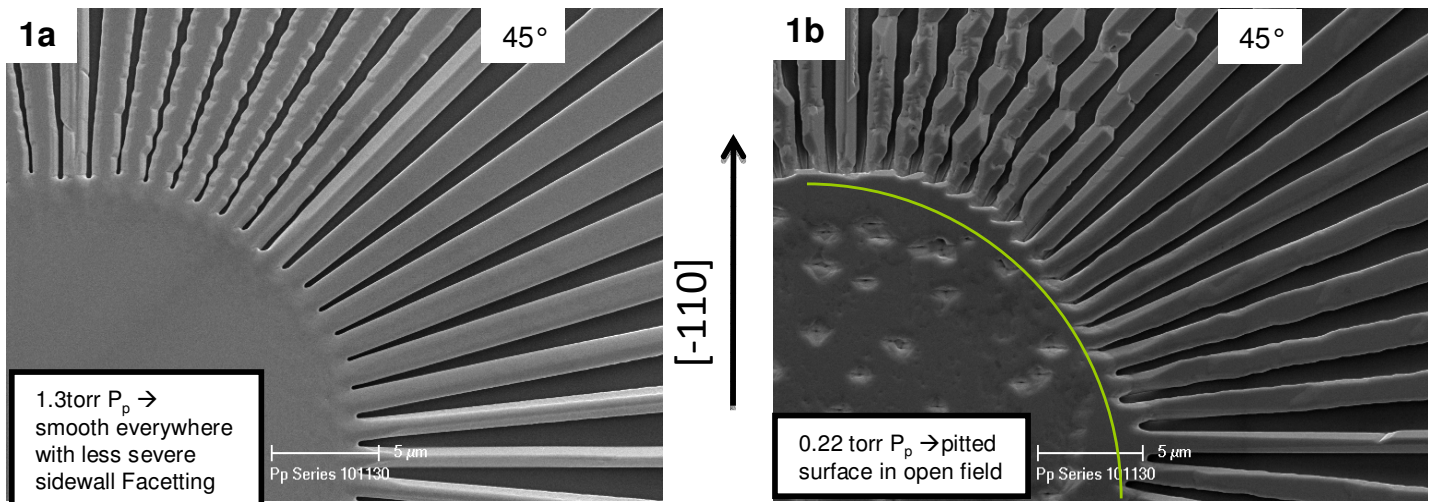
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“Growth Habit Control of Epitaxial Lateral Overgrown InP on Si Substrates by MOCVD”

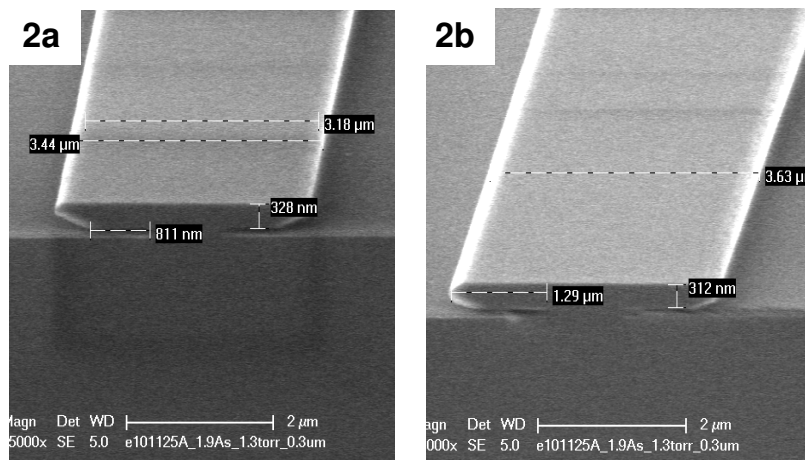
Phil Mages, Nick Julian, Chong Zhang, Steve Denbaars, Larry Coldren, John Bowers

Figures 1a,b: Wagon wheel patterns showing selectively grown stripes in plan view. A strong transition exists at the 45° [010] line. Facetted/rough sidewalls become very straight.



Most clearly in 1a it is seen that the [010] line is strongly pyramidal in cross section while lines between [-110] and [010] have slightly tapering sidewalls leading to a flat top. Lines between [010] and [110] (90°) have very flat tops, which cross section correlates with undercut “dovetail” sidewalls.

Figure 1b: Extremely low phosphorus pressure in figure 1a exaggerates sidewall faceting effects as well as preferential coalescence in directions *not* having the largest lateral growth rates.



Figures 2a,b: “Soft” transition between dovetail growth mode and semi-vertical sidewalls close to the [-110] direction. 2a shows a stripe at ~11° off of [-110] and 2b a stripe ~17° off.