InP-Based Photonic Integrated Circuits

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Abstract: The monolithic integration of a number of photonic components on a single InP chip for increased functionality and reliability as well as decreased power dissipation and cost is becoming an accepted goal for most component vendors. This tutorial will review current integration approaches and results, emphasizing our UCSB work.

1. Introduction

InP-based Photonic Integrated Circuits (PICs) have been discussed and researched since the late 1970s when the InP based materials were still in an early stage of development[1-3]. A significant amount of work in the 1980s and early 1990s demonstrated many of the integration techniques still in use today[3-8]. However, for many years success with hybrid integration techniques has slowed the commercial adoption of PICs, except for a few limited examples, such as the integration of an electro-absorption modulator (EAM) with a DFB laser (the so-called EML). In fact, some have argued that PIC approaches would rarely replace feasible hybrid approaches for many years to come. Recently, these 'hybrid-integration-forever' advocates seem to have gone quiet, and some have even had the epiphany that 'PICs are now the only way to go'. Clearly, there have been some recent existence proofs of complex PICs that appear to have numerous advantages over hybrid approaches[9,10]. Time will tell, but the thesis of this tutorial will be that PICs are now seen as the preferred approach for many applications, and as such, they will be the subject of intense R & D at many commercial component vendors in the next couple of years. It is even possible that some new PIC technologies, such as quantum-well intermixing (QWI)[11], will gain widespread acceptance for real commercial applications.

2. Integration Platforms

At the core of most PICs is a basic active-passive waveguide integration technique, and this largely determines the viability of the resulting integration platform. Figure 1 illustrates several active-passive integration approaches that have been used with some success. Of course, by 'passive' we may be referring to a modulator region or a truly passive interconnecting waveguide.

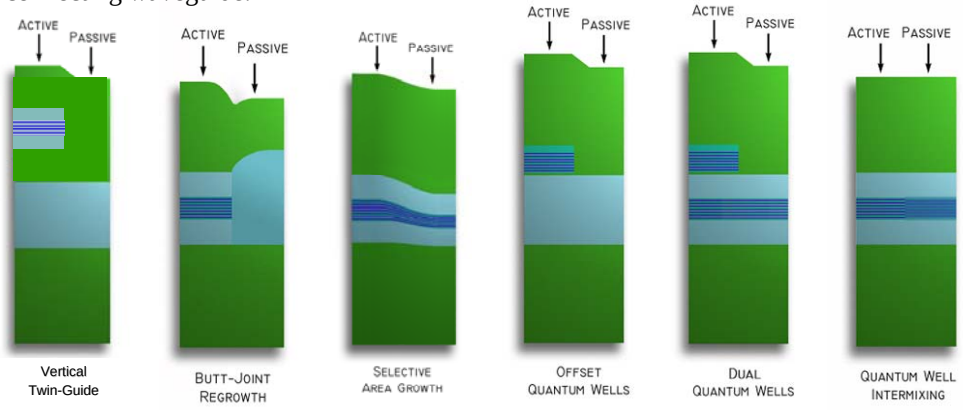

Figure 1. Schematics of six integration platforms. All have been used in commercial products.

Pros and Cons of each of the integration platform shown in Fig. 1 include the following: the vertical twin guide allows for independent properties in the upper and lower guides, but a long coupling length is needed to accomplish the vertical light transfer; the butt-joint regrowth approach also allows for independent properties in the active and passive sections, but a critical alignment of the regrown waveguides is necessary; the selective area growth technique provides a scaling of the vertical dimensions to change the absorption edge of the quantum-wells, but the properties of each are still linked and the patterned growth results in some transition length as well as being critically dependent on the lateral diffusion properties of the precursors; the offset quantum-well approach only requires an

unpatterned blanket regrowth over a small step after etching away the active wells, but offsetting the gain results in a reduced net gain for the mode; the dual quantum-well case adds higher bandgap wells in the waveguide to provide better modulators in the 'passive' guide; the quantum-well intermixing approach can provide multiple bandgaps from a single growth with multiple diffusion steps, but for higher saturation power SOAs or detectors additional blanket regrowths are necessary.

3. Example PICs

Figures 2 & 3 show schematics and results from two example 40 Gb/s PICs fabricated in the authors group. Figure 2 describes a single-chip all-photonic transceiver that includes a high-gain, high-saturation power SOA-UTC receiver and a widely tunable transmitter that combines an SGDBR laser with an electroabsorption modulator (EAM) [12]. The QWI platform is used. Figure 3 describes the use of the dual QW (DQW) platform to form a single-chip wavelength converter with a flared SOA-PIN receiver directly interconnected to a widely tunable SGDBR—Mach-Zehnder modulator (MZM) for the transmitter stage [13].

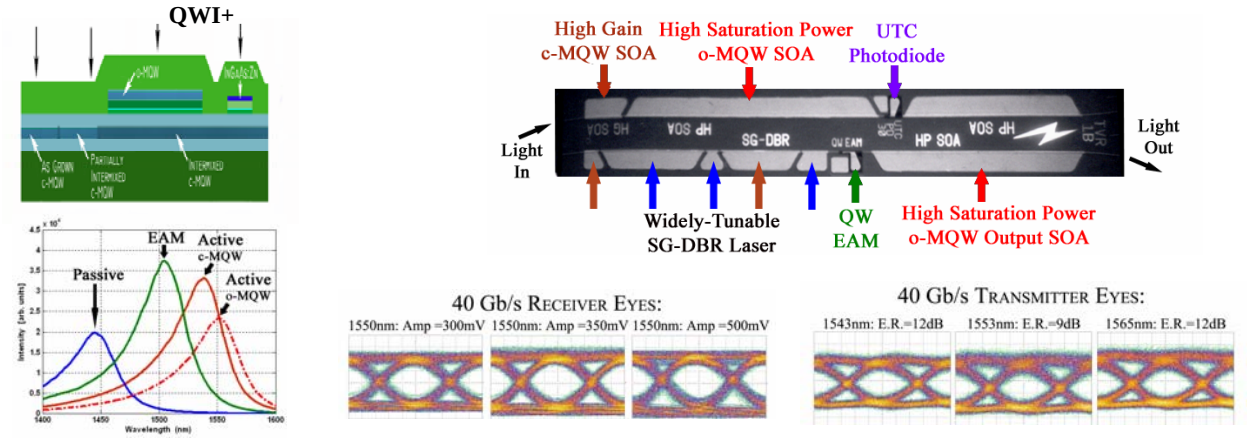

Figure 2. 40Gb/s single-chip transceiver fabricated with quantum-well intermixing (QWI) and blanket regrowths. A schematic device cross section and top view, photoluminescence plots of the various sections, and receiver and transmitter eye diagrams are shown. Receiver sensitivity @ 10^{-10} is -19.8 dBm; error-free wavelength conversion across a 32 nm range demonstrated.

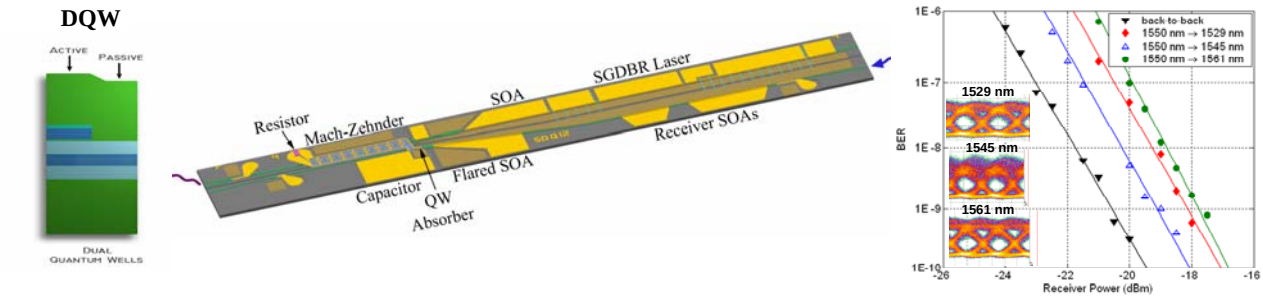

Figure 3. 40Gb/s single-chip wavelength converter fabricated with the "dual QW" integration platform. A series-connected traveling-wave MZM design is employed for chirp management. Only dc biases applied to chip for error free wavelength conversion over a 33 nm range.

References

[1] R. F. Leheny, R. E. Nahory, M. A. Pollack, A. A. Ballman, E. D. Beebe, J. C. DeWinter, R. J. Martin, *Electron. Letts*. **16**, 353 (1980).
[2] L.A. Coldren, B. I. Miller, K. Iga, and J.A. Rentschler, *Appl. Phys. Letts*, **38** (5) 315-317 (1981).
[3] Y. Abe, K. Kishino, Y Suematsu, and S. Arai, *Electron. Letts*. **17** (25) 945-947 (1981).
[4] M. Suzuki, Y. Noda, H. Tanaka, S. Akiba, Y. Kushiro, and H. Isshiki, *IEEE J. Lightwave Tech*., **LT-5**, 1277-1285 (1987)
[5] W.C. Dautremont-Smith, R. J. McCoy, R.H. Burton, and A.G. Baca, *AT&T Tech. J.*, **68**, 64-82 (1989).
[6] T. L. Koch, U. Koren, R. P. Gnall, F.S. Choa, R. Hernandez-Gil, C.A. Burrus, et al, *Electron. Letts*., **25**, 1621-1622 (1989).
[7] R. C. Alferness, T.L. Koch, L.L. Buhl, F. Storz, F. Heismann, and M. Martyak, *Appl. Phys. Letts*., **55**, 2011-2013 (1989).
[8] T. L. Koch and U. Koren, *IEEE J. Quantum Electronics*, **QE-27**, 641-653 (1991).
[9] Y.A. Akulova, G.A. Fish, H. Xu, E. Hall, M.C. Larson, P. Abraham, H. Marchand, et al, *Proc. IPRA*, paper IWF4, San Diego (2005).
[10] R. Nagarajan, C.H. Joyner, R.P. Schneider, et al, *IEEE J. Selected Topics in Quantum Electronics (JSTQE)*, **11** (1) 50-65 (2005).
[11] E.J. Skogen, J.W. Raring, G.B. Morrison, C.S. Wang, V. Lal, M.L. Masanovic, and L.A. Coldren, *IEEE JSTQE*, **11** (2) 343-355 (2005).
[12] J. W. Raring and L. A. Coldren, *IEEE Journal of Selected Topics in Quantum Electronics*, **13** (1) 3-14 (2007).
[13] A. Tauke-Pedretti, M. Dummer, M.N. Sysak, J.S. Barton, J.W. Raring, J. Klamkin, L.A. Coldren, *Proc. OFC*, Anaheim, PDP-36 (2007).