A 1-20 GHz InP HBT Phase-Lock-Loop IC for Optical Wavelength Synthesis

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***Abstract* — We report a PLL IC for locking, at a controlled frequency offset between 1 and 20 GHz, the optical phase and optical frequency of a slave semiconductor laser to that of a reference semiconductor laser. The IC, implemented in a 500 nm InP HBT process, contains an ECL digital single-sideband mixer to provide phase-locking at a +/- 20 GHz offset frequency, and also contains a wideband phase-frequency detector to provide loop acquisition given up to +/-40 GHz initial frequency offset.**

***Index Terms* — Phase locked loops, Mixers, Microwave circuits, Wavelength division multiplexing, Bipolar integrated circuits, Optoelectronic devices, High speed integrated circuits.**

I. Introduction

In wavelength-division-multiplexed (WDM) optical communications systems, optical channel spacings, typically ~25 GHz, are determined by optical resonators coupled to diode lasers. In marked contrast, in microwave systems, frequencies are precisely determined by PLL/synthesis techniques. Using optical phase-lock-loops (OPLLs) [1], pairs of lasers can be locked in both optical phase and frequency. By introducing frequency offsets within the OPLL, the frequency difference between a pair of lasers can be set to this injected frequency, allowing wavelength spacings within WDM, LIDAR, and other optical systems to be set precisely and under digital control. This is optical wavelength synthesis.

Optical PLLs differ from microwave PLLs in that the oscillator frequency is vastly larger, 231 THz for a 1300 nm laser. The large initial frequency offset between lasers forces development of frequency difference detectors operating over 100 GHz bandwidth. Because optical frequencies cannot be divided under programmable control, other techniques must be developed for optical frequency synthesis.

An OPLL contains an optoelectronic IC (OEIC) comprising locked laser, interferometer, and photodiodes, a microwave electrical IC (EIC) containing frequency offset control and phase-frequency detectors, and a low-frequency (GHz) loop filter. OEIC design is described in [2]. Optical wavelength synthesis results will be reported separately [3]. Here we report design and performance of InP HBT optical wavelength synthesis ICs comprising of a 1-20 GHz *digital* single-sideband (SSB) mixer, and a +/- 40 GHz phase-frequency difference detector.

II. Optical Synthesizer Design

In the OPLL (Fig. 1), the reference and slave laser are combined at (0°, 90°, 180°, 270°) phase offsets and interfered on photodiodes, producing photocurrents proportional to the cosine (I) and sine (Q) of the optical phase difference. The coupler and photodiodes thus form an I/Q mixer.

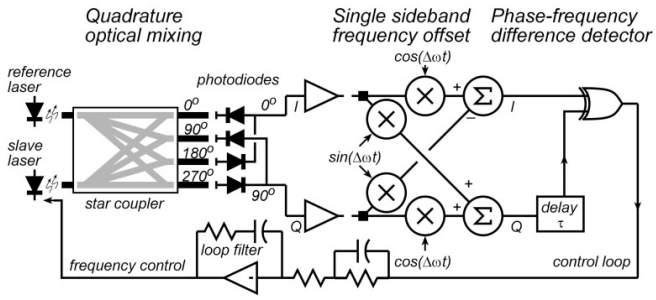

Fig. 1. Optical phase-lock-loop consisting of reference and locked lasers, 4-phase optical mixing, offset frequency injection with a single-sideband mixer, phase-frequency difference detector, and loop filter

To control optical frequency spacing, the slave laser must be locked to a controlled positive or negative frequency offset from that of the reference laser. The offset is introduced by shifting the I/Q photodetector signal frequencies using a two-stage (Weaver) single-sideband mixer implemented using quadrature optical and microwave mixers. The microwave mixer LO, provided by a microwave synthesizer, thus controls the optical frequency spacing. To permit tuning of this frequency offset over a wide +/- 1 to +/-20 GHz bandwidth, the electrical mixer is implemented digitally.

A PLL will not of itself acquire lock if the initial LO-RF offset frequency exceeds ~2-3 times the PLL loop bandwidth f_{loop}. At λ=1300 nm, +/- 0.02% wavelength detuning corresponds to a +/- 46 GHz offset frequency, much larger than the ~1 GHz f_{loop} feasible given the laser tuning characteristics. A Costas phase-frequency difference detector (PFD) provides an error signal proportional to the offset

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frequency, permitting automatic loop acquisition for offset frequencies below +/- 40 GHz.

III. Theory and Design

OEIC photocurrents vary significantly between fabricated OEICs; To make the loop parameters independent of such variations, PLL signals are converted to digital levels, and mixers and phase/frequency detectors are implemented in emitter-coupled logic (ECL).

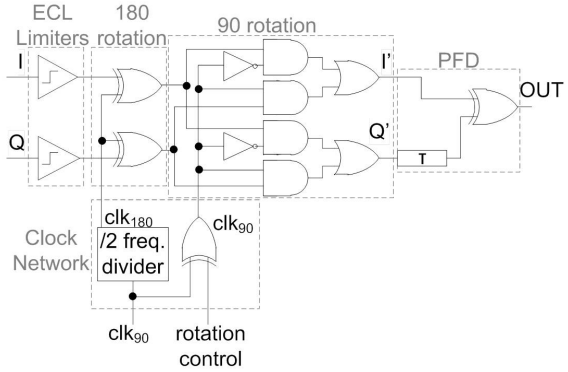

Fig. 2. Digital block diagram of the electrical PLL IC, consisting of input limiters, a digital SSB mixer implemented with 180° and 90° rotation blocks, and an phase-frequency difference detector implemented using a delay line and XOR gate. All digital blocks are in 2-level differential ECL.

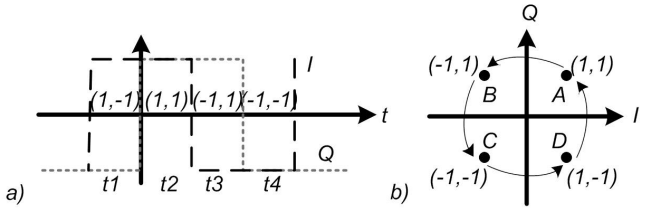

Fig. 3. Digitally limited I/Q signals for optical frequency offset. a) Time -domain square wave. b) Rotating constellation in the (I,Q) plane.

Subsequent to digital limiting, frequency shifts are introduced with a SSB mixer. This mixer, implemented digitally to permit a wide 20 GHz tuning range, is described in Fig. 1 and Fig. 2. Given a positive laser frequency offset f, the I/Q photocurrents rotate counterclockwise through the points (1,1), (-1,1), (-1,-1), (1,-1) in the (I,Q) plane (Fig. 3). For a negative frequency offset, - f, this rotation reverses. For zero frequency offset the constellation remains static at one of the four points as determined by the relative laser phases.

The digital SSB mixer provides a frequency offset by rotating this constellation, producing an output pair (I',Q'). It is formed of cascaded 180º and 90º rotation blocks. The 180º block rotates the (I,Q) state by 180º (i.e. A→C, B→D, etc.) when its input clock is 1 but provides no rotation when its input clock is 0. The 90º block rotates the (I,Q) state by 90º (i.e. A→B, B→C, etc.) when its input clock is 1 but provides no rotation when its input clock is 0. Applying high clock signals to both blocks rotates the state by 270º. Applying clock signals f_{clk90} , f_{clk180} at a 2:1 frequency ratio to the 180º and 90º rotation blocks rotates the I'/Q' constellation and provides a frequency shifts f; These signals are derived from a static frequency divider [4], (Fig. 2). Inverting the sign of f_{clk90} inverts the sign of the frequency offset.

The PFD is an ECL XOR gate with a delay line in the Q arm. To force equal transistor delays on both inputs, the gate uses two parallel multipliers with crossed inputs and shunt outputs. The PFD output (1) has one component proportional to the phase difference given zero frequency difference, and a second proportional to the frequency difference given zero phase difference.

$$\begin{aligned} I'(t) \oplus Q'(t-\tau) &= \cos(2\pi\Delta f t + \theta)\sin(2\pi\Delta f(t-\tau)+\theta) \\ &= 0.5\sin(4\pi\Delta f t - 2\pi\Delta f\tau + 2\theta) + 0.5\sin(2\pi\Delta f\tau) \end{aligned} \quad (1)$$

In PLL frequency locking mode, when the frequency offset between the reference and the offset laser, Δf, does not match the clk_{90} frequency (i.e. $f_{clk90} \neq 2\Delta f$), the (I',Q') state rotates at the error frequency driving (Fig. 5) the PFD to provide a non-zero average output.

In phase locking mode, when the laser offset, Δf, matches the clk_{90} frequency (i.e. $f_{clk90} = 2\Delta f$) under a suitable rotation control sign, the relative phase between the lasers will change the I/Q signals phase relative to clk_{90} and clk_{180}. This will eventually result in (I',Q') state oscillating at a frequency $2f_{clk90}$ between states two adjacent states (A and B, B and C, etc.) with a duty cycle determined by the phase offset (Fig. 4). For a 90º (I,Q) phase relative to clk_{90} the oscillation is at 50% duty cycle, hence the PFD provides zero DC average output. This brings the system into lock.

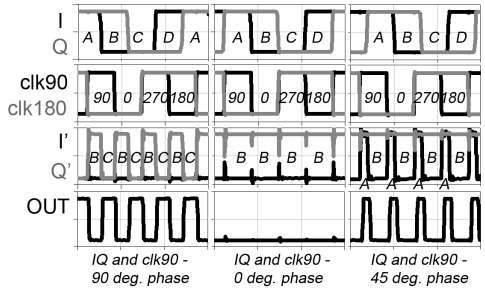

Fig. 4. SSB mixer at phase detection mode. Signal propagation as a function of various I/Q phase relative to clk_{90}. For 90º phase a 50% duty cycle output signal with zero average DC.

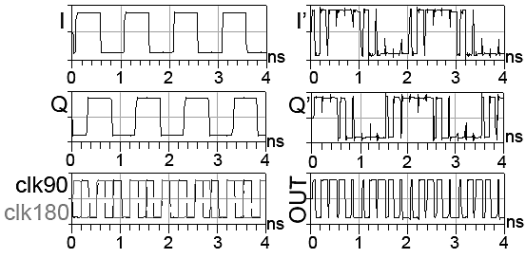

Fig. 5. SSB mixer at frequency locking mode. $f = 1$ GHz and $f_{clk90} = 3$ GHz. Since frequency lock occurs only for $f = 1.5$ GHz, the (I',Q') state will rotate at the error frequency of 0.5 GHz.

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IV. Experimental Results

The integrated SSBM chip was measured for phase and frequency detection using a sampling oscilloscope and a real time oscilloscope to observe and average the output signal. The optical I/Q signal was emulated by two synchronized microwave synthesizers while the clk_{90} signal was supplied by a third synthesizer. The applied input signals power was set to 0.4 mW for both the I/Q input and clk_{90}. Signals were delivered on-wafer using microwave wafer probes. The overall DC power for the IC was 5.3 W.

Fig. 6 shows experimental results. In Fig. 6a, the PFD output is measured as a function of phase difference with the emulated I/Q photocurrent signals set at 15 (20) GHz and with f_{clk90} set at 30 (40) GHz, i.e. with the system operating in phase-detection mode. The phase error signal varies +/- 300 mV at 15 GHz offset and +/- 120 mV at 20 GHz offset as the phase is varied through 360°. This indicates that the phase detector operates properly for frequency offsets as large as +/- 20 GHz.

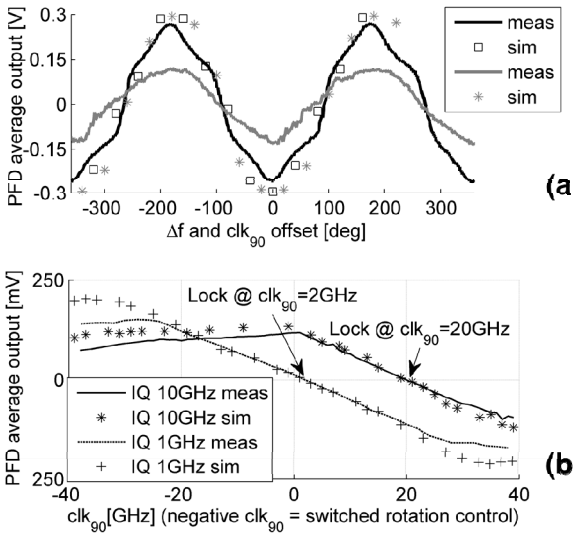

Fig. 6. PFD phase, frequency detection measurements. a) phase detection characteristics, measurement vs. simulation for f = 20 GHz, clk90 = 40 GHz (grey) and for f = 15 GHz, clk90 = 30 GHz (black). b) frequency detection characteristics, measurement vs. simulation for f = 10 GHz and f = 1 GHz.

In Fig. 6b, the PFD output is measured at a laser offset frequencies of Δf = 1 and 10 GHz, by adjusting SSB mixer LO frequency f_{clk90}. This measured the PFD characteristics in frequency detection mode. The frequency detection characteristics show frequency error detection over a +/-40 GHz range, with zero frequency detector output when, as designed, the laser offset frequency is equal to $f_{clk90}/2$. Fig. 7 shows the PFD output time waveforms in phase detection mode, as a function of phase offset, for Δf = 2 GHz and f_{clk90} = 4 GHz. The IC (Fig. 8) area is 1.8 mm^2.

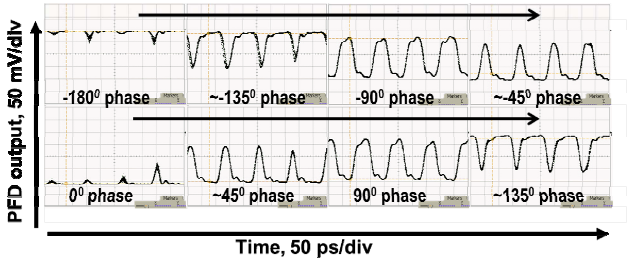

Fig. 7. PFD OUT measured waveforms in phase detection mode for f = 2 GHz and f_{clk90} = 4 GHz.

V. Conclusion

We have demonstrated a novel broadband +/-20 GHz optical frequency synthesis IC in 0.5 µm InP HBT technology. Further work on a full optoelectronic system for single side band frequency offset locking is underway.

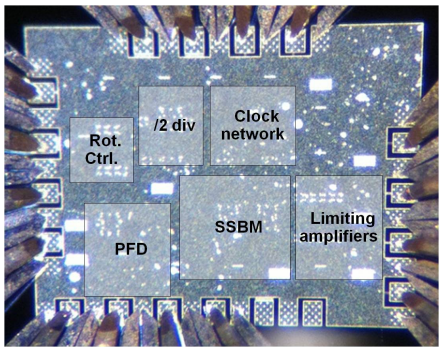

Fig. 8. IC chip image.

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