A 1–20-GHz All-Digital InP HBT Optical Wavelength Synthesis IC

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***Abstract*—An integrated circuit (IC) for heterodyne optical phase locking in a 1–20-GHz offset range is hereby reported. The IC, implemented in a 500-nm InP HBT process, contains an emitter coupled logic digital single-sideband mixer to provide phase locking at a ±20-GHz offset frequency, and a wideband phase-frequency detector designed to provide loop acquisition up to ±40-GHz initial frequency offset. The all-digital IC design has phase-frequency detection gain independent of IC process parameters or optical signal levels, and provides a wide offset locking range. A 100-ps delay decreases the overall loop delay, making wideband loop filter design possible. In addition, a medium-scale high-frequency logic design methodology is presented and fully discussed.**

***Index Terms*—Bipolar integrated circuits (ICs), high-speed ICs, microwave circuits, mixers, optoelectronic devices, phase-locked loops (PLLs), wavelength division multiplexing.**

I. Introduction

THE ever-growing data volume transmitted through the optical fiber communication systems requires increasingly efficient transmission and receiving techniques. Coherent communication methods have been of a great interest due to their superior noise performance comparing to the direct-detection ones. However, coherent communication is mainly based on a free-running optical local oscillator (LO) and digital processing after detection for data and clock recovery. Wavelength-division-multiplexed (WDM) optical communications systems use optical resonators coupled to diode lasers to produce optical channel spacing, typically ∼50 GHz. The WDM receiver, in turn, is implemented by optical filters to separate the channels. In marked contrast, in microwave systems, frequencies are precisely determined by phase-locked loop (PLL)/synthesis techniques, allowing close frequency spacing of communications channels and efficient use of the spectrum. Using optical PLLs [1], [2], pairs of lasers can be locked in both optical phase and frequency. By introducing frequency offsets within the optical PLL, the frequency difference between a pair of lasers can be set to this injected frequency, allowing wavelength spacing within WDM, LIDAR, and other optical systems to be set precisely and under digital control. This is optical wavelength synthesis.

Due to the large optical frequency (e.g., 193 THz for a 1550-nm laser), frequency-division techniques cannot be used for frequency synthesis. Due to the large ratio of optical oscillator frequency to the typical loop bandwidth in optical PLLs (∼200 MHz–1 GHz), it is also much more difficult to force the loop to lock. The large initial frequency offset between lasers forces development of frequency difference detectors operating over a 100-GHz bandwidth. To get a large loop bandwidth, yet preserving stability, the loop delay must be minimized [3]. One factor determining loop delays is the speed-of-light propagation delay on both optical waveguides and electrical interconnects. To minimize this delay, the loop must be physically small. This goal is best achieved by monolithic integration. Previously reported optical PLLs [1], [2], [4]–[6] have used an optical interferometer, which measures the sign of the phase offset between the two lasers. This is insufficient to extract the sign of the laser frequency offset, information required for either frequency offset detection or for frequency offset locking with an unambiguous sign to the frequency offset. By measuring both the sine and cosine of the laser phase offset in a quadrature-phase (I/Q) interferometer, both in-phase and quadrature-phase components of the offset signal are measured. This allows both measurement of frequency offset and use of a single-sideband (SSB) mixer to perform offset locking with controlled frequency offset magnitude and sign. Fan *et al.* [7] reported heterodyne phase locking of lasers using an external cavity. This work permits rapidly tunable phase-locked systems and does not require the addition of external optics.

Table I. summaries important milestones in optical offset phase locking.

An optical PLL contains a photonic integrated circuit (PIC) comprising a widely tunable sample grating distributed Bragg feedback (SG-DBR) laser, an I/Q detector including a star-coupler [8] and photodiodes, a microwave electrical integrated circuit (EIC) containing frequency offset control and phase-frequency detectors—reported in this study and recently reported

Manuscript received June 08, 2012; revised October 02, 2012; accepted October 15, 2012. Date of publication December 04, 2012; date of current version January 17, 2013. This work was supported by the Defense Advanced Research Projects Agency (DARPA) under the PICO program. This paper is an expanded paper from the IEEE MTT-S International Microwave Symposium, Montreal, QC, Canada, June 17–22, 2012..

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Digital Object Identifier 10.1109/TMTT.2012.2226599

TABLE I
HETERODYNE OPTICAL PHASE LOCKING—PARALLEL STUDIES

Work (year)	Loop Delay	Frequency detection	Single side-band locking	Comments
[1] R.J. Steed (2011)	1 ns	No	No	Hybrid XOR gate
[5] L.N. Langley (1999)	380 ps	No	No	Hybrid mixer and PD
[4] U. Gliese (1992)	400 ps	No	No	
[11] M. Lu (2012) using the reported IC	200 ps	Yes	Yes	Fully integrated SSB Mixer and PFD

in [9], and a high-frequency (500 MHz), low-delay feed-forward-compensated op-amp loop-filter [10]. PIC design and optical wavelength synthesis results are reported in [11]. Here, we report the design methodology and performance of an InP HBT optical wavelength synthesis IC comprised of a 1–20-GHz *digital* SSB mixer and a ±40-GHz phase-frequency difference detector (PFD). The digital design eliminates the dependence of loop bandwidth on optical signal levels (i.e., input photocurrent magnitudes) and enables a wide frequency locking range. In this paper, optical heterodyne locking methods and considerations are examined, a novel digital mixing technique is in-depth analyzed, and design methodologies of complex high-frequency digital ICs are discussed.

II. OPTICAL SYNTHESIZER DESIGN

Optical and electrical PLLs differ fundamentally in that the ratio of carrier frequency to loop bandwidth is a ratio of $\sim 10^4 : 1$ larger in optical than in electrical PLLs. This vast ratio of oscillator frequency to loop bandwidth has a profound impact upon the range of wavelengths over which an optical PLL will acquire lock, and greatly impairs the rate both at which the optical PLL can scan its frequency and its absolute frequency tuning range.

The wide (∼200 GHz) frequency tuning range of semiconductor lasers, of great value in tunable sources, imposes the demand for very wide bandwidth electronics. The initial frequency offset between reference and controlled lasers may exceed 200 GHz, approaching the range of operation of electronic amplifiers and far beyond the control bandwidth of feedback loops. To acquire a homodyne lock, the beat note between lasers must fall within the PLL loop bandwidth $f_{\rm PLL}$. In fact, PLLs have a maximum locking range of $\Delta f_{lock} \sim 3f_{\rm PLL}$, as noted by Razavi [12]. Attempts to increase the locking range by dividing the beat note frequency using a frequency divider have two main drawbacks: an increase in a loop delay due to an introduction of a divider into a loop, and a disability of the divider to operate in an absence of a beat note, when the loop is locked.

A simplified offset locked optical PLL block diagram is presented in Fig. 1. The loop is comprised of an optical interferometer acting as a phase detector, a microwave mixer to apply frequency offset $(\Delta f_{\rm ext})$, and a loop-filter to control the loop bandwidth and dynamics. For a reference laser frequency f_R

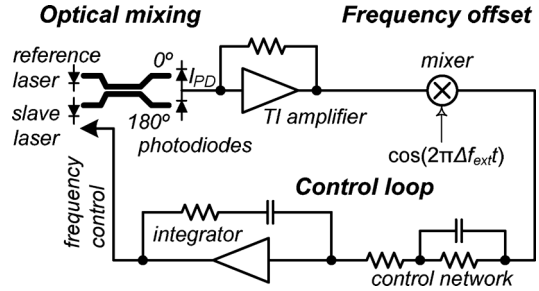

Fig. 1. Simplified optical PLL block diagram.

and a slave laser frequency f_L, the photodiodes output current, given by (1), is proportional to $\cos(\Delta\theta(t))$. Here, E_R, θ_R, and f_R are the electric field amplitude, phase, and frequency of the reference laser, while E_L, θ_L, and f_L are those of the locked laser, and $\Delta\theta(t) = 2\pi\Delta f t + \Delta\theta_0$, where $\Delta f = f_R - f_L$ and $\Delta\theta_0 = \theta_R - \theta_L$

$$I_{\rm PD} \propto \left|E_R e^{j(2\pi f_R t+\theta_R)} + E_L e^{j(2\pi f_L t+\theta_L)}\right|^2 = |E_R|^2 + |E_L|^2 + 2|E_R||E_L|\cos(\Delta\theta(t)) \quad (1)$$

$$K_{\rm PD} = I_{\rm PD} = 2|E_R||E_L|\cos(\Delta\theta(t)) \overset{\Delta\theta(t)\ll 1}{=} 2|E_R||E_L|. \quad (2)$$

Since $\cos(\Delta\theta(t)) = \cos(-\Delta\theta(t))$, the frequency offset sign cannot be extracted unambiguously; hence, measurement or control of the sign of the frequency offset is not possible. In addition, such loop topology imposes phase detection gain, $K_{\rm PD}$, directly proportional to the product of reference and LO laser field intensities (2). This makes the PLL open loop gain, and hence, bandwidth dependent upon optical intensity, potentially subjecting the loop to instability for varying component parameters or operating conditions.

The microwave mixer downconverts the beat note to $\cos(2\pi(\Delta f - \Delta f_{\rm ext})t + \Delta\theta_0)$. Since the downconverted signal frequency falls within the loop bandwidth range, the loop lock the lasers with $\Delta f_{\rm ext}$ offset.

In a type II PLL, which has a zero steady-state error in response to a ramp input, the loop filter includes an integrator with a compensating zero, with a loop filter current gain transfer function of $(1 + \tau_1 s)/\tau_2 s$, where τ_1 and τ_2 are integration and zero time constants. Given this filter transfer function, the overall PLL loop transmission is as in (3). A laser operates as a current-controlled oscillator (CCO) whose tuning coefficient is defined as $K_{\rm CCO} = df_L/dI$. As with a voltage-controlled oscillator (VCO), the CCO provides additional integration in the loop transmission.

The loop bandwidth, $f_{\rm PLL}$, is the frequency for which $\|T(2\pi j f_{\rm PLL}) = 1\|$ approximated by (4) and determined by the loop-filter time constants, phase-detection gain, and the laser's current-to-frequency conversion gain

$$T(s) = K_{\rm PD}\frac{K_{\rm CCO}}{s}\frac{1+\tau_1 s}{\tau_2 s} \quad (3)$$

$$f_{\rm PLL} \approx \frac{\tau_1}{2\pi\tau_2}K_{\rm PD}K_{\rm CCO}. \quad (4)$$

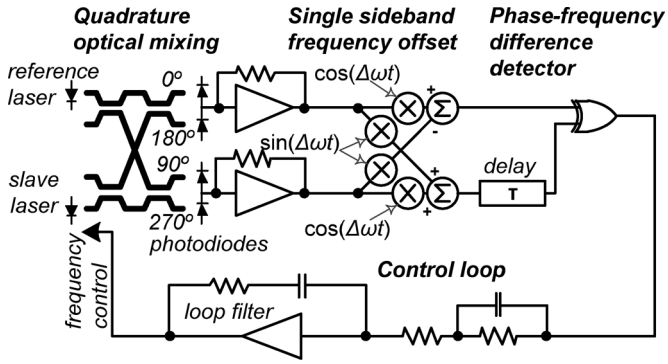

Fig. 2. General diagram of an optical PLL consisting of reference and locked lasers, four-phase optical mixing, offset frequency injection with an SSB mixer, PFD, and loop filter.

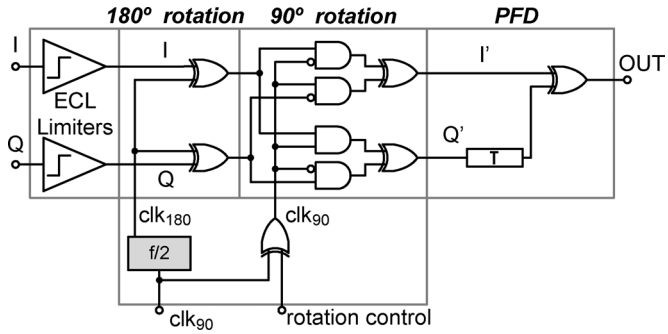

Fig. 3. Digital block diagram of the electrical PLL IC, consisting of input limiter amplifiers, a digital SSB mixer implemented with 180° and 90° rotation blocks, and a PFD.

To measure the sign of the frequency offset, both the in-phase (I) and quadrature-phase (Q) [(5) and (6)] components of lasers offset beat-note are required. Since a simple optical interferometer provides only the in-phase component, $I_{\rm PD}$, a 90° optical hybrid [8] should be used

$$I \propto \left|E_R e^{j(2\pi f_R t+\theta_R)} + E_L e^{j(2\pi f_L t+\theta_L)}\right|^2 = |E_R|^2 + |E_L|^2 + 2|E_R||E_L|\cos\left(\Delta\theta(t)\right) \quad (5)$$

$$Q \sim \left|E_R e^{j(2\pi f_R t+\theta_R)} + E_L e^{j(2\pi f_L t+\theta_L+\frac{\pi}{2})}\right|^2 = |E_R|^2 + |E_L|^2 + 2|E_R||E_L|\sin\left(\Delta\theta(t)\right). \quad (6)$$

A PLL will not by itself acquire lock if the initial reference-slave lasers offset frequency exceeds the required final offset frequency by ∼2–3 times the PLL loop bandwidth $f_{\rm PLL}$ [12]. At $\lambda = 1550$ nm, ±0.02% wavelength detuning corresponds to a ±39-GHz offset frequency, much larger than the ∼1-GHz $f_{\rm PLL}$, feasible given typical laser tuning characteristic [11] and minimum delays, achievable by a discrete loop. Hence, in order to obtain initial lock, the lasers should be manually brought into the locking range, and if the lock is lost, it will not be automatically obtained again.

The I/Q signals provided for the offset sign control allow designing a loop with an ability to measure the initial loop frequency detuning using a PFD [13]; the initial lasers detuning can then be as large as that of the available photodetectors and integrated circuit (IC) bandwidths, about ±100 GHz. The time to acquire frequency lock is set by the loop bandwidth operating in frequency-control mode and its damping factor.

Fig. 2 suggests a block diagram of an analog optical PLL loop with a SSB mixer for offset sign control, and a phase-frequency detection mechanism to extend the frequency locking acquisition range. In this optical PLL, the reference and slave laser are mixed at (0°, 90°, 180°, 270°) phase offsets and detected by photodiodes, producing photocurrents proportional to the cosine (I) and sine (Q) [(5) and (6)] of the optical phase difference. The coupler and photodiodes thus form an I/Q mixer.

To control optical frequency offset spacing, the slave laser must be locked to a controlled positive or negative frequency offset from that of the reference laser. The offset is introduced by shifting the I/Q photodetector signal frequencies using a two-stage (Weaver) SSB mixer implemented using quadrature optical and microwave mixers. The microwave offset reference LO, provided by a microwave synthesizer, thus controls the optical frequency spacing.

A Quadricorrelator PFD [14] provides an error signal proportional to the offset frequency [see (7)]. The first term of (7) is responsible for the phase detection, when $\Delta f = 0$, and provides a 180° period characteristic. In case of $\Delta f \neq 0$, the second term of the equation provides a frequency detection indication with detection range set by the τ delay

$$\begin{aligned} I'(t)Q'(t-\tau) &= \cos(2\pi\Delta f t+\Delta\theta_0)\sin\left(2\pi\Delta f(t-\tau)+\Delta\theta_0\right) \\ &= 0.5\sin(4\pi\Delta f - 2\pi\Delta f\tau + 2\Delta\theta_0) \\ &\quad + 0.5\sin(2\pi\Delta f\tau). \end{aligned} \quad (7)$$

The analog optical PLL loop will only operate well for I/Q signals within the linear range of the mixers and any amplifiers between them and the photodetectors. Given variable photocurrents, this will require automatic gain control (AGC). Even with such AGC, the phase detection gain, $K_{\rm PD}$, will still depend upon the reference and slave lasers optical intensity. It is also difficult to design a wideband SSB mixer using standard analog topologies since these require cosine and sine components of the RF signals [15], and hence, 90° phase shifters. Such phase shifters are generally narrowband. To obtain a wide offset locking frequency range, a digital frequency translation technique was developed.

III. Theory and Design

A. Operation Principles

To enable tuning of a frequency offset over a wide ±1 to ±20-GHz bandwidth, and to reduce the dependency on the photocurrents from the PIC, an all-digital SSB mixer is proposed (Fig. 3). The I/Q photocurrents generated by the PIC detectors are converted to digital levels using a chain of limiting amplifiers. Since the mixer and phase/frequency detector are entirely digital, the phase-detector and frequency-detector gains are independent of IC process parameters (transistor and passive element parameter values). In marked contrast, had a linear analog mixer and phase detector been designed, the loop bandwidth would have varied with variations of optical component parameters (hence, photocurrent amplitudes), and mixer and pream-

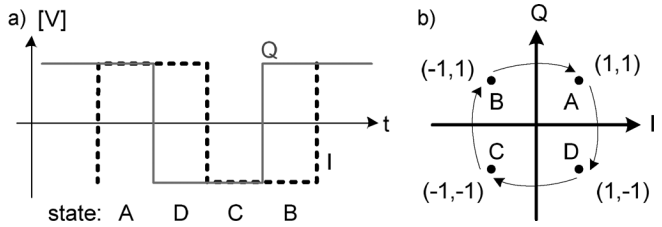

Fig. 4. Digitally limited I/Q signals for optical frequency offset. (a) Time-domain square wave. (b) Rotating constellation in the (I,Q) plane.

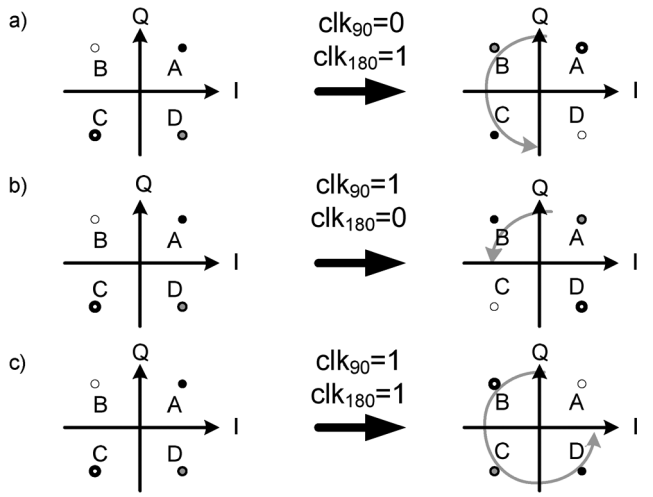

Fig. 5. Digital state rotation. (a) 180° rotation. (b) 90° rotation. (c) 270° rotation.

plifier gains. In this circumstance, precise control of the PLL bandwidth would have been difficult to obtain.

Subsequent to digital limiting, frequency shifts are introduced with a digital SSB mixer (Fig. 3). Given a positive laser frequency offset Δf, the I/Q photocurrents rotate counterclockwise through the points (1,1), $(-1,1)$, $(-1,-1)$, $(1,-1)$ in the (I,Q) plane (Fig. 4). For a negative frequency offset, $-\Delta f$, this rotation reverses. For zero frequency offset, the constellation remains static at one of the four points as determined by the relative laser phases.

The digital SSB mixer provides a frequency offset by rotating this constellation in the opposing direction, producing a static output pair $(\mathrm{I}', \mathrm{Q}')$. The mixer is formed of cascaded 180° and 90° rotation blocks. The 180° block rotates the (I,Q) state by 180° (i.e., $\mathrm{A} \rightarrow \mathrm{C}, \mathrm{B} \rightarrow \mathrm{D}$, etc.) when its input clock is 1, but provides no rotation when its input clock is 0. The 90° block rotates the (I,Q) state by 90° (i.e., $\mathrm{A} \rightarrow \mathrm{B}, \mathrm{B} \rightarrow \mathrm{C}$, etc.) when its input clock is 1, but provides no rotation when its input clock is 0. Applying high clock signals to both blocks rotates the state by 270° (Fig. 5). Applying periodically clock signals f_{clk90}, f_{clk180} at a 2:1 frequency ratio to the 180° and 90° rotation blocks rotates the I'/Q' constellation and provides frequency shifts Δf; these signals are derived from a static frequency divider [16], (Fig. 3). Inverting the sign of f_{clk90}, by changing the rotation control signal, inverts the rotation direction, and therefore, the sign of the frequency offset.

The PFD is an emitter-coupled logic (ECL) XOR gate with a delay line of 10 ps in the Q arm. This frequency detector

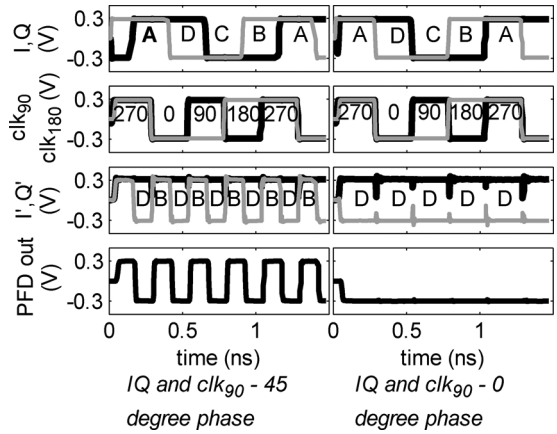

Fig. 6. SSB mixer at phase detection mode. Signal propagation as a function of various I/Q phases relative to clk_{90}. For 45° phase, a 50% duty cycle output signal with zero average dc.

permits automatic loop acquisition for offset frequencies below ±50 GHz. To force equal transistor delays on both inputs, the gate uses two parallel multipliers with crossed inputs and shunt outputs. The small-signal analysis of the PFD is developed in (7).

In the phase-locked mode, i.e., when the laser offset, Δf, matches the clk_{90} frequency (i.e., $f_{\mathrm{clk90}} = 2\Delta f$) under a suitable rotation control sign, the relative phase between the lasers will change the I/Q signals phase relative to clk_{90} and clk_{180}. This will eventually result in the $(\mathrm{I}', \mathrm{Q}')$ state oscillating at a frequency $2f_{\mathrm{clk90}}$ between two adjacent states (A and B, B and C, etc.) with a duty cycle determined by the phase offset (Fig. 6). In this operation mode, either I' or Q' is constant, while the other signal oscillates between 1 and 0 at a frequency of f_{clk90} with a duty cycle varying linearly with the phase offset. In this mode, the output of the XOR gate is a similar oscillating digital signal. For a 45° (I,Q) phase relative to clk_{90}, the oscillation has 50% duty cycle; hence, the PFD provides zero dc (average) output. This brings the system into lock. Since the PFD output is digital with only its pulse duty cycle varying as a function of loop phase offset, there is no dependence on the photocurrent magnitudes of the circuit's parameters.

In PLL frequency acquisition mode, which occurs when the frequency offset between the reference and the offset laser Δf does not match the clk_{90} frequency (i.e., $f_{\mathrm{clk90}} \neq 2\Delta f$), the I' and Q' outputs are quadrature square waves whose frequency is error frequency (Fig. 7). Since the PFD output is formed by forming the XOR product of these signals after introducing a relative delay τ, the PFD output has a dc component varying as $\sin(2\pi\Delta f\tau)$ (7). This dc signal forces the RF and LO lasers into frequency synchronization at the offset frequency f_{clk90}, i.e., forces the loop into lock. The digital frequency-detector gain is independent of all optical or electronic IC parameters, except that of the delay line τ, and hence, is well controlled in the presence of normal optical and IC process parameter variations.

B. High-Frequency Digital Design

The circuit is a complex digital IC operating with digital signals over a dc–40-GHz range. Circuit design and layout required

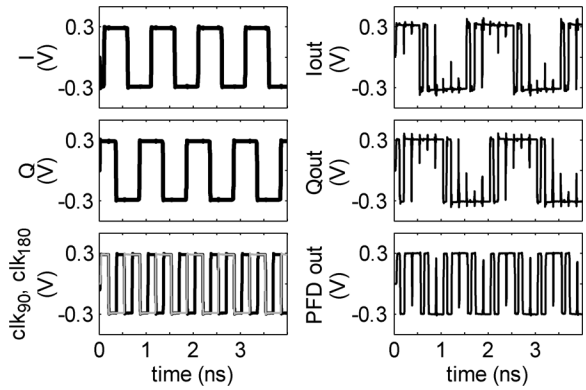

Fig. 7. SSB mixer at frequency locking mode. $\Delta_f = 1$ GHz and $f_{\mathrm{clk90}} = 3$ GHz. Since frequency lock occurs only for $\Delta_f = 1.5$ GHz, the (I′, Q′) state will rotate at the error frequency of 0.5 GHz.

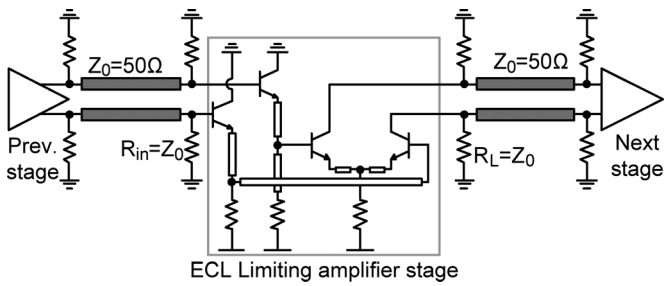

Fig. 8. ECL two-level logic with double terminated line interconnects.

a combination of digital and controlled-impedance millimeter-wave techniques. The limiting amplifiers and buffers were implemented using differential ECL (Fig. 8). To avoid reduced circuit bandwidth from interconnect capacitance, all digital interconnects between the gate were implemented as double-terminated transmission lines (Fig. 8) [17]. This introduces a resistive 25-Ω load to the driving stage. By working in such a 50-Ω environment, the degradation increase in gate delay caused by driving a long line is simply $\tau = l/v$, where l is the length and v is the propagation velocity. In contrast, if the gate were instead loaded with resistance $R_L \gg Z_0$, the additional delay would be $R_L C_{\mathrm{wire}} = (l/v)(RL/Z_0)$ [18].

The ECL emitter followers are placed at gate inputs rather than gate outputs. If emitter followers are instead placed at gate outputs, their inductive output impedance can interact with any load capacitance to cause ringing or instability.

To fully switch a bipolar differential pair with large noise margin, a logic voltage swing of $\Delta V \approx 6\ \mathrm{kT/q} + 3I_0R_{\mathrm{ex}}$ is selected, where R_{ex} is the emitter access resistance and I_0 is the differential tail current. Based on an equivalent collector load resistor of 25 Ω, the differential pair tail current is $I_0 = 12$ mA. Transistors are sized to operate at current densities approaching the Kirk-effect limit [19].

Boolean logic, such as the 180° and 90° rotation blocks, XOR gate, and frequency divider are implemented in two-level differential ECL logic. To maintain a 50-Ω interconnect environment, these cells were placed along a 50-Ω double-terminated bus (Fig. 9). Interconnects from the gate to the bus present wiring

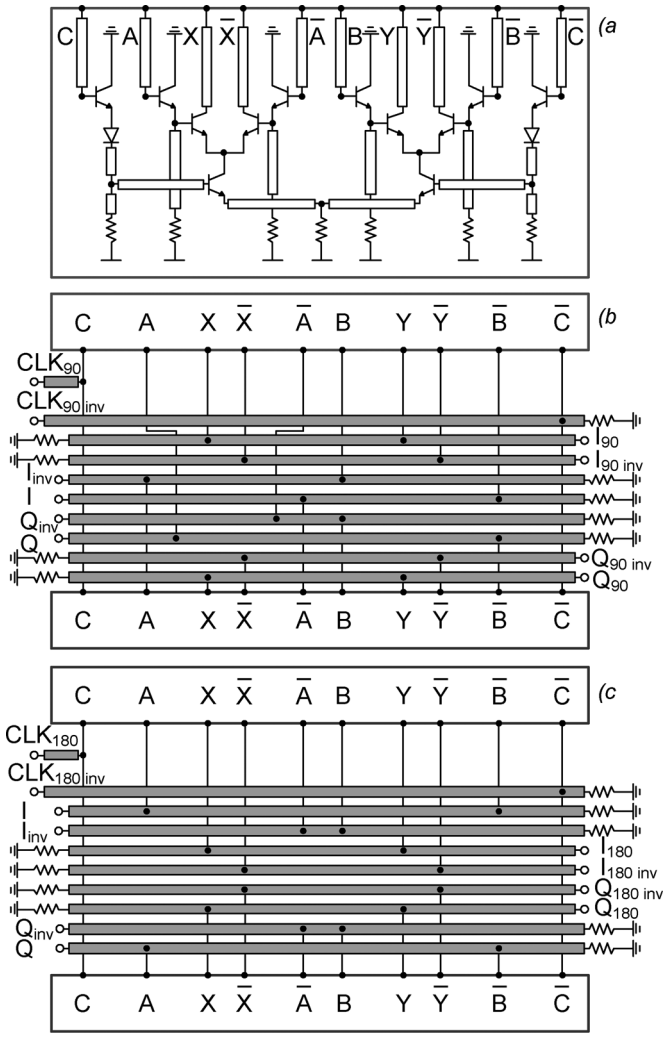

Fig. 9. (a) Gilbert cell as a building block for Boolean logic. (b) 90° rotation. (c) 180° rotation blocks schematics.

parasitics and are kept short. The typical length of such vertical stubs is 30 μm, much shorter than a typical wavelength of 2.5 mm at 40 GHz.

The two-level ECL cells [see Fig. 9(a)] have three inputs: two on the upper level (A,B) and one on the lower level (C). The lower level inputs have longer delay so when balanced delays are required, two parallel gates are used, with interchanged inputs and parallel outputs. Such realization was used with the PFD XOR gate.

High-frequency digital signal distribution (fan-out) was implemented by three techniques (Fig. 10). In the first method [see Fig. 10(a)], the fan-out is implemented by simply splitting the 50-Ω line into two high-impedance 100-Ω lines. The long line is correctly terminated in 50 Ω, while the driving buffer sees a total load of 25 Ω. The *RC* charging time is $\tau = 2C_L \cdot 25\ \Omega$. The second technique [see Fig. 10(b)] uses a pair of 50-Ω lines, driven from a second gate. Each line, in the absence of the next stage capacitive loading, C_L (Fig. 10), is correctly terminated. The *RC* charging time is $\tau = 2C_L \cdot 25\ \Omega$. Since the sending end of the transmission line is not correctly terminated, topologies shown in Fig. 10(a) and (c) suffer from round-trip pulse reflections if the CL is significant. This is eliminated in the

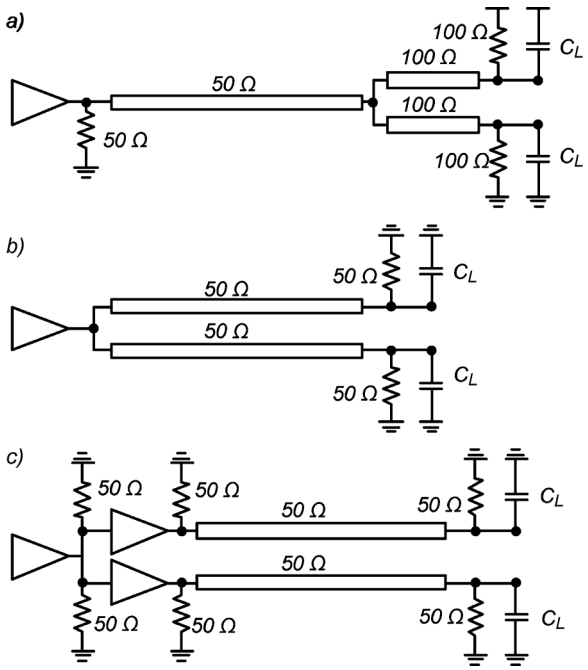

Fig. 10. Digital fan-out techniques. (a) Single-line fan-out. (b) Double-line fan-out. (c) Isolated double-line fan-out.

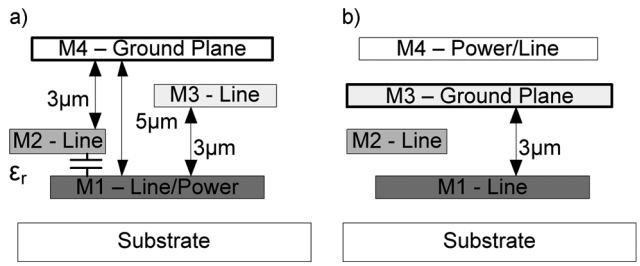

Fig. 11. Metal stack cross section. (a) M4 as a ground plane. (b) M3 as a ground plane.

final topology [see Fig. 10(c)] signals are split 2:1 locally and buffered with gates before distribution on 50-Ω doubly terminated interconnects. In this technique, the reflections are well controlled and the *RC* charging time is $\tau = C_L \cdot 25\ \Omega$. The technique shown in Fig. 10(c) introduces additional power consumption and layout complexity.

The design of a 40-GHz digital logic with a synchronized clock network requires precise electromagnetic (EM) modeling and verification, obtained by the Agilent Momentum computer-aided design (CAD) tool. The top metal (M4) was assigned as a ground plane, while the majority of interconnects were implemented on M1 and M2 in a form of inverted thin-film microstrip lines [see Fig. 11(a)]. M3 was primarily used for local routing solutions and local interconnects within gates. The use of inverted microstrip allows narrow line spacing (approximately two times the line-to-ground distance: 8–10 μm), and continuous ground plane without breaks, maintaining ground integrity and avoiding ground bounce. The use of a bottom ground plane within a complex IC environment would eventually lead to a highly fragmented ground (Fig. 12), unable to provide parasitics free current return paths. Due to the thin dielectric, the top ground plane makes the ground vias inductance negligible and

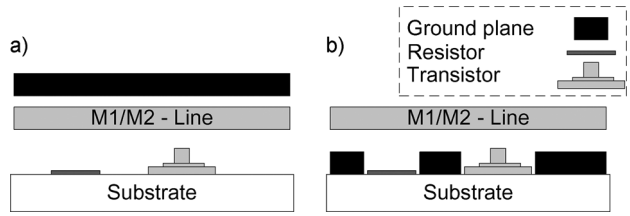

Fig. 12. (a) Top ground-plane versus (b) bottom ground-plane layout.

allows dense ground vias spacing, as requires in a complex IC. The drawbacks, however, of the thin dielectrics is the reduced line inductance, demanding thinner lines for high characteristics impedances. Thin lines also demonstrate increased skin loss and limit the maximum possible dc current [20].

Compared to M1, the dielectric thickness between M2 and the ground plane is smaller, creating difficulty in implementing high-impedance lines and leading to increased resistive losses. The power grid was routed on M1, crossing M1 lines with M3 bridges, and M2 from beneath. The crossovers of M1–M2 lines and M2—power lines introduce additional capacitance of $C_{\text{cross}} \approx 2$ fF for typical $5 \times 8\ \mu\text{m}^2$ overlaps [see Fig. 11(a)]. This capacitance creates signal crosstalk.

The other possible wiring strategy is to assign M3 as a ground plane [see Fig. 11(b)] and to use M4 mainly as a power grid or for sensitive lines requiring complete crosstalk isolation. This approach completely eliminates the parasitic capacitance formed between the power and signal lines and greatly simplifies the design by separating the routing of power grids from signal lines. However, this methodology also has limitations. Due to a thinner dielectric, M2 lines are made narrower (3-μm wide for 50-Ω impedance), presenting even higher losses and unsuitable for long connections. Even with M1, the implementation of high-impedance lines becomes impossible. To provide a power path to active devices, M3 needs to be perforated to allow vias to pass through, consequently violating the unity of the ground plane. However, the impact of these openings on M3 can be neglected if they are local and small in size. Eventually, both of the M3 and M4 ground-plane approaches allow a full EM simulation to be performed on the entire interconnects, rather than separately modeling individual segments.

All of the in-cell and external transmission lines were individually EM modeled. Fig. 9(a) shows the in-cell lines, which are not terminated due to their lumped behavior ($\sim$ 30 μm). However, both of them introduce capacitive and inductive parasitic loading with a delay and these effects must be taken into account for a precise simulation of the entire system.

The clock distribution network (Fig. 13) is the most critical part in terms of speed and timing precision. After the microwave offset reference has been split into 180° and 90° clocks, it must arrive in a synchronized fashion to both of the 180° and 90° rotation blocks. Each clock signal and its corresponding complementary must arrive simultaneously to all of the four ports at each rotation block (Fig. 13). In addition, clk_{90} must be delayed behind clk_{180} exactly the amount of time takes for the I/Q signal to pass the 180° rotation block and reach the 90° rotation block. This ensures synchronized operation of both of the rotation blocks on the same I/Q state. The delay was tuned

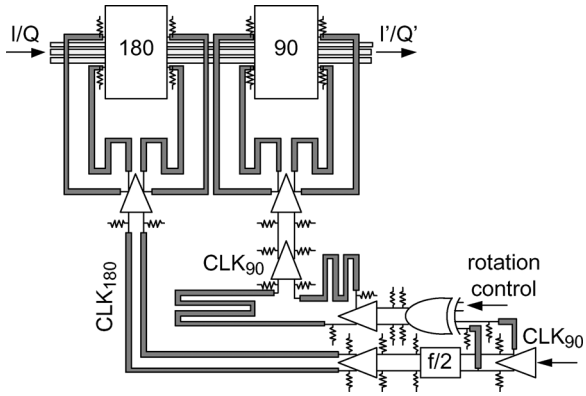

Fig. 13. Clock distribution diagram.

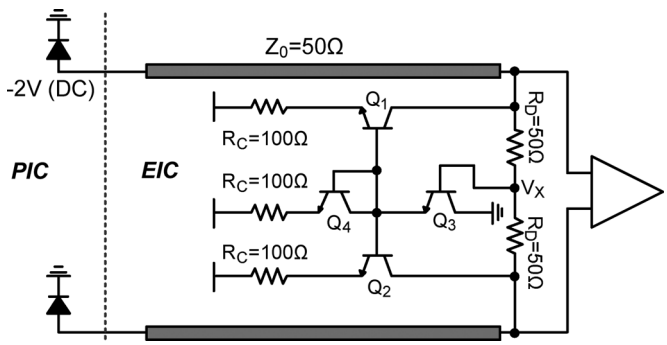

Fig. 14. Input biasing circuit.

by adjusting the line lengths as well as using buffer stacking. The clock network was implemented on M2, while the signal lines are mainly on M1. To maintain a symmetrical wiring structure and minimize the crossovers, the methodology shown in Fig. 10(b) was used for the final clock splitting. The IC demonstrates a total delay of 100 ps, reducing the limitation on wideband loops design. Delays achieved by hybrid mixers and phase detectors are typically longer [1].

The input differential limiting amplifiers are designed to operate with unbalanced photodiodes PIC [11]; hence, a new biasing topology was proposed (Fig. 14). The dc current provided by the photodiodes is drawn by Q_1 and Q_2, biasing the photodiodes at $V_X \approx -V_{EE} + 2V_{BE} \approx -2$ V, a dc voltage, enabling direct PIC–EIC connection without the use of dc blocks. In the differential operation mode, the node V_X becomes a virtual ground, providing a differential input impedance of $R_D = 50\,\Omega$. A common mode signal will alter the V_X voltage, activating the $Q_3 - Q_{1,2}$ negative feedback loop, which results in the common mode current drawn by $Q_{1,2}$. Small-signal analysis shows a common mode input impedance of $R_C/2$. This way the common and the differential input impedances can be controlled separately.

IV. Indium–Phosphide (InP) HBT Technology

The IC presented in this study was implemented using InP HBT 0.5-μm emitter width technology [21], [22] with cutoff frequencies $f_t = 300$ GHz and $f_{\max} = 300$ GHz.

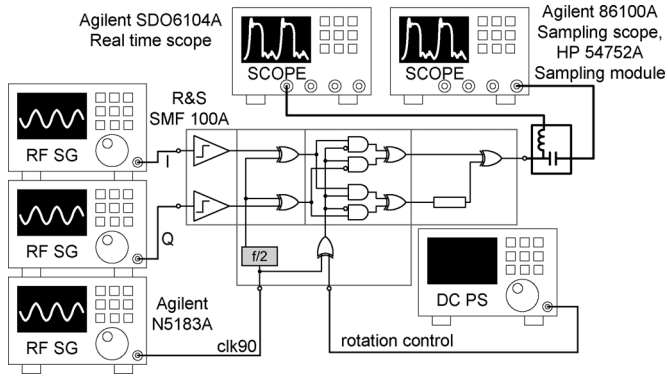

Fig. 15. SSB mixer measurement setup.

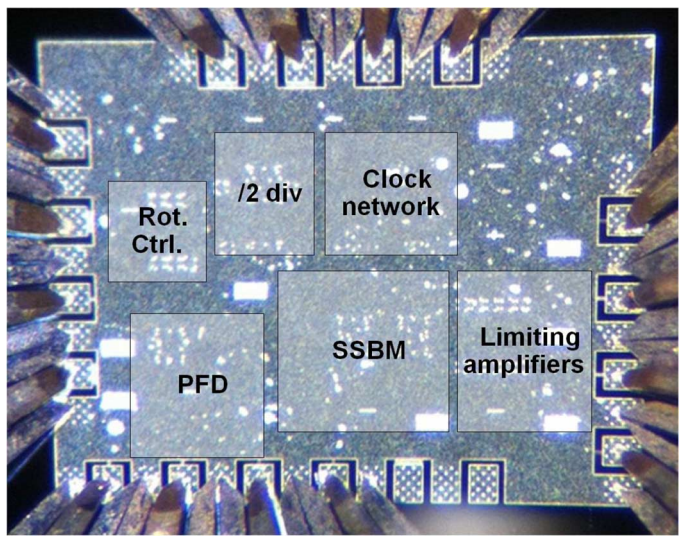

Fig. 16. IC chip image.

A four-metal interconnect stack was used with metal–insulator–metal (MIM) capacitors of 0.3 fF/μm^2 implemented between the first and the second metal layers. Signal lines were implemented using metal 1 and metal 2 as inversed microstrips with metal 4 serving as a ground plane. The resistors were implemented by a 50-Ω/sq thin-film deposition.

V. Measurement and Characterization

The integrated SSB mixer chip was measured for phase and frequency detection. To separate the output's average component from the time-varying component, a bias-tee was used (Fig. 15). The average component was inspected using an Agilent SDO6104A real-time oscilloscope with a sampling rate of 4 GSa/s, while the time-varying component was inspected using an Agilent 86100A sampling oscilloscope with a 50-GHz HP 54752A sampling module. The optical I/Q signals were emulated by two R&S SMF 100A synchronized microwave synthesizers and the clk_{90} signal was supplied by a third, an Agilent N5183A synthesizer. The input power was set to -4 dBm for both the I/Q input and clk_{90}. Signals were delivered on-wafer using microwave wafer probes. The IC was biased by a negative power supply of -3.8 V and the overall dc power was 5.3 W. The IC photograph is shown in Fig. 16 and the total area is 1.8 mm^2.

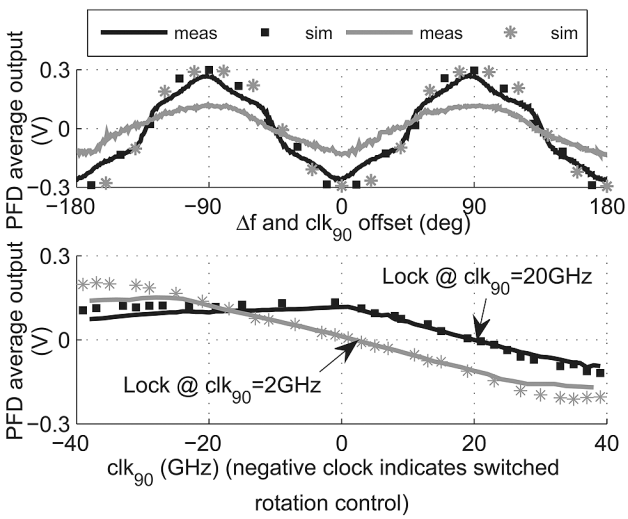

Fig. 17. PFD phase, frequency detection measurements. (*top*) Phase detection characteristic, measurement versus simulation for $\Delta f = 20$ GHz, $f_{\mathrm{clk90}} = 40$ GHz (grey) and for $\Delta f = 15$ GHz, $f_{\mathrm{clk90}} = 30$ GHz (black). (*bottom*) Frequency detection characteristic, measurement versus simulation for $\Delta f = 10$ GHz (black) and $\Delta f = 1$ GHz (grey).

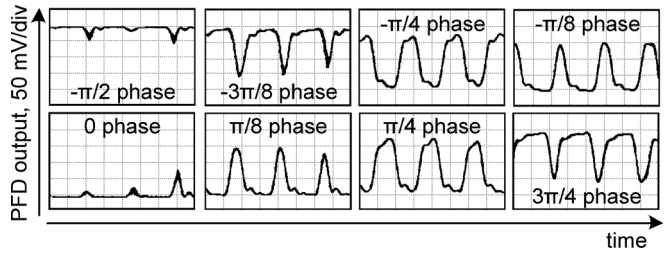

Fig. 18. PFD OUT measured waveforms in phase detection mode for $\Delta f = 2$ GHz and $f_{\mathrm{clk90}} = 4$ GHz.

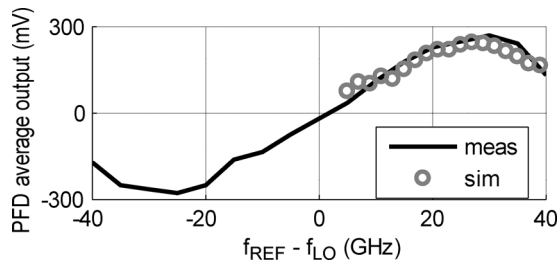

Fig. 19. PFD standalone frequency detection response, measurements versus simulation.

The experimental and simulation results are shown in Fig. 17. In Fig. 17 (*top*), the PFD output is plotted as a function of phase difference with the emulated I/Q photocurrent signals set at 15 (20) GHz and with f_{clk90} set at 30 (40) GHz, i.e., with the system operating in phase-detection mode. The phase error signal varies ± 300 mV at 15-GHz offset and ± 120 mV at 20-GHz offset as the phase is varied through 360°. This indicates proper operation of the phase detector for frequency offsets as large as ± 20 GHz. The phase detection characteristic demonstrates periodicity of 180°, forming two stable points for the loop to lock; a property enables the system to lock on a binary phase-shift keying (BPSK) modulated signal, thus potentially turning the system into a WDM selectable channel receiver. A phase-detection characteristic forms a triangle wave with K_{PD} independent on inputs photocurrents. Such phase-detection behavior results from a phase error measure between the I/Q signal and the offset signal rather than the actual phase between the two lasers; a phase error changing the SSB mixer output duty cycle only.

In Fig. 17 (*bottom*), the PFD output is measured at laser offset frequencies of $\Delta f = 1$ and 10 GHz, by adjusting the SSB mixer LO frequency f_{clk90}. This measured the PFD characteristic in the frequency detection mode. The frequency detection characteristic shows frequency error detection over a ± 40-GHz range, with zero frequency detector output when, as designed, the laser offset frequency is equal to $f_{\mathrm{clk90}}/2$.

The PFD output time waveforms in phase detection mode, as a function of phase offset, for $\Delta f = 2$ GHz and $f_{\mathrm{clk90}} = 4$ GHz are presented in Fig. 18. The output waveform duty cycle varies in a linear fashion as a function of phase offset, forming a triangle characteristic shown in Fig. 17. The ± 20-GHz offset limit for phase detection operation might be explained by the quadrupled frequency beat note, produced at the output of the PFD at a phase detection mode (Fig. 18), pushing the gates to their speed limit (i.e., 80 GHz).

Standalone PFD measurements in frequency detection mode were also performed for ± 40-GHz offset I/Q inputs. Fig. 19 demonstrates the measured triangular wave behavior with a ± 50-GHz period when extrapolated. The ± 50-GHz period is achieved by the 10-ps delay line $\sin(2\pi\Delta f\tau)$ [see (7)]. Modifying the delay line length will result in a tradeoff between the K_{FD} magnitude in the linear mode and the frequency acquisition range. The K_{FD} value and the triangular wave behavior are similar to Fig. 17 (*bottom*), only that the zero crossing point is shifted to the origin as expected for a PFD standalone.

The next 250-nm InP HBT technology node allows design of frequency dividers up to 204 GHz [16] and faster digital logic [18], [23], [24]. In complex ICs, however, the maximum clock rate might also be limited by fan-in, fan-out, gates delay or complex interconnects. By implementing the SSB mixer using the suggested technology it is possible to achieve clock rates of around 80–100 GHz for 40–50-GHz offset locking to meet the modern WDM standards.

A combined phase-frequency characteristic was also numerically generated using a behavioral model with $f_{\mathrm{clk90}} = -10$ GHz (the negative sign denotes a rotation control bit "zero" value) (Fig. 20). The linear frequency detection characteristic crosses zero at $\Delta f = -5$ GHz, where the frequency locking occurs. At this point, the loop switches to a phase detection mode characterized by a triangle function. Yet the plot suggests another phase detection mode for $\Delta f = +5$ GHz as well. This parasitic phenomenon occurs due to the digital (versus linear) nature of the mixer; however, since the frequency detection curve does not cross zero at this offset frequency, a lock cannot occur, as was also shown experimentally [11].

As in the phase-lock state, the IC output produces an output beat note with f_{clk90} frequency (Fig. 6), any attempts to perform lock on frequency offsets lower than the loop bandwidth

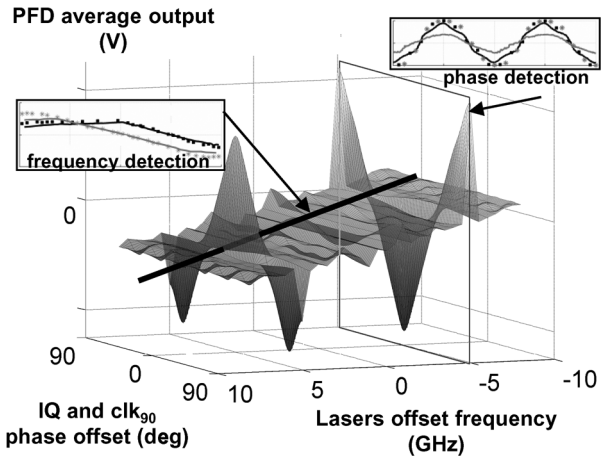

Fig. 20. Numerical PFD simulation for simultaneous phase–frequency detection modes. The offset clock, f_{clk90}, was set to -10 GHz while the laser offset was swept over various phases and frequencies.

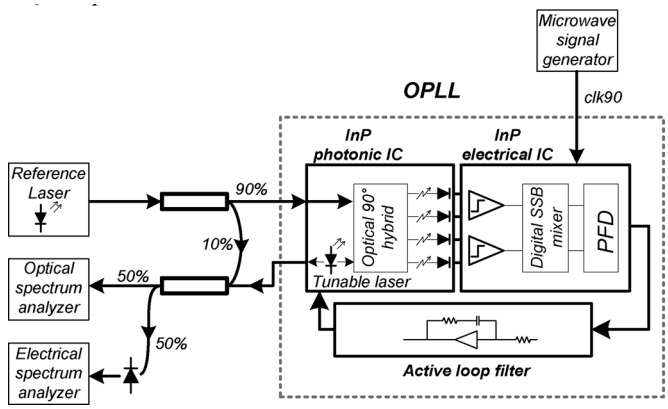

Fig. 21. Simplified offset locking experiment setup (Lu *et al.* [11]).

(f_{PLL}) will bring the loop to track the output beat note, driving the system into a direct laser modulation rather than locking. This behavior imposes a limitation on the lower limit of the frequency offsets range to be $\sim 2f_{\mathrm{PLL}}$.

VI. System Experiment

A system experiment comprising the reported SSB mixer IC was carried out by Lu *et al.* and was reported in [11].

The optical PLL was integrated on a 10×10 mm AlN carrier substrate. The system (Fig. 21) includes an InP photonic IC [8], the SSB mixer/phase-frequency detector IC described in this paper and an external 500-MHz loop bandwidth, feed-forward-compensated op-amp loop filter [10]. The photonic IC contains a tunable SG-DBR laser, an optical 90° hybrid, and four photodiodes for delivering a differential I/Q components of the lasers beat note.

The reference laser was provided to the photonic IC by an Agilent 8164B Lightwave Measurement System featuring a 100-kHz linewidth, while the offset frequency, clk_{90}, was set by an Agilent E8257D microwave signal generator. The local SG-DBR laser was coupled out and externally mixed with the reference laser for monitoring purposes. The linewidth of

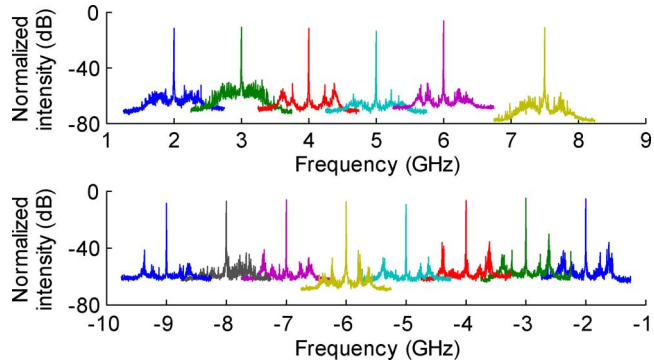

Fig. 22. Electrical spectrum analyzer image of the two lasers beat note when phase locked with various frequency offsets (Lu *et al.* [11]).

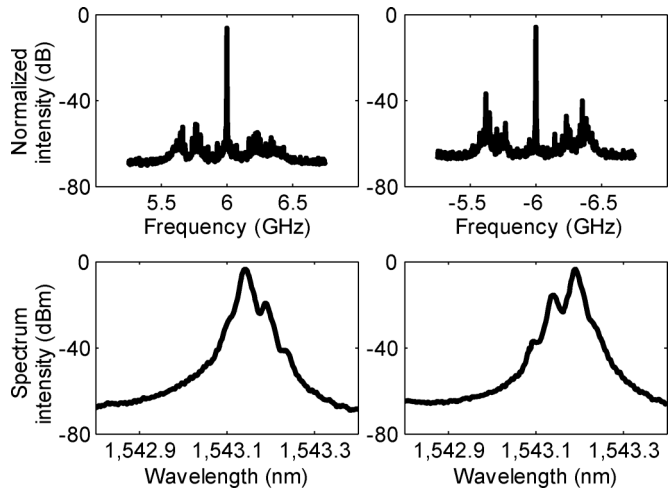

Fig. 23. (*left*) Beat note spectrum of two lasers (*top*) and optical spectrum (*bottom*) when phase locked with +6-GHz offset. (*right*) Beat note spectrum of two lasers (*top*) and optical spectrum (*bottom*) when phase locked with −6-GHz offset. The reference laser has the higher power. Measured with 5-kHz resolution bandwidth (Lu *et al.* [11]).

an unlocked SG-DBR laser was above 100 MHz. The overall optical spectrum was inspected by an HP 70004A optical spectrum analyzer to verify a SSB locking nature, while the locked laser linewidth was measured by inspecting the mixed beat note using the R&S FSU spectrum analyzer.

The integrated SG-DBR laser was successfully phase locked to the reference with offsets ranging from -9 to $+7.5$ GHz (Fig. 22). The offset locking sign was set by applying proper rotation control signal and the system kept locked while the RF offset frequency (clk_{90}) was gradually swept both in the negative and positive ranges. To confirm the SSB fashion of locking, the optical spectrum was measured to compare the reference and the local laser wavelengths (Fig. 23). It was impossible to lock with frequency offsets as low as the loop bandwidth since the low-frequency beat note provided by the PFD cannot be integrated.

The phase noise of the optical PLL includes contributions from the RF source, the EIC, and the optical system (laser open loop noise divided by the loop transmission). Additional study on a full system characterization and phase-noise performance is currently carried out.

VII. Conclusion

We have demonstrated a novel broadband ±20-GHz optical frequency synthesis IC in 0.5-μm InP HBT technology. The all-digital mixer topology eliminates the dependency on input photocurrent, increases the offset locking range, and improves the design robustness by shifting to a digital domain. The IC is comprised of a SSB mixer and a Quadricorrelator PFD with frequency acquisition range up to ±40 GHz. A full integration of the mixer with the PFD drastically reduces the limitation on loop delay, making larger loop bandwidths possible.

Acknowledgment

The authors would like to thank Teledyne Scientific and Imaging, Thousand Oaks, CA, for MMIC fabrication.

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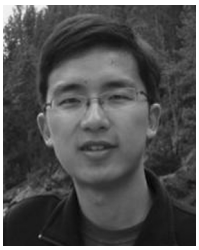

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