# Fully integrated hybrid silicon free-space beam steering source with 32 channel phased array

J. C. Hulme, J. K. Doylend, M. J. R. Heck, J. D. Peters, M. L. Davenport, J. T. Bovington, L. A. Coldren, and J. E. Bowers

ECE Dept., Univ. of California, Santa Barbara (United States)

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## ABSTRACT

Free-space beam steering using optical phased arrays is a promising method for implementing free-space communication links and Light Detection and Ranging (LIDAR) without the sensitivity to inertial forces and long latencies which characterize moving parts. Implementing this approach on a silicon-based photonic integrated circuit adds the additional advantage of working with highly developed CMOS processing techniques. In this work we discuss our progress in the development of a fully integrated 32 channel PIC with a widely tunable diode laser, a waveguide phased array, an array of fast phase modulators, an array of hybrid III-V/silicon amplifiers, surface gratings, and a graded index lens (GRIN) feeding an array of photodiodes for feedback control. The PIC has been designed to provide beam steering across a  $15^{\circ}x5^{\circ}$  field of view with  $0.6^{\circ}x0.6^{\circ}$  beam width and background peaks suppressed 15 dB relative to the main lobe within the field of view for arbitrarily chosen beam directions. Fabrication follows the hybrid silicon process developed at UCSB with modifications to incorporate silicon diodes and a GRIN lens.

**Keywords**: silicon photonics, LIDAR, free-space communication, optical phased array, laser, tunable laser, hybrid silicon, integrated optics, beam steering, photonic integrated circuit

## 1. INTRODUCTION

Free-space beam steering has a wide range of applications. Of particular interest is light detecting and ranging (LIDAR) which collects high resolution three-dimensional images at high data acquisition rates. LIDAR can be used regardless of ambient light conditions and has better resolution than radar. It can even capture high resolution images beneath forest canopy and camouflage netting<sup>[1]</sup>. Another application of interest is free-space point-to-point communication links where beam-steering maintains continuous data transmission by compensating for relative shifts in position between link points due to accidental (e.g. building sway) or purposeful (e.g. vehicle/satellite travel) movement. Additionally, one can select between several receiving points for selected bursts of data transmission.

Many implementations of free-space beam-steering require mechanically moving parts which are susceptible to mechanical wear and which typically suffer in performance due to vibrations and inertial forces.

#### 1.1 Optical phased arrays and silicon photonics

Optical phased arrays offer an alternative method of beam-steering and shaping that requires no moving parts<sup>[2]</sup>, and have been used to demonstrate both LIDAR<sup>[3]</sup> and free-space communication links<sup>[4]</sup>. Typically these applications have been implemented by assembling individually packaged optical components into a larger system. However, there are several advantages to using an integrated approach where most optical components are combined within a single photonic integrated circuit (PIC)<sup>[5][6]</sup>.

The integrated approach toward photonics reduces the overall size, weight, and cost of a device by removing packaging for individual components. It also removes much of the difficulty and cost of aligning each component with the others.

Additionally it is more tolerant to mechanical stresses from vibrations that might cause misalignment in assembled devices.

Silicon photonics provides a viable platform to realize integrated optical phased arrays while taking advantage of the CMOS processing facilities and knowledge that have accumulated over the past few decades. In recent years, optical phased arrays have been demonstrated using a silicon-on-insulator (SOI) platform with passive silicon waveguides and output gratings combined with resistive heaters for phase control<sup>[5][6][7]</sup>, but this approach has demonstrated beam-steering using off-chip laser sources. While partial integration is an improvement, these devices still suffer from the additional packaging and aligning needs and the vibrational intolerance which come from separate components. Fiber-coupling to SOI adds the further disadvantage of a large difference in refractive index which introduces coupling losses. Additionally, propagation losses along different channels will inevitably be unequal due to processing variations, which will limit the accuracy of the optical phased array. Optical coupling and propagation losses reduce the efficiency of the device and limit the output power in the main beam lobe.

The hybrid silicon platform developed at UCSB<sup>[8][9]</sup> offers a method well-suited for integrating an optical phased array with on-chip light amplification. III-V material is bonded to SOI wafers already patterned with passive waveguides, splitters, and output grating couplers. III-V devices are patterned and defined with lithography, giving nano-scale alignment. Light from the waveguides evanescently couples into the III-V quantum wells for light amplification and allows both amplifiers and lasers to be fully integrated with the passive devices. This report describes the design, fabrication, and demonstrated beam-steering of such a device.

## 2. CONCEPT

An optical phased array designed for two-dimensional beam-steering and shaping is typically formed by arranging emitter elements in a two-dimensional matrix. The far-field sum of the outputs can be shaped into a beam and steered to a desired angle by phase-tuning each element in the matrix. This method works well but has a fundamental problem with scalability. For an N x N matrix,  $N^2$  phase controls are needed.

Alternatively, two-dimensional beam-steering can be achieved with a one-dimensional optical phased array using a surface grating emitter which acts as the second dimension of the optical phased array. In this configuration, each tooth of the grating scatters power from the optical mode with a phase delay dependent on the effective index of the mode. Emission from a single channel becomes a line in the far-field (perpendicular to the waveguide direction of propagation) with the emission angle determined by wavelength ( $\lambda$ ), the waveguide effective index (n<sub>eff</sub>), and the grating period ( $\Lambda$ ) as shown in Eq. (1)

$$sin(\theta) = \frac{\Lambda n_{\rm eff} - \lambda}{\Lambda}.$$
 (1)

Thus, by simply tuning the wavelength, the beam can be steered in one axis. The beam will be passively collimated in that axis to a degree dependent on the length of emission along the grating. By combining an array of surface grating emitters two-dimensional beam-steering can be achieved where the axis parallel to the waveguides (henceforth referred to as  $\theta$ ) is tuned with wavelength and the axis perpendicular to the waveguides (henceforth referred to as  $\psi$ ) is tuned by phase-tuning the individual channels.

The simplest version of this configuration with *N* channels can be realized using a tunable laser coupled to a beamsplitter tree of *N*-1 splitters which separates the beam into *N* channels, a phase modulator for each channel, and a grating emitter for each channel. This can be achieved with an off-chip laser source and resist-heaters for tuning elements, and was demonstrated in Generation I<sup>[6]</sup>. However, better functionality can be achieved by using a hybrid silicon platform to incorporate an on-chip laser, a pre-amplifier, and gain elements for each channel to compensate for channel-dependent losses and to increase the overall output of the device. Such a PIC would require 2N + 2 controls as opposed to the  $N^2$  controls required by the standard configuration. Tuning the  $\theta$  axis with wavelength removes an entire dimension of control requirements. A CAD layout of a 32-channel design is shown in Figure 1.



Figure 1. Layout of the 32-channel PIC. Redundant tunable laser sources are followed by semiconductor optical amplifier (SOA) pre-amplifiers. The beam is split into 32 channels which are individually phase tuned and amplified. The channels feed an array of surface grating for free-space emission. The angle of emission of the beam is determined by wavelength in the  $\theta$  axis and by relative phase in the  $\psi$  axis. The remaining beam power is imaged into the far field with a Fourier lens feeding photodiode array for on-chip feedback.

## 3. COMPONENT DESIGN

#### 3.1 Channel output spacing and count

The angular separation between the main lobe and the side lobes in the  $\psi$  axis is determined by the channel spacing *d* between output waveguides (center to center). Decreasing the channel spacing increases angular separation. Also, the peak power in the side lobes is a function of the ratio of output waveguide width to channel spacing, so an optimized system requires large output waveguides with slightly larger channel spacing. Practically, there must be a finite spacing between waveguides to prevent the modes from overlapping and causing crosstalk between channels. A final consideration is that increasing the total width of the array (i.e. the product of  $(N-1)\cdot d$ , where *N* is the number of channels and *d* is the channel spacing) decreases the width of the beam and increases the ratio of power in the main lobe to power in the side lobes. Plots of the calculated side lobe separation vs. channel spacing and beam width vs. array width are shown in Figure 2.



Figure 2. (a) Calculated far field separation between main lobe peak and side lobe base (i.e. where the side lobe rises above - 10 dB relative to the main lobe peak) vs. waveguide pitch, and (b) calculated far field beam width vs. total array width.

#### 3.2 Laser and amplifiers

The gain elements for the tunable laser and the SOAs were based on the design reported by Kurczveil et al.<sup>[10]</sup> with an alteration of the width of the rib waveguide to 2.5  $\mu$ m within the SOA gain regions so as to increase mode volume and maximum output power. The length of the channel amplifiers was chosen as 2.3 mm for high output powers, while the preamplifier length was chosen as 1 mm.

The tunable laser (Figure 3) was designed using two bus waveguides, each with a gain section, coupled together using two ring resonators as described in <sup>[11]</sup>. The rings are chosen of circumferences 400  $\mu$ m and 420  $\mu$ m respectively such that their respective transmission spectra overlap only once within the gain bandwidth of the device (Figure 4). The tunable laser had a narrow linewidth of less than 1 MHz over the tuning range. Typical linewidth and side mode suppression measurements are shown in Figure 5. Thermo-optic tuning of the ring spectra allowed the transmission peak to be tuned over 41 nm (Figure 6).



Figure 3. (a) Schematic and (b) photo of the hybrid silicon tunable laser developed for the scanner



Figure 4. (a) Calculated transmission of the two rings, (b) calculated round-trip loss of the two rings, and (c) alignment of the FSR of the two measured rings showing the overlap of the FSR outside the gain of the hybrid silicon gain regions.



Figure 5. (a) Linewidth of the tunable laser and (b) side mode suppression of the other modes of the two cavities



Figure 6. Superimposed spectra of tunable laser showing (a) coarse tuning over 41 nm and (b) 0.1 nm resolution fine tuning over 2.5 nm.

#### 3.3 Phase modulators

The phase modulator was designed to tune phase thermo-optically by applying a forward bias to a p-i-n diode overlapping the waveguide. Phase-dependent losses in the waveguide due to free-carrier absorption were made negligible by placing the n and p regions 11 µm apart.

Diode dopant profile after ion implantation and annealing was modeled using the Silvaco ATHENA software package, and the current-voltage characteristics and associated carrier densities within the waveguide were modeled using the Silvaco ATLAS software package. Carrier lifetimes within the waveguide were assumed to be 0.9 ns for this calculation in accordance with the data reported by Dimitropoulos et al.<sup>[12]</sup>. Thermal tuning was predicted to be 57 mW/ $\pi$  using the relation given in Eq. (2)

$$P_{\pi} = \frac{\lambda \sigma w}{2t \frac{dn}{dt}},\tag{2}$$

where  $\lambda$  is the wavelength,  $\sigma = 1.35 \times 10^{-2}$ W cm<sup>-1</sup>K<sup>-1</sup> is the thermal conductivity of the buried oxide,  $w = 10 \,\mu\text{m}$  is the effective width over which the heat is dissipated (approximated by the width of the intrinsic region),  $t = 1 \,\mu\text{m}$  is the thickness of the buried oxide, and  $dn/dT = 1.86 \times 10^{-4} K^{-1}$  is the thermo-optic coefficient of silicon.

The phase modulator was designed to be 2 mm long. A cross-section of the device and plots of phase shift and expected carrier density-induced loss vs. bias are shown in Figure 7.



Figure 7. (a) Cross-section of the phase modulator profile, and (b) predicted thermo-optic tuning and free-carrier induced excess loss vs. thermal power.

## 4. FABRICATION

Device fabrication began with an SOI wafer with 500 nm top silicon and 1  $\mu$ m buried oxide. Rib waveguides were lithographically patterned and etched to a depth of 275 nm. Phase modulator diodes were formed by implanting the silicon with boron and phosphorus dopants and then annealing for 10 minutes at 1050°C. Output surface gratings were patterned using e-beam lithography and then etched to a depth of 50 nm. III-V epitaxial material was wafer-bonded to the top silicon and then patterned and etched to form the laser and amplifier gain sections. Metal contacts were then deposited in an e-beam evaporation chamber. Buffer layers of SU8 and PECVD SiO<sub>2</sub> were used to prevent optical losses in the waveguide from metal traces.

## 5. GENERATION I<sup>[6]</sup>

## 5.1 Generation I design

For simplicity, Generation I used an external laser capable of tuning from 1525 nm to 1605 nm. No gain elements were introduced on-chip, and active components were limited to resistive thermo-optic phase tuners overlaying the waveguides.

Specific goals for this system include a steering range of greater than  $20^{0}$  ( $\psi$ ) x  $10^{0}$  ( $\theta$ ), a full-width half-maximum (FWHM) less than  $2^{0}$  in both axes, and a side lobe suppression ratio (i.e. the ratio of the main lobe peak intensity to background peak intensity) of 10 dB within the  $20^{0}$  steering window. This translates into a matrix of 10 x 5 resolvable spots in the far field.

To achieve the required  $20^{\circ}$  field of view, side lobes greater than 10 dB must fall outside that window even when tuning to the maximum angle (i.e.  $\pm 10^{\circ}$ ). This requires that the channel spacing be no greater than 6.5 um at a wavelength of 1550 nm. For this system we chose a channel separation of 3.5 µm which limits the significant side lobe suppression to beyond 23.7° from the center of the main lobe. For a far-field beam width of less than 2° the total array width must exceed 35 µm, thus for d = 3.5 µm we chose N = 16. A 16-channel laser driver was purchased to interface with the device.

Surface gratings were chosen to have a pitch of 0.55 µm and a duty cycle of 20%.

The layout of the Generation I PIC is shown in Figure 8. Highlighted results are described below.



Figure 8. Layout of the Generation I device including 1x16 waveguide splitter, phase modulators, and grating array.

## 5.2 Generation I results

The output beam from the PIC was measured in the far field using an imaging lens system with an IR camera. A feedback algorithm adjusted the phase on each channel using the 16-channel laser driver, similar to the method described in [6].

Beam steering of  $20^0 \times 14^0$  was achieved. Profiles of the  $\psi$  axis normalized optical output power, both calculated and measured, are shown for four locations (Figure 9). Figure 10 contains plots of the beam profile for scanning across both dimensions, and 2D plots of the measured beam at the extents and center of the field of view are shown in Figure 11.



Figure 9. Plots of calculated and measured beam profiles in  $\psi$  with phase tuning to optimize side mode suppression at 0 and -7 degrees for 1525 nm and 1625 nm input wavelengths.



Figure 10. Normalized measured optical output power in the far-field (a) scanning wavelength and (b) phased array tuning.



Figure 11. Plots of the measured beam profiles in the far field at the extents of the field of view. Secondary peaks are outside the field of view and not shown.

## 6. GENERATION II<sup>[13][14]</sup>

## 6.1 Generation II design

The purpose of Generation II was to add on-chip laser and amplification sections. A reduction in the number of channels to N = 8 was required in order to drive channel amplifiers and phase modulators with the same 16-channel laser driver. To maintain a 2<sup>o</sup> beam width the channel separation was increased to 5.5 µm which limits the significant side lobe suppression to beyond 14.8<sup>o</sup> from the center of the main lobe and gives an expected field of view of greater than  $12^{o}$  in  $\psi$ . The on-chip laser described above was designed to have a 40 nm tuning range giving an expected field of view of 5.6<sup>o</sup> in  $\theta$ .

Phase modulators for this generation used the *p-i-n* diode design described in Section 3.3 above.

The layout of the Generation II PIC is shown in Figure 12.



Figure 12. Layout of the Generation II device including tunable laser, pre-amplifier, 1x8 waveguide splitter, channel amplifiers, phase modulators, and grating array.

## 6.2 Generation II results

## 6.2.1 Tunable laser

The second generation chip had an eight channel emitter with an integrated tunable laser. The on-chip lasers were characterized and were found to typically have 5.5 mW output power, < 340 kHz linewidth, 45 dB side mode suppression, and 41 nm tuning range (1556 nm to 1597 nm), as described in Section 3.2 above. However, the particular laser integrated with the emitting array had faulty ring tuners, so only one axis of tuning for the integrated PIC is characterized below. The Generation III design has redundant on-chip lasers to avoid this problem.

## 6.2.2 Phase modulators

Phase tuner current-voltage characteristics were used to estimate the effective carrier lifetime, which was determined to be 1.9 ns instead of the predicted value of 0.9 ns. Calculations of the carrier densities suggested free-carrier absorption of 0.75 dB and free-carrier induced phase shift of -0.8 radians for 100 mW of dissipated power. The thermo-optic tuning efficiency including the negative effects from free carriers was measured on a Mach-Zehnder interferometer to be 97 mW/ $\pi$ . The measured result is shown in Figure 13 along with a fit curve using the carrier lifetimes derived from the current-voltage characteristic and the measured thermo-optic efficiency.

The silicon slab was etched down to the buried oxide between devices to reduce thermal crosstalk between channels. However, thermal isolation between the phase modulators and the SOAs was not sufficient to remove phase-dependent fluctuations in output power based on chip-scale heating.



Figure 13. Thermo-optically tuned Mach-Zehnder interferometer transmission measurement and fit line. The fitted curve was calculated using the measured phase-tuning efficiency and the calculated attenuation from free-carrier absorption (deduced from the effective carrier lifetime).

## 6.3 Photonic Integrated circuit

Channel powers were equalized by emitting from one channel at a time and observing the intensity in the far field, then adjusting the SOA currents appropriately. One channel was found to be faulty in this device (channel 5) and was turned off for the remaining measurements – this limited the maximum possible background to 8.3 dB within the field of view. 7 dB background suppression was consistently measured with a beam width of  $1.8^{\circ}$  in the  $\psi$  axis and  $0.6^{\circ}$  in the  $\theta$  axis.

Due to poor thermal isolation between the SOAs and phase modulators, SOA gain was highly dependent on the phase modulator settings. To reduce this effect and the overall temperature of the chip, phase modulator and SOA currents were cycled at 125 Hz, with a 20% duty cycle. The preamplifier was used to blank the beam for the first 800  $\mu$ s to avoid any contamination of the far-field signal while the phase modulators and SOAs were ramping up. During the profiling, the chip was mounted on a heat sink held at 18<sup>o</sup> C.

While holding the wavelength constant the beam was profiled and steered across the far field at 1<sup>°</sup> increments from -6<sup>°</sup> to +6<sup>°</sup> in the  $\psi$  axis. Wavelength tuning was not possible in this circuit due to faulty heater pads. However, with the 41 nm of tuning observed in a similar device on the chip, and with the measured wavelength steering of 0.14 <sup>°</sup>/nm for the surface gratings<sup>[6]</sup>, an expected 5.7<sup>°</sup> of tuning in  $\theta$  axis is possible. A plot of measured and predicted beam crosssections for each axis is shown in Figure 14, and plots of the beam steered to directions in the far field across a 12<sup>°</sup> range are shown in Figure 15.



Figure 14. Measured and predicted beam cross-sections in (a) the phase-tuned  $\psi$  axis and (b) the wavelength-tuned  $\theta$  axis. The inset shows the two dimensional profile of the beam.



Figure 15. Measured beam profiles in the far field for the beam steered from  $-6^{\circ}$  to  $+6^{\circ}$  showing (a) both main and side lobes and (b) the aperture field of view.

As mentioned above, varying the phase modulator settings to change the output angle resulted in widespread chip heating. This affected the gain of the laser and amplifier elements and resulted in a non-uniform output beam power for disparate angles. However, it was found that these variations in beam output power could be completely compensated by adjusting the pre-amplifier pump current without altering the beam width or background suppression. Thus beam power was made flat as a function of steering angle.

The beam power was measured with a detector positioned in the far field and found to be 4.1  $\mu$ W. Side mode suppression and linewidth were measured by steering the beam to a fiber collimator connected to an APEX 2051A optical spectrum analyzer. Side mode suppression in the far field was 30 dB and linewidth was 36 MHz, both somewhat degraded from the standalone laser characteristics. This degradation is to be expected considering the many sources of feedback into the laser which come from the integrated device and is small enough as to not significantly affect the beam with respect to the target background suppression and beam width.

## 7. GENERATION III DESIGN

The Generation III design goals include > 20 dB background suppression,  $< 1^{0}x1^{0}$  FWHM, and a  $12^{0} x 6^{0}$  steering window. This translates into an array of 12 x 6 resolvable spots. Tuning speeds higher than 4 x  $10^{6}$  % c are also desired.

In addition to adjustments that have been made to the design of individual components such as phase modulators and gain elements, two additional components have been added to the PIC – A photonic crystal lens designed to convert the in-plane array output into the far field and a photodiode array were integrated for on-chip feedback. Figure 16 shows a block diagram of the 32 channel PIC.

Generation III chips are currently in fabrication and nearing completion with measured results pending.



Figure 16. Generation III device configuration. The inset shows the CAD layout of the PIC.

## 7.1 Generation III channel output spacing and count

To decrease the beam width, the total width of the output array has been increased by changing the channel count to 32. Also, the channel spacing has been decreased in order to increase the angular separation of the side lobes.

Although the Generation I & II designs used uniform channel spacing, this is not necessarily the optimum geometry. Calculations were done using uniform, Gaussian, Lorentzian, and parabolic spacing. It was found that uniform and Gaussian spacing were the most promising geometries and devices with each were designed. They have respective total array widths of 126  $\mu$ m and 144  $\mu$ m. The calculated far field beam is shown in Figure 17 for uniform output power and phase from each channel. Additional improvements can be made by varying the relative channel output powers and phases.

For the uniformly spaced channel device a star coupler was used to split the laser into the various channels with the intent that the central channels would receive more power relative to the outer channels. This should have a similar effect as the Gaussian spacing by concentrating more power toward the center of the output array. Adjustments to maximize the background suppression will be made with individual channel amplifiers.



Figure 17. Calculated far field for (a) uniform and (b) Gaussian channel spacing using no relative phase or output power differences between channels.

## 7.2 Lasers, amplifiers and phase modulators

The gain elements used in this design were based on the same design as in Generation II but with shorter adiabatic tapers in the III-V. It was suspected that the longer tapers were not being pumped well and therefore generating excess loss.

To maximize yield, several lasers were coupled to the input of the PIC. One was chosen as the same design as in Phase I, and the rest were chosen with a similar design but with only one gain region of increased length. Also, a phase section using a resistive heater was added in place of the second gain region.

A pre-amplifier 1.5 mm in length was placed after each laser to maximize the input power before being split into channels. Each channel amplifier was chosen to be 3 mm in length to maximize the total output power.

#### 7.3 Phase modulators

Phase modulators for this run were designed to employ electro-optic phase tuning in order to increase the tuning speed of the PIC. They were designed as *p-i-n* diodes similar to those in Generation II, but with the *p* and *n* regions closer together to decrease resistance. In this way less heat (which counteracts the electro-optic affect) is generated. The electro-optic tuning efficiency was measured on a Mach-Zehnder interferometer and found to be 14 mA/ $\pi$ . This falls within a low power regime where thermo-optic tuning is less present. The measured result is shown with a fit curve in Figure 18 along with the frequency response of the device. The device shows sufficient tuning speed for the proposed metrics with a 3 dB bandwidth greater than 50 MHz.



Figure 18. Output power relative to the loss of a straight waveguide (a) and frequency response (b) of a Mach-Zehnder modulator.

#### 7.4 Lens and photodiode array

An on-chip feedback mechanism was designed using a 1D graded index (GRIN) lens to image the  $\psi$  axis far field onto a photodiode array positioned in the Fourier plane. The lens was made by varying the effective index across the top silicon layer of an SOI slab. Sub-wavelength circles with varied diameters were etched into the silicon and filled with SiO<sub>2</sub>. A parabolic index profile was designed by linearly varying the circle diameters (parabolically varying area) across the lens (Figure 19). A focal length of 473 µm is expected.

The waveguides feeding the photodiode array are located on the lens focal plane and span 64  $\mu$ m. There are 32 photodiodes giving 1.3<sup>o</sup> far field resolution and a total field of view of 41<sup>o</sup>.

Simulations of the electric-field profile and the expected power profiles at the output of the lens feeding the photodiode array are shown in Figure 20. The output powers incident on the photodiodes are calculated for several configurations of linear phase differences between adjacent channels of a uniformly spaced grating array.



Figure 19. A plot of the calculated refractive index profile cross section for the GRIN lens.



Figure 20. Simulated electric field profile for silicon GRIN lens (a) and calculated output powers from the lens for linear relative phase delays between adjacent channels.

## 7.5 Integrated 32 channel device

The layout of the full 32-channel device is shown in Figure 1. One of the larger challenges in driving this device is the difficulty in interfacing with the 100 different signals required. A driver board of significant complexity was designed, built, and programmed to supply current to the chip and receive communication from an external computer. As photonic integrated circuits grow in complexity, driving them and interfacing with them will be an increasingly difficult task.

## 8. CONCLUSION

A photonic integrated circuit fabricated on a hybrid silicon platform was demonstrated with free-space steering of a laser beam using an optical phased array integrated with a tunable laser. Phase controlled steering over  $12^{0}$  was achieved in  $\psi$  with a  $1.8^{0} \times 0.6^{0}$  beam width, and the on-chip tunable laser was shown to having a tuning range providing  $5.6^{0}$  of steering in  $\theta$  which results in a  $7 \times 9$  resolvable spots in the far field with 7 dB background suppress.

A new photonic integrated circuit has been designed to achieve  $12\times6$  resolvable spots with a beam width less than  $1^0\times1^0$  and rapid beam steering of steering  $4\times10^{6}$  % in  $\psi$ .

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