Single-chip integrated transmitters and receivers

Larry A. Coldren,* Leif. A. Johansson, Mingzhi Lu, Hyun-chul Park, John Parker, Abirami Sivananthan, and Mark Rodwell

Department of Electrical and Computer Engineering, University of California, Santa Barbara, California 93106, USA

coldren@ece.ucsb.edu

Abstract: Compared to traditional optics, photonic integrated circuits have advantages in size, weight, performance, reliability, power consumption, and cost. The size and stability also enable them to realize unique functions in coherent optics. Optical phase-locked loop (OPLL) based transmitters and receivers are examples. With photonic integration, the loop bandwidth of the OPLL can increase by orders of magnitude, and stable OPLLs have been achieved with closed-loop bandwidths >1 GHz.

OCIS codes: (250.5300) Photonic integrated circuits; (060.0060) Fiber optics and optical communications; (060.1660) Coherent communications; (250.0250) Optoelectronics.

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1. Introduction

Since the invention of the first semiconductor laser fifty years ago, significant efforts have been devoted to the area of photonic integration [1–21]. Not only have the photonic integrated circuits (PICs) become more functional, the integration scale has also gone up significantly. Currently, researchers have demonstrated the ability to integrate most of the optical components on a single chip, including: lasers, modulators, detectors, amplifiers, phase shifters, couplers, and polarization rotators. By integration, the size, weight, and combined insertion loss of the optical components decrease greatly. Within the footprint of a millimeter scale, the full function of transmitting, receiving, filtering, or even O-E-O conversion can be realized [5].

Besides size and weight, smaller power consumption is also an advantage for photonic integration. Semiconductor lasers, amplifiers and other integrated components can have quite high wall-plug efficiency. By integrating a lot of components monolithically, the insertion loss will be greatly reduced, less optical power will be needed, and total thermoelectric cooler (TEC) power consumption will also decrease significantly.

Photonic integrated systems also have better performance and are more reliable. Integration makes the system much more stable and more resistive to environment fluctuations, compared to free-space optics and fiber-pigtailed components. Large-scale integration also cuts down the number of fiber couplers, which not only decreases the insertion loss, but also improves the reliability of the system.

As the most important driving force of photonic integration, the ever-increasing data stream of fiber optic communication requires the transmitters and receivers to have a smaller footprint, higher bandwidth efficiency, higher data rate, lower power consumption, and relatively low cost [6]. Therefore, a large number of integrated transmitter and receivers have been demonstrated in the recent literature and released on the market. An 8-by-8 tunable optical router has been demonstrated, operating at 40 Gb/s per channel [7]. 500 Gb/s monolithic transmitters and receivers are already on the market, and 1 Tb/s monolithic transmitters and receivers have been realized and will be commercially available soon [8].

Furthermore, besides improving and replacing the already-existing system, PICs have an important role of creating new optical systems that are difficult or even impossible to be realized using free-space optics or fiber-pigtailed components, especially in the area of coherent optics. The stability of the PIC enables the possibility of full engineering control

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over the phase of light. A series of PICs have been demonstrated with superior performance, such as a linear analog receiver with push-pull modulators and an optical feedback loop [9], several designs of tunable and programmable microwave photonic filters [10], 2D beam-steering PICs [11,12], and several prototypes for optical phase-locked loops [13–18].

The phase-locked loop (PLL) was proposed in 1930s and has been widely used in most of the communication systems that we are using today, including FM radios, cell phones, computers, and GPS. The optical phase-locked loop (OPLL) on the other hand, was realized in 1965, yet it has never been sold commercially. The major reason behind this has been the difficulties of building stable OPLL using traditional optic building blocks, such as free-space lenses and fiber-pigtailed devices, because a stable OPLL needs a very short loop delay and the bulk optics are simply too big and lack stability. However, photonics integration has solved the loop delay problem and makes the OPLL more accessible for real applications.

In this paper, we will overview recent advances in photonic ICs for coherent communications and sensing applications within our research groups at UCSB. The commonly-used integration platform and integration technology will be introduced. Taking the advantage of the compactness and phase stability of integration, several OPLL PIC engines have been built based on the same integration platform and integration technology for coherent optics applications. A phase-locked tunable transmitter that might be useful in communication or sensor systems, and a homodyne coherent receiver based on Costas loop are included as examples.

2. Integration technology

Before diving into the specific PICs and the transmitter/receiver performance, it is worth describing the technology that allows us to achieve the integration of different optic components without compromising device performances. Several commonly used integration platforms and active/passive definition technologies are illustrated in Ref [3]. based on InGaAsP/InP material system, including vertical twin-guide, butt-joint regrowth, selective area regrowth, offset quantum wells, dual quantum wells and quantum well intermixing (QWI) technology [19]. Among all these, QWI platform has advantages of high gain, low loss in passive section, almost no reflection in the active/passive transition and simple fabrication, while offset quantum well and butt-joint are also widely used in academia and industry research. The structure of the QWI platform is shown in Fig. 1 as well as a scanning electron microscope (SEM) picture.

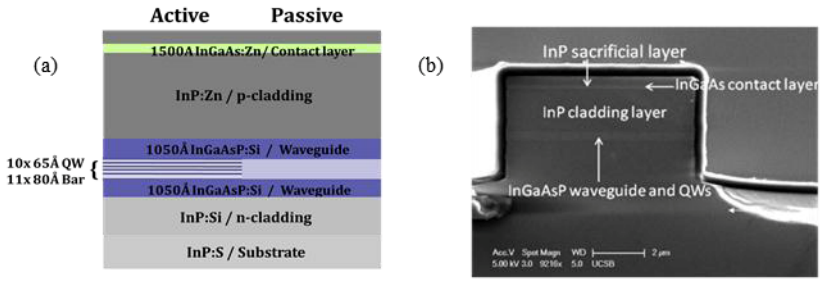

Fig. 1. (a) The epitaxial structure of the QWI platform. (b) A SEM picture of the cross section of a waveguide based on QWI platform.

The QWI process starts with a base epitaxial structure including waveguide layers, centered quantum wells and a 450 nm InP buffer layer above them. A selective-area phosphorous implant is then carried out with a energy of 100 keV and a dose of 5e14 cm^{-2} to create point defects. By annealing at 675 °C, vacancies move through the quantum-well region, intermixing barriers with wells, and the photoluminescence (PL) peak blue-shift increases linearly for the first 80 nm. The maximum PL peak shift can be as large as 130 nm,

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which ensures low-loss at the operating wavelength. Therefore, active and passive areas are defined on the wafer. Moreover, multiple bandwidth band edges are also possible to achieve on the same wafer. By removing the 450 nm InP implanted buffer layer on top of the waveguide layer, PL blue shift will be stopped even when further annealing is carried out. Figure 2 shows the QWI process and the peak photoluminescence peak shift as a function of annealing time [19].

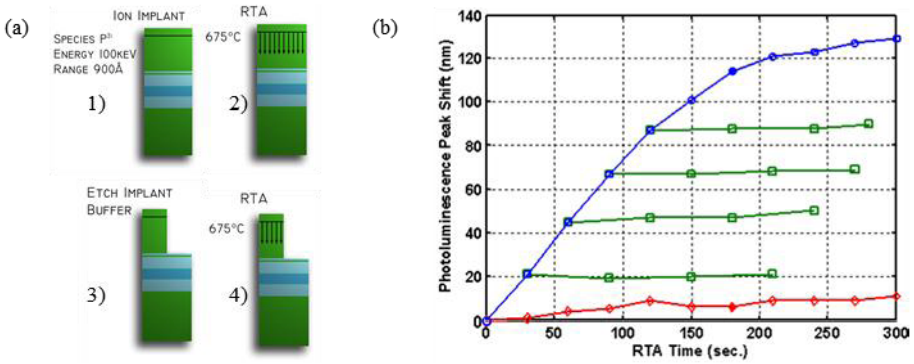

Fig. 2. (a) shows the QWI process. (b) The photoluminescence peak shift as a function of anneal time, showing the initial linear increase in the peak shift and the complete halting of the peak shift for samples for which the implant buffer layer has been etched. Symbols indicate nonimplanted (triangles), implanted (circles), and samples with partial anneal followed by the removal of the implant buffer layer (squares).

After QWI, the buffer layer is removed, gratings are defined by electron-beam lithography, and a blanket P-InP cladding and P-InGaAs contact regrowth will be carried out. Thus, the p-i-n photodiode is formed.

Following that is the waveguide definition. Both surface ridge waveguides and deeply etched waveguides are frequently used. The surface ridge waveguide has better heat dissipation and less reflection, but the waveguide bending angle is limited because of the crystallographic wet etch process. On the other hand, the deeply etch waveguide has a higher mode confinement, and has more design flexibilities to achieve sharp bends and rings. The process of the surface ridge waveguide is fairly straightforward. A Methane/Hydrogen/Argon reactive ion etch (RIE) is used, and PECVD Si_3N_4 acts as the hard mask. An HCl-based crystallographic wet etch is used to finish the waveguide definition. As for the deeply etched waveguide, they are defined with photoresist on a Cr/SiO_2 bilayer hardmask. The Cr is etched using a low power Cl_2/O_2 ICP-RIE etch, and SF_6/Ar ICP-RIE is used for a vertical SiO_2 etch. The resulting 600 nm SiO_2 mask acts as a hardmask to define the InGaAsP/InP deeply etched waveguides using a Cl_2/H_2/Ar ICP-RIE etch with the substrate temperature of 200 °C.

After the waveguide definition, N-contact etch and top N metal deposition, BCB definition, P contact open and P metal deposition will be carried out in sequence. Capacitors, RF transmission lines are also defined simultaneously.

By using the integration platform and the process flow shown above, different optic components can be integrated on one single InGaAsP/InP substrate. A series of PICs have been fabricated at UCSB based on this platform and fabrication process [10,11,13,15–18,20,21], including the OPLL-based single-chip transmitter and receiver engines, which are going to be shown in the following sections.

3. Single-chip integrated transmitters

Using the integration technologies illustrated in Section 2, the concept of an OPLL-based, Hertz-accuracy, widely-tunable transmitter has been proven. The transmitter includes a heterodyne OPLL and a mode-locked laser chip. This can provide a terahertz chirped LIDAR

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transmitter that can potentially sweep over a more than 2.5 THz (even 5 THz, depending on the width of the comb source) range with Hertz level accuracy.

The architecture of the OPLL is shown in Fig. 3. It includes a PIC, an electronic IC (EIC) and a loop filter. All the photonics components are integrated on a single PIC, including a widely-tunable sampled-grating DBR (SG-DBR) laser, an optical 90 degree hybrid, four quantum well photodetectors, and microstrip transmission lines. Conducting substrate is chosen, and QWI is used to define the active and passive area. The process flow is as discussed in Section 2. Both surface and deeply etched waveguides are defined on the same device. The picture of the PIC is shown in Fig. 4(a) and the cross sections are shown in Fig. 4(b).

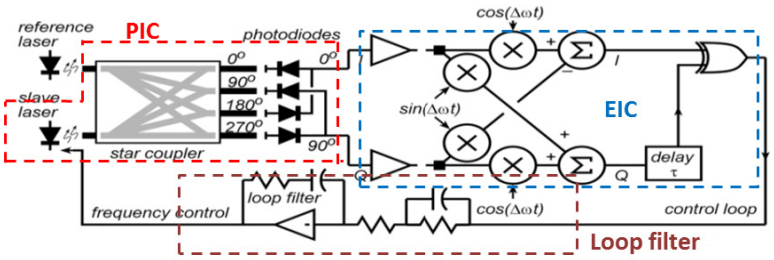

Fig. 3. The architecture of the heterodyne OPLL.

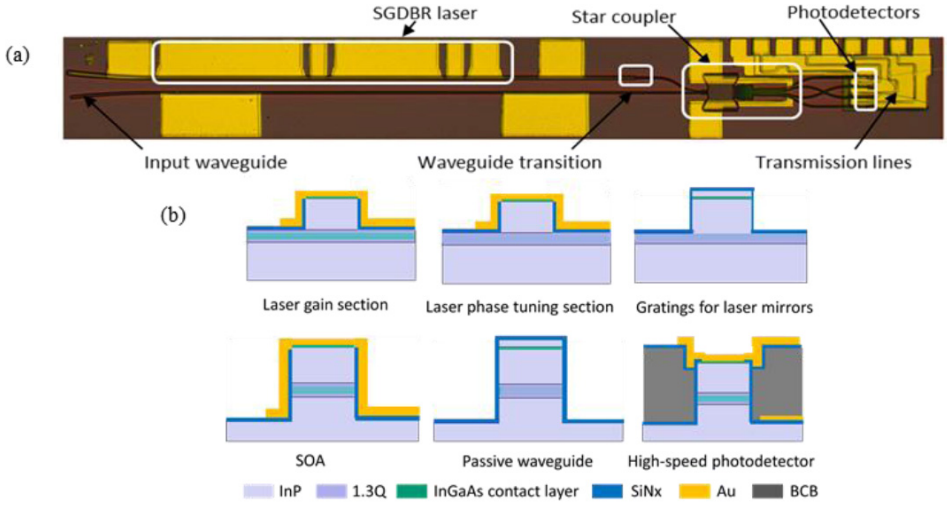

Fig. 4. Shows a picture of the fabricated PIC and the cross sections of the integrated components.

The PIC, EIC and loop filter are connected together using wirebonding. A reference laser is coupled into the PIC using lensed fiber and mixed with the on-PIC SG-DBR laser in the 90 degree hybrid. I/Q signals are then generated and detected in the four photodetectors, and feedback to the SG-DBR laser phase tuning section through the EIC and the loop filter. On the EIC, limiting amplifiers, a single-sideband mixer (SSBM) and a quadricorrelator phase/frequency detector are integrated. The details of the EIC can be found in Ref [22]. Because all the photonics components are integrated within a footprint of millimeter scale, the delay in the photonics part is only 40 ps, and total loop delay is around 200ps, which is mainly from the EIC and the interconnections. The size of the whole OPLL system is 10 mm × 10 mm. The picture of this heterodyne OPLL is shown in Fig. 5.

First, in order to verify that the OPLL system is working, we used a commercial external cavity continuous-wave laser as the reference laser. By applying different RF frequency

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references, the SG-DBR laser can phase lock to the reference laser with different frequency offsets. The phase/frequency detector enables the OPLL to function not only as a phase lock system, but also as a frequency locking system. This means that the phase/frequency of the SG-DBR laser will be stably lock to the reference, even if the SG-DBR laser free-running frequency drifts out of the phase locking bandwidth. The single-sideband mixer enables the OPLL to phase lock at either a positive or a negative frequency offset between SG-DBR and the reference laser. The sign of the offset frequency is set by a control signal to the EIC. The test setup is shown in Fig. 5.

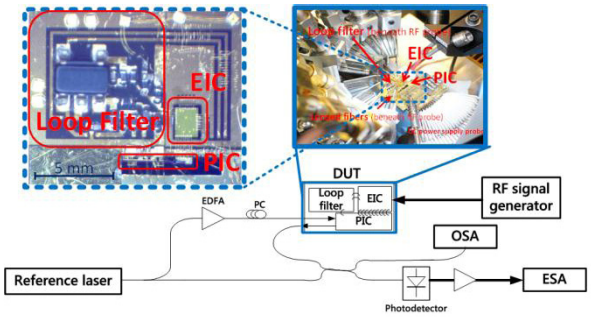

Fig. 5. The schematics of the OPLL test setup is shown in the lower part of this figure. Thinner lines indicate fiber connections and thicker lines show the RF cable connections. Pictures of the OPLL are also shown.

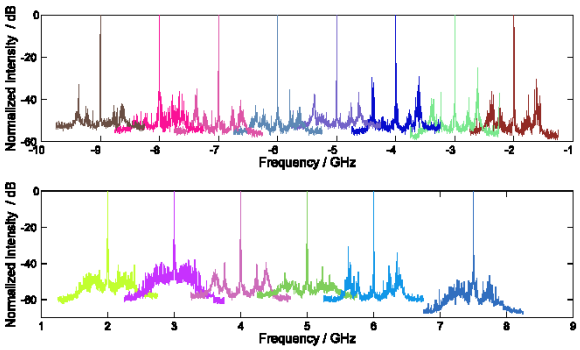

Fig. 6. Shows the beating tones of the two lasers when they are phase locked at various frequency offsets: –9 GHz, –8 GHz, –7 GHz, –6 GHz, –5 GHz, –4 GHz, –3 GHz, –2 GHz, 2 GHz, 3 GHz, 4 GHz, 5 GHz, 6 GHz, and 7.5 GHz.

Offset locking has been achieved with an offset frequency from –9 GHz to –1.5 GHz and from + 1.5 GHz to + 7.5 GHz, and the locking spectra are shown in Fig. 6. The phase error variance is 0.03 rad^2, integrated from 100 Hz to 10 GHz. The closed-loop bandwidth of the OPLL is around 400 MHz. Approximately 10 GHz pull-in range and > 15 GHz hold-in range has been achieved.

Besides the heterodyne OPLL, another important building block of this LIDAR transmitter engine is an InGaAsP/InP mode-locked laser [21]. An SEM of the mode-locked laser is shown in Fig. 7(a). The offset quantum well integration platform is used with deeply etched waveguides. A similar MLL has shown more than 2.5 THz comb width, while here a relative narrow comb is used on purpose for the demonstration of phase locking a CW laser to a MLL. The beating spectrum of two lasers is shown in Fig. 7(b). The SG-DBR in the OPLL system is phase locked to one of the comb lines of the MLL with a frequency offset of 6.5 GHz. A strong beating tone is observed at 6.5 GHz, as well as two tones at 11.69 and 24.69 GHz (i.e. 18.19 ± 6.5 GHz), corresponding to the adjacent comb lines of the MLL. The MLL

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repetition rate is 18.19 GHz. 13 GHz peak is the harmonic of the 6.5 GHz offset frequency. The narrow beat observed indicates the high coherence between the MLL and the comb. The MLL linewidth is 100 MHz, whereas the linewidth of the 6.5 GHz beat term is < 800 kHz.

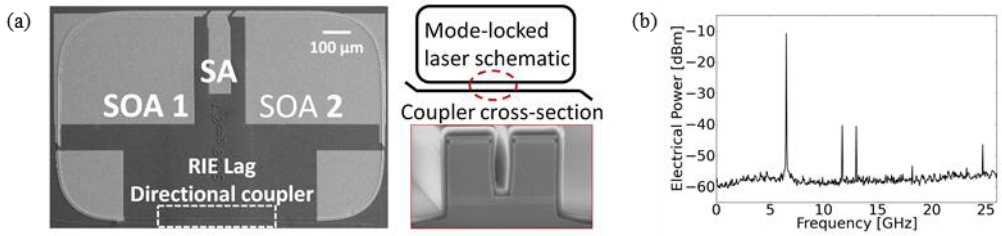

Fig. 7. (a) shows SEM pictures of the MLL and its cross section as well as the schematic. (b) Frequency spectrum of SG-DBR beating with the MLL measured on an electrical spectrum analyzer (RBW 50 kHz). The offset locking frequency is 6.5 GHz.

The offset frequency between MLL and SG-DBR laser is set by the RF reference. By changing the RF frequency, the frequency of the SG-DBR laser can be swept from one comb line to the adjacent one, and then offset lock to this line. This can be continued through all the comb lines, and a quasi-continuous frequency sweeping could be achieved, with the sweeping range as large as the width of the comb [20]. The bandwidth of the RF synthesizer, EICs and photodetectors only needs to be as large as the spacing between the MLL lines.

Furthermore, since the PIC in the OPLL system and the MLL share a similar integration platform and almost the same fabrication process, monolithically integrating these two PICs is viable.

4. Single-chip integrated receivers

With the exponential increase of internet data stream, a lot of effort has been devoted to the research of coherent receivers, while most are focused on DSP based intradyne receivers. Compared to other types of receivers, homodyne receivers have a high sensitivity, and no DSP is needed for short or mid-distance communication, where dispersion is not severe. Most of the research on the homodyne receivers was carried out in 1980s before the invention of EDFA, while the loops proved hard to stabilize. One of the major problem that researcher were facing was, again, the loop bandwidth, which is limited by the loop delay. Expensive external cavity lasers were commonly used as the LO laser because of the high requirement on the linewidth and stability introduced by the limited loop bandwidth.

By integration, we successfully achieved a homodyne coherent receiver within a footprint of 10 mm × 10 mm [17,18]. The total loop delay is only 120 ps. The design is based on optical Costas loop, and the architecture is shown in Fig. 8. Compared to the heterodyne OPLL architecture shown in Fig. 8, there is no SSBM in this EIC, and loop filter parameters are different. The receiver system also includes a PIC, an EIC and a loop filter.

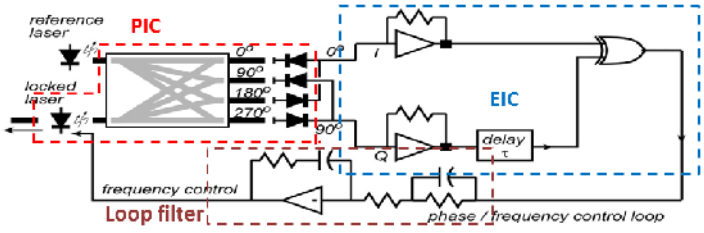

Fig. 8. The architecture of the homodyne coherent receiver.

The functionality of this PIC is the same as the one used in the heterodyne receiver, while the performance is improved. Uni-travelling-carrier (UTC) photodetectors are integrated, and

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30 GHz 3-dB bandwidth and 18 mA saturation current are achieved. As for the processing, UTC layers need to be regrown and UTC photodetectors need to be defined after the QWI. The rest of the process steps remain the same. In order to reduce the reflection in the PIC and avoid injection locking, the whole device is based on surface ridge waveguide structure. The picture of the PIC and the cross sections are shown in Fig. 9(a)(b).

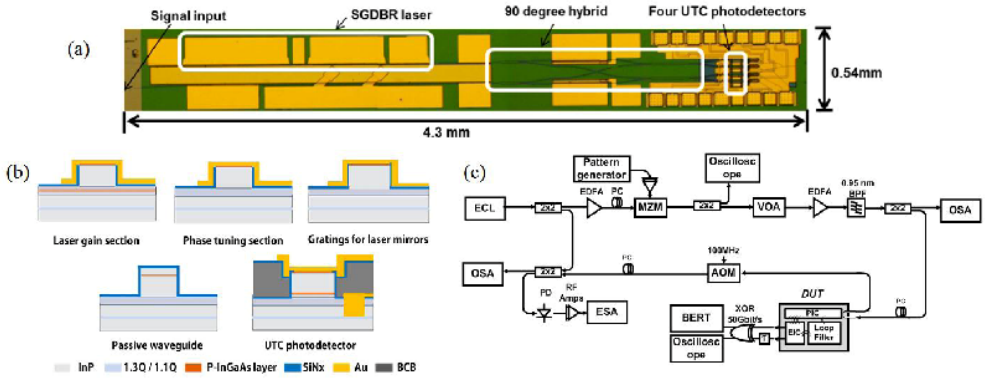

Fig. 9. (a) shows the microscope picture of the fabricated PIC. (b) shows the cross sections of the integrated components on this PIC. (c) The setup for the coherent receiver testing.

The test setup is shown in Fig. 9(c). 1.1 GHz closed-loop bandwidth has been realized. The test results show that the OPLL is very stable, and 40 Gb/s BPSK signal has been demodulated successfully. Bit error rates with different input OSNRs are plotted in Fig. 10, and the eye diagrams are also shown.

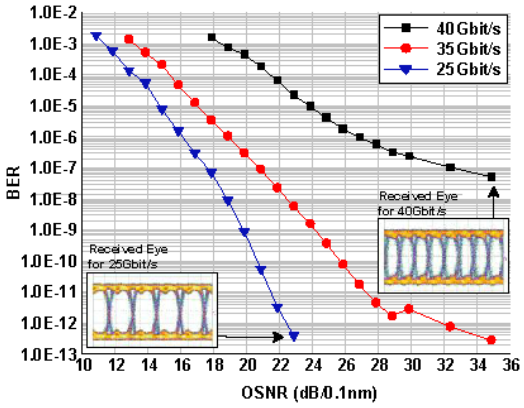

Fig. 10. BER vs. OSNR for 25G to 40Gb/s and received eye outputs for 25Gb/s and 40Gb/s.

5. Conclusions

In this paper, we overview the advantage of optical integration, and two examples of optical phase-locked loops are illustrated. Not only can photonic integration replace and improve the existing optic systems, it also has an important role of creating new optical systems that are difficult or even impossible to be realized using free-space optics or fiber-pigtailed components, especially in the area of coherent optics. The OPLL-based widely-tunable transmitter and homodyne receiver are feasible to build and operate due to photonic integration.

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