A 50 Gbps 9.5 pJ/bit VCSEL-based Optical Link

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***Abstract*—We present an 850 nm VCSEL-based NRZ optical link operating at 50 Gbps. The full link uses no external equalization and has a power efficiency of 9.5 pJ/bit.**

Keywords—VCSEL, optical link, transmitter, receiver

I. Introduction

There is increasing demand for high speed, low cost, and power efficient optical links to meet the demand created by data center network traffic growth. There have been demonstrations of non-return-to-zero (NRZ) VCSEL links operating at speeds up to 71 Gbps with bit error rate (BER) < 10^{-12} [1]. VCSEL links have also been demonstrated with low power consumption of 1 pJ/bit at 25 Gbps and 2.7 pJ/bit at 35 Gbps [2]. Operation at 56 Gbps below the 7% forward error correction (FEC) BER level was shown with an efficiency of 4.5 pJ/bit [3]. We report here a full 50 Gbps NRZ VCSEL link with BER of 1.7×10^{-4} and power efficiency of 9.5 pJ/bit.

II. Design

The transmitter (Tx) and receiver (Rx) assemblies for this link use the transimpedance amplifier (TIA) design described and characterized in earlier work [4]. The TIA was found to provide sufficient current to drive the VCSEL. Since the VCSEL driver has significantly more gain than is typical, an input signal of just 65 mVppd is sufficient to drive the link. While this additional gain in the Tx contributes to higher full-link power consumption, the reduced input swing reduces power consumption in the SERDES electronics. An array of NVIDIA VCSELs was copackaged with the driver chip on a custom PCB to form the Tx assembly, shown in Fig. 1(a). The NVIDIA VCSELs are 28 Gbaud NRZ or PAM4 compatible laser array consisting of four 850 nm GaAs/InGaAs QW VCSELs with 25 GHz BW, shown in Fig. 1(c). VCSEL anodes were wirebonded to the differential driver outputs, and cathodes were connected to independent supplies. The VCSEL used for data transmission was biased at 7.5 mA, and the unused VCSEL was turned off for power savings. The driver has a continuous time linear equalizer (CTLE) on the output stage to extend the link bandwidth. The total Tx power consumption was 268 mW. The Rx assembly consists of a 12 µm photodiode (Albis 40C1-TW2) copackaged with the Rx TIA on a separate custom PCB, shown in Fig. 1(b). The unused input of the differential TIA was left unconnected. The total Rx power consumption was 207 mW.

III. Experimental Results

For link characterization, a bit pattern generator (SHF 12105A) generates a PRBS31 pattern, which drives the Tx IC and VCSEL. Lensed multimode fiber is coupled to the VCSEL on the Tx assembly and the photodiode on the Rx assembly. The Rx TIA output is then either connected to a sampling oscilloscope (Tektronix DSA8300) with 70 GHz sampling module (Tektronix 80E11) for eye diagram measurements, or to a bit error rate tester (SHF 11104A) for BER measurements. An optical eye of a 50 Gbps waveform at the Tx output is shown in Fig. 2(a) and was measured with a reference receiver (Picometrix DG-32xr) with 28 GHz bandwidth, which is contributing to significant eye closure. Electrical eye diagrams at the Rx output for full-link operation up to 50 Gbps are shown in Fig. 2(b), (c), and (d). The measured full-link BER vs. average optical power (assuming infinite extinction ratio) at the receiver is shown in Fig. 2(e), and the corresponding BER bathtub curves measured at maximum optical modulation amplitude (OMA) are shown in Fig. 2(f). As there is no indication of a BER floor at these datarates, the achieved BER of 1.7×10-4 at 50 Gbps is limited by the achievable OMA, the full link BER can be expected to improve commensurately with increased Tx output OMA or coupling efficiency.

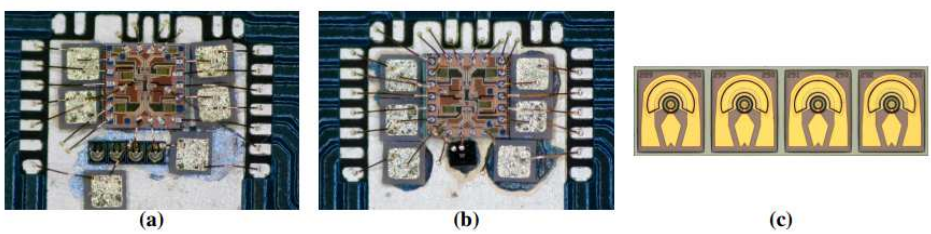

Fig. 1. The assembled transmitter (a) and receiver (b). The NVIDIA VCSEL array (c).

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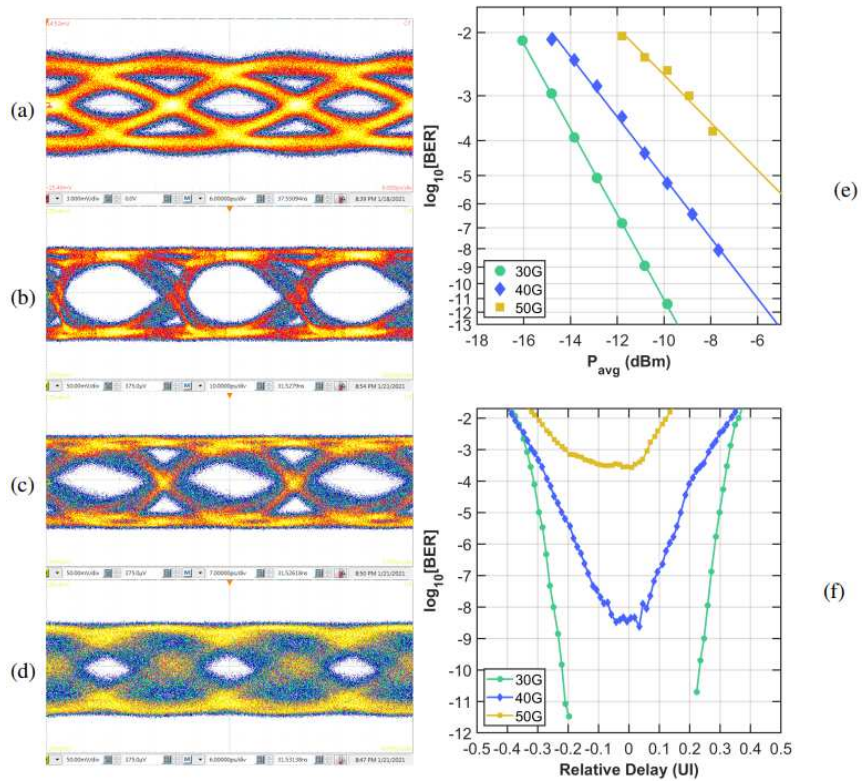

Fig. 2. The optical eye diagram at the Tx output at 50 Gbps (a) with a scale of 3 mV/div. Electrical eye diagrams at the Rx output showing full-link operation at 30 (b), 40 (c), and 50 (d) Gbps, with scales of 50 mV/div. Full-link BER vs. average optical power received (assuming infinite extinction ratio) at various datarates (e). Measured full-link BER bathtub curves at various datarates (f).

Table 1. State-of-the-art comparison.

Reference	[1]	[2]		[3]	This Work
Technology	130 nm SiGe	32 nm SOI CMOS		130 nm SiGe	130 nm SiGe
DR (Gbps)	71	25	35	56	50
Energy Efficiency (pJ/bit)	25.5	1.0	2.7	4.5	9.5
Equalization	2-Tap FFE	No Eq.		No Eq.	CTLE
BER	10^{-12}	10^{-12}		5×10^{-4}	1.7×10^{-4}
Driver Input Swing (Vppd)	800	200		650	65

IV. Conclusion

We have demonstrated a full VCSEL link operating at 50 Gbps with a BER of 1.7×10^{-4} and power efficiency of 9.5 pJ/bit. A comparison of this result with state-of-the-art VCSEL-based full link demonstrations is shown in Table 1. Notably, this link operates with only 65 mVppd driver input swing, a significant improvement over the state-of-the-art.

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References

[1] D. M. Kuchta et al., “A 71-Gb/s NRZ Modulated 850-nm VCSEL-Based Optical Link,” IEEE Photonics Technology Letters, vol. 27, no. 6, pp. 577–580, Mar. 2015.

[2] J. E. Proesel et al., “35-Gb/s VCSEL-Based Optical Link using 32-nm SOI CMOS Circuits,” in Optical Fiber Communication Conference/National Fiber Optic Engineers Conference 2013 (2013), paper OM2H.2, Mar. 2013, p. OM2H.2.

[3] N. Ledentsov Jr. et al., "Energy efficient 850-nm VCSEL based optical transmitter and receiver link capable of 56 Gbit/s NRZ operation," Proc. SPIE 10938, Vertical-Cavity Surface-Emitting Lasers XXIII, 109380J (1 March 2019).

[4] L. A. Valenzuela et al., "A 108-Gbps, 162-mW Cherry-Hooper Transimpedance Amplifier," in 2020 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS), Monterey, CA, USA, 2020, pp. 1-4.