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Evolution of Chip-Scale Heterodyne Optical Phase-Locked Loops towards Watt Level Power Consumption

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***Abstract*—We design and experimentally demonstrate two chip-scale and agile heterodyne optical phase-locked loops (OPLLs) based on two types of InP-based photonic integrated coherent receiver circuits. The system performance of the first generation OPLL was improved in terms of offset-locking range, and power consumption with the use of a power-efficient and compact photonic integrated circuit (PIC). The second generation PIC consists of a 60 nm widely-tunable Y-branch laser as a local oscillator with a 2×2 MMI coupler and a pair of balanced photodetectors. This PIC consumes only 184 mW power in full operation, which is a factor of 3 less compared to the first generation PIC. In addition, the sensitivity of these OPLLs was experimentally measured to be as low as 20 μw. A possible solution to increase the sensitivity of these OPLLs is also suggested.**

***Index Terms*—Photonic integrated circuits, optical phase-locked loop, heterodyne, integrated optics**

I. Introduction

Optical phase-locked loops (OPLLs) have been of great interest for the last couple of decades due to the promising applications in the areas of communications, sensing and frequency control [1, 2]. These applications include short to medium range coherent optical communications [3], laser linewidth narrowing [4-6], terahertz signal generation [6, 7] and optical frequency synthesis [8-11]. With the improvements in the photonic integration, OPLLs became more attractive since they can offer small loop delay, which allows having OPLLs with loop bandwidths as large as 1.1 GHz [3]. However, these prior OPLLs consume almost 3 Watts of electrical power [3]. This high-power consumption makes the use of OPLLs in practical applications questionable.

Manuscript received July 1, 2017; revised August 23, 2017; accepted September 25, 2017. This work was supported by DARPA-MTO under the DODOS Project, and National Science Foundation under Grant No. 1402935.

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Therefore, realizing a low-power consumption OPLL is important to take advantage of recent advances in photonic integration. A chip-scale, compact, low power consumption OPLL can push the technology in the aforementioned application areas further forward. With the proper design of compact photonic integrated circuits (PICs), power consumption in such PICs, therefore OPLLs, can be lowered [12]. In this work, two chip-scale, highly-integrated OPLLs are designed and experimentally demonstrated using two different InP-based photonic integrated coherent receiver circuits.

After successfully achieving OPLLs with reasonable offset locking range and power consumption, a detailed sensitivity analysis and some relevant experiments were performed. A minimum input optical power to demonstrate the phase-locking using our OPLLs was measured as 20 μw both theoretically and experimentally. A novel solution is proposed that can be implemented in such OPLLs in order to lock input power levels as low as nanowatts.

This paper is organized as follows. This paper begins with a short summary of OPLL system design together with the PIC design. We then present the experimental results for the first, and second generation OPLL. After this, the power budget for both OPLLs is given. Finally, the sensitivity analysis and a proposed solution for high sensitivity OPLL is provided.

II. Optical Phase-Locked Loop System Design

A. PIC Design

Since two different types of PICs are used in this study for demonstrating heterodyne OPLLs, we have named them as gen-1 and gen-2 PICs for clarity. All active/passive components in these PICs are monolithically integrated on an InGaAsP/InP material platform. Details of the fabrication of such PICs can be found in [13, 14]. Microscope images of both PICs are shown in Fig. 1(a) and (b).

Out of two PICs, gen-1 PIC (see Fig. 1(a)) consists of 40 nm widely-tunable sampled-grating distributed-Bragg-reflector (SG-DBR) laser, 2×2 MMI coupler, a balanced photodetector pair and a couple of semiconductor optical amplifiers (SOAs) on reference and local-oscillator (LO) optical paths. Reference optical signal was coupled into this PIC using the upper arm and amplified by two SOAs. SG-

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DBR laser output propagated in the lower arm. These two optical signals were combined in a 2×2 MMI coupler and mixed in a balanced photodetector pair to produce the beat note for the electronics part. The SG-DBR laser also has a second output from its backside for monitoring purposes.

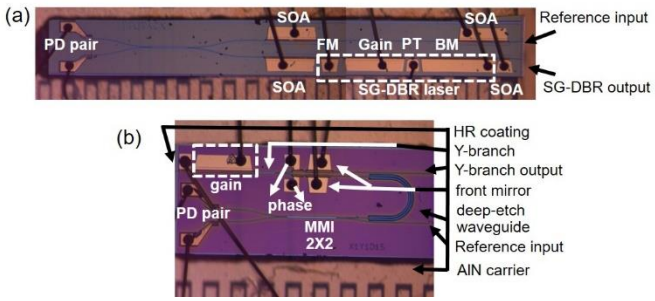

Fig. 1. (a) Microscope image of the gen-1 InP based PIC. (b) Microscope image of low power consumption gen-2 InP based PIC. (BM: back mirror, FM: front mirror, PD: photodiode, PT: phase tuner, SG-DBR: sampled-grating distributed-Bragg-reflector, and SOA: semiconductor optical amplifier)

Gen-2 PIC (see Fig. 1(b)) was designed for low power consumption. This PIC incorporates a widely tunable, compact Y-branch laser, formed between a high-reflectivity coated back cleaved mirror and a pair of Vernier tuned sampled-grating front mirrors, as well as a 2×2 MMI coupler and a balanced photodetector pair. The optical output from one of the front mirrors was connected to the MMI coupler, while the other output from another front mirror was used externally for monitoring the OPLL operation. The Y-branch laser has a compact cavity with short gain and mirror sections, requiring low current and therefore low drive power. It is tuned via Vernier effect and has been designed for high efficiency at 30º C. The measured tuning range exceeds 60 nm with >50 dB side-mode suppression ratio [15].

B. Feedback Electronics Design and OPLL Assembly

Both OPLLs use SiGe-based commercial-off-the-shelf (COTS) electronic ICs and loop filters built from discrete components as the control electronics. Figure 2 shows an exemplary OPLL system assembled by mounting gen-1 PIC and electronic components on a patterned AlN carrier.

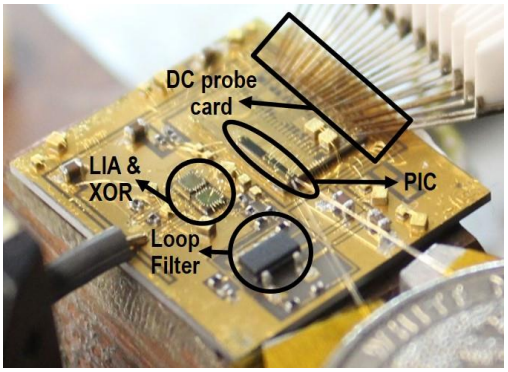

Fig. 2. OPLL system under measurement setup integrated on an AlN carrier including gen-1 PIC and control electronics

In this study, both OPLLs are designed to be heterodyne-type, which takes input offset frequency from external RF synthesizer and locks LO laser to the reference oscillator at this offset frequency. The second order loop filter with fast feedforward path was used in feedback electronics in order to get a high loop bandwidth. The circuit schematics of both OPLL systems can be seen in Fig. 3(a) and (b).

A limiting amplifier with 30 dB differential gain and 17 GHz 3-dB bandwidth, and a digital XOR gate functioning as a phase detector [16], together with an op-amp-based loop filter were used in the feedback electronics. The on-chip LO laser of the PIC was mixed via the external reference laser through the 2×2 MMI coupler and the PD pair to produce the beat note. This beat note then feeds the electronic ICs. First, it is amplified to logic levels through limiting amplifier and then mixed via external RF frequency synthesizer in order to produce an error signal. This error signal goes through the loop filter and feeds back to the phase-tuning section (PT) of on-chip LO laser. With sufficient feedback gain, this error signal becomes zero and LO laser is locked to external reference laser at given RF offset frequency.

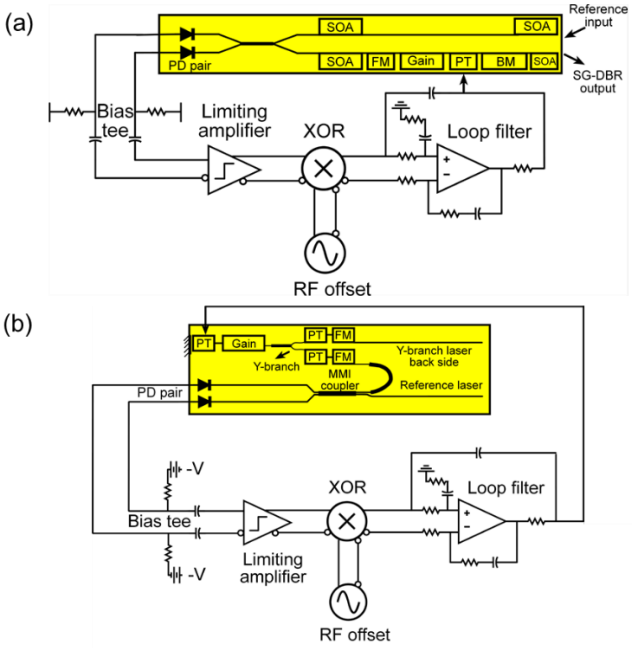

Fig. 3. (a) Circuit diagram of the first generation OPLL including gen-1 PIC in yellow and the control electronics. (b) Circuit diagram of the second generation OPLL including gen-2 PIC in yellow, and the control electronics. (BM: back mirror, FM: front mirror, PD: photodiode, PT: phase tuner, SG-DBR: sampled-grating distributed-Bragg-reflector, SOA: semiconductor optical amplifier)

Open loop transfer function of an OPLL can be written as a product of gain, and the time constants of the loop [17]. Therefore, open loop transfer function of both OPLLs in this work can be expressed as follows:

$$T(s) = K_{\mathrm{PD}} K_{\mathrm{CCO}} \frac{1}{(\tau_{\mathrm{laser}} s + 1)} e^{-\tau_{\mathrm{d}} s} \times \times \left(\frac{\tau_2 s + 1}{\tau_1 s} \frac{1/R_{out}}{\tau_{\mathrm{op}} s + 1} e^{-\tau_{\mathrm{dop}} s} + \frac{C_{\mathrm{FF}}}{2} \right)$$

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where K_{PD} is the phase detection gain, K_{CCO} is the laser tuning sensitivity, τ_{laser} is the laser tuning frequency responsivity, τ_1 is the loop filter pole, τ_2 is the loop filter zero, τ_{OP} is the op-amp parasitic pole, R_{out} is the voltage to current conversion resistance at the output, C_{FF} is the feed-forward capacitor and τ_{dop} is the op-amp delay, and τ_d is the total loop delay. Here K_{PD} is a constant value $\left(2*V_{logic}/\pi\right)$ due to the limiting amplifier, which makes the system loop bandwidth insensitive to the optical power level variations. This loop was designed to have a safe phase margin of around 50-60° at unity gain crossover frequency for both OPLLs in order to realize a robust and stable system.

III. First Generation OPLL Experimental Results

The experimental setup, as shown in Fig. 4, was used in order to demonstrate the offset locking with the OPLL using the gen-1 PIC. The reference external cavity laser (ECL) was coupled into the PIC using lensed fiber from the back side of the PIC. It was then combined with the tunable on-chip SG-DBR laser output in the MMI coupler and mixed to form the desired beat note in the PDs. Light from the SG-DBR laser was coupled out from the lower arm for monitoring purposes. The superimposed optical spectra of the reference laser together with on chip SG-DBR laser were measured by an optical spectrum analyzer (OSA). At the same time, the resulting RF beat-note was measured by an electrical spectrum analyzer (ESA) through a high speed photodiode.

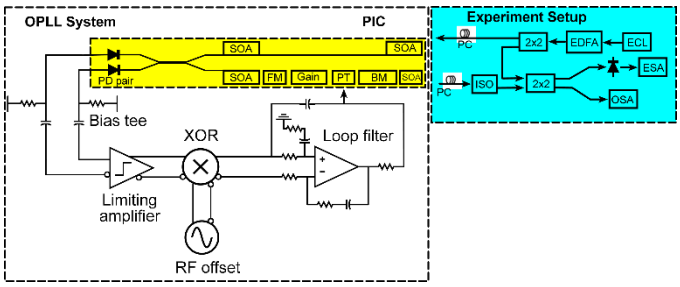

Fig. 4. (a) Experimental setup for the first generation OPLL system. (ECL: external cavity laser, ESA: electrical spectrum analyzer, OSA: optical spectrum analyzer, PC: polarization controller, ISO: isolator)

This experiment shows offset-phase locking between the on chip SG-DBR laser and the external cavity laser (ECL) as the reference. ECL used in this study has the optical linewidth of 100 kHz. Figure 5(a) demonstrates the optical spectrum when the reference laser and the on chip SG-DBR are offset locked at 6 GHz, which is determined by the RF frequency synthesizer. As can be seen in the figure, the separation between the two peaks are about 0.05 nm, which corresponds to 6 GHz frequency separation. In Fig. 5(b), the RF beat-note of the reference laser and the on chip SG-DBR laser is presented both in locked and unlocked cases. The relative linewidth of the locked beat note at 6 GHz is in the order of sub-Hz, which is limited by the resolution bandwidth of the ESA. It should be noted that the optical linewidth of our free-running on-chip laser is 10 MHz.

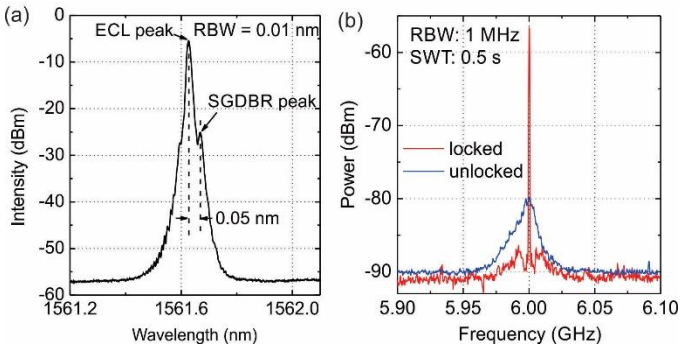

Fig. 5. (a) OSA spectrum when SGDBR is offset locked to the reference laser at 6 GHz offset, which corresponds 0.05 nm separation in optical domain. (b) Corresponding ESA spectrum when SGDBR is offset locked to the reference laser at 6 GHz offset, blue is before locking and red is after locking.

In order to measure the absolute linewidth of the locked beat note, the measurement was performed after adding 20 km of fiber between the upper and lower external 2x2 couplers to de-correlate the ECL from the SG-DBR. In this case, one would expect to get a linewidth of the RF beat note equal to the optical linewidth of the ECL. Figure 6 demonstrates this result. On chip SG-DBR is offset locked at 4.4 GHz, but this time long fiber is added to de-correlate the ECL from the SG-DBR. In this case, the absolute linewidth of the locked beat tone was measured as 100 kHz, indicating the linewidth cloning of the SG-DBR to the ECL.

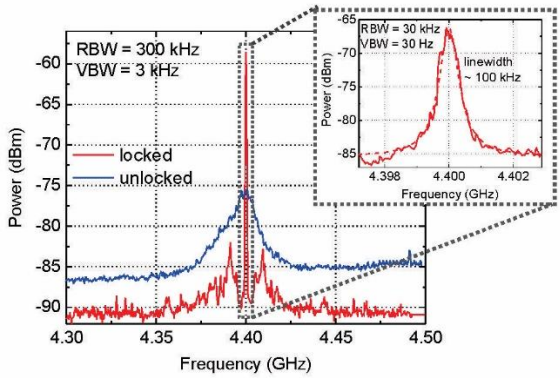

Fig. 6. (a) ESA spectrum when SG-DBR is offset locked to the reference laser at 4.4 GHz offset. In this case, ECL and SG-DBR are de-correlated using a long fiber. Therefore, relative linewidth of the beat note is equal to 100 kHz, which is the linewidth of the ECL (reference laser).

After proving the phase locking, the offset-locking range was demonstrated for different offset frequencies from 1.14 GHz up to 15.2 GHz as can be seen in Fig. 7. The higher the offset locking range, the easier it became for the OPLL to track the reference signal over a broad range of frequencies [18, 19].

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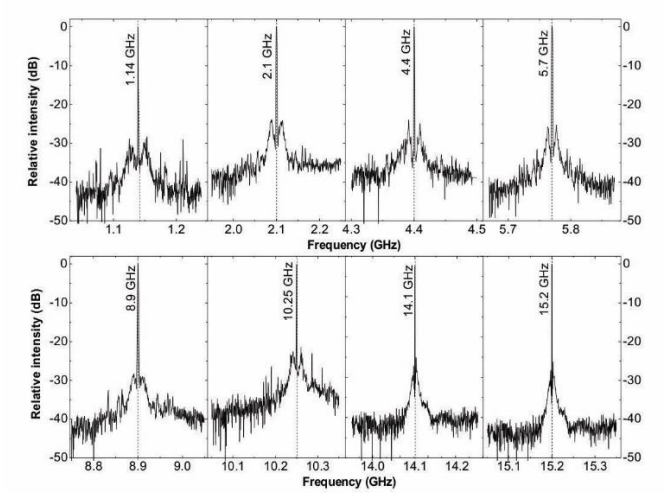

Fig. 7. (a) Offset locking at multiple frequencies with the first generation OPLL at a RBW of 3 MHz

IV. SECOND GENERATION OPLL EXPERIMENTAL RESULTS

Similar to the first generation OPLL, the experimental setup shown in Fig. 4 was used to demonstrate phase locking for the second generation OPLL. In this case, gen-1 PIC was replaced with the gen-2 PIC.

This experiment demonstrates phase locking between the on-chip Y-branch laser and the reference laser. Fig. 8(a) shows the optical spectrum when the reference laser and the on chip Y-branch laser are offset locked at 8.6 GHz, which is determined by the RF frequency synthesizer. As can be seen in the figure, the separation between the two peaks are about 0.07 nm, which corresponds to 8.6 GHz frequency separation. In Fig. 8(b), the RF beat-note between the reference laser and the on chip Y-branch laser is displayed both before the locking and after the locking. The relative linewidth of the locked beat note at 8.6 GHz is in the order of sub-Hz, which is limited by the resolution bandwidth of the ESA. The beat note has a relative linewidth in the order of a MHz before the locking, which is the unlocked Y-branch laser's linewidth [12].

With similar arguments presented for the first generation OPLL, one can add a long enough fiber at the output between the upper and lower external 2×2 couplers to de-correlate the ECL from the Y-branch laser and measure the actual linewidth of the beat note, which is equal to the linewidth of the ECL ~ 100 kHz.

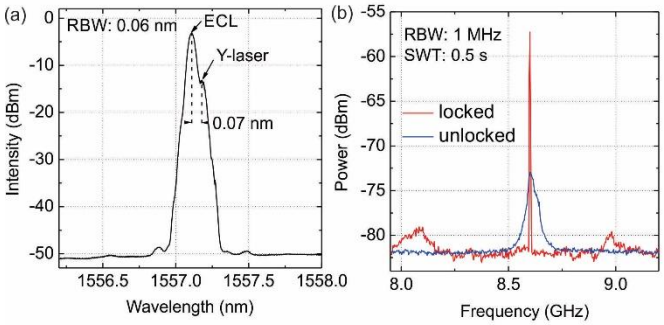

Fig. 8. (a) OSA spectrum when on chip Y-branch laser is offset locked to the reference laser at 8.6 GHz offset, which corresponds 0.07 nm separation in optical domain. (b) Corresponding ESA spectrum when Y-branch laser is offset locked to the reference laser at 8.6 GHz offset.

As the next experiment, several offset frequencies from 1 GHz to 20 GHz were applied from the RF frequency synthesizer, and the same phase locking experiment was performed. Figure 9 presents offset locking at several offset frequencies ranging from 1.6 GHz to 17.8 GHz.

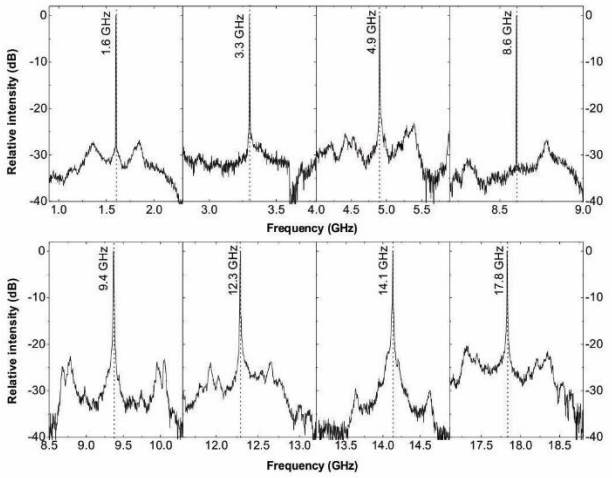

Fig. 9. Offset locking at multiple frequencies with the second generation OPLL at a RBW of 3 MHz

In addition to the phase locking experiments, the residual phase noise spectral density of the OPLL system was measured when on chip local oscillator is offset locked to the reference laser. Since the loop parameters and order were not changed from the OPLL with gen-1 PIC to the gen-2 based OPLL, we only provide phase noise spectrum of the former one. Figure 10 shows phase noise spectrum when on chip SG-DBR laser is offset locked to reference ECL at 2.5 GHz. This figure also demonstrates the ESA background and RF synthesizer phase noise spectrum at 2.5 GHz. The phase noise variance is calculated to be 0.067 rad^2 from 1 kHz to 10 GHz offset interval. This corresponds to 14.8° standard deviation from the locking point. This OPLL achieves -100 dBc/Hz phase noise at offset of 5 kHz. These results are comparable with the state of the art results in [20, 21].

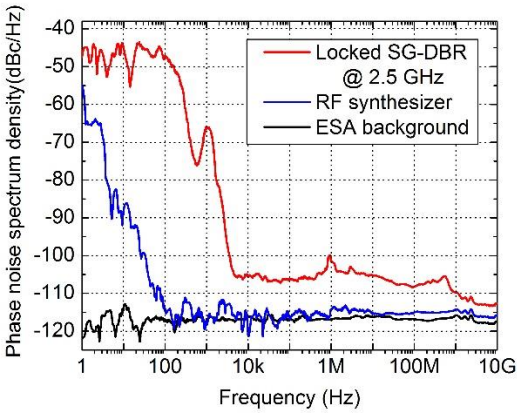

Fig. 10. Single-sideband residual phase noise of the heterodyne OPLL at 2.5 GHz offset locking. Phase noise results of the RF synthesizer at 2.5 GHz, and background is also shown here.

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For our OPLL system, the time domain equivalent of the phase error variance is equal to the timing jitter in the frequency range from 1 kHz to 10 GHz [22], which can be calculated as:

$$\text{Jitter} = \frac{\sqrt{0.067}}{2\pi \times 2.5\times 10^{9}} = 16.48\text{ps}$$

This study is a proof-of-principle demonstration of optical phase locking to a reference laser with low power consumption. This system can be integrated with a better reference sources such as microresonator based optical frequency combs to synthesize arbitrary pure optical frequencies [10, 15]. Also, such narrow RF beat tones generated by beating on-chip laser with the comb lines can be used in wide range of applications, including short to medium range optical communications, as well as broadband wireless communication in microwave photonic link technology.

V. Power budget of both OPLLs

As mentioned, one of the primary objectives for this work was to realize a compact, chip-scale OPLL with Watt-level power consumption. In order to do this, one can improve the control electronics, PIC or both. In this work we proposed a novel, compact, low power consumption PIC as a possible solution to realize a chip scale, a Watt level OPLL. Table 1 and 2 provides the power consumption of gen-1 PIC, gen-2 PIC, control electronics and overall OPLL systems. (Numbers in the parentheses for each section in the PIC part tell how many of them are integrated in the PIC, BM: back mirror, FM: front mirror, LIA: limiting amplifier, PD: photodiode, PT: phase tuner, SOA: semiconductor optical amplifier)

TABLE I
Power budget for first generation PIC Providing 10 mW Optical Power and overall OPLL system

	Section	Current (mA)	Voltage (V)	Power (mW)
Gen-1 PIC	Gain(1)	73	1.5	109.5
	FM (1)	30	1.5	45
	PT (1)	7	1.3	9.1
	PD (2)	1	2	4
	BM (1)	120	1.5	180
	SOA (3)	70	1.5	315
PIC-1 TOTAL				**662.6**
	LIA	180	3.3	594
	XOR	130	3.3	429
	Op-amp	16	6	96
Electronic ICs TOTAL				**1119**
Total Power Consumption Gen-1 OPLL				**1.78 (W)**

TABLE II
Power budget for second generation PIC Providing 10 mW Optical Power and overall OPLL system

	Section	Current (mA)	Voltage (V)	Power (mW)
Gen-2 PIC	Gain(1)	73	1.5	109.5
	FM (2)	20	1.3	52
	PT (2)	7	1.3	18.2
	PD (2)	1	2	4
PIC-2 TOTAL				**184**
	LIA	180	3.3	594
	XOR	130	3.3	429
	Op-amp	16	6	96
Electronic ICs TOTAL				**1119**
Total Power Consumption Gen-2 OPLL				**1.3 (W)**

As can be seen from these tables gen-1 PIC consumes 660 mW, whereas gen-2 PIC consumes only 184 mW. Together with the control electronics, the OPLL with gen-2 PIC only consumes record-low 1.3 Watts of electrical power.

IV. Sensitivity of the OPLL system

For practical applications including coherent optical communications and optical frequency synthesis, OPLLs should be able to lock to input reference power levels in the order of μWs or even 10s of nWs. In this section, sensitivity analysis of the OPLL is given and experimental sensitivity results are reported. In addition to these results, a novel high gain trans-impedance amplifier (TIA) is presented and possible OPLL is proposed using this TIA, which can lock to input power levels as low as 25 pW.

Both OPLLs in this work employs SiGe based COTS limiting amplifier, which has 30 dB differential gain. InP based PICs have on chip tunable lasers, which produces reasonable amount of optical power. This is mixed with the reference input power through 2×2 MMI coupler and the PDs. The detected electrical signal is then fed into the limiting amplifier having a 50 Ohms common mode logic interface. In this system, the minimum required input current level from the balanced PD pair can be found as follows, where $V_{INPUT,MIN}$ represents the minimum required voltage level just before the limiting amplifier and $I_{BEAT,MIN}$ represents the minimum required beat current produced by the photodiodes:

$$Gain_{LIA} = 30dB = 31.6$$

$$V_{INPUT,MIN} = \frac{300mV}{31.6} = 9.5mV$$

$$I_{BEAT,MIN} = \frac{9.5mV}{50} = 0.19mA$$

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From the above equations, we found out that the minimum input current level for offset locking with the designed OPLLs is around 0.19 mA. Given the responsivity of the on-chip PDs is around 1 A/W, the minimum input beat power is around 0.19 mW. If we use this in the coherent detection equation, we can get the minimum required input power level from the reference laser as follows, where I_{BEAT} represents the beat current produced by the PDs, I_{LO} is the current produced by LO laser and I_{INPUT} is the current produced by the reference laser.

$$I_{BEAT} = 2\sqrt{I_{LO} I_{INPUT}}$$

$$I_{INPUT,MIN} = \frac{I_{BEAT,MIN}^{\ 2}}{4I_{LO}}$$

$$I_{INPUT,MIN} = 9\mu A$$

Therefore, the minimum input power required to offset lock this OPLL is theoretically about 9 µW, which is close to the experimental results demonstrated in Fig. 11(b), in which the minimum input power level required to operate the OPLL system was found to be 20 µW.

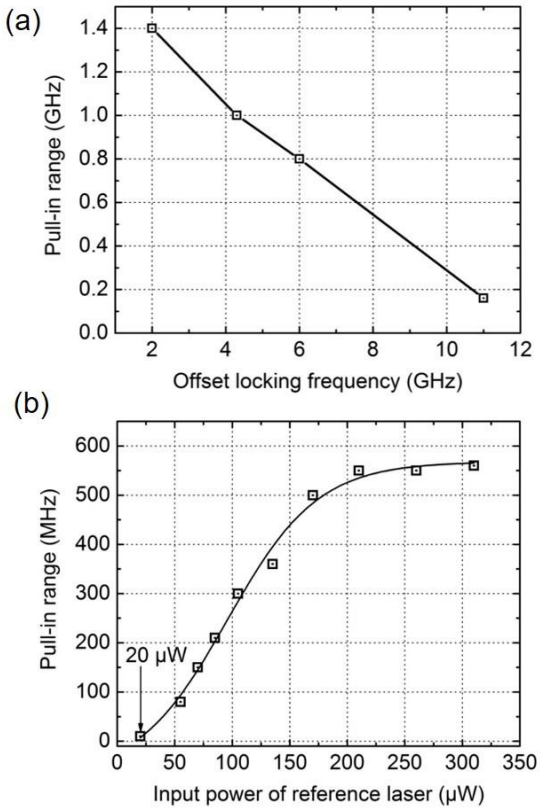

Fig. 11. (a) Pull-in range vs. offset locking frequency (b) Pull in range vs. input power of the reference external cavity laser. Minimum input power required for locking was found 20 µW experimentally.

Fig. 11(a) and (b) demonstrates the pull-in range of the OPLL system with respect to offset locking frequency and input power levels respectively. Pull-in range varies from 1.4 GHz to 200 MHz depending on the offset frequency range. As expected, the pull-in range decreases with increasing offset frequencies, since the gain of the overall loop reduces. Similarly, decreasing input power levels reduces the pull-in range, and eventually at some point OPLL stops working with the certain input power levels. This minimum input power level was found to be 20 µW, as can be seen in Fig. 11(b).

In order to improve the sensitivity of the OPLL further, an application specific trans-impedance amplifier (TIA) with low noise, high gain and wide bandwidth using 130 nm SiGe HBT process was designed. This chip was designed for 80 dB voltage gain and 120 dB ohm trans-impedance gain with 30GHz 3-dB bandwidth. It has less than 10 pA/$\sqrt{Hz}$ input referred noise current density up to 20 GHz with respect to 50 fF photodiode capacitance according to the circuit level simulations. With this TIA minimum input power level of reference signal can be reduced to as low as 22.5 pW as follows, where each symbol is used the same way as explained previously:

$$Gain_{TIA} = 120dB\Omega = 1M\Omega$$

$$I_{BEAT,MIN} = \frac{300mV}{10^6\Omega} = 0.3\mu A$$

$$I_{BEAT} = 2\sqrt{I_{LO} I_{INPUT}}$$

$$I_{INPUT,MIN} = \frac{I_{BEAT,MIN}^{\ 2}}{4I_{LO}}$$

$$I_{INPUT,MIN} = 22.5pA$$

Using this TIA, one can make a highly sensitive OPLL, which can be used in optical communications and optical frequency synthesis systems. Figure 12 shows the proposed OPLL system using this novel TIA. The COTS SiGe limiting amplifier is replaced by this TIA in the proposed OPLL system. Please note that TIA gain was measured functionally to be 60 dB without DC restoration loop. With a proper DC restoration loop, one can get the simulated gain of 80 dB from the TIA. The study relating to the sensitive OPLL system with these high-performance TIAs is ongoing and will be reported in the future.

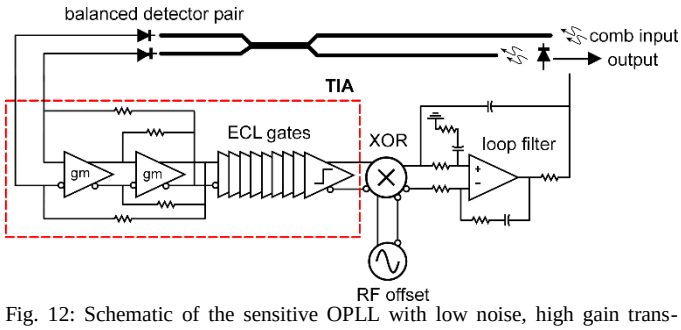

Fig. 12: Schematic of the sensitive OPLL with low noise, high gain trans-impedance amplifier.

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V. CONCLUSIONS

In this paper, two chip-scale OPLLs were designed and demonstrated. By designing a novel, low power consumption InP-based photonic integrated receiver circuit, overall power consumption of the first generation OPLL was significantly reduced. The second generation OPLL consumes only 1.35 Watts of electrical power, which is the lowest power consumption reported for an OPLL to the best of author's knowledge. Both OPLLs have 500 MHz loop bandwidth, with 0.067 rad^2 phase noise variance, integrating from 1 kHz to 10 GHz. Offset locking ranges are 15.2 GHz and 17.8 GHz respectively. Minimum input power level required from the reference side for phase locking was measured to be 20 µW. Novel, application specific electrical IC was proposed for lowering the sensitivity of such OPLLs to as low as 25 pW.

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