First Demonstration of an O-Band Coherent Link for Intra-Data Center Applications

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***Abstract*—We report the first demonstration of a full O-band coherent link for intra-data center applications, including custom photonic and electronic integrated circuits for the transmitter and receiver. Full-link 112 Gbps (56 Gbaud QPSK) transmission is shown with $2.1 \cdot 10^{-4}$ measured BER, and record baud rate 128 Gbps (64 Gbaud QPSK) transmission is shown for the stand-alone coherent transmitter. The link architecture is based on analog coherent detection (ACD), which improves power consumption substantially by performing functions in the analog domain that are normally implemented with power-hungry digital signal processing (DSP). Energy efficiency of 9.5 pJ/bit is demonstrated for the O-band coherent link, with 12.5 pJ/bit expected with next-generation circuits that include integrated optical gain. These results show the potential for next-generation data center networks based on low-power O-band coherent links.**

***Index Terms*—Coherent optical link, O-Band, silicon photonics, data center, energy-efficiency.**

I. Introduction

As data center network traffic continues to increase, future intra-data center optical interconnects must scale to higher data rates while improving overall cost and power efficiency. Through in-phase and quadrature (IQ) modulation with polarization multiplexing, coherent optical link technologies provide a path to increased data rates over intensity modulation direct detection (IMDD) technologies. Short-reach O-band applications with low chromatic dispersion make power-efficient coherent links an attractive replacement for IMDD technologies for the 1.6 Tbps generation and beyond [1]. In an analog coherent detection (ACD)-based link architecture, power consumption is further reduced by performing carrier and polarization recovery in the analog domain without high-speed analog-to-digital conversion and digital signal processing (DSP). We previously reported an ACD link architecture analysis that showed 5-10 pJ/bit energy efficiencies are possible with 13 dB of unallocated link budget [2].

The design tradeoffs for coherent links change significantly when moving from conventional longer reach long-haul, metro, and inter-data center links to shorter intra-data center ones. Power consumption and cost improvements are crucial for this high-volume application, so link performance must be sacrificed in key areas for coherent link technology to be viable. The ACD link architecture does this by eliminating the carrier and polarization recovery functions traditionally performed by the coherent DSP application specific integrated circuit (ASIC) and replacing them with an optical phase locked loop (OPLL) and analog polarization controller. DSP-based chromatic dispersion compensation is obviated by operating in the O-band, near the zero-dispersion point of single mode fiber. Long-reach coherent links have thus far operated in the C-band because it offers the lowest attenuation and chromatic dispersion can be straightforwardly compensated in DSP, but an additional 0.2 dB/km of loss is tolerable for intra-data center reaches and an O-band coherent link can omit DSP-based chromatic dispersion compensation with negligible penalties [3]. Further power savings come from using QPSK transmission, which enables power-efficient limiting electronics and removes the need for power-hungry analog-to-digital converters. Analog techniques for carrier recovery have been previously demonstrated with an OPLL in [4], and with a carrier phase synchronization chip in a polarization-multiplexed-carrier self-homodyne link, in [5].

The design requirements for intra-data center coherent links goes beyond the transceivers themselves, however. ACD links with large unallocated link budgets enable data center networks with passive arrayed waveguide grating routers (AWGRs) or active optical switches, improving overall network latency, cost, and power consumption [6]. Dynamic network reconfigurability from optical switching can optimize server and resource utilization for specific workloads, with projections of >2X energy efficiency improvement for the entire system [7]. In fact, optical switching is already deployed at scale in data centers. In [8], Google report 41% reduced power consumption and 30% reduced cost for their overall data center networks, including switches and interconnects. Furthermore, dynamically reconfigurable optical circuit switches have yielded advantages in network throughput and incremental installment. These optical switches have been widely and

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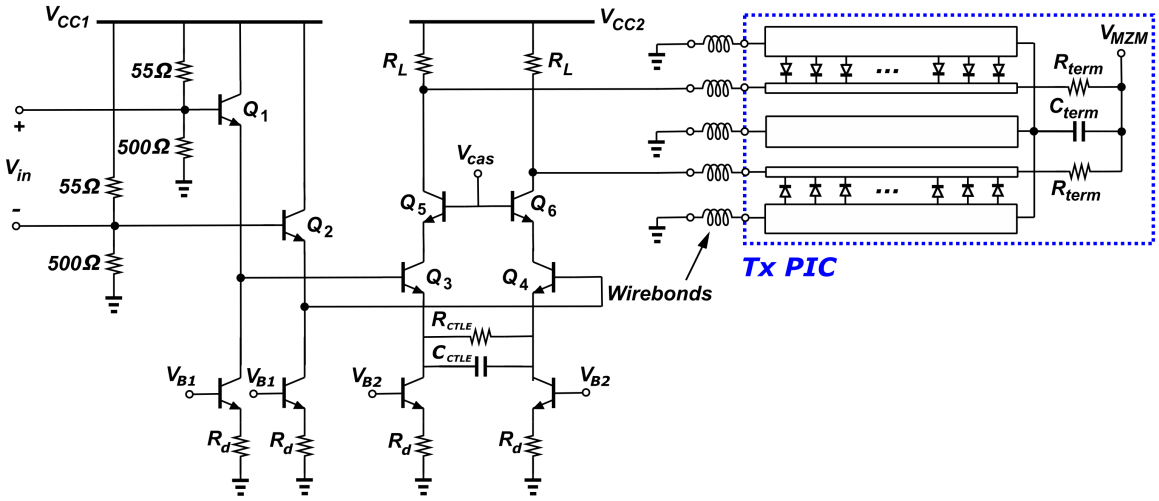

Fig. 1. Schematic of one differential driver and MZM channel. The full Tx includes 4 channels for the DP-IQ-MZM.

reliably deployed in production traffic, and are enabled by optical link technologies that support additional loss in their link budgets. As data rates scale, low-power analog coherent links are the ideal link technology to support widespread adoption of optical circuit switching across the industry.

This paper expands on the result initially published in [9]. We present here the first full-link demonstration of an O-band coherent link designed for intra-data center applications, with 56 Gbaud quadrature phase shift keying (QPSK) operation for 112 Gbps per polarization with a bit error rate (BER) of $2.1 \cdot 10^{-4}$. The achieved BER is below the threshold for KP4 forward error correction (FEC). We have designed and fabricated custom transmitter (Tx) and receiver (Rx) electronic and photonic integrated circuits (EICs and PICs) for an ACD-based link. Previously reported O-band coherent results for either high-speed Tx PICs [10] or Rx PICs and EICs [11] have relied on test equipment in the absence of integrated photonics or electronics for the full link. Our custom Tx was also measured stand-alone, resulting in record-high 64 Gbaud operation with a BER $< 10^{-4}$ for a combined O-band coherent driver and modulator. Section II will describe the design of the O-band coherent Tx and Rx, Section III will present results of component and link characterization experiments, and concluding remarks will be made in Section IV.

II. Design

The Tx and Rx PICs were fabricated in Intel's silicon photonics process. The Tx and Rx EICs were fabricated in the GlobalFoundries 9HP 90 nm and 8XP 130 nm SiGe BiCMOS processes, respectively. The driver has 2 Vppd output swing and 45 GHz bandwidth across four differential channels that drive a dual-polarization (DP)-IQ travelling wave Mach-Zehnder Modulator (MZM) on the Tx PIC. The output stage load resistor R_L is 200 Ω. This quasi-open collector design maintains low power consumption while suppressing back-reflection effects from the travelling wave MZM, thereby averting the need for DSP-based equalization to recover Tx signal integrity [12]. The driver also included a continuous time linear equalizer (CTLE) circuit in the output stage to peak the output and compensate for bandwidth degradation in the Tx PIC and receiver. The nominal design had 9.5 dB of peaking at 30 GHz, and a schematic of one channel of the driver circuit integrated with a MZM on the Tx PIC is shown in Fig. 1.

The Rx EIC design was reported previously [13], and included the data path Rx chain with transimpedance amplifiers (TIAs) and variable gain amplifiers (VGAs) as well as the phase-frequency detector (PFD) circuit required for closed-loop OPLL operation. Since the target modulation format is QPSK, the Tx and Rx both took advantage of power-efficient limiting amplifier circuits. Analog OPLL operation for this ACD-based receiver architecture does not require sampling clock information [3]. Thus, while it is not considered in detail in this work, conventional clock and data recovery (CDR) techniques can be performed on the outputs of the Rx EIC to interface with standard Serializer/Deserializer (SerDes) blocks. The Rx PIC is similar to a conventional dual-polarization coherent receiver with differential photodiodes (PDs), except that it includes an analog polarization controller formed from a series of phase shifters and 2x2 multi-mode interferometers (MMIs) after the polarization splitter rotator (PSR) in the signal path. Endless reset-free polarization control has been previously demonstrated [14], including recent demonstrations with integrated phase shifters [15]. This polarization controller is based on integrated thermal phase shifters and can perform arbitrary polarization rotation, but not in a reset-free manner. Thermal phase shifters are compact and easily integrated into the silicon photonics platform with low loss and good phase efficiency, but they have relatively low bandwidth compared to electro-optic phase shifters. However, studies performed to-date have indicated that short-reach links in data center environments would only be required to track polarization rotations on the order of roughly 100 rad/s [16], which is well within the capabilities of thermal phase shifters. In this work, in addition to an external fiber-based manual polarization controller, the integrated polarization controller was controlled by manually

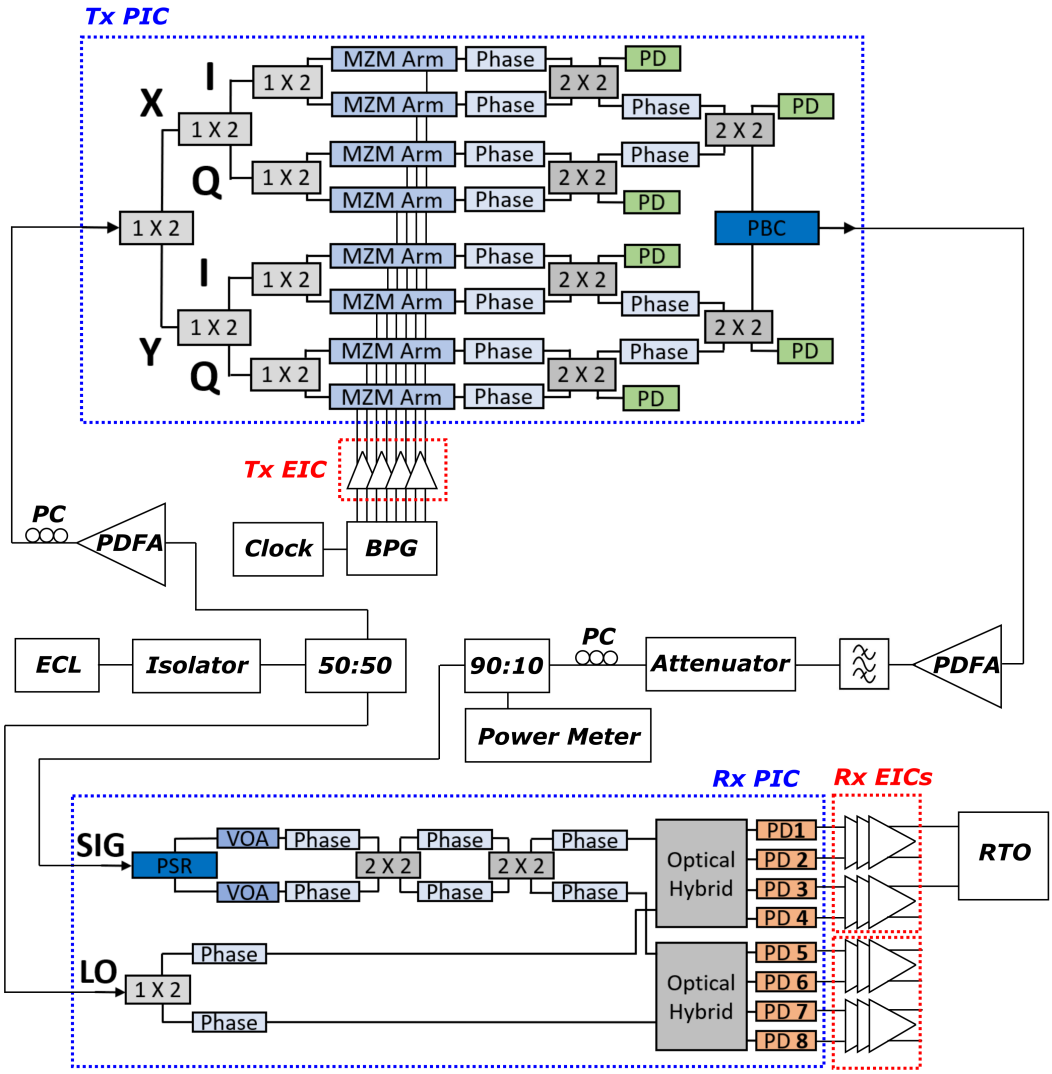

Fig. 2. Schematic of the full link measurement setup, including optical component block diagrams of Tx and Rx PICs. The integrated polarization controller in the Rx PIC, formed from cascading three pairs of phase shifters with 2x2 MMIs, was used for manual static polarization control.

applying voltages to the phase shifters to provide a static polarization rotation at the receiver. Appropriate feedback and closed loop control will be incorporated in a future ACD-based receiver PIC.

The Tx and Rx EICs and PICs were packaged with wire-bonds on FR4 PCBs, with mini-SMP connectors and coaxial cables forming a high-speed interface to test equipment. Additional details of the PCB packaging platform used in this work are described in [17]. The assemblies are compatible with a permanent fiber attachment process, forming complete dual-polarization designs capable of capable of 224 Gbps/λ. During the design process, electronic and photonic circuit and component performance was optimized using full-link time-domain simulations. The link model included component losses, bandwidths, packaging parasitics, and noise contributions, and incorporated co-simulation of high-speed opto-electronic device performance with transistor-level electronic circuit simulations. In this manner, the designs were optimized with the direct goal of full-link integration. This allowed for co-optimization of driver output stage CTLE, driver load resistor, and travelling wave MZM phase efficiency and bandwidth to minimize ISI and noise across both the Tx and Rx, and to improve the overall available link loss budget.

III. Results

A. Experimental Setup

As the integrated lasers required for an OPLL were not included in these first-gen PICs, a 1310 nm external cavity laser (ECL) was split into local oscillator (LO) and signal paths in a self-homodyne link configuration. The link measurement setup is shown in Fig. 2 along with block diagrams of components of the Tx and Rx EICs. 500 mV PRBS15 differential signals from a bit pattern generator (BPG) (SHF 12105A) drove the Tx EIC, and Rx EICs outputs were detected by a real-time oscilloscope (RTO) (Keysight UXR0702A) with a 0.875 μs acquisition time at 256 GSa/s. A post-processing script corrected static constellation rotation, then sampled and counted bit errors.

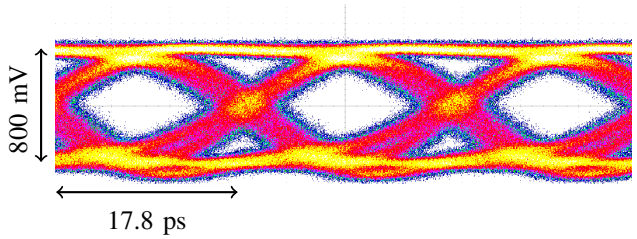

Fig. 3. Measured all-electrical eye diagram of 56 Gbaud NRZ driver operation for one single-ended output.

No external equalization or additional post-processing was performed, so the results reported in this work represent native link performance, including all ISI and packaging effects. These results are for the first Tx and Rx subsystems we have built, and due to assembly yield we are reporting dual-polarization QPSK transmission with only single-polarization 112 Gbps receiver operation. Future assemblies will be capable of full dual-polarization 224 Gbps/λ operation. In a future full ACD-based link implementation, the OPLL would correct for time-varying and static frequency and phase errors between the Tx and LO lasers, removing the need for the constellation rotation performed in post-processing in this work. Assuming 1.3 MHz combined Tx and LO laser linewidths, as reported in [18], the OPLL locking process would give a residual phase error that would degrade the system SNR by roughly 0.5 dB [3].

B. Transmitter Characterization

The driver EIC all-electrical time-domain performance was measured by driving a single channel with 650 mVppd from the BPG and measuring the output with a 70 GHz electrical sampling module (Tektronix 80E11). The resulting 56 Gbaud eye is shown in Fig. 3 for a driver EIC variant that included output stage CTLE. This eye diagram includes bandwidth effects from the PCB packaging and coaxial cables at both the input and output.

A Tx subassembly consisting of a DP-IQ-MZM PIC and a driver EIC variant without output stage CTLE was then characterized in a standalone configuration with a reference receiver. The packaged transmitter is shown in Fig. 4. The Rx PIC and EICs in Fig. 2 were replaced by a reference optical hybrid (Kylia COH28X-FCAPC-1300nm) and balanced 70 GHz PDs (Finisar BPDV3320R), shown in Fig. 5. Resulting 56 and 64 Gbaud sampled constellations with BER $< 10^{-4}$ are shown in Fig. 6. Raw unsampled constellations are shown in 6(a) and (b), I-channel eye diagrams are shown in 6(c) and (d), and sampled constellations are shown in 6(e) and (f). BER sensitivity curves for this standalone Tx and reference Rx are shown in Fig. 7. As the unamplified output signals from the PDs were measured directly by the real-time oscilloscope, the absolute Rx input power sensitivity of this measurement does not correspond to the sensitivity of a full-link with an integrated TIA-based receiver EIC. Due to the lack of a receiver EIC and the 70 GHz PD bandwidths, however, the link inter-symbol interference (ISI) is dominated

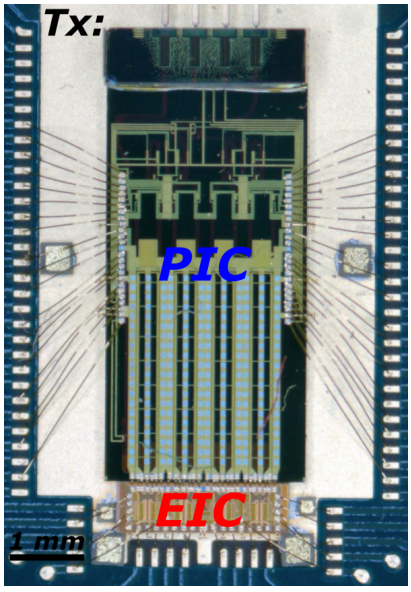

Fig. 4. Transmitter EIC and PIC, packaged on a PCB with wirebonded connections.

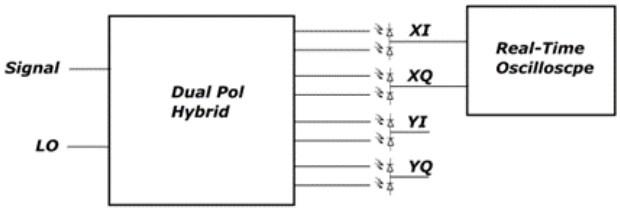

Fig. 5. Schematic of the reference receiver setup used for standalone transmitter characterization.

by bandwidth limitations in the Tx. The 28 Gbaud curve in Fig. 7 is noise-limited with negligible ISI penalty, and since no external or post-processing equalization was performed, the power-penalties shown in the 56 and 64 Gbaud curves can be attributed to the increased Tx ISI at higher symbol rates.

C. Full-Link Demonstration

Finally, the full-link performance with custom Tx and Rx EICs and PICs was characterized. The assembled transmitter is shown in Fig. 4, and the assembled receiver is shown in Fig. 8. The raw unsampled 56 Gbaud QPSK constellations for full-link transmission are shown in Fig. 9(a) and (b), the projections of each constellation onto the in-phase (I) received channel are plotted as eye diagrams in Fig. 9(c) and (d), and sampled constellations are shown in Fig. 9(e) and (f). Single-polarization transmission is shown in Fig. 9(a), (c), and (e). Dual-polarization transmission, with one polarization channel operating at the receiver, is shown in Fig. 9(b), (d), and (f). Sampled constellations for single- and dual-polarization QPSK transmission at 28 Gbaud are shown in Fig. 10. All of these constellations correspond to measured BER $< 10^{-3}$. Because no external equalization is being performed, cumulative link ISI from bandwidth limitations in the EICs, PICs, and packaging manifests in the sampled

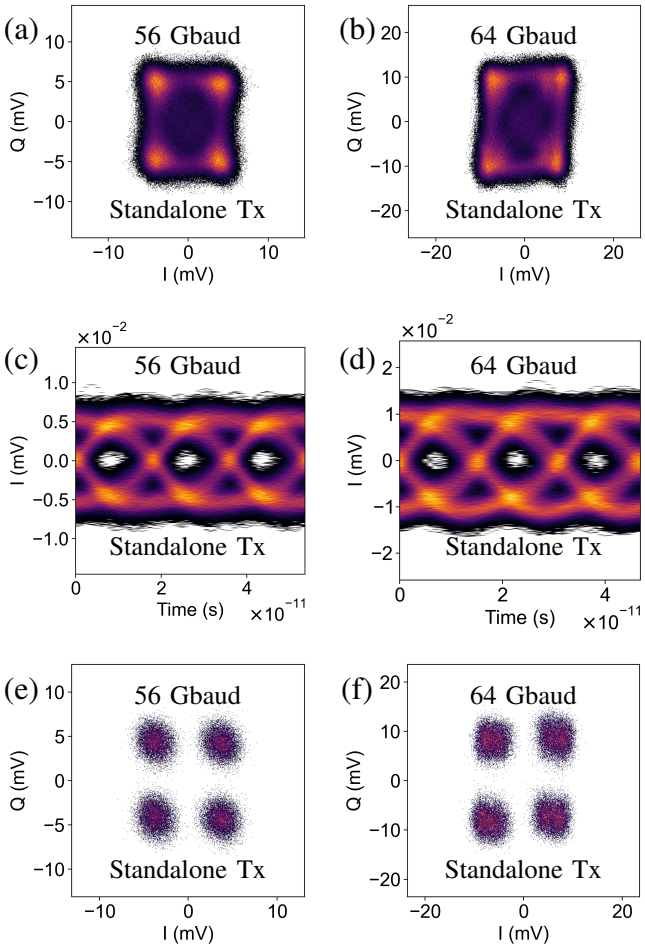

Fig. 6. Measured raw unsampled constellations (a-b), I-channel received waveforms (c-d), and sampled constellations (e-f) for standalone transmitter 56 and 64 Gbaud QPSK operation with reference receiver.

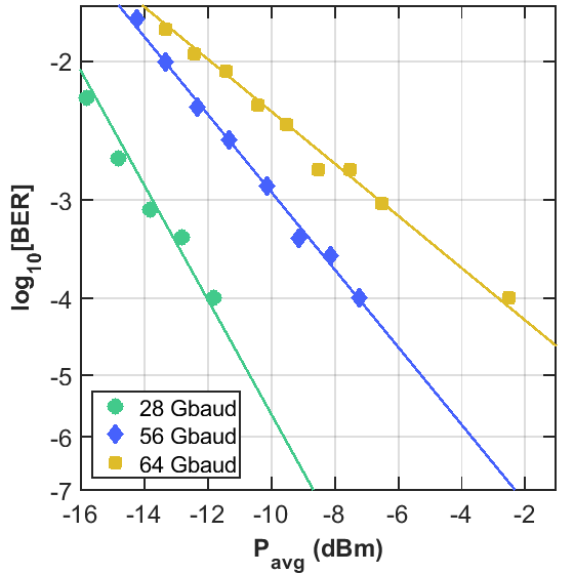

Fig. 7. Measured BER vs Rx input power for the standalone Tx with a reference receiver with −2 dBm LO power per PD.

constellations shown here. Constellation points resulting from

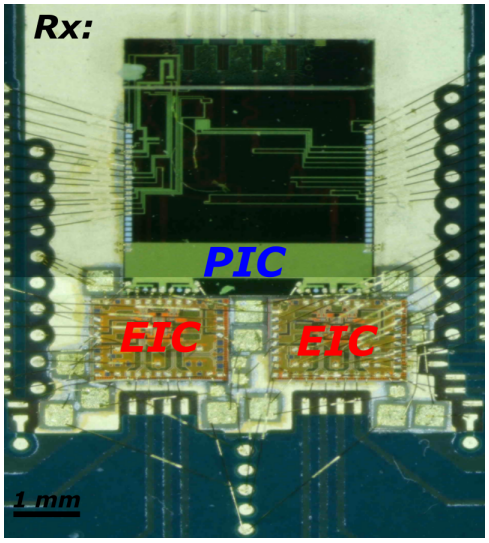

Fig. 8. Receiver EIC and PIC, packaged on a PCB with wirebonded connections.

lower baudrate transmission are noise-limited and appear as circular additive white Gaussian noise (AWGN) distributions, as in Fig. 10. Meanwhile, constellation points from higher baudrate operation appear more square, as in Fig. 6(f) and Fig. 9(e) and (f). The constellations shown in Fig. 9 and Fig. 10 are also slightly asymmetric and diverge from the ideal square QPSK constellation shape. This is likely due to instability and thermal drift in the DP-IQ-MZM biasing configuration. The thermal phase shifters used to set the bias points for the child and parent MZIs were adjusted manually, but a future practical system would incorporate active feedback control to improve the stability of the transmitted constellations.

The impact of polarization crosstalk can be seen by comparing corresponding measured constellations. BER vs average signal power at the Rx input for the full link is plotted in Fig. 11 for 28 and 56 Gbaud. The achieved BER is $2.1{\cdot}10^{-4}$ at 56 Gbaud. Rx input power is reported for a single polarization to normalize the results, and the measured power penalty from polarization crosstalk is 1 dB. The 9 dB power penalty between the 28 and 56 Gbaud sensitivity curves is a measure of the ISI from cumulative link bandwidth impairments, including PICs, EICs, and packaging.

Total power consumption with both polarization channels on was 2.1 W (9.5 pJ/bit). This includes 1.0 W (4.5 pJ/bit) from the driver, 0.2 W (1 pJ/bit) from the Tx PIC, and 0.9 W (4 pJ/bit) from the Rx EIC. Although external optical amplifiers were employed in this first demonstration, received photocurrents were kept below levels expected from next-gen PICs designed with integrated lasers and SOAs. The average LO power incident on each PD was -3.3 dBm, and the received signal power sensitivity values plotted here are expected to improve with higher LO power. Thus, the absolute receiver sensitivity values shown in Fig. 11 don't correspond directly to the sensitivity of a realistic link implementation. For reference, an ACD-based receiver with an integrated 13 dBm output power LO laser and 2 dB of on-chip excess losses would have 2 dBm LO power incident on each PD. Measurement results

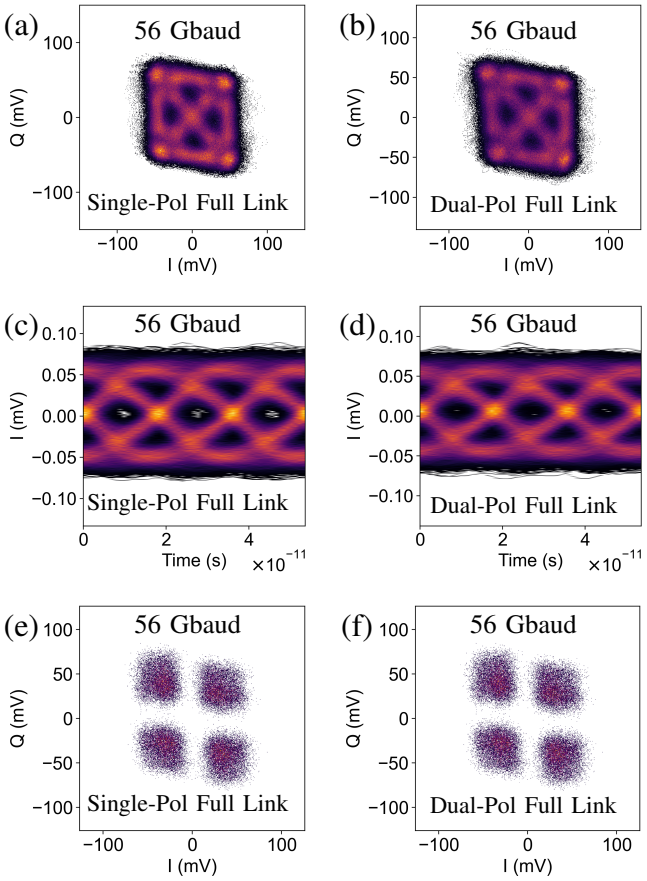

Fig. 9. Measured raw unsampled constellations (a-b), I-channel received waveforms (c-d), and sampled constellations (e-f) for single- and dual-polarization 56 Gbaud QPSK full-link transmission.

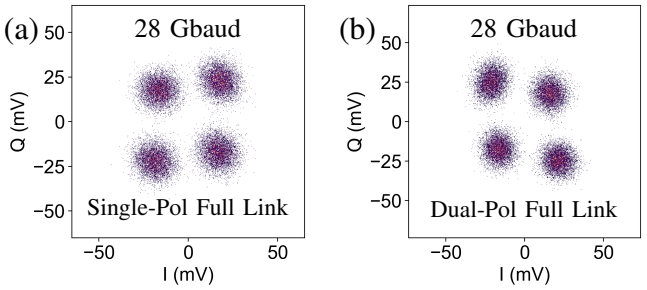

Fig. 10. Measured sampled constellations for single- and dual-polarization 28 Gbaud QPSK full-link transmission.

with next-generation Tx and Rx PICs that include integrated lasers and SOAs are forthcoming. These PICs will improve on the relatively constrained link budget demonstrated in this work by removing unneeded Tx and Rx fiber coupling as well as signal/LO splitting losses. We expect the full ACD-based link based on these PICs to operate below the KP4 FEC threshold with 13 dB of available link loss budget on the fiber, without any external amplification.

IV. Conclusion

We have demonstrated the first full O-band coherent link, including custom driver and receiver EICs integrated with

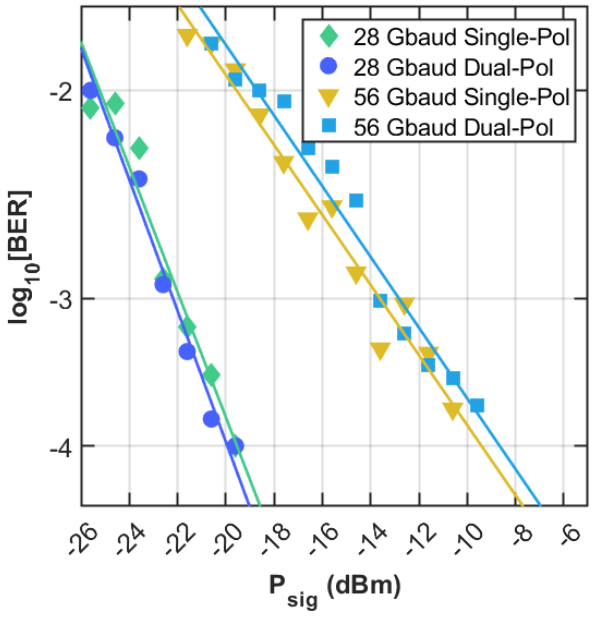

Fig. 11. Measured BER vs Rx input power (per polarization) for the full Tx + Rx link with and without polarization crosstalk.

Tx and Rx PICs. Stand-alone O-band coherent Tx operation was shown at a record 64 Gbaud. Full-link 56 Gbaud dual-polarization QPSK transmission was shown with a BER of $2.1 \cdot 10^{-4}$ with 2.1 W (9.5 pJ/bit) power consumption. We expect 2.8 W (12.5 pJ/bit) power consumption for the full 224 Gbps/λ link, including the OPLL based on next-generation PICs with integrated optical gain. Tunable O-band lasers integrated in this silicon photonics platform were previously reported in [18]. We have also demonstrated a 224 Gbps/λ O-band coherent link with full dual-polarization Tx and Rx operation in [19].

Coherent interconnects for intra-data center applications remain an attractive solution to the meet the demands of rising data rates, but require significant redesign to achieve competitive power consumption and cost. The analog coherent approach outlined in this work aims to obviate and offload functions from the coherent DSP ASIC, which represents the dominant contribution to transceiver power consumption and cost in conventional coherent architectures. Performing polarization recovery, carrier recovery, and bandwidth equalization in the analog domain removes the need for power-hungry analog to digital converters (ADCs), and O-band operation removes the need for chromatic dispersion compensation. Perhaps the most significant benefit of intra-data center coherent link adoption would be the optical switching networks enabled by larger link budgets. Optical switching deployment has already demonstrated significant and quantifiable improvements to data center networks, and short-reach O-band coherent links will empower them by efficiently scaling links with higher data rates and expanded link budgets. While integration challenges remain, the full-link optimization, analog techniques, and new design spaces described in this work are building blocks for future low-power short-reach O-band coherent link deployment. These results show the potential of a low-power

ACD architecture and pave the way for bringing coherent links inside data centers.

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