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Realization of silicon nanopillar arrays with controllable sidewall profiles by holography lithography and a novel single-step deep reactive ion etching

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ABSTRACT

A simple and efficient approach for fabricating silicon nanopillar arrays with a high aspect ratio and controllable sidewall profiles has been developed by using holographic lithography and a novel single-step deep reactive ion etching. During the etching process, scalloping of the sidewalls can be avoided while reserving the high mask selectivity and high etching rate. Besides, the sidewall angle of resultant patterns can be adjusted by tuning the composition of the gas mixture of single-step DRIE process. We further fabricate a tapered silicon nanopillar array and observe its photonic bandgap property. We believe that the good optical performance of this tapered silicon nanopillar array realized by the proposed approach shows the promising of this process for various applications.

INTRODUCTION

Silicon nanopillar arrays have been extensively used in many emerging technologies including bio-medical sensing [1], chemical sensing [2], and electronic field emission [3] via a large surface-to-volume ratio, optical wave-guiding [4, 5] via photonic bandgap properties, field effect transistors [6] via sub-100-nm single-crystalline silicon features, and antireflection coating on silicon [7, 8] via a lower effective index. Except for bottom-growth techniques, a sequence of patterning and etching processes is usually required to realize nanostructures in semiconductors. For patterning, most of nanostructures are realized using electron-beam lithography, covering only a small area. The disadvantages of being time consuming and with very low throughput are also the shortcomings for this technique. Nanoimprint lithography shows potential to replicate patterns with high throughput. But the key concerns of overlay, defects, and template patterning will distort the profile of the resultant patterns and degrade its uniformity. On the other hand, holographic lithography is an attractive method for periodic pattern generation with high regularity over a large area. Holographic system only requires easy-attainable and relatively inexpensive optical components to generate uniform interference patterns without using any mask. For etching, numerous methods have been reported for attaining high-aspect-ratio nanostructures. However, most of them require a metal hard mask formed mostly by lift-off process for the following deep etching [9-12]. This addition lift-off step will degrade the resolution of the profile and increase process complexity. Recently, self-masked dry etching technique is proposed by depositing nanosized clusters formed by reactive gas mixtures [13, 14]. However, the resultant nanostructure arrays are lack of regularity. Deep reactive ion etching (DRIE) is mainly used for micro-electro mechanical systems (MEMS) and microfluidic device

fabrication. Multiple-cycles of the two-step Bosch process enable anisotropic etching of silicon with high mask selectivity (>200:1 for silicon oxide and >75:1 for photoresist) and high etching rate (several µm per min) [15]. However, this technique is not suitable for etching nanostructures due to its scalloping of the sidewalls (the peak-to-valley height is typically the scale of around several hundred nanometers). Recently, with the development of this technology, X. Wang et al. have applied Bosch etching to realize submicron trenches [16] while C.-H. Choi et al. have shown the possibility to control the sidewall profile of nanostructure array by tuning the parameters of Bosch process [17]. More recently K. J. Morton et al. have demonstrated high-aspect-ratio pillar arrays with optimized Bosch conditions and the scalloping of the sidewalls have been minimized to around 10 nm [18]. Nevertheless, due to the alternative etching/deposition nature of Bosch process, we can still see the periodic “ripples” on the sidewalls of the best pillars to date. The scalloping effect will become serious with increased etching depths of patterns.

In this work, we have realized two-dimensional (2D) resist templates by using holography lithography with a double exposure and a rotation of samples before the second exposure. An analysis model is developed and an antireflection layer is used for eliminating the back-reflection from the substrate. To keep the advantages of high mask selectivity and high etching rate in the Bosch process but avoiding its scalloping effect, we have developed a mean of directly transferring photoresist patterns into silicon by using a single-step deep reactive ion etching (SDRIE) with a controlled mixture of $Ar/SF_6/C_4F_8$ gases. The influence of the composition of gas mixture to the resultant profile is also investigated. Optical characterization of SDRIE-realized silicon nanopillar array is also performed.

FABRICATION APPROACHES

<u>Holographic realization of resist template</u>

For 2D resist template realization, a holography setup based on a two-beam interference principle shows much attractive due to its simplicity and flexibility. A hexagonal array with a circular shape can be realized by triply exposing the same interference pattern with the sample rotated by 0°, 60° and 120°, respectively. Unfortunately, this method suffers from the alignment issue for realizing hexagonal structures in large area [19]. On the contrary, if a double exposure of two-beam interference is executed at 0° and 60°, one can fabricate 2D periodic structure with a hexagonal lattice of elliptical geometry. Figures 1 (a) and (b) show the interference patterns of the 1st and 2nd exposure steps on the sample. A 60-degree tilted interference pattern is obtained by rotating the sample before 2nd exposure. The resultant 2D intensity distribution on the sample and the final pattern after development are shown in Figure 1 (c) and (d), respectively. Although the shape of resultant pattern is elliptical, there still exists a broad photonic bandgap inside this structure [19]. The width of the resultant patterns can be adjusted and fine tuned by controlling the total exposure energy and development time [20]. The relatively simple fabrication procedures and experimental setup of this method will improve the manufacturing yield, thus reducing the cost.

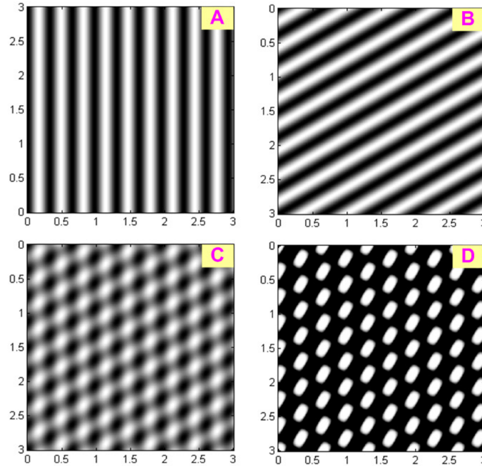

Figure 1 Schematic diagram of process procedures for realizing hexagonal 2D resist template by means of two-beam interference principle with double-exposure steps.

Single-step deep reactive ion etching

For silicon etching, we use a Plamsa-Therm 770 SLR series system with a loadlock for deep etching silicon pillars. The system has an inductively coupled plasma (ICP) coil and a capactively coupled substrate RF supply to independently control plasma density and ion energy in the system. This system is dedicated to deeply etching in silicon for MEMS structures using conventional Bosch process which cycles between a polymer deposition cycle using C_4F_8 gas (no substrate bias) and an etching cycle using a SF_6 mixture with substrate bias. However, due to the isotropic etching nature of SF_6 dry etching, scalloping of the sidewalls results from this process. We have developed a SDRIE process with a controlled mixture of $Ar/SF_6/C_4F_8$ gas to avoid this scalloping issue while simultaneously keeping the high etching rate and high mask selectivity. Figure 2 shows the comparison of process flow between conventional Bosch process and SDRIE process. Polymer deposition for protecting lateral sidewalls and deep silicon etching proceed simultaneously in SDRIE process. With an optimized gas mixture for balancing the deposition and etching rate, pillars with vertical sidewalls can be realized.

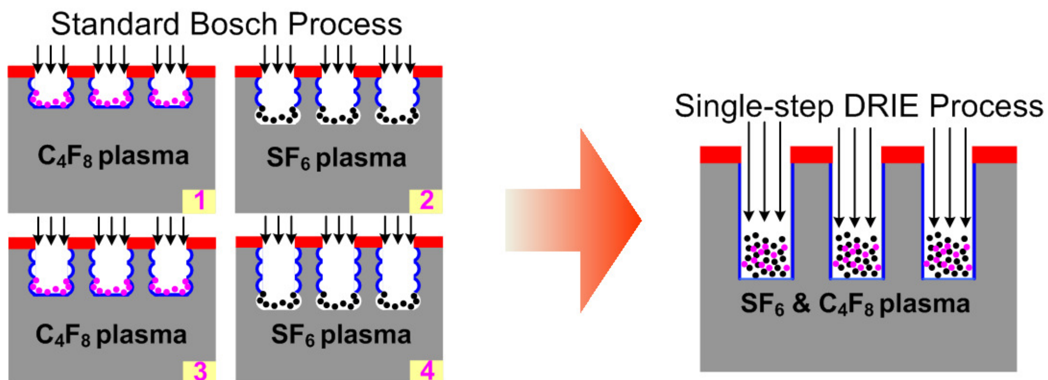

Figure 2 Comparison of process flow between conventional Bosch process and SDRIE process

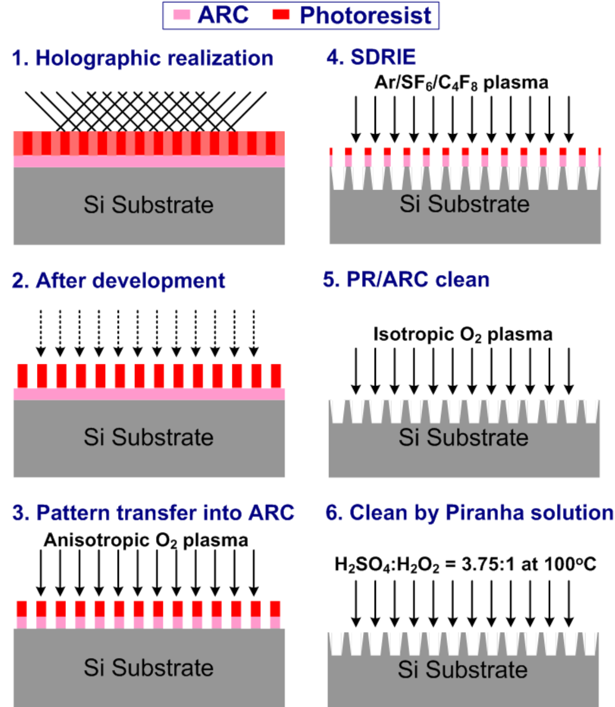

Figure 3 Fabrication procedures of silicon nanopillar arrays by holographic lithography and SDRIE process

Fabrication procedures of silicon nanopillar arrays

Instead of using a thin photoresist (PR) layer (~20 nm) for holography [17] which may limit the final etched height of silicon pillars, a thick PR template with a periodicity of 350 nm and an aspect ratio of 2 is fabricated uniformly over a large area with the help of antireflection coating [20]. Figure 3 shows the overall process for fabricating silicon nanopillar arrays by holographic lithography and SDRIE process. A silicon substrate is cleaned by ultrasonification in acetone and iso-propanol and blown dry with nitrogen gas. An antireflection coating (ARC) layer is deposited by spin-coating at 3000 rpm for 30 seconds. After pre-baking the ARC layer on a hot plate at 165 degrees for 60 seconds, a positive PR layer is deposited at 3000 rpm for 30 seconds and soft baked at 90 degrees for 90 seconds. The sample is then transferred to the laser holography system and exposed twice with a dose of 30.24 mJ/cm^2 for each exposure. Following the double-exposure, a post-exposure bake is performed on a hot plate at 115 degrees for 120 seconds to further reduce the standing-wave effect in the resist sidewalls. After that, the sample is dipped into developer for 10 seconds to attain a periodic structure. After development, the sample is clean by rinsing it in de-ionized water. The sample is finally hard-baked to complete the cross-linking process. Transferring PR patterns into bottom ARC layer is then carried out by anisotropic O_2 plasma using a conventional reactive ion etching (RIE) machine with an O_2 flow of 10 sccm, a pressure of 10 mTorr, and a RF voltage of 250V. The substrate is then etched by SDRIE using the PR/ARC pattern as a hard mask. After SDRIE, the remaining PR/ARC is removed by isotropic O_2 plasma with an O_2 flow of 20 sccm, a pressure of 80 mTorr, and a RF voltage of 250V. Finally, the substrate is cleaned with a Piranha solution (H_2SO_4:H_2O_2 = 3.75:1

by volume with a lifted temperature of 100 degree Celsius). The resultant structures are then characterized using a scanning electron microscope (SEM).

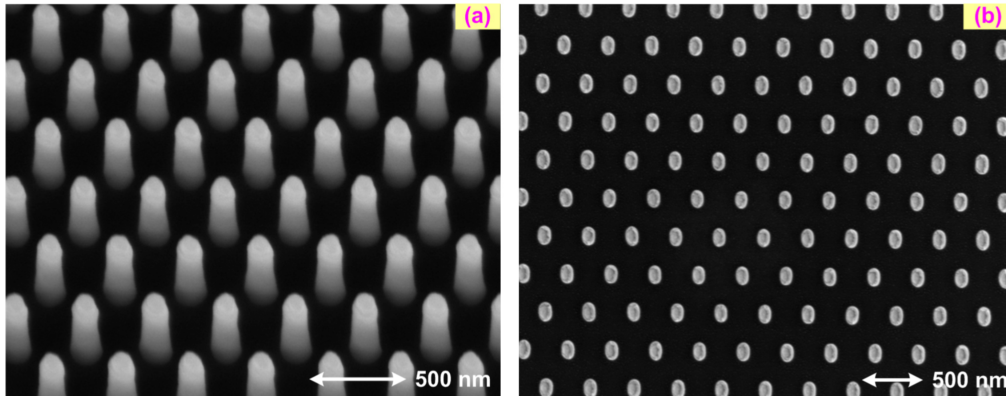

Figure 4 (a) Tilted and (b) top SEM views of resultant 2D PR/ARC templates

Results and discussion

Figure 4 shows the tilted and top SEM views of resultant 2D PR/ARC templates after holographic exposure and anisotropic O_2 plasma etching. The diameters of the resultant patterns are around 147 and 104 nm for major- and minor-axis of ellipse, respectively. The height of this template is around 250 nm. Samples with a hexagonal lattice, high uniformity and vertical sidewalls are demonstrated over a large area.

For pattern transferring into silicon, different mixtures of reactive gases are used to understand how it will affect the resultant slope of sidewall profiles. Detail process conditions are listed in Table 1. Sidewall angle is defined as the inner angle of the pillar. The cross-section and tilted SEM views of the corresponding samples are shown in Figure 5. For the mechanism of this reactive gas mixture, isotropic etching of the silicon is carried out by SF_6 plasma while sidewall protection (lateral etching suppression) is carried out by plasma deposition of C_4F_8. Balance between etching and deposition steps is the key to attain high-aspect-ratio patterns with vertical sidewalls. In this experiment, we fix the flow of Ar gas and the total flow of C_4F_8 and SF_6 to 20 and 80 sccm, respectively. The pressure in the chamber is set to be 19 mTorr. The power of RIE generator and ICP are fixed at 9 W and 850 W, respectively. The flow of C_4F_8 increases from 50 to 54 sccm while the flow of SF_6 decreases from 30 to 26 sccm. Total etching time for each process condition is varied in order to attain pillars with almost the same height. The different etching rate is due to different flow combinations of C_4F_8 and SF_6 gas mixture (More SF_6 or less C_4F_8 will have higher silicon etching rate). Due to excess SF_6, the width of the resultant pattern in Figure 5 (a) changes from 113 nm at the top to 62.7 nm at the bottom, resulting in a sidewall angle of 92.4 degree. On the contrary, with excessive C_4F_8, the width of the resultant pattern in Figure 5 (c) changes from 31.3 nm at the top to 157 nm at the bottom, resulting in a sidewall angle of 84.1 degree. Almost vertical sidewalls on the resultant patterns can be realized with balanced etching/deposition rate. The widths of the resultant pattern in Figure 5 (b) are almost the same between the top (109 nm) and the bottom (117 nm), resulting in vertical sidewalls with a sidewall angle of 89.6 degree. The etching rate of silicon under this

process recipe is around 222 nm/min. It should be noted that smooth sidewalls on the resultant patterns are observed in Figure 5, showing that SDRIE can really avoid the scalloping effect. Samples under those SDRIE conditions are highly uniform over a large area. Besides, Figure 5 also shows that the sidewall angle can be adjusted by tuning the composition of gas mixture. We currently achieve an 8-degree tunable range of sidewall angles for this 350 nm spaced 2D nanostructure. This profile tuning range is limited by the width of nanostructure.

Table 1 Profiles of resultant patterns under different DRIE process conditions

Silicon nanopillars	**SDRIE process conditions**				**Resultant profiles**	
	Time (min)	**C_4F_8 (sccm)**	**SF_6 (sccm)**	**Ar (sccm)**	**Height (μm)**	**Sidewall Angle (degree)**
Sample (a)	3	50	30	20	1.2	92.4
Sample (b)	5	52	28	20	1.11	89.6
Sample (c)	14	54	26	20	1.22	84.1

* The pressure is set to be 19 mTorr. The power of RIE generator is fixed at 9 W while the power of the ICP is fixed at 850 W.

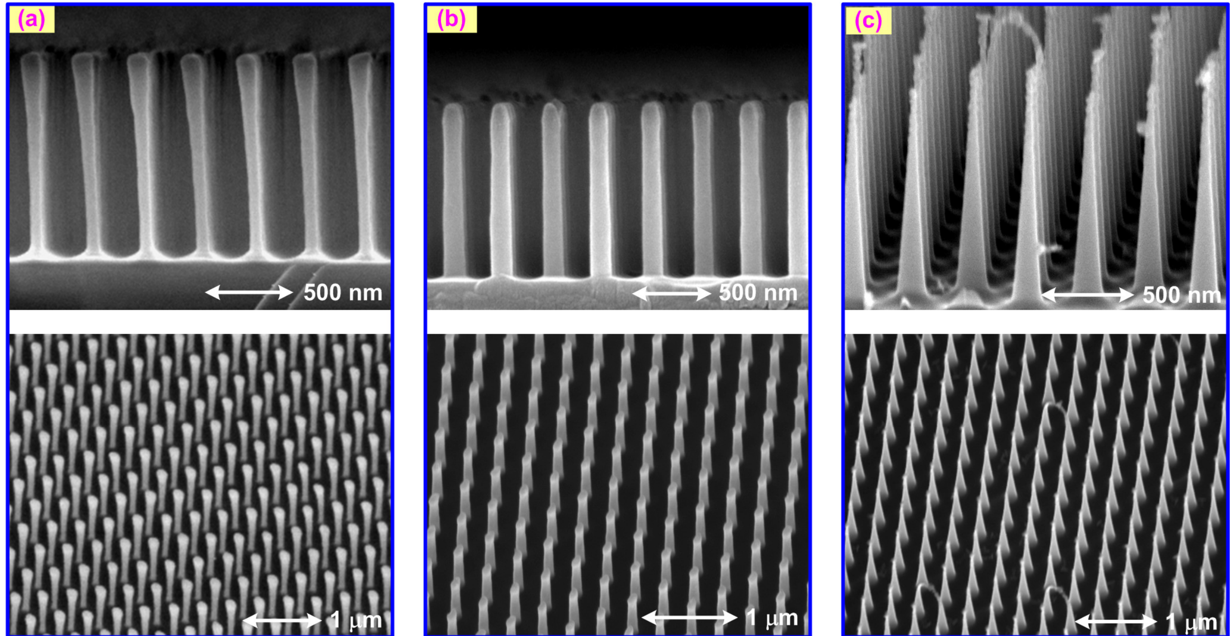

Figure 5 Cross-section and tilted SEM views of resultant profiles under different process conditions

Mask selectivity is also an important factor for the SDRIE process. Figure 6 (a) shows the cross-section SEM view of the original PR template after holographic exposure and development. The thickness of PR pattern and ARC layer are 270 nm and 120 nm, respectively. After transferring patterns from PR into ARC layer by anisotropic O_2 plasma etching, the height of the

resultant template is around 250 nm, as shown in Figure 4. Figure 6 (b) shows the cross-section SEM view of the resultant pattern after SDRIE process using the process recipe of sample (b) in Figure 5. After attaining a tall 1.11 μm silicon pillar array, the thickness of the remaining PR/ARC is still about 237 nm, corresponding to a high mask selectivity of ~85:1. It should be noted that the hard-baking of the PR and ARC before SDRIE process is the key to attain high mask selectivity between silicon and PR/ARC. The diameters of the resultant silicon pillars are around 115 and 82 nm for major- and minor-axis of ellipse, respectively. By comparing those values with that of the original PR/ARC templates, the lateral etching rate using vertical-etched recipe of SDRIE is around 4-6 nm/min.

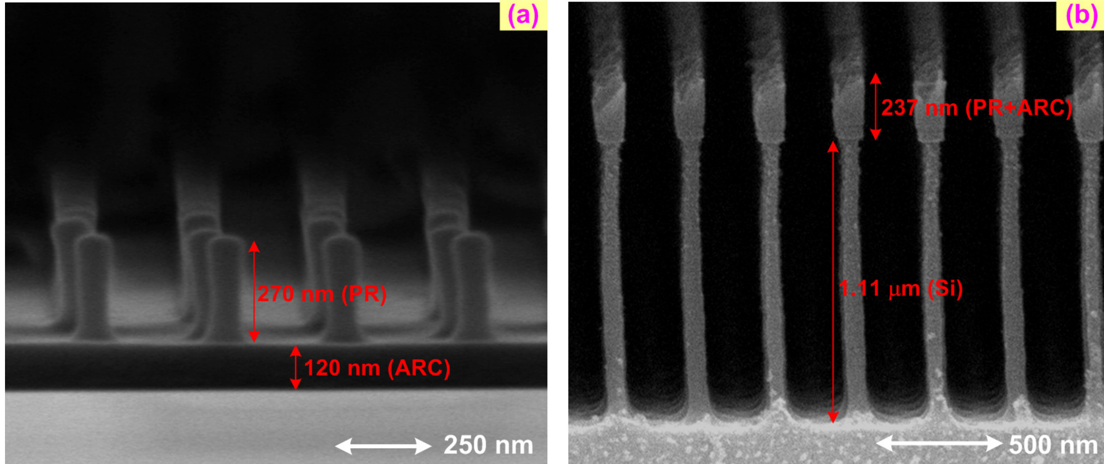

Figure 6 Cross-section SEM views of (a) the original resist template after holographic exposure and development and (b) the resultant pattern after SDRIE process using the process recipe of sample (b) in Figure 5.

TAPERED SILICON NANOPILLARS AND ITS OPTICAL PROPERTY

As we mention that the slope of etched sidewall profile can be easily controlled by engineering the composition of gas mixture. Realization of tapered silicon nanopillar array becomes possible. To verify the good quality of the resultant patterns, we fabricate a tall 800 nm silicon nanopillar array with a hexagonal lattice of elliptical geometry, a sidewall angle of 86.3 degree (tapered sidewall profile), smooth sidewalls, an averaged ellipticity of 1.6228, and a filling factor (radius-to-period ratio) of 0.146 for testing its optical property. In this case, less SF_6 (26 sccm) and more C_4F_8 (54 sccm) is used during SDRIE process to obtain tapered nanostructures. Figure 7 (a) shows the SEM picture and the photograph of the resultant silicon nanopillar array sample. This resultant nanostructure is highly uniform over the entire sample area, around 1 cm^2. Superior antireflection and enhanced absorption property of this tapered silicon nanopillar array has been mentioned in our previous work [21]. Here, the same sample is used as an example for showing the good optical performance of SDRIE-realized structure. We will focus on the photonic bandgap property of this tapered silicon nanopillar array.

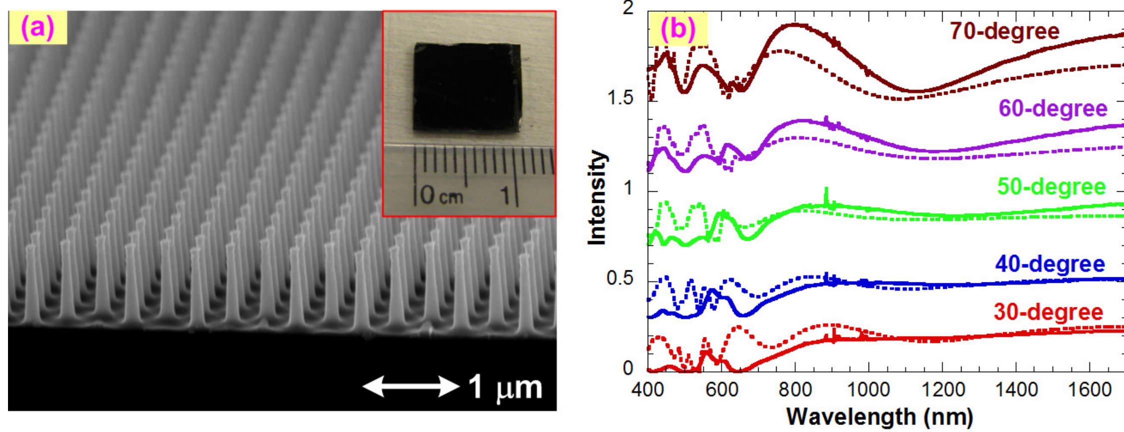

Figure 7 (a) SEM picture and photograph of resultant silicon nanopillar array sample (b) Measured (solid) and calculated (dash) reflection spectra at different incident angles along the ΓM-direction of hexagonal silicon nanopillar array for TM-polarization. The curves are offset for clarity.

Optical characterization of this resultant nanostructure is performed by using an angle-variable spectroscopic ellipsometer. Reflection spectra of this nanostructure under different incident angles and polarizations are measured for observing its optical resonant effect. It is believed that the TM resonance in this structure is mainly due to the existence of PBG which causes dips in the angular reflection spectra. In order to verify this effect, the PBG location is calculated by solving the Maxwell equation with rigorous coupled-wave analysis (RCWA) method, taking both dispersion and absorption of materials into account. The geometry of the silicon nanopillars for RCWA simulation is set according to the real structure as shown in Figure 7 (a) except the slope of sidewalls which is set to be vertical in the simulation model. Figure 7 (c) compares the measured and calculated reflection spectra under different incident angles and polarizations along the ΓM-direction of the hexagonal silicon nanopillar array for TM-polarization. The curves are offset for clarity. Similar behavior is found along the other symmetric points of this structure. From the dips in the measured angular reflection spectra, the PBGs locate at the wavelengths around 650 nm and 1100 nm. There is a good agreement between the experimental and calculated spectra, although measured reflection spectra show weaker and much complex resonances. We believe that this is due to the tapered sidewall of the real structure which reduces the resonant effect.

Spectroscopic ellipsometer is also used for further verifying this unique PBG phenomenon. The measured ellipsometry parameters along the ΓM symmetry direction of hexagonal silicon nanopillar array under different incident angles are shown in Figure 8. Parameters $\tan(\psi)$ and $\cos(\Delta)$ represent the reflection ratio between the TM and TE polarizations and the phase difference through the material-light interaction, respectively. For oblique incidence, the reflection of different polarized light would manifest differently in their corresponding spectra. Theoretically, the reflection caused by the TM photonic bandgap would appear as a dip and a steep slope in the $\tan(\psi)$ and $\cos(\Delta)$ spectrum, respectively. We indeed find similar phenomenon at the wavelengths of 650 nm and 1100 nm along the symmetry points, verifying the existence of full TM PBGs inside the material.

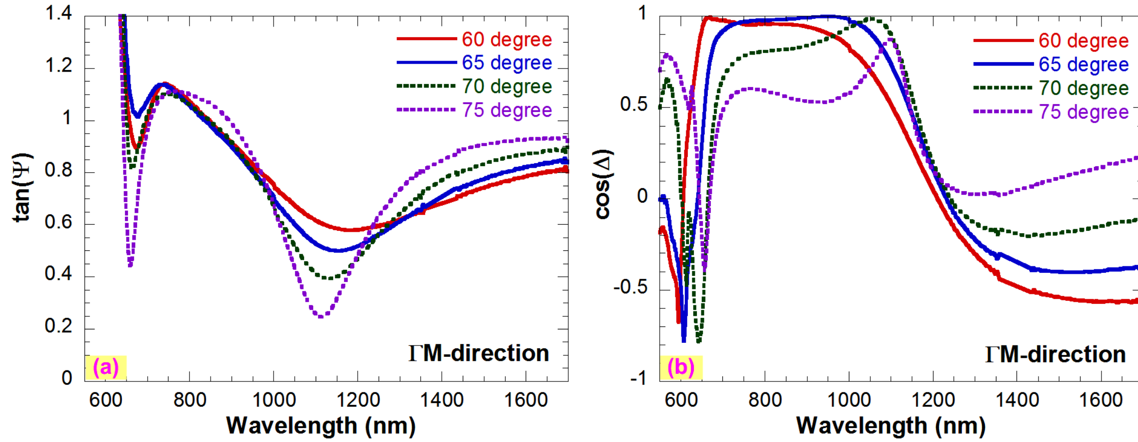

Figure 8 Measured spectra of PBG ellipsometry parameters (a) tan(ψ) and (b) cos(Δ) along ΓM symmetry direction of the hexagonal silicon nanopillar array under different incident angles.

CONCLUSIONS

We have developed a simple and efficient approach for making silicon nanopillar arrays with high regularity and uniformity over a large area. We have demonstrated that 2D resist templates realized by holographic lithography can be used as the hard mask for the following silicon etching process. Instead of using conventional Bosch process, a single-step DRIE with a controlled mixture of $Ar/SF_6/C_4F_8$ gas is used to attain smooth and controllable sidewalls on the resultant patterns while simultaneously keeping the advantages of high mask selectivity and high etching rate. A tall 1.11 μm silicon nanopillar array with an aspect ratio of > 10 and vertical sidewalls (the sidewall angle is about 89.6 degree) is realized with high regularity and uniformity. The sidewall angle of resultant patterns can be adjusted by tuning the composition of the gas mixture of SDRIE process. An 8-degree tunable range of sidewall angle is achieved in the 350 nm spaced two-dimensional nanostructure.

We further fabricate a tapered and 800 nm tall silicon nanopillar array with a sidewall angle of 86.3 degree for testing its optical property. Optical characterization of this nanostructure is performed by using an angle-variable spectroscopic ellipsometer. Reflection spectra are further verified by performing a RCWA simulation. From the dips in the measured angular reflection spectra and the dip and steep slope in the measured spectra of PBG ellipsometry parameters, full photonic bandgaps are found inside this material. We believe that the good optical performance of this tapered silicon nanopillar array realized by the proposed approach shows the promising of this process for various applications.

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