Fabrication of Highly Ordered Silicon Nanowire Arrays With Controllable Sidewall Profiles for Achieving Low-Surface Reflection

Yung-Jr Hung, *Student Member, IEEE*, San-Liang Lee, *Senior Member, IEEE*,
Brian J. Thibeault, *Senior Member, IEEE*,
and Larry A. Coldren, *Fellow, IEEE*

***Abstract*—A novel and simple approach is demonstrated for fabricating silicon nanowire arrays (SNWAs) with controllable sidewall profiles. A single-step deep-reactive-ion etching (SDRIE) is used to transfer the holography patterned photoresist template to silicon or silicon-on-insulator substrates. With the SDRIE etching process, scalloping of the sidewalls can be avoided while reserving the high-mask selectivity over resist and high-etching rate. The sidewall angle of resultant patterns can be adjusted by tuning the composition of the gas mixture of the process. A modified-SDRIE process with a linearly changed gas flow is further developed to extend its capability. A post-high-energy argon plasma treatment is used to create sharp tips on the top of SNWAs and to increase the filling factor. Broadband antireflective (AR) window with a low reflectivity can be realized from tall SNWAs with high-filling factor. Depositing silicon dioxide over SNWAs can further enhance the AR performance. The position and bandwidth of the AR window can be controlled by tuning the SNWA parameters.**

***Index Terms*—Antireflection (AR), holography lithography, silicon nanowire array (SNWA), single-step deep-reactive-ion etching (SDRIE).**

I. Introduction

SILICON nanowire arrays (SNWAs) have been extensively used in many emerging technologies, including biomedical sensing [1], chemical sensing [2], electronic field emission [3], optical waveguiding [4], [5], field-effect transistors [6], and photovoltaic devices [7]–[9]. Except for bottom-growth techniques, a sequence of patterning and etching processes are usually required to realize nanostructures in semiconductors. Most of nanostructures are patterned using electron-beam lithography, which has the disadvantages of being time consuming and low throughput. However, holographic lithography is an attractive method for periodic pattern generation with high uniformity over a large area. For transferring the SNWA patterns to semiconductor structures, numerous etching schemes have been reported for attaining high-aspect-ratio nanostructures. Most of them require a metal hard mask for the following deep etching [10]–[13]. The metal hard mask may require an additional liftoff step that will degrade the profile resolution and increase process complexity. Recently, self-masked dry etching technique is proposed by depositing nanoclusters formed by reactive gas mixtures [14], [15]. However, the resultant nanostructure arrays are lack of regularity. Deep-reactive-ion etching (DRIE) is mainly used for microelectromechanical systems (MEMS) and microfluidic device fabrication. Multiple cycles of the two-step Bosch process enable anisotropic etching of silicon with high-mask selectivity [$>$200:1 for silicon oxide and $>$75:1 for photoresist (PR)] and high-etching rate (several micrometer per minute) [16]. The major concern for using this technique to etch nanostructures is the scalloping of the sidewalls, where the peak-to-valley height can be in the scale of several hundred nanometers. Recently, researchers have demonstrated the use of Bosch etching to realize submicrometer structures [17], [18] and silicon nanopillar arrays with a high-aspect ratio and reduced scalloping of the sidewalls [19]. However, the scalloping effect is still a critical issue for etching deeper nanowires.

In this paper, we have realized 2-D resist templates by using the holography lithography [20]. We developed a single-step DRIE (SDRIE) scheme using $Ar/SF_6/C_4F_8$ chemistry to directly transfer the PR patterns into silicon-based structures. The effects of various process parameters are investigated in order to control the resultant profile. A modified-SDRIE process is developed for obtaining tall SNWAs. A tip-sharpening scheme is also developed to realize tapered nanowires with large filling factor. The antireflection (AR) characteristics of the SNWAs realized with the new fabrication schemes are then measured and discussed.

II. Single-Step Deep-Reactive-Ion Etching

We developed a novel SDRIE technique for fabricating SNWAs by simply using the PR template as the mask. For the etching of silicon nanowires, we use a Plasma-Therm 770 SLR series system with a loadlock for deep-etching silicon pillars. The system has an inductively coupled plasma (ICP) coil

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Y.-J. Hung and S.-L. Lee are with the Department of Electronic Engineering, National Taiwan University of Science and Technology, Taipei 106, Taiwan (e-mail: yungjrhung@gmail.com; sllee@mail.ntust.edu.tw).

B. J. Thibeault and L. A. Coldren are with the Department of Electrical and Computer Engineering, University of California at Santa Barbara, Santa Barbara, CA 93117 USA (e-mail: thibeault@ece.ucsb.edu; coldren@ece.ucsb.edu).

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and a capacitively coupled substrate RF supply to independently control the plasma density and ion energy in the system. This system can be used to deeply etch silicon by means of the conventional Bosch process, which cycles between a polymer deposition cycle using C_4F_8 gas without substrate bias and an etching cycle using a SF_6 mixture with substrate bias. Due to the isotropic etching nature of SF_6 dry etching, it causes scalloping on the sidewalls. We developed a SDRIE process with a controlled mixture of $Ar/SF_6/C_4F_8$ gas to avoid this scalloping issue, while simultaneously achieve high-etching rate and high-mask selectivity. Polymer deposition for protecting lateral sidewalls and deep silicon etching proceed simultaneously in the SDRIE process.

The difference in the etched profiles between the conventional Bosch process and SDRIE can be clearly observed from Fig. 1 for etching a 2-μm-wide waveguide. Detailed information of the process condition is listed in Table I. Although higher etching rate ($\sim$2.3 μm/min) and higher selectivity ($\sim$88.46) can be obtained in the Bosch process, serious scalloping occurs on the sidewalls ($\sim$265 nm) of the resultant profile. On the contrary, patterns with smooth and vertical sidewalls become possible by using the SDRIE process. Although the elimination of the scalloping sidewall profile is achieved at the expense of reduction in etching rate, around 300–400 μm/min of etching rate is still comparable with the existing single-step approaches [21]–[24]. Table II shows the comparison of the proposed SDRIE with other state-of-art single-step etching approaches. $Cl_2/HBr/N_2$-based etching technique has been widely used in IC manufacturing and known to have a good controllability over the sidewall slope [21], [22]. $SF_6/O_2/HBr$-based etching technique has shown the ability to realize high-aspect-ratio features in silicon because silicon etching by F radical is a lot faster than Cl and Br ones [23], [24]. However, both approaches require oxide or nitride hard mask and relatively complicated control of gas composition (three different gases involved) for deep silicon etching. On the contrary, $Ar/SF_6/C_4F_8$-based SDRIE technique provides high-etching selectivity over both resist ($\sim$16) and silicon nitride ($\sim$32) materials. Directly pattern transfer from resist template into silicon becomes possible by SDRIE process, which is particularly useful for etching high-aspect-ratio silicon nanostructures, since it is difficult to define nanometer-scale patterns in very thick resist layers or thick oxide/nitride layers. Unlike $Cl_2/HBr/N_2$ and $SF_6/O_2/HBr$ approaches, which create SiOx or SiNx layers for sidewall protection, sidewall passivation in $Ar/SF_6/C_4F_8$-based SDRIE is achieved by directly depositing polymers on the surfaces, allowing higher etching selectivity. Besides, SDRIE only requires the control of gas composition between two reactive gases (SF_6 for etching and C_4F_8 for passivation, the effect of Ar flow is neglectable).

Fabrication of SNWAs includes two steps: pattern formation by holography lithography and silicon etching by SDRIE. 2-D SNWA resist patterns are realized by means of two-beam interference principle with double exposure and sample rotation steps. The sample is exposed to a 1-D interfered stripe with a sinusoidal intensity profile at 0° and 90° of sample rotation for obtaining square-oriented 2-D periodic patterns. With an optimized process procedure, the width of the resultant patterns can

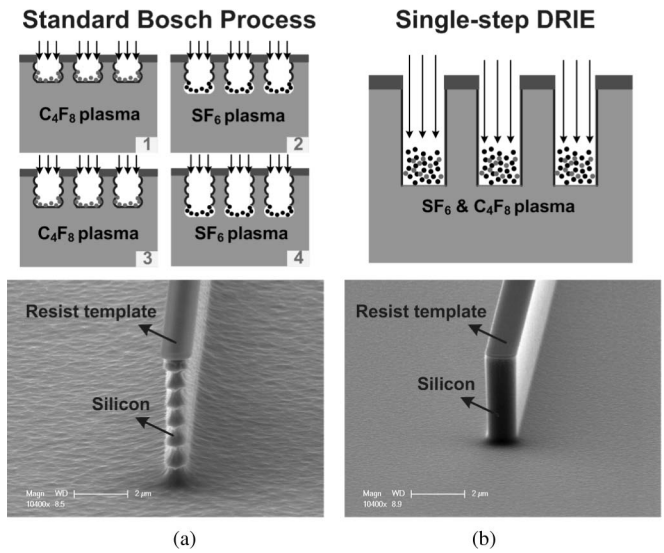

Fig. 1. Schematic of etching process and the resultant profiles for (a) Bosch and (b) SDRIE process.

be adjusted and fine-tuned by controlling the total exposure energy and development time [20]. In this paper, a 270-nm-thick PR template (OHKA THMR-M100) rather than a thin one [18] is used as the mask for deep etching. The SNWAs have a square lattice with a lattice constant of 350 nm. High uniformity can be achieved over a large area with the help of an AR coating (ARC). Transferring PR patterns into the bottom ARC layer is carried out by using the anisotropic O_2 plasma using a conventional RIE machine with an O_2 flow of 10 sccm, a pressure of 10 mTorr, and a RF voltage of 250 V. The substrate is then etched by SDRIE using the PR/ARC pattern as a mask. After SDRIE, the remaining PR/ARC is removed by the isotropic O_2 plasma with an O_2 flow of 20 sccm, a pressure of 80 mTorr, and a RF voltage of 250 V. Finally, the substrate is cleaned with a Piranha solution (H_2SO_4:H_2O_2 = 3.75:1 by volume) at a lifted temperature of 100°C. The resultant structures are then characterized using a SEM.

In order to control the SNWA profile, we will report the effects on the resultant profile by varying the process conditions. For comparisons, the reference process condition is set as the flow rate of Ar, SF_6, and C_4F_8 being 20, 26, and 54 sccm, respectively, the dc-bias power of 9 W, ICP power of 800 W, and the chamber pressure of 19 mTorr.

A. *Effect of $Ar/SF_6/C_4F_8$ Gas Mixture*

The gas mixtures will affect the etching rate and slope of nanowire sidewalls. The incorporation of Ar gas during the SDRIE process is to stabilize the helium gas in the system. The contribution of additional physical bombardment by Ar gas to the silicon etching rate in the SDRIE process is relatively small. Therefore, in this experiment, we vary only the relative flow rate of SF_6 and C_4F_8 from the reference condition. The total flow rate of SF_6 and C_4F_8 is fixed at 80 sccm. Fig. 2(a) shows the silicon etching rate and the corresponding sidewall angle against the gas flow rate of C_4F_8. The C_4F_8-dominated

TABLE I
ETCHING CONDITIONS OF BOSCH PROCESS AND SDRIE, AND THE CORRESPONDING RESULTANT PROFILES

Dry etching	Time (min)	$C_4F_8/SF_6/Ar$ (sccm)	Pressure (mTorr)	ICP/Bias (W)	Height (μm)	Scalloping (nm)	Selectivity over resist
Bosch process	2	0/100/40 70/0/40	23	825/13	4.6	265.5	88.46
SDRIE	10	52/28/20	19	850/9	3.15	0	16.52

TABLE II
COMPARISON OF THE PROPOSED SDRIE WITH OTHER STATE-OF-ART SINGLE-STEP ETCHING APPROACHES

Technique/Chemistry	Mechanism		Etching rate (nm/min)	Mask material	Selectivity	Reference
	Silicon etching	Sidewall protection				
$SF_6/C_4F_8/Ar$ (SDRIE)	F^-	CF_2 (main product)	300~400	PR Silicon nitride	~16 ~32	This work
$Cl_2/HBr/N_2$	Cl^-	SiNx and SiBr	450~530	Silicon nitride	~15	[21, 22]
$SF_6/O_2/HBr$	F^-	SiOx and SiBr	500~800	Silicon oxide	~15	[23, 24]

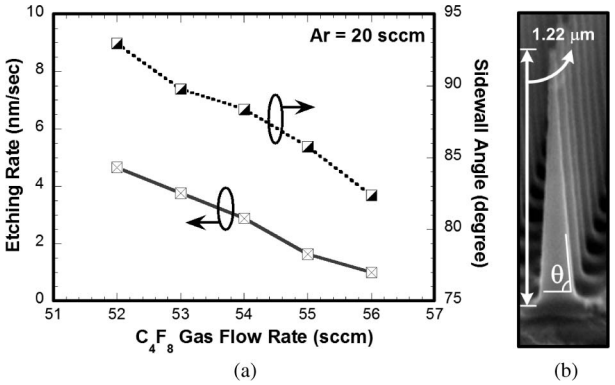

Fig. 2. Etching rate and sidewall angle, as defined in (b), for different C_4F_8 gas flow rate.

(SF_6-dominated) process condition has lower (higher) silicon etching rate and smaller (larger) sidewall angle. Here, the sidewall angle is defined as the inner angle of the pillar, as shown in Fig. 2(b). When the etching and deposition processes are balanced, high-aspect-ratio patterns with vertical sidewalls can be obtained. However, pillars with a tapered profile and a sharp tip can be realized by increasing the flow rate of C_4F_8. Undercut can appear in the pillars as the SF_6 flow rate rises, which may lead to the collapse of patterns. In our previous report, we have demonstrated hexagonal-oriented SNWAs with almost the same height, but different sidewall angles by tuning the gas mixture and etching time [25]. Here, the etching time is fixed at 3 min for obtaining the variation of etching rate and SNWA profile under different gas mixture. Lower C_4F_8 (SF_6) flow rate results in lower (higher) silicon etching rate and smaller (larger) sidewall angles. Around 10° sidewall tunable angle is achieved, verifying that tall SNWAs with controlled profiles can be realized by adjusting the gas mixture.

B. Effect of Chamber Pressure

The chamber pressure can also affect the etching rate and slope of nanowire sidewalls. SNWA samples are fabricated by varying only the chamber pressure from the reference condition.

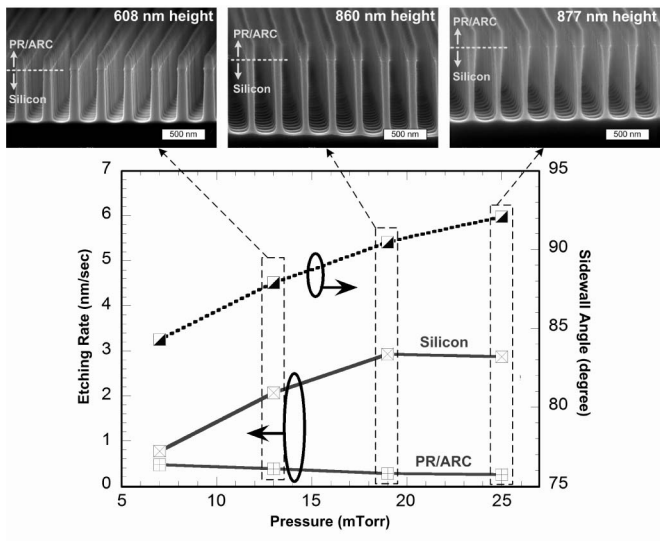

Fig. 3. Silicon etching rate and SNWA sidewall angle against the chamber pressure.

The etching time is fixed at 5 min. Fig. 3 shows the silicon etching rate and the SNWA sidewall angle against the chamber pressure. The silicon etching rate is increased with the chamber pressure due to the increased fluorine radical density [26], [27]. However, the increased fluorine radical density also causes the undercut-etching problem. The saturation of silicon etching rate happens as the pressure is higher than 19 mTorr.

C. Effect of DC-Bias and ICP Power

The degree of dissociation of fluorine is of primary importance in determining etching rate and profile shapes. As the electromagnetic field induced by the ICP source power, a low-source power process can lead to neutral-driven etching rather than ion-driven etching. From our experimental results, the etching rate is relatively insensitive to the ICP source power.

To study the influence of dc-bias power on the SDRIE process, SNWA samples are fabricated by SDRIE with the reference process condition except that the dc-bias power is set as

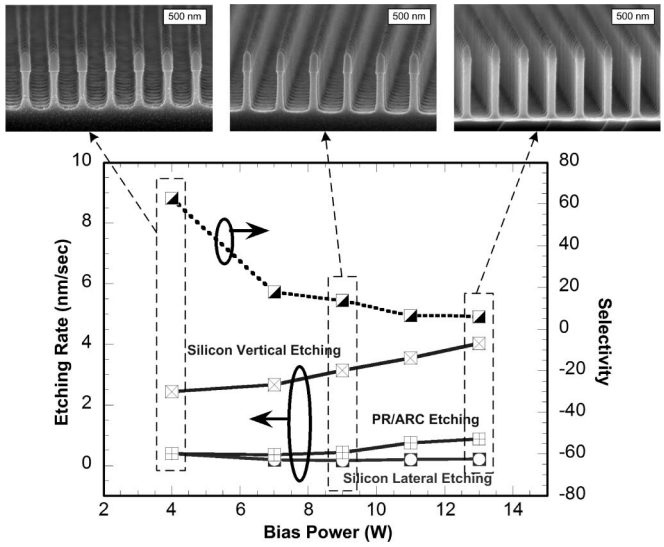

Fig. 4. Etching rate of SDRIE and etching selectivity to resist template under different dc-bias power.

4, 7, 9, 11, and 13 W, respectively. The etching time is fixed at 3 min. Fig. 4 shows the etching rate and selectivity of SDRIE under different dc-bias power. Lowering the physical bombardment on the wafer surface induced by the ion acceleration leads to isotropic etching with undercut etching. By increasing the dc-bias power, the addition of physical etching enhances the etching rate of silicon and PR/ARC and minimizes the silicon lateral etching rate, which will eliminate the pattern shrinkage. However, in case that the physical etching process dominates, the etching selectivity decreases as the dc-bias power rises. Besides, the sidewalls become rough as a high-dc-bias power is applied in the SDRIE process. The compromised value for the dc-bias power of SDRIE is around 9 to 11 W, which will provide an etching rate of around 3 nm/s, a selectivity of around 16, and smooth sidewalls.

III. Modified SDRIE and Tip Sharpening

A. Modified SDRIE With Linearly Changed Gas Flow

Low-silicon surface reflection can be realized with the help of tall nanostructure arrays [29]. Tapered profile of nanostructures could further improve the AR properties [30]. The goal of this paper is to realize tall silicon wire arrays with tapered rods and moderate filling factor (radius to lattice-constant ratio). Although the SDRIE process is good for making silicon nanopillar arrays with a high-aspect ratio and smooth sidewalls, the issues of pattern shrinkage, RIE-lag [26], and undercut etching may limit the process flexibility. We can realize tall nanostructures by increasing the etching time of SDRIE. However, as the etching proceeds deeper, the etching rate in the vertical direction will be decreased due to the RIE-lag effect. Thus, it will require a longer etching time to achieve taller pillar structure. However, the pattern shrinkage becomes serious for a long etching process due to the lateral etching of the PR and silicon. For example, the SDRIE A and B processes, as listed in Table III, result in very narrow pillars as the height exceeds 900 nm. Thus, it is difficult to realize tall nanowire structures, while maintaining a large filling factor by using the SDRIE process. It can be clearly seen from Fig. 3 that the lateral undercut is serious in tall nanostructures, since it is hard for both the etching (SF_6) and protection (C_4F_8) gases to flow into the high-aspect-ratio nanostructures. From Fig. 2, more C_4F_8 gas flow for sidewall passivation is needed to achieve vertical sidewalls. The reduced total gas flow inside tall nanostructures will result in the SF_6-dominated etching process, thus cause lateral undercut etching in the bottom of pillars. Serious lateral undercut may lead to the collapse of patterns.

From Fig. 4, the pattern shrinkage problem can be reduced by increasing the physical bombardment (increase the dc-bias power) and decreasing the chemical etching (decrease/increase the SF_6/C_4F_8 gas flow). To verify this point, we change the bias power from 9 to 13 W and the SF_6/C_4F_8 gas mixture from 26/54 to 25/55 sccm. The process condition and resultant profile is listed as "SDRIE C" process in Table III. After 5 min etching, a 906-nm-tall silicon array can be realized to have an improved filling factor of 0.13 and vertical sidewalls.

In order to obtain silicon wire arrays with larger filling factors, we demonstrate here a "modified SDRIE" process, as listed in Table III, by linearly changing the gas flow. During the process, the flow rate of C_4F_8 (SF_6) changes linearly from 55 (25) to 55.8 (24.2) sccm in five steps. Silicon nitride (SiNx) is used as the hard mask for deep silicon etching. A stronger hard mask is also good for maintaining the width of the resultant patterns. Pattern transfer from PR/ARC into SiNx is carried out by anisotropic CHF_3 plasma etching. The etching time in each step is set to 1.5 min. Higher bias power (13 W) is used to eliminate the pattern shrinkage. The resultant profile after each step of the process is shown in Fig. 5 and the corresponding parameters are summarized in Table III. The pillar height can reach 632 nm after 3 min etching (after step 2). A 1340-nm tall and tapered silicon wire array with an aspect ratio of 10.89 and a filling factor of 0.18 is obtained with a total etching time of 7.5 min (after step 5).

B. Tip-Sharpening Process

Another approach for making nanotip array is to utilize the post-tip-sharpening process. Tip sharpening can be performed by using high-energy argon plasma treatment after the SDRIE etching. In the experiment, two set of samples with almost the same sample area are fabricated by the SDRIE process to have a height of 464 nm (Sample A) and 880 nm (Sample B), respectively. These samples are then exposed to the plasma atmosphere for 20 min with an argon gas flow of 20 sccm, a chamber pressure of 80 mTorr. The RF-bias voltage is varied from 50 to 500 V for observing the tip-sharpening process.

Fig. 6 shows the SEM photos of resultant profiles after postargon plasma treatment for different RF-bias voltages. It can be found that a bias voltage of 50 V for the tip-sharpening process has little effect on the resultant pattern profiles. The top of the pillars become rounded as the bias voltage is raised to 200 V. The tip sharpening of Si pillars happens with a bias voltage of 350 V or larger. We believe that the tip-sharpening effect is due

TABLE III
COMPARISON BETWEEN THE ORIGINAL AND MODIFIED-SDRIE PROCESS

Etching processes		SDRIE process conditions				Resultant profiles		
		Time (min)	C_4F_8 (sccm)	SF_6 (sccm)	Bias power (W)	Height/Width (nm)	Filling Factor	Sidewall Angle (degree)
SDRIE A		5	54	26	9	978/30.2	0.04	90.6
SDRIE B		7	54	26	9	1390/24	0.03	90.3
SDRIE C		5	55	25	13	906/93.5	0.13	90
Modified SDRIE	Step 2	1.5 per Step	55 ↓ 55.8	25 ↓ 24.2	13	632/150	0.21	90.5
	Step 3					849/139	0.20	89.6
	Step 4					1110/130	0.19	89.1
	Step 5					1340/123	0.18	88.4

* The pressure, ICP power and Ar gas flow are fixed at 19 mTorr, 800 W and 20 sccm, respectively. Original SDRIE process uses PR/ARC as the mask. Modified SDRIE process uses silicon nitride as the hard mask.

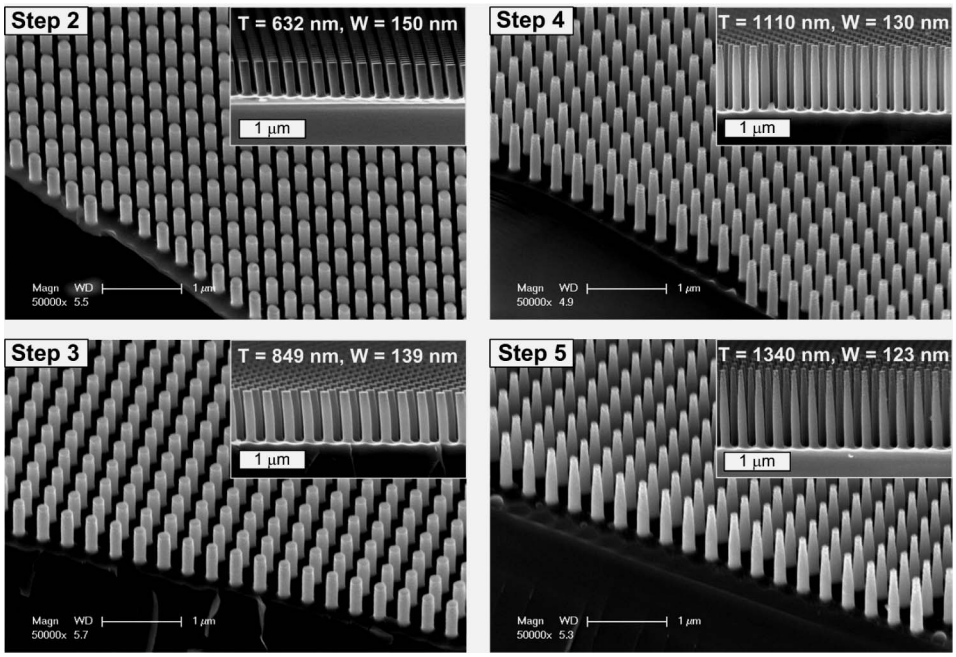

Fig. 5. SEM views of resultant profiles after each step of the modified SDRIE with linearly changed C_4F_8/SF_6 gas flow.

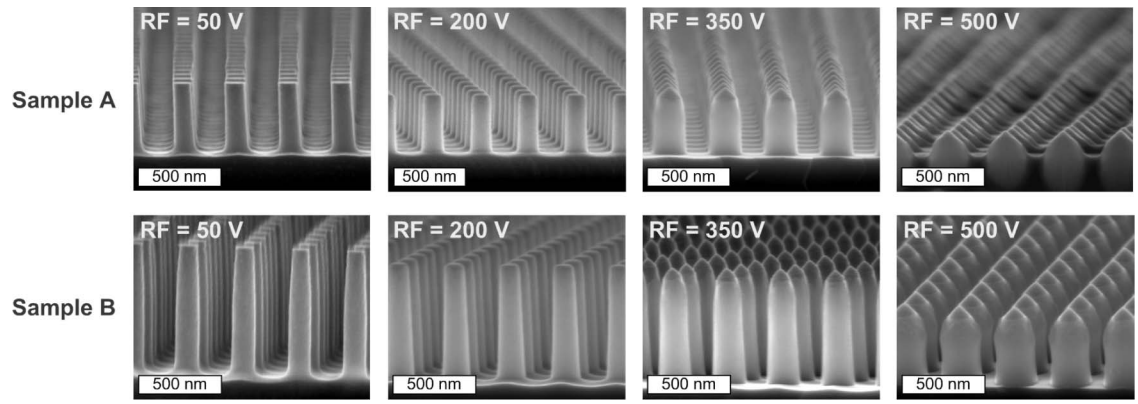

Fig. 6. SEM views of resultant profiles (Samples A and B) after postargon plasma treatment with different RF-bias voltages.

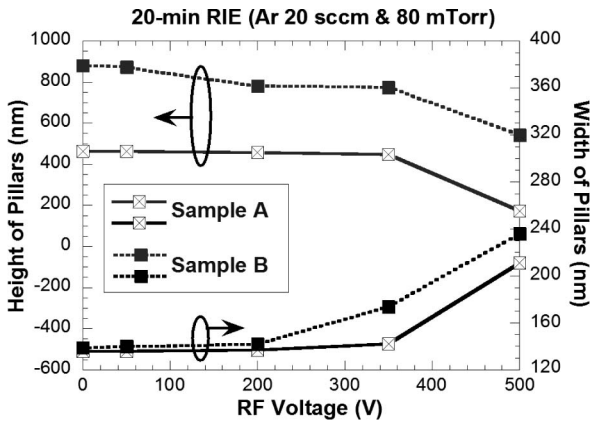

Fig. 7. Height and width of resultant profiles (Samples A and B) after postargon plasma treatment with different RF-bias voltages.

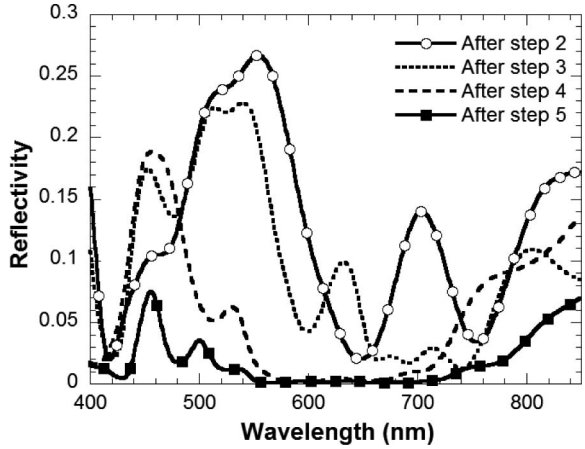

Fig. 8. Measured reflection spectra of SNWAs after each step of the modified SDRIE with linearly changed C_4F_8/SF_6 gas flow, as listed in Table III.

to the existence of higher electric field at the pillar edges, resulting in an enhanced sputtering rate there. However, the height of resultant patterns decreases as the bias voltage increases because of the enhanced physical bombardment, as shown in Fig. 7. It is interesting to find that the width of resultant patterns increases with the bias voltage. This might be due to the fact that the silicon material of pillar arrays is sputtered out and attached on the sidewalls, resulting in an increase in the filling factor of silicon wire arrays.

IV. Optical Reflection

A. Modified-SDRIE Realized SNWAs

We have fabricated tall SNWAs with moderate filling factor by using the modified-SDRIE process. Optical reflection spectra of the resultant SNWA samples are characterized using a spectrophotometer (Filmetrics F20-UV). Fig. 8 shows the reflection spectra of the SNWAs after each step of the modified-SDRIE process. Since the resultant SNWAs are not tall enough after step 2 of the modified SDRIE, the reflection can be as high as 25% in the visible region. The AR effect is improved as the SNWAs become taller and tapered. The reflectivity between 550 and 700 nm of wavelength can be as low as 0.2% for the SNWAs after step 5 of the modified SDRIE. The reflectivity can be less than 7% over the whole visible region.

B. SNWAs After Argon Plasma Treatment

The argon plasma treatment after SDRIE etching can be used to sharpen the tips of SNWAs and to increase their filling factor. Fig. 9 shows the reflection spectra of the SNWAs after argon plasma treatment with different RF-bias voltages for Sample A and B in Figs. 6 and 7. Since the original SNWAs of Sample A are relatively short, low reflectivity can only be obtained over a narrow wavelength range. The lowest reflectivity for the original Sample A is around 3% at 625-nm wavelength. The reflection spectrum of Sample A after 200 V argon treatment is slightly improved to be around 2.4%. For Sample A, after 500 V argon treatment, the height and width of the resultant SNWAs change to 173 and 211 nm, respectively, with sharp tips on the top. Due

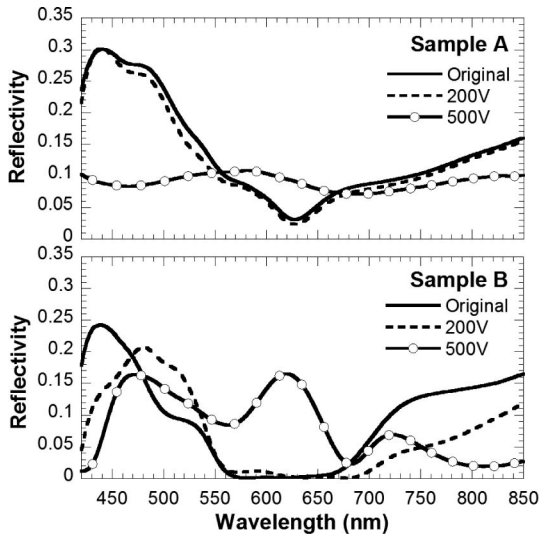

Fig. 9. Measured reflection spectra of Samples A and B in Fig. 6 after postargon plasma treatment with different RF-bias voltage.

to the shallow nanostructures, the resultant SNWAs lose the photonic crystal property, but provide surface roughness effect, resulting in an around 10% reflectivity throughout the visible region.

For the taller Sample B, the minimum reflectivity is around 1.2% in the visible region. The reflectivity is slightly reduced to be around 1% after 200 V argon treatment. The height and width of resultant SNWAs change dramatically to 543 and 236 nm, respectively, after 500 V argon bombardment. With sharp tips on the top and enlarged filling factor, 33.7%, the low-reflectivity window is red-shifted. The reflectivity is increased for shorter SNWAs.

C. SiO_2 Coated SNWAs on Silicon-on-Insulator Substrate

The SNWAs reported in previous sections are fabricated on bare silicon substrate. In this section, we address the properties of SNWAs on silicon-on-insulator (SOI) wafers, which are often used for fabricating optical ICs or thin-film optoelectronic

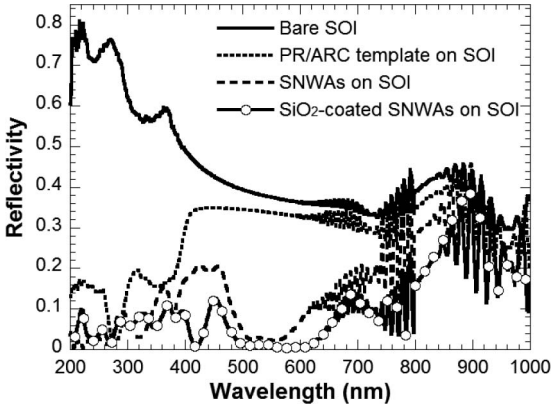

Fig. 10. Measured reflection spectra of bare SOI, 250-nm-tall PR/ARC templates on SOI, 700-nm-tall square SNWAs on SOI, and the 700-nm-tall SNWAs coated with a 186-nm-thick SiO_2 film.

devices. The SOI wafer contains a 2-μm-thick silicon dioxide as the intermediate layer and a 6-μm-thick silicon layer on the top. SNWA samples are fabricated using the SDRIE process. Fig. 10 shows the reflection spectra of the bare SOI, 250-nm-tall PR/ARC templates on SOI, 700-nm-tall SNWAs on SOI, and the 700-nm-tall SNWAs coated with a 186-nm-thick SiO_2 film. The SiO_2 film is deposited by plasma-enhanced CVD (PECVD) over the tall SNWAs to serve as a buffer layer between SNWAs and air.

Lower reflectivity of PR/ARC templates on SOI is due to its lower effective index, which serves as a buffer layer between air and silicon substrate. Reduced reflectivity over the UV wavelengths is due to the absorption characteristic of the ARC film. SNWAs on the SOI substrate can provide lower reflectivity than the bare SOI wafer over a wide wavelength range due to its deeper subwavelength structure. The overall reflectivity of this nanostructure is below 20% in the entire UV to visible region and is around 2.5% in the wavelengths between 500 and 550 nm. The reflectivity is further reduced by depositing a SiO_2 film on top of the SNWAs. The reflectivity is below 10% over the entire UV to visible region and below 1% for the wavelengths between 500 and 600 nm. It verifies that SNWAs coated with a SiO_2 film of right thickness can also improve the AR performance. Since SOI wafer contains Si–SiO_2–Si structures, multicavity resonance can be observed in the longer wavelength side of the reflection spectra.

D. Change of AR Spectra With SNWA Parameters

To figure out how the SNWA parameters affect the characteristic of AR window, we fabricated several SNWA samples on SOI substrate to have different widths, lattice constants, and heights. Fig. 11(a) shows the reflection spectra for SNWAs with different holography exposure time that leads to different pillar widths. The SNWAs with smaller pillar width have blue-shifted reflection spectrum and reduced bandwidth of AR windows. Fig. 11(b) compares the reflection spectra for SNWAs with different lattice constants. Again, the low-reflectivity window becomes narrower and moves to shorter wavelengths for the SNWAs with a smaller lattice constant. The trend shown

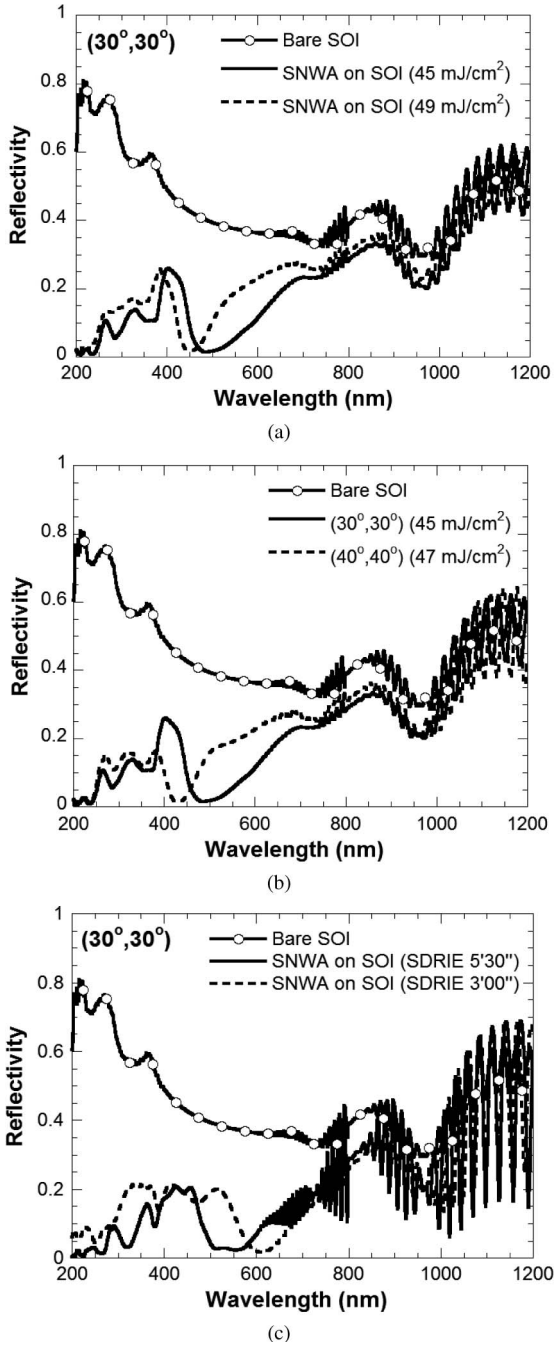

Fig. 11. (a) Measured reflection spectra of 330 nm spaced square SNWAs on SOI substrate with different exposure time during holography for obtaining different pillar widths. (b) Measured reflection spectra of SNWAs on SOI substrate with different lattice constants. (c) Measured reflection spectra of square SNWAs on SOI substrate with different SDRIE etching time for obtaining different pillar heights.

in Fig. 11(a) and (b) agrees with the rigorous coupled-wave analysis (RCWA) simulation results. Fig. 11(c) shows the reflection spectra for the SNWAs with different SDRIE etching time that result in different pillar heights. The RCWA simulation indicates that taller SNWA results in the broadening and redshifting of the AR spectrum. However, for SNWAs realized by the SDRIE process, pattern shrinkage in taller SNWAs leads to

TABLE IV
OPTICAL PROPERTY VARIATION FOR DIFFERENT SNWA PARAMETERS

SNWA parameters	Simulated AR spectrum	Measured AR spectrum	AR bandwidth
Pillar height ↑	Red shift	Blue shift	Increased (↑↑)
Pillar width ↑	Red shift	Red shift	Increased (↑)
Lattice constant ↑	Red shift	Red shift	Increased (↑)

smaller pillar width because of the lateral silicon etching. Thus, the overall reflection spectrum is broadened, but blue-shifted, as shown in Fig. 11(c). The effects of the SNWA parameters on the AR property of SNWAs are summarized in Table IV.

V. CONCLUSION

A novel and simple approach for fabricating tall SNWAs with high uniformity is demonstrated. PR templates realized by the holographic lithography can be used directly as the mask for the SDRIE etching. The SDRIE process with a controlled mixture of $Ar/SF_6/C_4F_8$ gas can be used to attain smooth and controllable sidewalls on the resultant SNWA patterns, while simultaneously keeping the advantages of high-mask selectivity and high-etching rate. The sidewall angle of resultant patterns can be adjusted by adjusting the composition of the gas mixture of SDRIE process. A modified-SDRIE process with a linearly changed gas flow is developed to solve the undercut-etching issue, to eliminate the pattern shrinkage by using a higher dc-bias power and a stronger hard mask. The high-energy argon plasma treatment after SDRIE etching can be used to increase the filling factor and create sharp tips on SNWAs. This postetching process can be used to amend the reflection spectra of SNWAs.

We also demonstrate that SNWAs coated with a SiO_2 film can be used to obtain good AR performance, which is comparable to what we have achieved from tapered SNWAs [8]. How the SNWA parameters affect the characteristic of AR window is also investigated. With increased height, width, and lattice constant of SNWAs, the AR window will be widened and red-shifted. The highly ordered SNWAs fabricated with the SDRIE process and the postetching treatment can be used for reducing surface reflection with high controllability.

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Yung-Jr Hung (S'07) received the B.S. and Ph.D. degrees in electrical engineering from the National Taiwan University of Science and Technology (NTUST), Taipei, Taiwan, in 2005 and 2010, respectively.

In 2009, he was a Visiting Scholar in the Department of Electrical and Computer Engineering, University of California at Santa Barbara, partly supported by the National Science Council, Taiwan. He is currently a Postdoctoral Fellow in the Department of Electronic Engineering, NTUST. His research interests include holographic photonic crystals, semiconductor lasers, solar cells, and photonic integrated circuits.

San-Liang Lee (SM'07) received the B.S. degree in electronics engineering from the National Chiao Tung University, Hsinchu, Taiwan, in 1984, the M.S. degree in electrical engineering from the National Taiwan University, Taipei, Taiwan, in 1986, and the Ph.D. degree in electrical and computer engineering from the University of California, Santa Barbara, in 1995.

In 1988, he joined the faculty of the Department of Electronic Engineering, National Taiwan University of Science and Technology (NTUST), Taipei, and became an Associate Professor in 1995 and a Professor in 2002. From 2002 to 2005, he was the Director of the Center for Optoelectronic Science and Technology, College of Electrical and Computer Engineering, NTUST. He is currently the Dean of the Academic Affairs of NTUST, where he was the Chairman from 2005 to 2008. From 2005 to 2009, he was also the Director of the program office for the National Innovative Education Program on Image Display Technology, sponsored by the Ministry of Education, Taiwan. He has authored or coauthored more than 150 referred papers in international journals and conferences. He holds 22 patents. His research interests include semiconductor optoelectronic components, photonic integrated circuits, nanophotonics, and optical switching technologies.

Brian J. Thibeault (S'89–M'97–SM'05) received the B.S. degree in electrical engineering from the University of California, Irvine, CA, in 1990, and the M.S. and Ph.D. degrees in electrical engineering from the University of California, Santa Barbara (UCSB), in 1991 and 1997, respectively.

In 1996, he started WideGap Technologies, LLC, where he was engaged as a Principal Investigator and a member of the Technical Staff in GaN-based high-electron mobility transistor technologies, and ultraviolet and visible light emitting diodes, which was later merged with Cree, Inc. in 2000. In December 2000, he joined the staff at the UCSB nanofabrication facility as a Principal Development Engineer, where he is currently a Project Scientist. He has authored or coauthored more than 115 journal and conference papers. He has also coauthored one book chapter. He is also an Inventor in ten U.S. patents. His research interests include the area of fabrication of electronic and optoelectronic devices.

Larry A. Coldren (S'67–M'72–SM'77–F'82) received the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, in 1972.

In 1984, he joined University of California, Santa Barbara (UCSB), where he is currently the Fred Kavli Professor of optoelectronics and sensors and the Director of the Optoelectronics Technology Center, and also engaged with materials, and electrical and computer engineering. At UCSB, he continued work on multiple-section tunable lasers; in 1988, he invented the widely tunable multielement mirror concept, which is now used in some JDSU products. During the late 1980s, he also developed efficient vertical-cavity multiple-quantum-well modulators, which led to novel vertical-cavity surface-emitting laser (VCSEL) designs that provided unparalleled levels of performance. He is engaged in developing new photonic IC (PIC) and VCSEL technology, including the underlying materials growth and fabrication techniques. In 1990, he was the Co-Founder of Optical Concepts, later acquired as Gore Photonics, to develop novel VCSEL technology. In 1998, he was the Co-Founder of Agility Communications, later acquired by JDS Uniphase Corporation (JDSU), to develop widely tunable integrated transmitters. At Bell Labs, he was involved in waveguided-surface-acoustic-wave signal processing devices and coupled-resonator filters, and then, developed tunable coupled-cavity lasers using novel reactive-ion etching technology that he created for the new InP-based materials. He has authored or coauthored more than 1000 journal and conference papers, seven book chapters, one textbook, and has issued 63 patents. His research interests include the creation of efficient all-epitaxial InP-based and high-modulation speed GaAs-based VCSELs as well as a variety of InP-based PICs incorporating numerous optical elements for widely tunable integrated transmitters, receivers, and wavelength converters operating up to 40 Gb/s.

Prof. Coldren has presented dozens of invited and plenary talks at major conferences. He was the recipient of the 2004 John Tyndall and 2009 Aron Kressel Awards. He is the Fellow of the Optical Society of America and Institution of Electrical Engineers. He is also a member of the National Academy of Engineering.