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Integrated SOAs enable energy-efficient intra-data center coherent links

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Abstract: Coherent optical links are becoming increasingly attractive for intra-data center applications as data rates scale. Realizing the era of high-volume short-reach coherent links will require substantial improvements in transceiver cost and power efficiency, necessitating a reassessment of conventional architectures best-suited for longer-reach links and a review of assumptions for shorter-reach implementations. In this work, we analyze the impact of integrated semiconductor optical amplifiers (SOAs) on link performance and power consumption, and describe the optimal design spaces for low-cost and energy-efficient coherent links. Placing SOAs after the modulator provide the most energy-efficient link budget improvement, up to 6 pJ/bit for large link budgets, despite any penalties from nonlinear impairments. Increased robustness to SOA nonlinearities makes QPSK-based coherent links especially attractive, and larger supported link budgets enable the inclusion of optical switches, which could revolutionize data center networks and improve overall energy efficiency.

1. Introduction

Fiber optic intra-data center network bandwidth has grown rapidly in recent years, and is projected to continue to do so, driving the need for continued optical transceiver performance scaling. As transceiver datarates surpass 1 Tb/s, scaling current pulse amplitude modulation (PAM) intensity modulation direct detection (IMDD) links requires increasing some combination of the baudrate, the number of PAM modulation levels, or the number of parallel fibers/wavelengths. Each of these strategies have significant challenges, and while IMDD may be able to support transceiver datarates above 1 Tb/s, it will soon become preferable to use coherent modulation and detection for high-bandwidth intra-data center links [1].

Coherent links, which can provide 4X increased datarate per wavelength relative to a comparable IMDD system due to polarization multiplexing and in-phase and quadrature (IQ) modulation, have been widely used in long haul and metro network applications, and more recently for inter-data center links below 120 km using the 400ZR standard [2]. Advances in photonic integrated circuit (PIC) technologies and continued scaling of coherent digital signal processing (DSP) application-specific integrated circuits (ASICs) implementation nodes are improving the form factor, cost, and power consumption of coherent links to rival IMDD links for short-reach intra-data center applications. In addition, our recent work has investigated the possibility of using an analog coherent detection (ACD) architecture to perform the DSP functions of carrier recovery and polarization recovery in the optical domain. This approach could remove the need for power-hungry analog-to-digital converters (ADCs) and potentially further improve coherent link power efficiency [3].

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Developing coherent links for short-reach applications requires new design tradeoffs to meet the stringent power efficiency, size, cost, and interoperability requirements for intra-data center links, as opposed to the fiber capacity maximization requirements typical of longer reach coherent link implementations. Already in the 400ZR architecture, module power consumption is reduced by driving the Mach-Zehnder modulator (MZM) with an input swing well below 1 V_π. There have been several proposals for modified DSP implementations targeted for power savings in short-reach coherent links [4,5]. Most notably, chromatic dispersion (CD) is negligible for 50 Gbaud links under 2 km, and thus CD compensation can be bypassed or omitted in the DSP [6]. Higher baudrate links may become more sensitive to CD, limiting their application to shorter reaches, or requiring the re-introduction of CD compensation. Short-reach coherent architectures using analog signal processing [7] or self-homodyne [8,9] techniques to reduce DSP power consumption have also been proposed. The trend of optimization for shorter reach applications will have to continue and be applied to other aspects of the link to enable viable intra-data center coherent links.

The power efficiency of an optical transceiver is not, however, a complete picture of its effect on overall data center power consumption. Advances in the field of optical switching have brought forward the possibility of including passive arrayed waveguide grating routers (AWGRs) or actively controlled optical switches into data center network architectures. There are proposals to replace a layer of electrical switches in current data center architectures with a layer of AWGRs or optical switches, achieving great power savings [10,11]. Additionally, data center network requirements are rapidly morphing with the rise of diverse artificial intelligence and machine learning workloads. This makes real-time network reconfiguration though optical switching especially attractive, as it has the potential to not just save power by replacing electrical switches, but also by increasing server utilization across the data center [12–14]. The potential power savings from this approach is not limited to the portion of overall data center power that is consumed by the network, but by the possible overall improvements in server utilization across the data center. Overall data center efficiency improvement of >2X was projected in [15]. Thus, a critical consideration for supporting future data center growth is not just the power efficiency of the optical links themselves, but also their ability to support the inclusion of optical switches or AWGRs in the network. The available link budget of future intra-data center links is therefore crucial, since optical switches and AWGRs introduce additional losses that need to be accommodated. Coherent receivers have improved sensitivity over IMDD, and coherent links that use QPSK modulation can support greater overall link budgets than comparable IMDD links, making them attractive for optical switching applications [3].

Optical amplification is commonly used in conventional coherent links in the form of erbium doped fiber amplifiers (EDFAs) to extend link reach, and integrated semiconductor optical amplifiers (SOAs) to boost the optical power output of the transmitter (Tx), or to preamplify the signal at the receiver (Rx) [16,17]. In this paper, we present an analysis of optical amplification, namely SOAs integrated with the coherent PICs, as applied to short-reach coherent links. Design tradeoffs between Rx sensitivity, total link budget, compatibility with optical switching, inter-symbol interference (ISI), and link power consumption will be examined, with the goal of outlining short-reach coherent link architectures with optimized power efficiency and viability for implementation in data centers. Optimization for link power consumption gives rise to new design spaces for short-reach coherent links in which shot, thermal, and amplified spontaneous emission (ASE) noise can all contribute substantially to overall noise at the receiver. This hybrid regime contrasts sharply with both conventional coherent links dominated by ASE noise and IMDD links dominated by thermal noise, and thus careful design is required to optimize coherent links for short-reach applications.

Section 2 will describe the various link architectures that will be examined. Section 3 will examine the link performance penalties associated with the addition of optical amplification under

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various architectures. Section 4 will present an analysis of link power efficiency incorporating optical amplification. These results will be compared to other coherent link architectures in Section 5. Concluding remarks will be made in Section 6.

2. Link architecture

The generalized coherent link architecture that will be considered in this paper is shown in Fig. 1, where 5 possible locations for SOAs have been highlighted. The optical components in this diagram can be integrated into a Tx, Rx, or combined PIC using a photonic integration platform such as [18] or [19]. The SOA in position #1 serves to directly boost the Tx laser output power with minimal impairment to the link, since a constant input power will not induce an SOA pattern effect. The principle drawback of using an SOA in this position is that the high input optical power will saturate the SOA gain. In positions #2 and #3, which come after the MZM, the attenuated input signal allows higher SOA gain, but the SOA pattern effect will introduce ISI. In these positions, the SOAs each amplify one of the two polarization channels, since SOAs are typically implemented as single-polarization devices. If wavelength division multiplexing (WDM) is used, as in the ACD-based architecture described in [3], a single pair of SOAs in position #3 can amplify all the wavelengths simultaneously after the multiplexer (MUX). Compared to position #2, this has the potential to greatly reduce power consumption in the SOAs, but will suffer from additional gain saturation, ISI, and crosstalk impairments. Similarly, SOAs in positions #4 and #5, before and after the demultiplexer (DEMUX), respectively, would act as Rx pre-amplifiers. SOAs in either of these positions would benefit from reduced nonlinear effects due to a further attenuated input signal, but would also contribute higher ASE noise at the Rx. Variations or extensions of the architectures considered in this work are also possible.

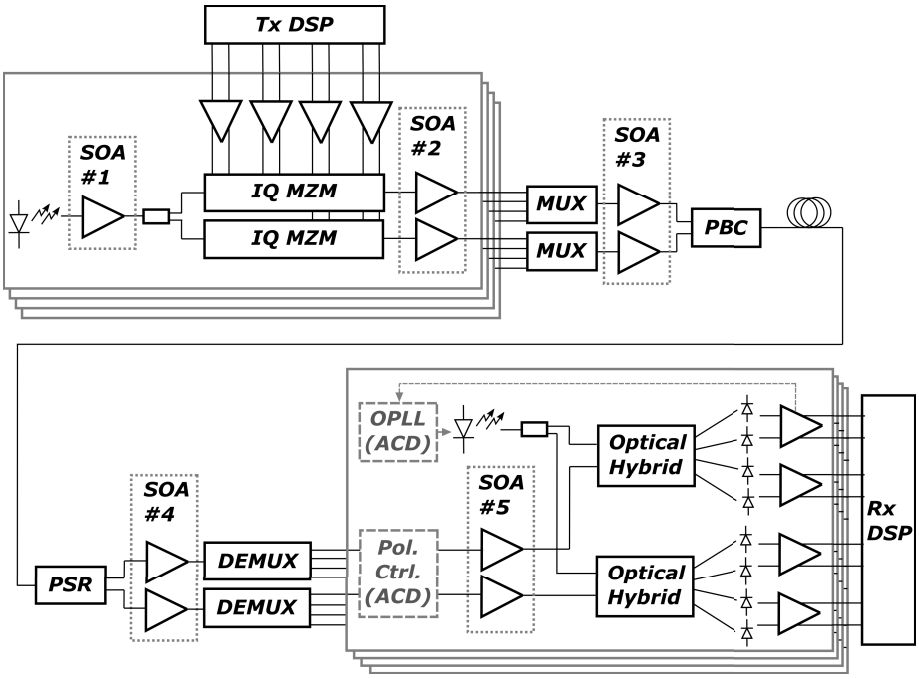

Fig. 1. General coherent link architecture. Boxes labeled SOA #1-5 indicate potential SOA insertion points throughout the link. The optical phased locked loop (OPLL) and polarization controller (Pol. Ctrl.) are used in ACD-based links, but omitted for conventional DSP-based ones.

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In particular, for DSP-based coherent links, unbalanced Tx/LO laser power splitting can be employed to improve link SNR. In the cases of either equal or unequal splitting, the SOA in position #1 could be replaced by two SOA with independent bias points. This approach could improve link budgets relative to the baseline architecture, especially since gain saturation can be reduced in one of the SOAs, but for optimization parameter space simplification it is not considered in this work.

In-line fiber amplifiers are commonly included in longer reach coherent links, but are not considered in this analysis, as power and size requirements for intra-data center applications would be prohibitive compared with SOAs that can be readily integrated with transceiver PICs or packages. Moreover, as will be shown, additional in-line amplifiers are not needed to close short reach coherent links that have <1 dB of fiber losses, even for demanding link budgets that include optical switches.

3. SOA noise and gain saturation

In the architectures proposed here, the ASE noise in the SOAs introduces a current noise at the photodiodes (PDs) dominated by the beating of the LO signal with the SOA ASE noise. The ASE-induced current noise variance when detected at a PD can be expressed as

$$\sigma_{ASE}^2 = 4\mathbb{R}^2|E_{LO}|^2 S_{ASE}\Delta f \tag{1}$$

where $\mathbb{R}$ is the PD responsivity, E_{LO} is the normalized field from the LO, S_{ASE} is the optical power spectral density of the SOA ASE noise, and Δf is the receiver bandwidth. The ASE noise spectral density at the SOA output is calculated from

$$S_{ASE} = n_{sp}\frac{hc}{\lambda}(G-1) \tag{2}$$

where n_{sp} is the population inversion factor of the SOA, hc/λ is the photon energy, and G is the SOA gain [20]. Due to the mixing in the optical hybrid, the ASE-induced noise currents at each differential PD pair are correlated, and the total ASE-induced RMS current noise is $\sigma_{ASE,I} = \sigma_{ASE,Q} = \sqrt{2}\sigma_{ASE}$.

In addition, SOA gain saturates with increasing input optical power, and can be written as

$$G = G_0 e^{-(G-1)P_{in}/P_{sat}} \tag{3}$$

where G is the saturated gain of the SOA, G_0 is the unsaturated or low input power gain of the SOA, P_{in} is the input optical power, and P_{sat} is the saturation power parameter [21]. P_{sat} is an internal parameter that does not correspond directly to either the input or output 3 dB gain saturation points. Static gain saturation would have the largest effect on SOA #1 in Fig. 1, since the optical input power will be the highest directly after the Tx laser.

For SOAs in positions #2-5, instantaneous changes in the power of the modulated signal at the SOA input will cause the saturated gain to fluctuate, inducing nonlinear signal distortions known as the pattern effect and nonlinear phase noise (NLPN). The pattern effect and NLPN have been well studied for IMDD applications [22,23], as well as coherent 16QAM [24,25] and RZ-QPSK [26,27]. A QPSK-modulated signal, which is used in the ACD architecture, has a quasi-constant power envelope where the only SOA input power fluctuations occur during bit transitions. Thus, it is inherently more robust to SOA nonlinearities than IMDD or higher order QAM modulation formats. Empirical characterization of SOA amplification of multi-channel QPSK links in the WDM regime was previously carried out in [28]. In this work, we experimentally investigate SOA nonlinear effects on a single-channel QPSK-modulated link. These results are then used to validate a time-domain SOA simulation model. The optical field at the SOA output is described

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by

$$E_{out}(t) = E_{in}(t)e^{h(t)(1+j\alpha)/2} \tag{4}$$

where $E_{in}(t)$ is the modulated field at the SOA input, $h(t)$ is the instantaneous SOA gain parameter, and α is the SOA linewidth enhancement factor, which describes the relationship between gain fluctuation and the induced NLPN. The instantaneous SOA gain is described by

$$\frac{d}{dt}h(t) = \frac{h_0}{\tau_c} - \frac{h(t)}{\tau_c} - (e^{h(t)} - 1)\frac{|E_{in}(t)|^2}{\tau_c P_{sat}} \tag{5}$$

where h_0 is the unsaturated SOA gain parameter and τ_c is the SOA carrier lifetime [21]. The SOA gain parameter $h(t)$ is related to the total SOA gain by $G = e^{h(t)}$.

In order to confirm this model for QPSK modulation, a coherent link was tested with an SOA (Thorlabs S9FC1132P) biased at 300 mA. The measured G_0 was 23 dB and the P_{sat} was 5 dBm. Measured output constellations for a reference link operating at 10 Gbaud QPSK are shown in Fig. 2 for SOA input power levels between −10 dBm and −22 dBm. For higher SOA input power levels, the SOA NLPN contributes substantial additional phase noise. The measured link results in Fig. 2 were replicated in a simulation that modelled the SOA using the above measured parameters as well as link component bandwidths and shot, thermal, and ASE noise contributions. The SOA carrier lifetime of τ_c = 200 ps and linewidth enhancement factor of α = 5 were estimated from the literature [21]. The measured and simulated root-mean-square (RMS) phase noise characteristics are compared in Fig. 2(e), showing good agreement across SOA input power levels and validating the above SOA analytical model for application to NLPN effects on quasi-constant power envelope QPSK modulation.

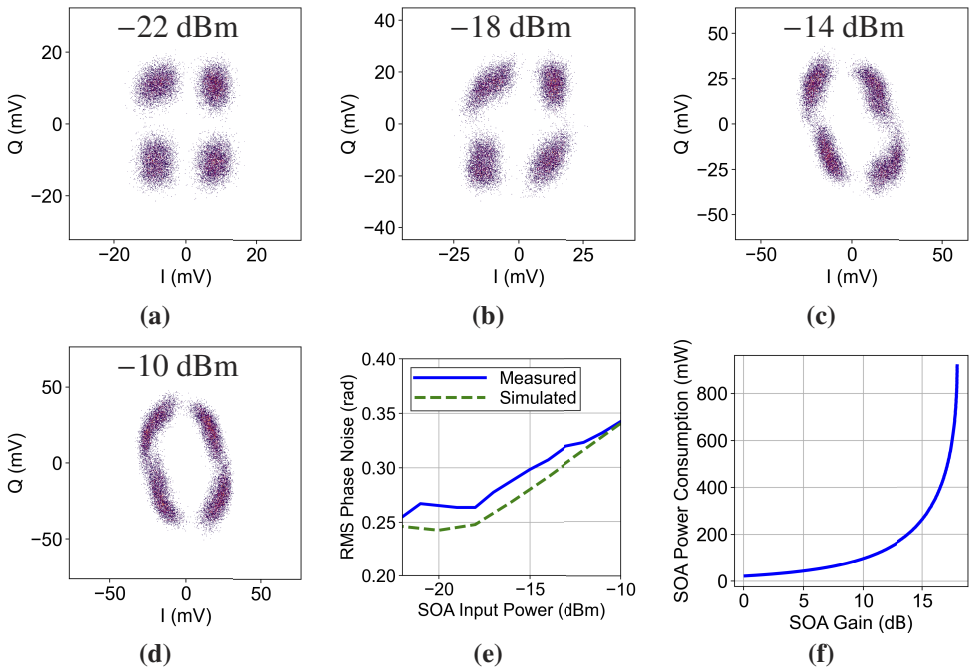

Fig. 2. Measured sampled QPSK constellations depicting the SOA pattern effect and NLPN for SOA input power levels of −22 dBm (a), −18 dBm (b), −14 dBm (c), and −10 dBm (d). (e) Measured vs modeled RMS phase error for various SOA input power levels. (f) Simulated SOA power consumption P_{soa} vs saturated gain G.

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4. Power efficiency optimization

4.1. Simulation model

The performance and power efficiency of the links considered here will now be modelled and compared in simulation. The simulation model incorporates static optical losses of various components, modulation efficiency of the Tx MZM, SOA gain, time-domain simulation of BW effects and SOA nonlinearities, and various noise sources to compute the bit error rate (BER) at the receiver. All the simulations used a full PRBS15 sequence. One of the conclusions of our previous work analyzing short reach coherent links [3] was that for typical ACD links, optimal power consumption was achieved when the Tx and LO lasers were operating at high power, which is limited by laser reliability considerations. Therefore, a constant, realizable integrated laser power of 13 dBm is assumed in this work for both the Tx and LO lasers in ACD-based coherent links. For DSP-based coherent links, a 16 dBm ITLA is assumed, with equal Tx/LO splitting. All BW impairments are assumed to be single-pole low-pass filters. CD and polarization mode dispersion (PMD) are neglected. Nonlinear WDM crosstalk in each SOA is simulated in time-domain with uncorrelated aggressor signals. All of the parameters used in the simulations are shown in Table 1, for both ACD- and DSP-based coherent link configurations. These parameters represent a particular set of assumptions, and differences in actually realized device insertion loss or performance will directly affect the overall link loss budget, and potentially change SOA noise or saturation characteristics, requiring reanalysis. For the parameters and design spaces explored in this work, WDM SOA amplification was found to be an attractive and energy-efficient approach to improving coherent link performance.

The power consumption of the link is optimized by trading off driver output voltage swing and SOA gain in simulation. All other link components are assumed to have a static contribution to the overall link power consumption, which will be considered in Section 5. The driver power consumption is calculated from

$$P_{driver} = c_0 + c_1 \frac{V_{driver}}{Z_0} + c_2 \frac{V_{driver}^2}{Z_0} \tag{6}$$

where V_{driver} is the desired output swing, Z_0 is the MZM impedance, and $c_{1,2,3}$ are coefficients that depend on the driver design and process. In this work, we define the output swing of the drivers in an ACD-based link by the rail-to-rail differential voltage, since limiting electronics may be used in concert with driver output stage peaking circuits. We define the output swing of the linear drivers required for DSP-based links by the peak-to-peak differential voltage, including any peaking from linear equalization. The SOA power consumption is calculated from

$$P_{SOA} = V_d I_{SOA} + R_s I_{SOA}^2 \tag{7}$$

where V_d is the diode voltage drop and R_s is the SOA series resistance. The modeled SOA power consumption vs. saturated gain is shown in Fig. 2(f) for −11 dBm of input power.

4.2. Simulation results

The link simulation was carried out for each of the coherent architectures outlined in Section 2. For each configuration of driver output voltage and SOA gain, the link was simulated multiple times for a full PRBS word with progressively increasing unallocated link budget (ULB), modelled as additional insertion loss on the fiber. The maximum achievable ULB while meeting the target BER was thus characterized for each link configuration. The simulation results for various architectures are shown in Fig. 3, where Fig. 3(a-d) show the combined driver and SOA power consumption vs. the saturated SOA gain G. ACD-based and DSP-based link power consumption are normalized to 200 and 400 Gbps/λ, respectively, ignoring forward error correction (FEC) overhead bits.

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Table 1. Link simulation parameters.

Simulation Parameter	Value for ACD	Value for DSP	Notes
Modulation Format	QPSK	16QAM	
Baudrate	56 Gbaud	60 Gbaud	
Target BER	$3.8 \cdot 10^{-3}$	$1.25 \cdot 10^{-2}$	HD-FEC and CFEC thresholds
Rx Adaptive Equalizer Taps	1	31	No DSP equalization in ACD link
Laser Power on PIC	13 dBm	16 dBm	Integrated for ACD, ITLA for DSP
Laser Splitting	N/A	50:50	
Driver Power Coefficient c_0	0.075 W	0.1 W	Linear driver power fit to commercial driver performance. Limiting driver power fit to performance in [29].
Driver Power Coefficient c_1	0.175 V	−0.375 V	
Driver Power Coefficient c_2	1.225	1.25	
Driver CTLE Peaking	6 dB		
Driver CTLE Frequency	50 GHz		
Driver Bandwidth	40 GHz		
MZM Bandwidth	30GHz		
TIA Bandwidth	40 GHz		
MZM Phase Efficiency V_π	6.7 V		
MZM Z_0	30 Ω		
SOA Carrier Lifetime τ_c	200 ps		
SOA P_{sat}	15 dBm		Fit to performance in [30]
SOA α	5		
SOA n_{sp}	3.5		
SOA V_d	0.88		
SOA R_s	10 Ω		
Operating Wavelength	1310 nm		
Photodiode Responsivity $\mathbb{R}$	1 A/W		
TIA RMS Input Noise	7.2 μA		Fit to performance in [31]
Tx Excess Losses	9 dB		
Mux+Demux Excess Losses	2 dB		Based on performance in [32]
Rx Excess Losses	5.5 dB		
LO Excess Losses	2 dB		
Fiber Loss	1 dB		

Across the simulations, power consumption is generally improved by operating at lower driver swings and higher SOA gains. Figure 3(a) shows the link design space for an ACD-based link with an SOA in position #2, where compensating for reducing driver output voltage by increasing SOA gain results in lower overall power consumption for all ULBs plotted. Further modest improvements in power consumption are achieved by moving from SOAs in position #2 to WDM amplification with SOAs in position #3, as shown in Fig. 3(b) and (d), despite increased input power and crosstalk at the SOA from three other simulated WDM channels. WDM amplification improved power efficiency by a larger amount for the ACD-based architecture than for the DSP-based architecture due to QPSK's increased tolerance to SOA NLPN.

The expected drawback of an architecture with an SOA in position #1 was that the high input power from the laser would saturate the SOA. Indeed, Fig. 3(c), shows that large SOA gains were not attainable, as they were in Fig. 3(a), (b) and (d). This limits the power efficiency of this

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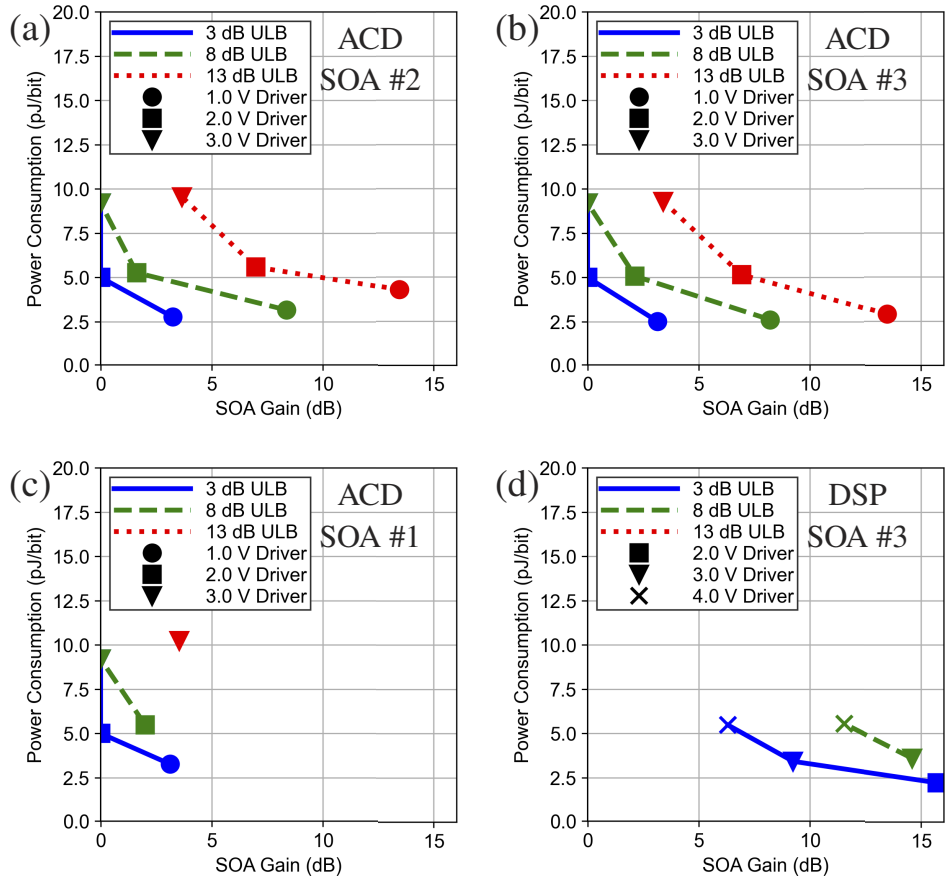

Fig. 3. Driver and SOA Power consumption vs. SOA gain for an ACD-based link with SOA in position #2 (a), #3 (b), and #1 (c), and for a DSP-based link with SOA in position #3 (d), where each curve corresponds to a particular supported ULB, and the differential peak-to-peak driver output voltages are marked.

architecture compared to one with SOAs in position #2 or #3, where the minimally saturated SOA gain enables 6 pJ/bit better power efficiency for link operation at 13 dB ULB. Links with SOAs in positions #4 or #5 were dominated by ASE noise at the receiver that was unattenuated by link losses, and did not see improved performance for the link parameters assumed here.

The shot, thermal, and ASE noise components, referred to the input of the receiver and corresponding to the plotted results in Fig. 3(b) and (d), are shown in Fig. 4(a) and (b), respectively. While the shot and thermal noise levels remain constant, the ASE noise varies strongly with SOA gain. The ASE noise in the DSP-based link simulations was comparable to the receiver shot and thermal noise levels, and the ACD-based link simulations had lower, although non-negligible ASE noise contributions. The power consumption vs SOA gain curves in Fig. 3(c-f) do not reach an optimized minimum, however, because they were limited by the 16 dB maximum gain determined by the SOA model parameters that were chosen for this analysis. A higher-gain SOA design could enable power efficiency improvement with increased ASE noise contribution at the optimal operating point. These results suggest that short-reach coherent links optimized for power efficiency will operate in a hybrid regime in which the shot, thermal, and ASE noise contributions are all appreciable. This is a notable departure from current conventional links, where long-reach coherent links are dominated by ASE noise and short-reach IMDD links

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are dominated by receiver thermal noise. In describing the links that operate in this hybrid noise regime, receiver BER sensitivity can no longer be characterized solely with respect to either received optical power or OSNR, but now requires a combination of both optical power and ASE noise information.

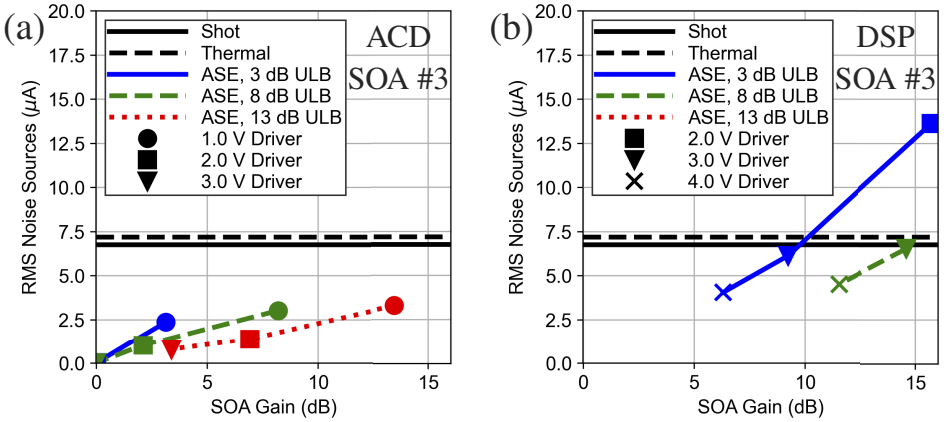

Fig. 4. RMS noise currents at the receiver vs position #3 SOA Gain for an ACD-based link (a) and a DSP-based link (b).

4.3. *Optimization theory*

The simulation results in Fig. 3 were carried out for discrete and somewhat arbitrary driver swing and SOA gain values. Those results showed that driver voltage and SOA gain can be traded off for improved power efficiencies and supported link budgets. Here, we will develop a theoretical model for continuous optimization by examining figures of merit (FOMs) for the driver and SOA link budget improvement per additional pJ/bit of power consumption. Optimal link operation will then be characterized by a set of driver swing and SOA gain operating points where the respective driver and SOA FOMs are equal.

For coherent modulation with an IQ-MZM, the driver swing determines the effective optical loss of the modulator, which is given by the modfactor

$$F_M = sin(\frac{\pi}{4}\frac{V_{driver}L_{mod}}{V_\pi L})^2 \tag{8}$$

where V_{driver} is the differential peak-to-peak driver output voltage swing, L_{mod} is the phase shifter length of one MZM arm, and $V_\pi L$ is the modulator phase efficiency. The modfactor describes the effective loss due to not driving a full $2V_\pi$ in the MZM transfer function. For 16QAM, due to the presence of lower power inner constellation points, the MZM effective loss is degraded by an additional static 2.55 dB. In this analysis, the modfactor loss directly corresponds to reduced available link budget. By defining $P_{driver}(V_{driver})$ as the driver power consumption in pJ/bit for a given driver voltage swing, converting the modfactor to dB, and differentiating, the driver figure of merit can be written as

$$\left.\frac{dF_M}{dP_{driver}}\right|_{dB} = \frac{5\pi}{ln(10)F_M}\frac{L_{mod}}{V_\pi L}sin(\frac{\pi}{4}\frac{V_{driver}L_{mod}}{V_\pi L})cos(\frac{\pi}{4}\frac{V_{driver}L_{mod}}{V_\pi L})\frac{dV_{driver}}{dP_{driver}} \tag{9}$$

where the driver power consumption is modelled as shown in Eq. (6) and the differential is

$$\frac{dV_{driver}}{dP_{driver}} = \frac{1}{\sqrt{\frac{c_1^2}{Z_0^2} - \frac{4c_2(c_0-P_d)}{Z_0}}}. \tag{10}$$

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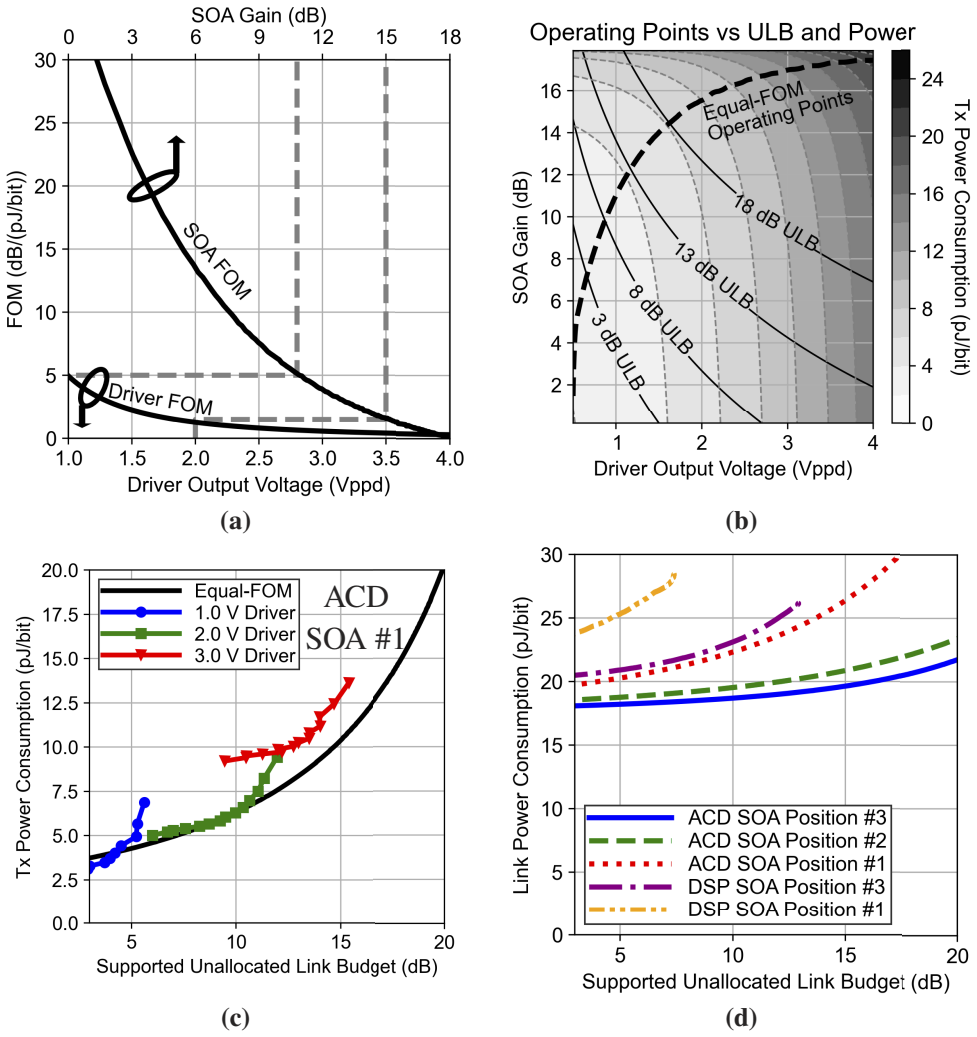

Fig. 5. Driver and SOA FOMs vs output voltage and gain operating points (a). Optimal equal-FOM operating points plotted with Tx power consumption and ULB contours for an ACD-based link with SOA in position #2 (b). Equal-FOM curve for an ACD-based link with SOA in position #1 vs. time-domain simulation results (c). Calculated full-link power consumption vs. ULB for multiple architectures (d).

A similar calculation can be carried out for an $FOM_{SOA} = dG/dP_{SOA}$, following well-known SOA gain and bias relationships [33]. The resulting power consumption and gain relationships are described by Eq. (7) and Fig. 2(f). These FOMs, with units of dB/(pJ/bit), quantify the marginal link budget improvement associated with a marginal increase in power expenditure in either the driver or SOA, enabling a comparison of the efficiency of each component. The final FOMs for the driver and SOA, plotted against the driver voltage swing and the SOA gain, for the parameters assumed in this paper for an ACD-based link, are shown in Fig. 5(a). In agreement with the simulation results in Fig. 3, it is clear that at low SOA gains, the ULB can be increased more efficiently by increasing SOA gain than by increasing driver swing. In fact, the FOM curves show that it is most efficient to raise the SOA gain to 11 dB before raising the driver swing above 1 Vppd, and again up to 15 dB before raising the driver swing past 2 Vppd.

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This reasoning can be extended to form a continuous set of operating points where $FOM_{driver} = FOM_{SOA}$, yielding optimal link performance per watt. This equal-FOM curve is plotted in Fig. 5(b), along with a shaded contour map showing total driver and SOA power consumption and contour lines showing supported ULBs for each operating point. The equal-FOM operating points indeed achieve the minimum power consumption for each desired ULB. This theoretical analysis agrees well with time-domain simulation results for each of the link architectures reported above. The equal-FOM curve for an ACD-based link with and SOA in position #1 was normalized to the link receiver sensitivity and is shown in Fig. 5(c) alongside corresponding simulation results for power consumption vs. supported ULB for different driver voltages. This Equal-FOM analysis accurately describes optimally power efficient driver and SOA operating points, including SOA saturation effects.

5. Architectural comparisons

The results reported above show that integrated optical amplification in various configurations can improve short-reach coherent link power consumption, but the analysis has been confined to the power consumption changes in the drivers and SOAs alone. We will now consider the power consumption of the full link in order to compare the performance across various ACD- and DSP-based short-reach coherent links.

The estimated power consumption of all of the components of a short-reach coherent link, namely the lasers, thermo-electric coolers (TECs), transimpedance amplifiers (TIAs), biasing components, and DSP/CDR (clock data recovery) chips are shown in Table 2 for ACD-based and DSP-based links for two ULB cases. The numbers reported here do not consider any power supply overhead, which can be on the order of 10%. Driver and SOA power consumption was taken from Fig. 3, assuming SOAs in position #3. The DSP ASIC power consumption for the DSP-based coherent link is estimated from 400ZR DSP performance [34] scaled from 7 nm CMOS to 3 nm. DSP ASICs specifically tailored for short-reach applications could further improve power consumption substantially by removing CD and PMD compensation and optimizing equalizer implementations [5]. Since the ACD architecture employs limiting drivers and receivers and does not require polarization recovery or carrier recovery in DSP, power-hungry ADCs and digital-to-analog converters (DACs) can be eliminated and a greatly simplified CDR circuit can be used. Since such an ASIC tailored to ACD-based links does not yet exist, we estimate that it will consume half the power of a conventional coherent DSP chip, but have tabulated scenarios where ACD ASIC power consumption is either 1X, 0.75X, or 0.5X the conventional coherent DSP power consumption. The most aggressive scenario is based on removal of the ADCs/DACs, which account for roughly half the power consumption in the DSP ASIC for 400ZR [35], as well as the removal and simplification of dispersion compensation, equalization, carrier recovery, polarization recovery, and FEC blocks. As coherent DSPs scale to future CMOS nodes, DSP-based links will have more attractive power consumption, albeit with higher ASIC development costs. DSP-based 16QAM links also require half the quantity of lasers, modulators, and receivers as an ACD-based QPSK link with the same overall data rate, leading to cost and size advantages. DSP-based coherent links could also operate with QPSK modulation (for 200 Gbps/λ with 50 Gbaud lanes), yielding similar link budget scaling and SOA noise tolerance as ACD-based links, with the additional improvements of DSP-based equalization. This approach would trade off power consumption, however, since it would require a full coherent DSP ASIC, including power hungry ADCs/DACs and linear drivers and TIAs, which are amortized over half as many bits, and so consume much more power. There are promising efforts to build efficient DSP-based QPSK links by leveraging higher baudrate signalling, laser sharing, and efficient limiting drivers to overcome these hurdles [35]. Full-link power consumption for several link architectures, calculated from optimal equal-FOM operating points derived in Section 4, and including the static contributions in Table 2, are shown in Fig. 5(d). An ACD-based coherent

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link can improve power consumption by 2.5 and 8 pJ/bit over a DSP-based coherent link for 3 and 13 dB ULB, respectively.

Table 2. Full-link power consumption tabulation for short-reach coherent links.

Component	ACD-Based						DSP-Based	
	1X DSP Power		0.75X DSP Power		0.5X DSP Power			
DSP/CDR	10 pJ/bit		7.5 pJ/bit		5 pJ/bit		10 pJ/bit	
Lasers (with cooling)	6.5 pJ/bit						6 pJ/bit	
TIAs	1 pJ/bit						1.5 pJ/bit	
OPLL	1.5 pJ/bit						0 pJ/bit	
Biasing	2 pJ/bit						1 pJ/bit	
ULB	3 dB	13 dB	3 dB	13 dB	3 dB	13 dB	3 dB	13 dB
Drivers + SOAs	2.5 pJ/bit	3 pJ/bit	2.5 pJ/bit	3 pJ/bit	2.5 pJ/bit	3 pJ/bit	2.5 pJ/bit	8.5 pJ/bit
Total (pJ/bit)	23.5	24	21	21.5	18.5	19	21	27

Considering the power consumption of the transceivers themselves, however, does not capture their full impact on data center energy efficiency. The introduction of AWGRs or optical switches has the potential to reduce data center latency, and enable network topologies that can increase server utilization in high performance computing (HPC) and artificial intelligence (AI) clusters, and in the data center overall. These changes, which are only enabled by optical links that support higher link budgets, will directly impact overall data center efficiency. Networks with optical switching save power by reducing the total number of electrical switches and optical transceivers needed in the data center, directly improving effective transceiver energy efficiency by $>2X$ [11]. In addition, the network reconfiguration potential of optical switching is still being explored, but efficiency improvements of $>2X$ for the *overall* data center have been projected [15]. It is clear that modest increases in server utilization can lead to data center power savings greater than the total power consumption of all of the optical transceivers. Thus, optical transceivers that consume more power, but support ULBs that enable optical switching, could still bring about a more efficient overall data center.

As we have seen in Section 4, SOAs are a key enabler of efficient link operation with large ULBs. Links with SOAs in positions #2 and #3 supported higher ULBs than those with an SOA in position #1, despite any ISI penalties due to the SOA pattern effect and NLPN. Furthermore, ACD-based QPSK links are able to support higher ULBs than their DSP-based 16QAM counterparts, in part due to receiver sensitivity and SNR requirements [3], but also in part due to decreased susceptibility of QPSK signals to SOA NLPN. DSP-based SOA NLPN compensation algorithms exist, but come at the expense of additional DSP power consumption and complexity [25].

6. Conclusion

As per-wavelength data rate requirements for short-reach optical interconnects rise, coherent links will become an attractive option for intra-data center applications. The stringent power consumption and cost constraints placed on intra-data center links will require an evolution of conventional coherent link architectures and designs. SOAs integrated with coherent PICs enable link operation with reduced driver output voltages, supporting larger link budgets with reduced power consumption. Positioning SOAs after the Tx modulator results in the most improved link performance, with simulated power savings of 6 pJ/bit shown for a 13 dB ULB. Figures of merit for driver and SOA link budget improvement per additional unit of power consumption were

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proposed and used to derive optimal driver and SOA operating points. For typical operating points, SOAs are more energy-efficient than drivers at increasing the link budget.

While DSP-based coherent architectures using 16QAM modulation benefit from SOA gain, their performance is hampered by SOA NLPN. Due to its quasi-constant power envelope, QPSK-based modulation is more tolerant to SOA saturation effects, making ACD-based coherent links that use power-efficient limiting drivers and TIAs especially attractive for short-reach coherent links with large ULBs. Since optical amplification can efficiently increase the supported link budget, it enables the inclusion of AWGRs or optical switches, which can revolutionize data center networks and improve overall server utilization and energy efficiency. Integrated optical amplification is the key to meeting link performance and energy efficiency targets for intra-data center coherent optical interconnects.

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