Asynchronous 2x2 Optical Packet Synchronization, Buffering, and Forwarding

John P. Mack, Kimchau N. Nguyen, John M. Garcia, Emily F. Burmeister, Matt M. Dummer, Henrik N. Poulsen, Biljana Stamenic, Geza Kurczveil, Kurtis Hollar, Larry A. Coldren, John E. Bowers, and Daniel J. Blumenthal

Electrical and Computer Engineering Department, University of California, Santa Barbara
jmack@ece.ucsb.edu

Abstract: We demonstrate the first asynchronous 2x2 optical packet switch capable of synchronizing, buffering, and forwarding 10 Gb/s packets generated from independent transmitters with better than 99% packet recovery measured using a burst mode receiver.

OCIS codes: (060.1810) Buffers, couplers, routers, switches, and multiplexers; (230.4480) Optical amplifiers

1. Introduction

Optical packet switching provides a means of communication that is flexible, scalable, and high capacity [1]. Asynchronous operation of routers is the key to scaling large networks where multiple independent nodes are used, each with their own packet and bit-level clock sources. This causes inherent timing uncertainties on the clock and packet-level due to the frequency drift between plesiochronous clocks [2]. These uncertainties create unique challenges to optical technologies and switch architectures. In order to utilize synchronous buffer architectures with asynchronous packets, incoming packets must be aligned to the packet timeslots of the switch through the use of synchronizers. Packets are then synchronously loaded and unloaded from buffers to resolve temporal collisions of packets destined for the same output port [3]. Synchronous buffering is a critical component of any router as synchronization guarantees minimal uncertainty of the location of packets within buffers and allows for efficient time division multiplexing of packets onto output ports. In addition to optical buffering, the switch also requires photonic technologies to forward packets to different output ports. Optical synchronization, buffering, and forwarding approaches have been demonstrated individually with low power penalties at 40 Gb/s [4-6]. Previously, asynchronous optical forwarding of labeled optical packets was demonstrated for high bit-rate variable length 40 Gb/s payloads based on lower bit-rate 10 Gb/s labels [7]. End-to-end asynchronous optical transmission, forwarding, and detection have been shown for Internet protocol (IP) packets adapted to a labeled optical packet format for 12.5 Gb/s payloads with 3.125 Gb/s labels [8]. Asynchronous transmission, buffering, forwarding, and detection of 160 Gb/s payloads based on all-optical label processing has also been demonstrated [9]. In all of the previous work, contention of optical packets was pre-engineered using a single transmitter. The results reported here are the first demonstrations of synchronizing, buffering, and forwarding asynchronous optical packets generated by multiple independent sources.

2. Architecture

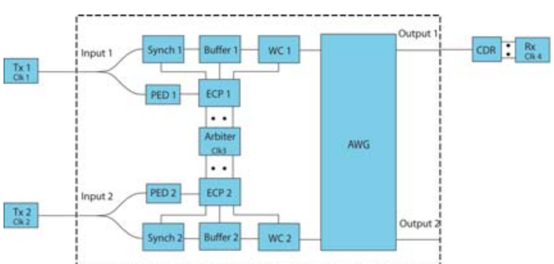

Fig. 1. Asynchronous 2x2 optical packet switch architecture.

Fig. 2. Transmitted packet stream, NRZ format, and packet format.

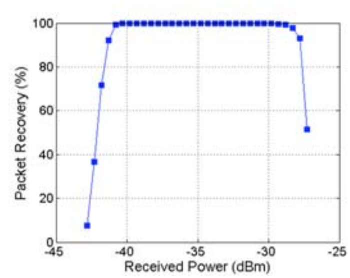

Fig. 3. Asynchronous back-to-back packet recovery measurement.

The asynchronous 2x2 optical packet switch architecture is depicted in Fig. 1. Multiple transmitters (Tx), an optically buffered switch, and a receiver (Rx) operate on independent clocks that are completely asynchronous to one another. The asynchronous FPGA based transmitters and burst mode receiver are capable of generating and detecting 10 Gb/s optical packets [10]. In the following experiments, a PC loads the transmitters with the same data

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stream, which is serialized to a 40 byte NRZ packet at 10 Gb/s with a total period of 128 ns as shown in Fig. 2. The 40-byte packets contain a 32-bit idler for clock recovery, 64-bit unique packet identifier, and repeated PRBS 2^7-1. The fixed timeslots used in the following experiments are 64 ns, which consist of a 40-byte packet and 32 ns of guard band. In this work, it is assumed packets are of fixed size due to the architecture of the implemented optical packet buffer. Packet recovery measurements were conducted for an asynchronous back-to-back experiment and are depicted in Fig. 3. Packet recovery > 99.99% was achieved for > 10 dB dynamic range of received powers. Achieving a large dynamic range for the receiver is critical when detecting incoming packets that have variations in amplitudes and signal to noise ratios.

Synchronization, buffering, and forwarding of 10 Gb/s asynchronous optical packets is performed using photonic integrated technologies. The synchronizers are a 4-stage feed forward design with binary delays based on discrete commercially available SOAs, as shown in Fig. 4 [4]. The synchronizer's resolution is 6.4 ns and the tuning range is 64 ns, as only 10 of the 16 delays are used in the following experiments. The buffers consist of packaged 2x2 InP SOA based switches and fiber delay lines equivalent to 64 ns, as shown in Fig. 5 [5]. The monolithically integrated field modulated wavelength converters consist of a high bandwidth photo detector and electro-absorption modulator (PD-EAM) and a highly tunable sampled grating distributed Bragg reflector (SG-DBR) laser, as shown in Fig. 6 [6]. Payload envelope detectors (PED), electronic channel processors (ECP), and a central arbiter are used for all synchronization, buffering, and forwarding decisions.

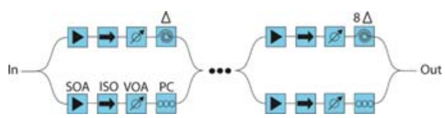

Fig. 4. Feed forward 4-stage optical packet synchronizer.

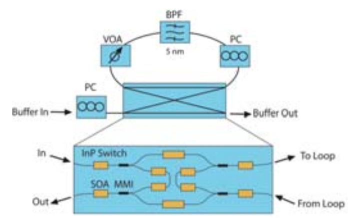

Fig. 5. Re-circulating optical packet buffer with inset of 2x2 InP switch.

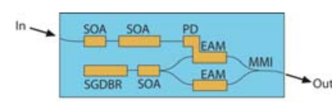

Fig. 6. Monolithically integrated field modulated wavelength converter.

3. Electronic Lookup and Arbitration

Asynchronous optical packets enter the switch fabric and the packet envelopes are extracted using the PEDs, which provide a precise time reference of the rising and falling edges of the packets. The envelopes are clocked into the electronic lookup time domain using D flip-flops in the ECPs running at 156.25 MHz. The ECPs then forward the envelopes to the arbiter for synchronization, contention, and forwarding lookup. The rising edge of the envelope is found and compared to the current count of the timeslot counter. Based on the count, the number of clock cycles needed to delay the rising edge of the packet to the next timeslot is determined. The arbiter generates SOA gating signals to select the delay of the optical synchronizer in order to align incoming optical packets to the local timeslots. The envelopes are then synchronized to the beginning count of the next timeslot and expanded to 64 ns. Next, the arbiter compares the synchronized expanded envelopes from the input ports to determine if contention is present. For this experiment, it is assumed that all packets request the same output port. The arbiter uses a round robin approach to determine which packet from the incoming ports should be buffered. Here, it is assumed that the buffers will only have to either pass a packet through or circulate a packet for one timeslot. The arbiter generates SOA gating signals to latch packets in and out of the buffers. Screenshots were taken for the outputs of the synchronizers and buffers operating asynchronously triggered by the respective transmitter and are shown in Fig. 7 and 8. The packets appear blurred because the delays needed to synchronize and buffer change over time since the transmitters and electronic lookup are asynchronous to one another. The synchronized and buffered packets are then fed into the input of the wavelength converter so that they are forwarded through the AWG. The WCs convert packets to a new wavelength using a highly tunable SG-DBR laser and an EAM that is modulated by the incoming signal. The wavelengths are mapped to the AWG to forward packets to different output ports.

4. Performance Measurements

Packet recovery measurements were conducted for various aspects and configurations of the optical switch, which were compared to the back-to-back measurements. The results of this section can be summarized using a single plot that shows power penalty versus packet recovery at 80, 90, and 99%, as depicted in Fig. 9. This includes asynchronous optical packet synchronization (S), asynchronous synchronization and buffering (SB), and asynchronous time division multiplexing (TDM) with greater than 99.99% packet recovery and minimal power penalties. Asynchronous synchronization, buffering, and forwarding (SBWC) was also demonstrated by placing a wavelength converter on each port and converting synchronized and buffered packets from 1560.5 nm to 1554.5 and

1559.5 nm with greater than 99.8% packet recovery and power penalties less than 5 dB. This also included asynchronous synchronization, buffering, TDM, and forwarding (TDM/WC) where the output of the buffers were coupled and injected into a single wavelength converter under DC biasing converting multiplexed packets from 1560.5 nm to 1554.5 nm and 1559.5 nm with greater than 99.8% packet recovery and power penalties less than 6 dB. Finally this included the asynchronous switch ports that were both TDM and WDM (TDM/WDM) where multiple synchronizers, buffers, and wavelength converters, and an AWG were implemented. Here Tx 1 and Tx 2 were tuned to 1560.5 and 1557.5 nm respectively to utilize multiple input wavelengths. Dynamically synchronized and buffered packets were forwarded to output 1 by tuning WC 1 and WC 2 to 1543.3 nm and 1553.5 nm respectively, as well as, forwarded to output 2 by tuning WC 1 and WC 2 to 1553.7 nm and 1562.9 nm respectively. Packet recovery rates greater than 99% were achieved for both outputs. The power penalties increase in both magnitude and variation as the number of cascaded devices and states increases due to variations in accumulated noise, saturation, insertion losses, and extinction ratios.

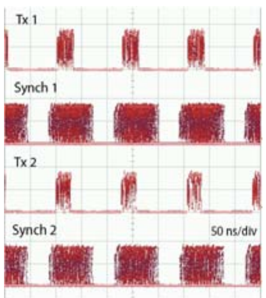

Fig. 7. Screenshots of transmitted and synchronized packets.

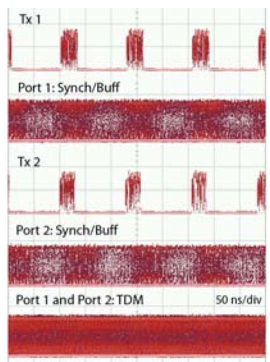

Fig. 8. Screenshots of transmitted, synchronized/buffered, and TDM packets.

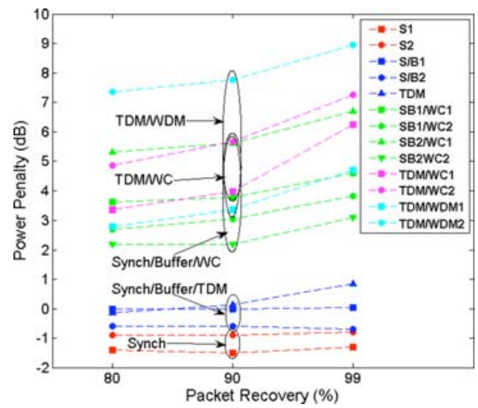

Fig. 9. Power penalty vs. packet recovery for various aspects of the asynchronous optical packet switch.

5. Conclusions

In this work, greater than 99% packet recovery was achieved for a 2x2 asynchronous 10 Gb/s optical packet switch that implemented multiple optical packet synchronizers, buffers, and wavelength converters. The demonstrated optical switch can reach 40 Gb/s with no change to the photonic devices, firmware, or power consumption. The optical switch can scale to 8x8 ports with additional photonic devices, electronics, and firmware updates.

6. Acknowledgement

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