The World's First InP 8x8 Monolithic Tunable Optical Router (MOTOR) Operating at 40 Gbps Line Rate per Port

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Abstract: We demonstrate the first InP monolithic tunable optical router with error-free 40 Gbps operation per port. The device has eight wavelength converters and an 8x8 arrayed-waveguide grating router, yielding more than 200 on-chip functional elements.

OCIS codes: (250.5300) Photonic integrated circuits; (130.0250) Optoelectronics

1. Introduction

Advanced photonic integrated circuits (PIC) in InP are a critical technology for next-generation optical networks [1,2]. In addition to a reduced device footprint and the elimination of component-to-component coupling losses, PICs also provide a path to scale networks to higher bandwidths with a lower power consumption requirement than that of electronic routers. Although devices like advanced transmitters and wavelength converters that exploit these benefits have been realized [3-5], there have only been a few demonstrations of large-scale integration in InP [2].

In this paper, we report on the world's first 8-channel monolithic tunable optical router (MOTOR) operating at 40 Gbps per port. The InP/InGaAsP device integrates an array of 8 tunable wavelength converters (WC) with a low-loss passive 8x8 arrayed-waveguide grating router (AWGR) and functions as a wavelength-based switching element. The MOTOR chip requires a very high level of integration with more than 200 integrated functional elements.

2. Device Design

A schematic of the overall MOTOR chip is shown in Fig. 1a. The details of a single input channel are shown in Fig. 1b. Each individual tunable wavelength converter has a high degree of complexity, consisting of a sampled-grating DBR (SG-DBR) laser, semiconductor optical amplifiers (SOAs), passive phase shifters, an integrated differential delay line, MMIs, and variable optical attenuators. The SG-DBR is operated in the continuous wave regime and consists of five sections: an active gain section, front and back tuning mirrors, a phase tuning pad, and an active absorber. For wavelength conversion, the CW light generated by the on-chip SG-DBR laser is used inside an SOA-based, differentially-delayed Mach-Zehnder interferometer (MZI). In the MZI region, nonlinear (i.e., highly saturable) SOAs are used so that input pulses deplete the carriers in the SOA causing cross phase modulation of the SG-DBR generated light. Additionally, two SOAs are used to amplify the input data signal before the MZI, and two

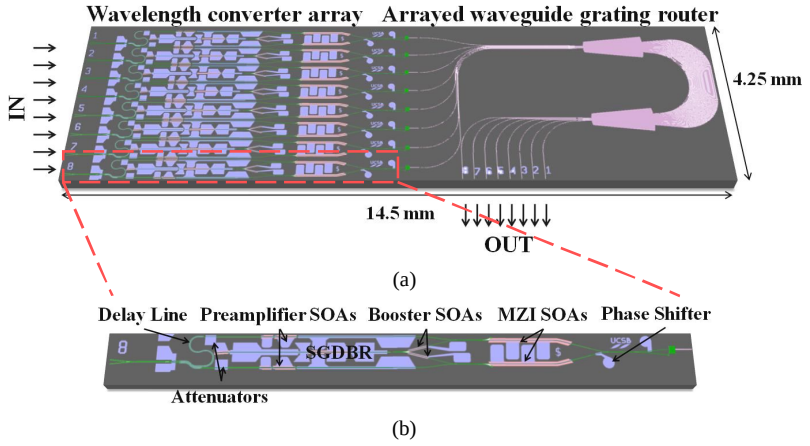

Figure 1. Schematic of the MOTOR chip: (a) overall device; (b) close-up of the wavelength converter design.

SOAs are used to boost the output power of the SG-DBR, one in each branch of the MZI. The differential integrated delay line is used to overcome carrier recovery time limits at 40 Gbps in the MZI SOAs. Low power penalty wavelength conversion at 40 Gbps in the RZ data format using a stand-alone device similar to Fig. 1b was demonstrated previously [3]. The output of the wavelength converter is connected to the AWGR, which passively routes the converted signal based on the new wavelength of the data, as set by the SG-DBR [6].

The integration platform supports both active and low-loss elements using a novel, single regrowth, quantum-well intermixing approach. This platform allowed us to reduce absorption losses in the AWGR and delay line regions by exploiting an undoped InP setback layer in the passive sections of the device [7] while optimizing active functions. The chip has 3 different waveguide types: a surface ridge waveguide design in the wavelength converter section, a high-contrast deeply etched waveguide in the delay line for compactness, and a buried rib waveguide in the AWGR region for low scattering losses. The epitaxial structure consisted of 10 compressively-strained quantum wells (QW) centered in a quaternary waveguide. Quantum-well intermixing was used to blue-shift the band-edge of all passive regions. The completed chip was soldered to a copper mount and held at 16°C during operation.

3. AWGR Performance

The performance of the AWGR was characterized using on-chip light sources and an optical spectrum analyzer (OSA). First, amplified spontaneous emission (ASE) was generated by forward biasing the MZI SOAs on a single WC, and the output of each egress port was fiber coupled to the OSA (Fig. 2a). The free spectral range (FSR) of the AWGR was measured to be 11.1 nm. Next, the MZI SOAs of each WC were biased and the resulting spectrum was measured from a single output port (Fig. 2b). By changing the biasing conditions on the front and back mirrors of the SG-DBR, the laser can be tuned to any of the allowed output wavelengths of a given port in order to achieve full channel switching (Fig. 2c). Lastly, the single-channel crosstalk of the AWGR was found to be 16 dB or more.

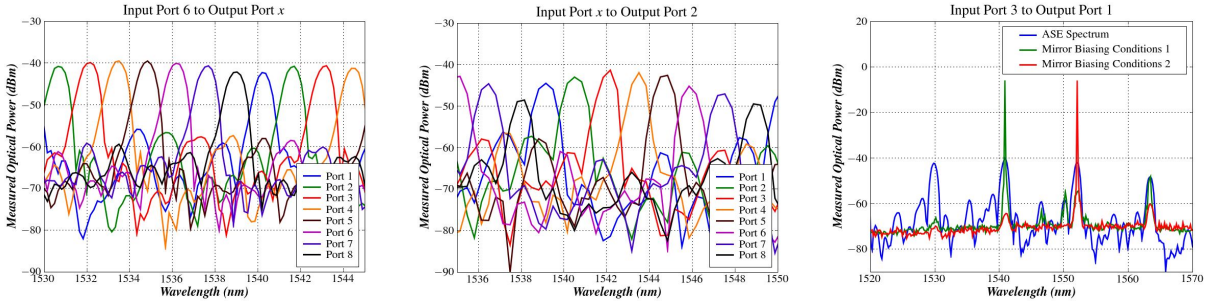

Figure 2: Output response of the integrated AWGR: (a) measured optical output from all output ports using input WC port #3; (b) measured optical output from output port #2 using each input WC port; and (c) lasing spectra for different biasing conditions using the SG-DBR of input WC port #3 superimposed on the ASE spectrum for that channel, all measured from output port #1.

4. Wavelength Conversion and Routing Results

The MOTOR chip was tested during single-channel operation using PRBS 2^{31}-1 data at 40 Gbps. The RZ data signal was amplified with an erbium doped fiber amplifier (EDFA) and was transmitted through an attenuator to control the power level, a 5-nm filter to remove ASE, and a polarizer to ensure TE polarization before it was coupled into the chip. The fiber-coupled output was passed through a 5-nm filter to remove the original input signal and was transmitted to a preamplified receiver. Bit-error-rate (BER) measurements were made using a 40 Gbps SHF BERT.

Fig. 3 shows the BER and eye diagrams for multiple input channels while monitoring a constant output port (Input WCs #1 and #5 each had a ridge defect near the MZI, and Input WC #2 had a shorted preamplifier and thus data are not shown for these channels). Additionally, Fig. 4 shows the BER results for two different output ports using a constant input channel and open eye diagrams for all eight output ports. These results indicate error-free operation. The measured power penalties at a BER of 10^{-9} for the conversion and routing process range from approximately 4.3 to 6.9 dB (depending on the input port).

The noise floor and high power penalty are likely attributable to two main factors. First, the tested MOTOR chip was not antireflective (AR) coated. Given the high output powers of the centered gain regions, it is probable that minor reflections exist in the device during operation. Second, to minimize regrowth quantity and complexity, the input preamplifier SOAs are made from the centered QW band-edge. Because there is a relatively high modal overlap with the centered wells, the output saturation power of the SOA is low. In order to provide enough gain to

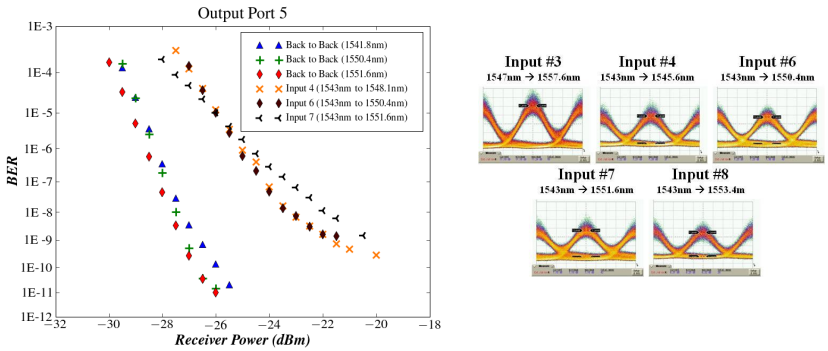

Figure 3. 40 Gbps BER measurements and eye diagrams for various input ports monitored at output port #5.

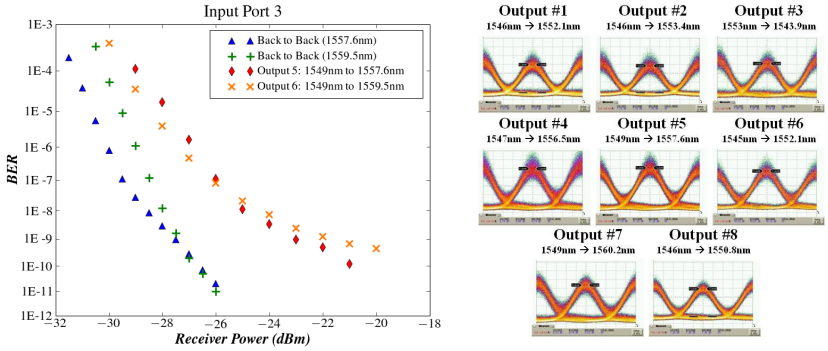

Figure 4. 40 Gbps BER measurements and eye diagrams for input port #3 and various output ports.

the input signal to deplete the MZI SOAs of carriers and modulate the MZI, the preamplifier SOAs had to operate in the nonlinear regime. This resulted in pattern distortion effects and an increased BER. Future MOTOR designs with AR coatings and an optimized preamplifier structure with combined centered and offset QWs are planned to address these issues.

5. Conclusion

We report demonstration of the world's first InP 8x8 monolithic tunable optical router (MOTOR) capable of error-free 40 Gbps operation per port. The device represents one of the most densely-integrated InP chips ever reported, with more than 200 integrated functions and power penalty as low as 4.3 dB at 40 Gbps. Improved power penalty is expected with future designs employing AR coatings and optimized preamplifier SOAs.

6. Acknowledgements

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7. References

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