8-channel InP Monolithic Tunable Optical Router for Packet Forwarding

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Abstract: Advancements in photonic integration allow development of complex, large-scale circuits suited for future optical packet switched networks. We review our 8-channel InP monolithic tunable optical router chip capable of 40 Gbps operation per port.

OCIS codes: (250.5300) Photonic integrated circuits; (130.0250) Optoelectronics

1. Introduction

Optical packet switching (OPS) is a potential option to deal with the increasing power demands of future networks as data rates scale [1]. If packets at a router node remain in the optical layer, many of the power-consuming optical-to-electrical and electrical-to-optical data conversions could be eliminated. In order for OPS to become competitive with traditional electronic routers, the functions of dynamic buffering, wavelength conversion and packet forwarding must be available in low-power, multi-channel, small-footprint photonic modules. Large-scale photonic integration has emerged as a commercially viable approach that may be able to meet these demands in the near future [2].

In this paper, we review our 8-channel monolithic tunable optical router (MOTOR) chip designed for optical packet forwarding at a data rate of 40 Gbps per port [3]. This device demonstrates the switching core of a label-switched optical router (LASOR), developed at UC Santa Barbara [4]. The InP/InGaAsP device combines more than 200 functional elements in a single chip and consists of an array of 8 widely-tunable wavelength converters (TWC) with a passive 8x8 arrayed-waveguide grating router (AWGR). Single-channel error-free wavelength conversion and switching has been demonstrated with the device at bit-error rates below 10^{-9}.

2. Device Design

As shown in Fig. 1, the MOTOR chip replaces an array of discrete tunable wavelength converters and a discrete AWGR in the LASOR architecture. Several different monolithic approaches to 40 Gbps wavelength conversion have been realized in the past few years, but these were typically single-port devices [5-7]. Because MOTOR combines eight independent channels on the same chip, we use an SOA-based approach to wavelength conversion similar to [5] as it is simpler to fabricate. However, these TWCs still have a high degree of complexity, each consisting of a sampled-grating DBR (SG-DBR) laser, semiconductor optical amplifiers (SOAs) with different desired levels of linearity, passive phase shifters, MMIs, and variable optical attenuators (Fig. 2). Unlike the 8x8 routing switch of [8] that was limited to only 10 Gbps per port, our TWC architecture incorporates an integrated differential waveguide delay line in each channel to enable operation at 40 Gbps. However, this delay line creates a switching window that requires an RZ data modulation format at high-speeds.

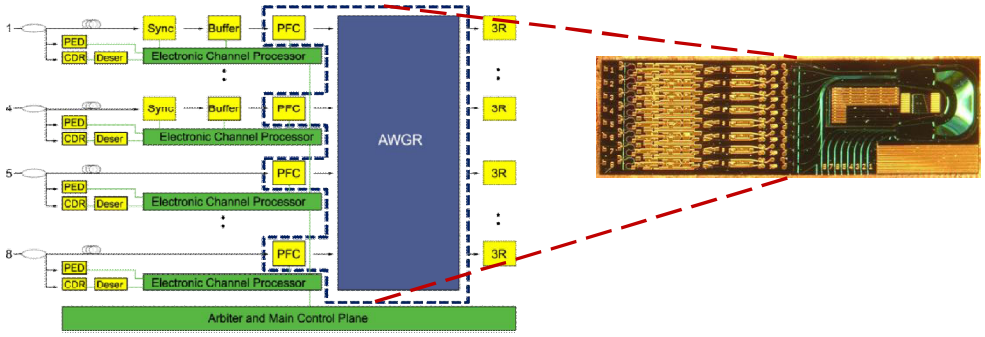


Figure 1. Schematic of the LASOR router. The discrete array of 8 WCs and the AWGR can be replaced by a single MOTOR chip.

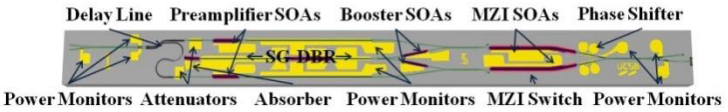


Figure 2. Schematic of a single MOTOR input TWC showing monolithic integration of many "off-the-shelf" components.

The photonic integration scheme used for the MOTOR chip was designed with a view towards fabrication simplicity. Because yield was our major concern, we sought to minimize the process risk wherever possible. Inevitably, this means not all device components can be simultaneously optimized. Future improvements to device performance are therefore possible with more complex integration platforms, which are more suitable to an industrial environment and require better process control. Our device employs a robust quantum-well intermixing technique to create active and passive band-edges [9] and only one epitaxial regrowth to clad the waveguide. We also use 3 different waveguide architectures across the chip to better optimize particular functions and components. This includes a surface ridge waveguide in the wavelength converter section, a high-contrast deeply etched waveguide in the differential delay line region, and a buried rib waveguide in the AWGR region.

3. Device Performance

The fabricated chip was soldered to a copper block and held at a constant temperature of 16°C during operation. The performance of the AWGR was measured using SOAs within the TWCs as on-chip amplified spontaneous emission (ASE) sources. First, SOAs in a single TWC were forward biased and the output of each egress port of the AWGR was fiber coupled to an optical spectrum analyzer (OSA) (Fig. 3a). We measured a well-defined response with an average channel spacing of 1.36 nm, corresponding to 173 GHz at 1536.2 nm (the design target was 200 GHz). The free spectral range (FSR) for the 8-port router was measured to be approximately 11.1 nm and the single-channel crosstalk was between -15.8 to -20.9 dB across all eight output ports. Next, the SOAs of each TWC were biased one at a time and the spectrum was measured from a constant output port (Fig. 3b). This measurement shows some deviation in crosstalk performance between different TWCs, likely due to fabrication variations across the device. With the AWGR response mapped, we then demonstrated the switching capacity of the device by tuning the SG-DBR signal to each of the different allowed output wavelengths of a given port (Fig. 3c).

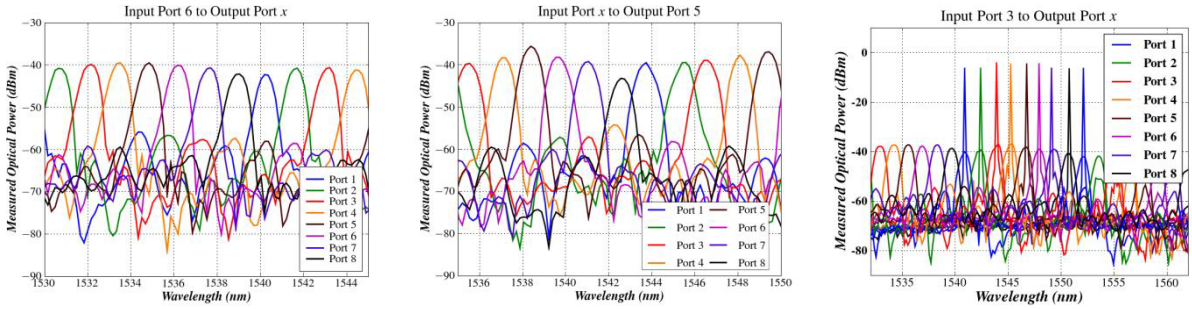


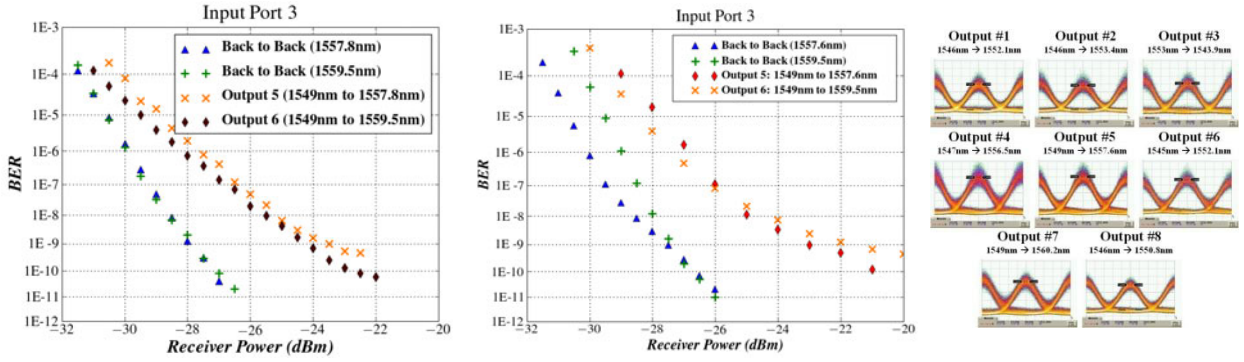
Figure 3: (a) measured AWGR response to ASE from input WC port #6 at each output port; (b) measured AWGR response at output port #5 from each input WC port; and (c) lasing spectra at different SG-DBR biasing conditions (the ASE spectrum for that channel is superimposed).

The wavelength conversion and routing capacity of MOTOR were next tested using a single input channel. The LASOR router is designed to operate with 40 byte packets, but we used longer PRBS data streams at 40 Gbps to better gauge device performance. The initial RZ data pattern was generated and amplified off-chip and then transmitted through an attenuator (to control the input power level), a 5-nm filter (to remove ASE from the EDFA), and a polarization controller (to ensure TE polarization) before it was coupled into the chip. The fiber-coupled output signal was passed through a 5-nm filter to remove the original input signal and was then transmitted to a preamplified receiver. Bit-error-rate (BER) measurements were made using a 40 Gbps SHF BERT.

Fig. 4a shows the BER for wavelength conversion and routing of a 2^7-1 PRBS using a single input channel at multiple output ports. Power penalties as low as 3.5 dB at a BER of 10^{-9} were measured. The pattern length was then increased to 2^{31}-1 bits (Fig. 4b) and power penalty increased to 4.5 to 7 dB depending on the input/output port combination used. A noticeable error floor is apparent at low BERs with longer pattern lengths but open eyes were still obtained for all output ports. This increased power penalty is believed to be the result of nonlinearities in

preamplifier SOAs at the front-end of the WCs. These SOAs are used only to amplify the input data signal prior to wavelength conversion and hence should be linear. In the future this could be overcome by adjusting our integration platform to enable highly linear SOAs or lower loss optical waveguides to reduce the required input power level.

Under normal operating conditions, the single-channel drive power of the device is less than 2 W. An additional ~0.5 W was required for TEC cooling. This translates into an overall power consumption of 0.0625 W/Gbps. The TEC demand and overall drive power will increase with multiple channels running, but it unknown how this will scale. Thermal crosstalk between channels could also lead to higher required bias levels.



(a) (b) (c)

Figure 4. Single-channel BER measurements at: (a) 2^7-1 data rates; (b) 2^{31}-1 data rates; and (c) open eye diagrams at 2^{31}-1 data rates.

4. Future Implementation

These results suggest the future potential of a label-switched router architecture with a switch fabric based on photonic ICs. However, there are still hurdles to reach a commercial technology maturity level. For instance, reduction in power consumption is still needed to make our approach competitive with electronic routers. From the perspective of the MOTOR chip, efforts to improve our metallization schemes indicate we can appreciably reduce our probe pad contact resistance to lower our drive power. Furthermore, implementing an optimized packaging scheme can help with heat sinking to reduce the TEC drive requirements. This will be especially important for multi-channel operation where thermal crosstalk will impact performance.

5. Acknowledgements

This work was funded by DARPA MTO and the Army under the DOD-N LASOR Project (W911NF-04-9-0001). Fabrication was done in the UCSB nanofabrication facility, part of the NSF funded NNIN network.

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