QPSK Transmitter Photonics Integrated Circuit (PIC) with Integrated Micro-Transfer-Printed EAMs and Custom Driver Compatible with 3D Integration

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2023 IEEE 73rd Electronic Components and Technology Conference (ECTC) | 979-8-3503-3498-2/23/$31.00 ©2023 IEEE | DOI: 10.1109/ECTC51909.2023.00127

***Abstract*—We present a 64 Gb/s O-band Quadrature Phase Shift Keying (QPSK) coherent transmitter, consisting of a silicon photonic transmitter (TX) integrated with micro-transfer printed (MTP) InP electro-absorption modulator (EAM) and a differential driver. We also show a co-designed flip-chip compatible electronic integrated circuit (EIC) and the photonic integrated circuit (PIC) based on the previous design.**

Keywords—coherent transmitter, data center, QPSK, MTP, flip-chip

I. Introduction

With the increasing amount of network traffic within data centers, the demand for higher bandwidth and better energy efficiency is growing. Coherent technology is a promising approach to meet these requirements for intra-data center links (<2km), by introducing another degree of freedom for modulation. Additionally, it has higher spectral efficiency and improved sensitivity. A completely analog coherent scheme improves energy efficiency further by eliminating the need for analog-to-digital converters (ADC) and digital signal processing (DSP).

The silicon photonics integrated circuit (PIC) is widely used and becoming more attractive due to its mature process technique and low cost. Because of silicon's material properties, it is challenging to modulate light efficiently and reach higher speeds with low voltage swings. MTP brings the III-V coupon, which has a better modulation performance, onto the silicon platform. By taking advantage of both the III-V and Si platforms, the PIC can be more efficient with a smaller footprint. Moreover, it enables flip-chip integration between the EIC and the PIC. Therefore, these improvements can increase the bandwidth due to the reduction of parasitic capacitance and inductance and better signal integrity.

This paper presents a complete O-band coherent optical transmitter consisting of a coherent TX PIC with MTP EAMs fabricated on the Rockley platform and wirebonded to an EIC. The TX shows good performance up to 64 Gb/s. The co-design for the flip-chip EIC and PIC is then presented.

II. Platform and Packaing Design

The design of the QPSK transmitter (TX) photonic integrated circuit (PIC) is based on the Rockley Photonics silicon photonics technology. Key advantages of the Rockley Photonics multi-micron waveguide platform are relaxed fabrication tolerance for the silicon photonic devices with larger waveguides and integration of III-V actives achieved by attaching fully-processed known-good-die III-V devices in a recess in the silicon waveguide layer and performing edge coupling. In this work, QPSK Transmitter PICs made in the Rockley platform with MTP InP EAMS were wirebonded to GlobalFoundries EIC with current and future packaging methods including: wirebonding, flip-chip, and custom high-speed Rogers printed circuit board (PCB).

A. Multi-Micron Waveguide with integrated III-V actives

Multi-micron silicon over insulator (SOI) is used in the Rockley silicon photonics platform. The multi-micron rib waveguide enables 0.18 dB/cm propagation loss while maintaining polarization independence. Moreover, its mode size is closer to that of the III-V device, which enables low coupling loss and larger alignment tolerance. Consequently, simpler edge coupling is possible without the need for tapers and spot-size converters [1].

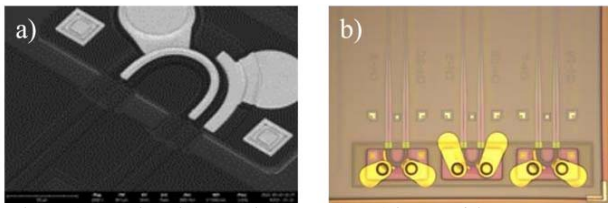


Fig. 1. a) Scanning electron microscope (SEM) image of the MTP EAM. b) MTP EAM with redistribution layer (RDL).

B. Micro-Transfer Printed EAM U-bend EAM

Previously, 106 Gb/s per channel was demonstrated on a Rockley's flip-chip-bonded U-bend EAM [2]. However, the non-planar topography after flip-chipping constrains the integration between the EIC and the PIC. Thus, Rockley developed a micro-transfer printing technique to integrate III-V devices onto a silicon substrate without substantially affecting the fabrication process flow [3]. MTP is a method of integration of III-V active devices in the form of thin coupons compatible with wafer planarization, micro-bumping, and 3D integration of electronics. This approach is particularly well suited for maximizing the high-speed performance of high-speed modulator, owing to the minimization of electrical interconnects

The information, data, or work presented herein was funded by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DE-AR0001273.

2377-5726/23/$31.00 ©2023 IEEE
DOI 10.1109/ECTC51909.2023.00127

and associated capacitance and parasitics. MTP also facilitates high integration densities and high throughput compared to flip-chip bonded devices. The low profile nature of the device coupons allows for tight packing, and stamp-based MTP printing process can print many coupons simultaneously [4]. The Rockley high-speed transmitter platform features InP U-bend EAMs with a 60 µm diameter. U-bend EAM coupons are bonded via micro-transfer printing into the waveguide cavity of the Si wafer, where the thin coupons sit flush with the wafer surface. Electrical connections are made after MTP in the standard wafer-level build-up process. As a result, the InP EAMs are planarized with the PIC without protrusion. Fig. 1 a) shows the planar surface topology with MTP EAM. The planar surface facilitates the flip-chip of the EIC onto the PIC. Additionally, the integration of the EAM onto the PIC allows for shorter electrical connections, thereby reducing parasitic capacitance and inductance. Fig. 1 b) shows MTP EAMs with the redistribution layer (RDL) on the silicon substrate. III-V devices transfer printed onto a silicon platform enable a smaller footprint and more efficient optical modulation compared to their silicon counter parts.

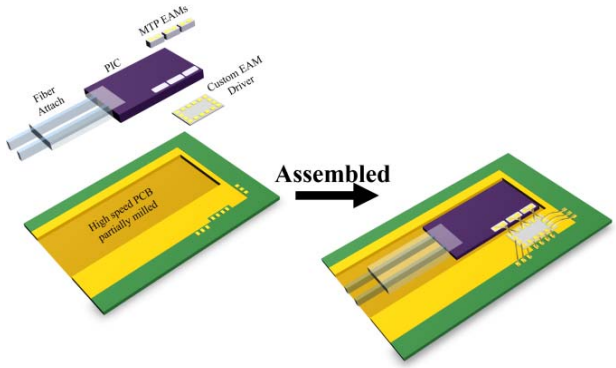


Fig. 2. The schematic of the 2D integration with wirebond.

C. 2D Integration with Wirebond

Wirebonding is a common approach for packaging. The EIC is placed next to the PIC, and electrical connections are made using pressure and ultra-sonic vibration to bond gold wires to the aluminum pads. The wire induces parasitic inductance which increases with length and can decrease the system bandwidth. To shorten the wirebond length between the EIC-PIC, as shown in Fig. 2, the carrier PCB is partially milled to match the height of the PIC and EIC. However, short wirebonds are only attainable to a single row of pads on the PIC edge adjacent to the EIC. Therefore, the number of high-speed connections on the PIC is limited by the width.

D. Flip-chip EIC on PIC for 3D integration

Flip-chipping the EIC onto the PIC provides a shorter electrical connection between the EIC and PIC compared to wirebonding. As shown in Fig. 3, further planarization and wafer-level bumping of Cu pillars (CuP) on the PIC is performed after transfer printing of the EAM coupons using Rockley's back-end-of-line wafer processing. Further details are described in Section IV-B. The EIC can then be diced and chip-level bonded to CuPs. A packaging interconnect length of ~100 µm, equal to the pillar bump pitch, can be assumed, resulting in a ~70% reduction compared to wirebonding [5]. With less parasitic inductance, higher speed can be achieved. High-speed devices can be scaled up and have more flexibility in placement. Nevertheless, the dimension for the PIC must be large enough to mechanically support the EIC. Also, additional traces are needed on the PIC to route EIC electrical signals to bondpads for wirebonding to the PCB.

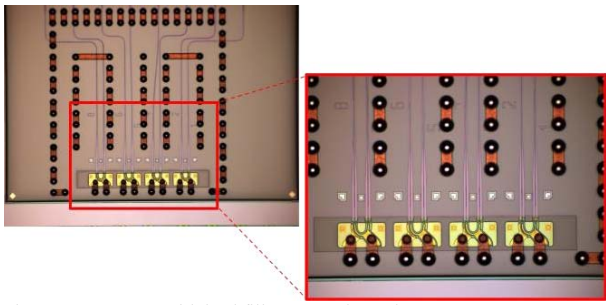


Fig. 3. MTP EAMs with backfill, RDL and CuP bump.

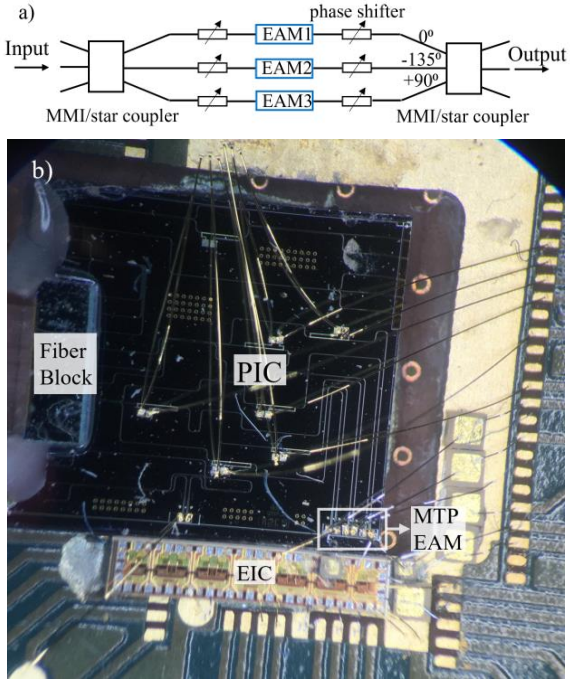


Fig. 4. a) Schematic of the PIC design. b) Assembly of the wirebond TX.

III. Wirebond TX Design and Measurement

The O-band coherent optical TX described below has been measured up to 32Gbaud QPSK operation. The PIC was fabricated in the Rockley silicon photonics platform with three MTP EAMs in a 260- µm pitch. The EIC was fabricated in the GlobalFoundries 130 nm BiCMOS 8XP process. The EIC and PIC are packaged on a custom FR-4 PCB [6] where all electrical connections are wirebonded.

A. Coherent TX PIC Design

The TX PIC design originates from the three-arm interferometer. Two outer arms have a 90° phase difference

while the center arm has a 135° phase difference from both the outer arms. There are two phase shifters in each arm, which are biased to achieve this phase relation [7]. The three-arm design requires the outer to center power ratio to be 2:1 to achieve a symmetrical QPSK constellation. The MTP EAM in the center arm is biased by DC voltage to attain the required optical power ratio. The high-speed signal, amplified by the GlobalFoundries EIC, modulates the two EAMs on the outer arms. This results in a QPSK constellation at the output of the transmitter. Fig. 4 shows the schematic of the PIC design and a photo of the assembly.

B. Measurement

Fig. 5 shows a schematic of the measurement setup. Light from an external cavity laser (ECL) is split with 90% going to the LO port of the commercial reference receiver (RX) through a polarization controller (PC) and a 20-meter. The remaining 10% goes through a semiconductor optical amplifier (SOA) and a PC, which is then coupled to the TX PIC for modulation. The modulated light is sent to the commercial reference RX after being amplified by the praseodymium-doped fiber amplifier (PDFA) and passing through a PC. The measurement is taken with 1290 nm laser wavelength to match the EAM absorption at 75 °C. Two streams of PRBS15 pattern decorrelated by a bit delay were used to drive the outer two EAMs of the Rockley TX.

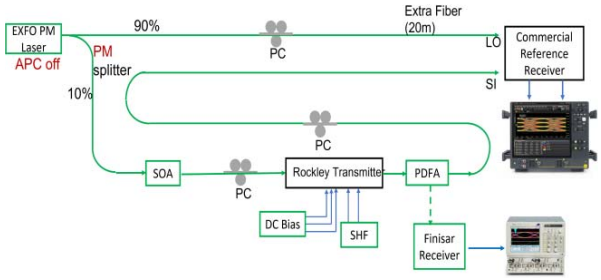
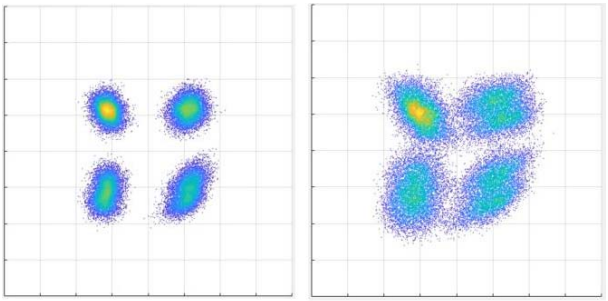


Fig. 5. Schematic of the wirebond TX measurement setup.



a) b)

Fig. 6. Constellation diagram a) 25 GBaud, 0 errors in 65600 bits b) 32 GBaud, BER=7.9X10^{-3}.

A MATLAB script was used to control the real-time oscilloscope and process data. To correct for random phase rotation due to the measurement setup, all the data points in an acquisition record are rotated by the same angle to produce a square QPSK constellation. Constellation diagrams were constructed using at least 32800 symbols, representing a full cycle of the PRBS15 pattern.

Constellation diagrams and BER at different bit rates are shown in Fig. 6. Fig. 6 exhibits 7.9x10^{-3} BER at 32 GBaud, which is below the SD-FEC BER limit (2x10^{-2}). The result showcases Rockley's ability to transfer III-V coupons with a tight pitch without diminishing the devices' performance. Additionally, the constellation shows that complex modulation is attainable using MTP EAM arrays and future work is focused on improving the packaging to push Rockley's MTP EAM technology to faster speeds.

IV. Driver Co-design and Flip-chip

Planar surface topography after MTP enables the next level of integration: flip-chip between the PIC and EIC. The design of the flip-chip can be broken into two sections: 1) driver co-design and measurement, 2) flip-chip PIC design, and 3) the assembly of the flip-chip.

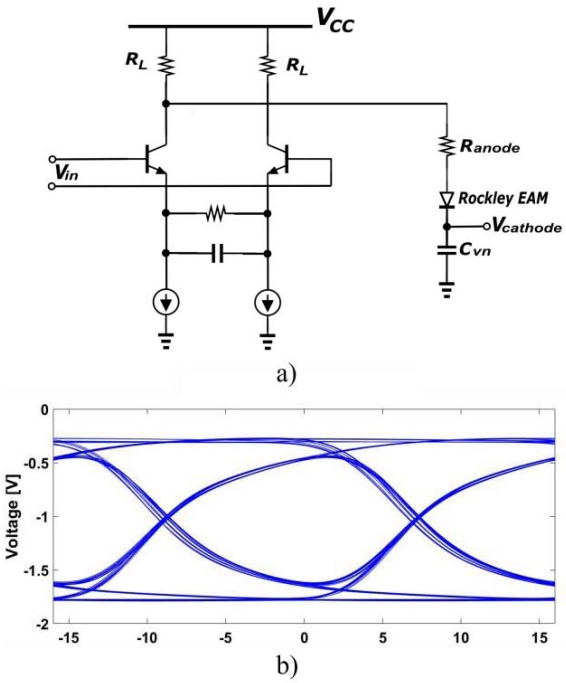


Fig. 7. a) Generalized schematic of co-designed driver b) Co-simulation eye diagram at 60 Gb/s of the driver and EAM circuit model with 50 ohm R_L and 35 ohm R_{anode}.

A. Driver Co-design and Measurement

The driver was fabricated on GlobalFoundries 90 nm BiCMOS 9HP process. Fig. 7 a) shows a generalized schematic of one channel of the co-designed driver for the Rockley InP EAM. It's a two-channel cascode differential driver with differential input and single-ended output. Power supplies and biases are shared between two channels. Each channel drives one EAM's anode. An on-chip resistor is added between the driver output and EAM anode to damp the oscillations caused by impedance mismatch and parasitic inductance. On-chip decoupling capacitors are also used for the cathode bias when co-designing the driver. Load resistance and anode resistance values were chosen, based on the co-simulation of the driver

and the EAM circuit model. Fig. 7 b) shows the eye diagram from the co-simulation at 60 Gb/s.

Fig. 9 shows the measurement setup, assembly, and eye diagram for the driver's standalone electrical-in electrical-out (EE) measurement. The driver is assembled on a test platform which operated up to 108 Gb/s [6]. Although Fig. 9 shows the measurement result of one channel, it can represent the output from both channels since the two channels are mirrored in design and should provide similar results. The driver showed good performance up to 70 Gb/s. We were able to get about 74 mV voltage swing at the single-ended output, after 20 dB of attenuation, with 500mV$_{pp}$ differential input. Since the driver is optimized for operation with EAMs as load, we expect it to perform better with EAMs as load, we expect it to perform better with EAMs than with 50-ohm load in this measurement.

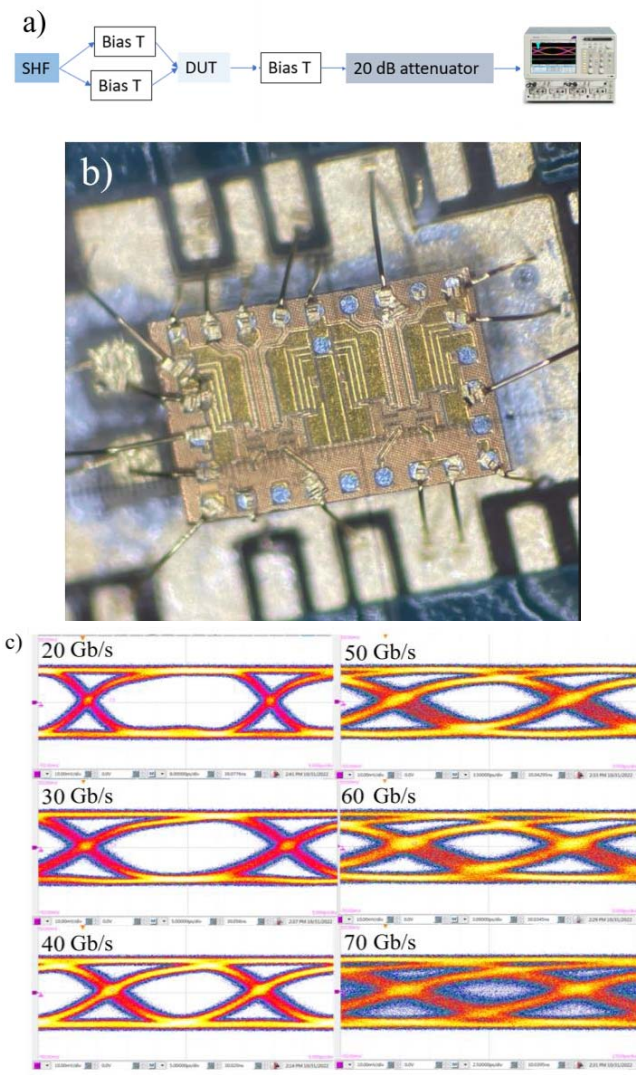


Fig. 8. a) Driver standalone EE measurement setup b) Assembly for the 50 ohm R_L, 50 ohm R_{anode} driver standalone test c) Output eye diagram of the 50 ohm R_L, 50 ohm R_{anode} driver at different bit rates.

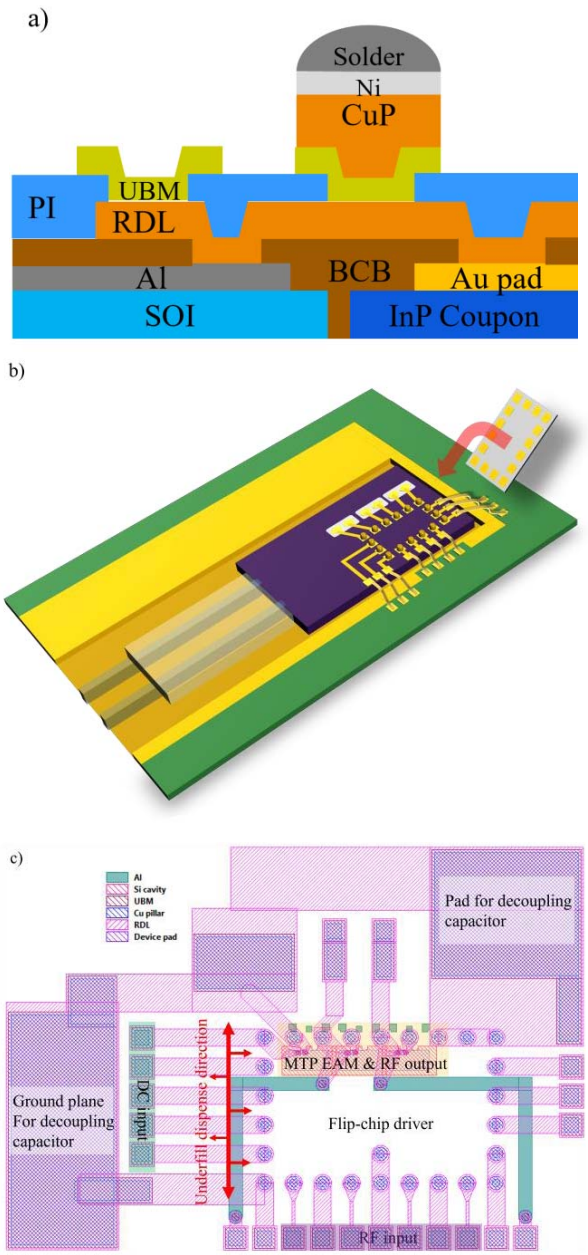


Fig. 9. a) Schematic of the metal stack for EIC flip-chip b) Schematic of the EIC flip-chip onto the PIC c) Metal traces design for EIC flip-chip.

B. Flip-chip PIC Design

In this flip-chip PIC design, we kept the photonic design consistent with the previous design seen in section III-A but added BCB planarization, metal routing, and Cu pillars using Rockley's back-end processing for flip-chip compatibility with the custom GlobalFoundries driver. Fig. 9 a) shows the metal stack for the flip-chip. Al and RDL layers were used for electrical routing. Fig. 9 b) is the schematic of the flip-chip assembly. Fig. 9 c) shows the metal routing layout for the driver flip-chip. Bondpads on the PIC, which are wirebonded to the PCB, on the PIC are routed to the driver's inputs through metal

traces. The output of the driver is connected to the EAM through the Cu pillar and short metal trace. Large pads are designed for wirebondable decoupling capacitors. Fig. 3 shows the MTP EAMs with backfill, RDL, and CuP bump. They were characterized and no degradation in DC and RF performance was observed.

C. Flip-chip Assembly Process for 3D integration

The flip-chip assembly process involves die-level bumping of the driver EIC followed by EIC dicing, then flip-chip bonding to the PIC, followed by reflow. To make the whole assembly mechanically reliable, underfill will be dispensed and cured as the final flip-chip step. The fiber block will be attached using UV epoxy to minimize misalignment during flip-chip bonding. Wirebonding will be done before the underfill dispense or after, depending on the underfill fillet. A large fillet could potentially cover the bondpads.

V. Conclusion

In this paper, we achieved 64Gb/s QPSK transmission with a coherent TX based on MTP EAMs fabricated in the Rockley Silicon Photonics platform. This demonstrates the capability of the Rockley platform to use MTP InP coupons for high-speed devices. Simulation and design efforts to further improve transmitter performance have been discussed, including flip-chip integration design and EIC-PIC co-simulation. EIC driver based on the co-simulation has been characterized up to 70 Gb/s.

Acknowledgment

The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), US Department of Energy, under Award Number DE-AR0001273. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

The authors would like to thank GlobalFoundies for their foundry services. In particular, the authors thank to T. Latavic, N. Cahoon, and M. Peters at GlobalFoundries for their support with EIC fabrication.

The authors would also like to thank Dr. Bruce Chou, Dr. Aaron Maharry, and Stephen Misak for their support.

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