Integration of Active Optical Components

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ABSTRACT

Integration of active optical components typically serves five goals: enhanced performance, smaller size, lower power dissipation, higher reliability, and lower cost. We can differentiate between horizontal and vertical integration schemes. Horizontal integration combines many elements of the same functionality, like laser arrays. Vertical integration combines different functionality into a single element. Hybrid integration exhibits advantages over monolithic integration, if incompatible fabrication processes are employed. We are manufacturing widely tunable laser diodes with an integrated high speed electro absorption modulator for metro and all-optical switching applications. The monolithic integration combines the functions of high power laser light generation, wavelength tuning over the entire C-band, and high speed signal modulation in a single chip. The monolithically integrated optical amplifier boosts the cw output power of the packaged laser to over 20mW and provides a convenient way of power leveling. The modulator is based on the Franz-Keldysh effect for a wide band of operation. The time averaged power is in excess of 5dBm and the Rf extinction ration is larger than 10dB across the 40nm wavelength tuning range. Data transmission at 2.5Gbit/s is error-free over 350km of standard single mode fiber. Integration is the key technology for this device to achieve high performance, small footprint, and low cost all at once.

Keywords: tunable laser, monolithic integration, electro-absorption modulator, optoelectronic integration.

1. INTRODUCTION

Integration of electronic devices has been the enabling technology for the information technology. Starting with the first integrated circuit in 1958 [1] the monolithic transistor integration has now enabled over 1 billion transistors on a single chip. However, it is not only quantity, but integration also enables new functionality. Microprocessors would not even be possible without integration, because of the parasitic electrical elements of discrete devices.

The electronic integration of a large number of elements is most easily achieved, if all elements are made in the same manufacturing process. The integration is then primarily the intelligent connection of the various elements. DRAM chips are a good example. This horizontal type of integration is illustrated in Fig. 1a.

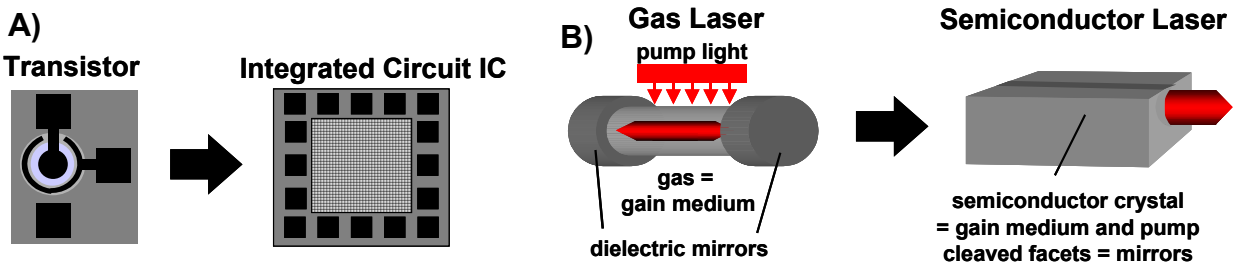

Figure 1: Examples of integration: A) Horizontal integration of many transistors into an integrated circuit, B) Vertical integration of the different components of a conventional gas laser into the single semiconductor laser diode chip. The semiconductor laser chip combines the different functionality of optical gain medium, pump, and mirrors for optical feedback.

The photonics world has not seen the degree of integration as the electronics. However, the semiconductor laser diode is already the first example of integration in photonics. As illustrated in Fig. 1b the laser diode can be viewed as the monolithic integration of the functions: optical gain medium, pump source for the optical gain medium, and optical feedback provided by the cleaved facets of the semiconductor crystal. This type of vertical integration combining different functionality is a good example how integration can create much smaller and more robust devices compared to the conventional gas laser. Besides advantages in terms of space, power, and reliability, we also achieve tremendous cost savings at the same time.

We will discuss the benefits and challenges of the integration of active optical components in more detail in the following chapters. However, one remark should be made upfront. There is a fundamental difference between photonic and electronic integration. Large scale electronic integration requires a shrinkage of the electronic elements at the same time. Transistor dimensions and feature sizes are already smaller than the wavelength of visible light. In photonics on the other hand shrinkage is always limited by the wavelength of the light we use for transmission. This wavelength is adjusted to the absorption minimum of silica optical fiber to 1.55μm. In some short distance applications the wavelength is below that. Nevertheless, the light wavelength of around 1μm creates a fundamental limit of device shrinkage and therefore integration. The large bending radius (several hundred micrometer) of optical waveguides provides a good illustration of this limitation.

2. INTEGRATION OF OPTOELECTRONIC COMPONENTS

In this chapter we will discuss applications and ways of optoelectronic component integration. Figure 2 shows a generic transmission system for long haul transmission [2].

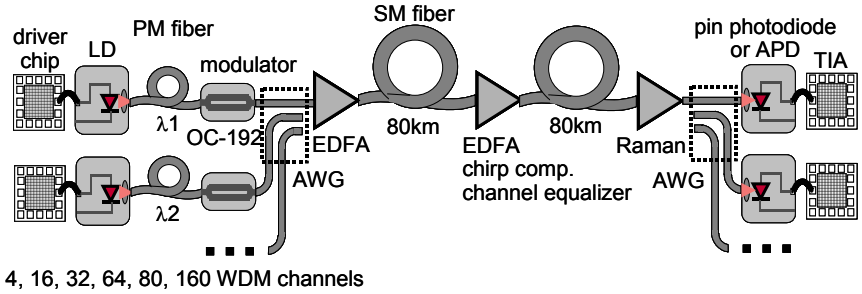

Figure 2: Generic DWDM transmission system for OC-192 data traffic. Integration has focused on the optoelectronic elements: Laser-modulator, photodiode-preamplifier (TIA).

A lot of work has been done on the integration of laser diodes and modulators. The main driver is cost and footprint reduction. On the receiver side the integration of photodiodes and the preamplifier has been demonstrated. Photodetectors based on MSM structures and FET based amplifiers have been monolithically integrated and are widely employed in 850nm Gigabit Ethernet datacom applications. These are examples where elements with different functionality are combined in a single element.

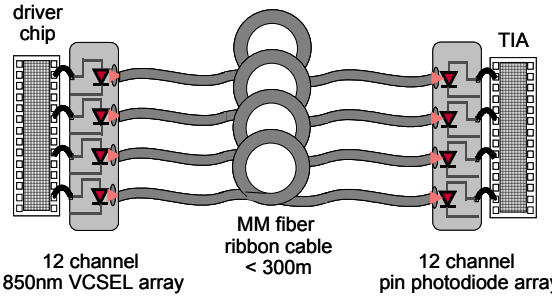

Figure 3: Parallel optical link employing monolithically integrated VCSEL arrays and photodiode arrays on the transmit and receive side, respectively. These elements are an example for horizontal type integration.

An example for horizontal integration where many elements of the same functionality are combined in a single device is the parallel optical link as shown in Fig. 3. Most parallel links are employing 12 channels with multimode fiber ribbon cables to connect transmitters and receivers [3]. The operating wavelength for this short distance datacom application is 850nm. VCSELs are the light sources of choice, because of their good performance and easy packaging capability [4], [5]. For the parallel optical link 12 VCSELs are monolithically integrated in a single chip. The high uniformity of the VCSEL performance is essential for low cost architectures. Monolithic integration and excellent process control are the enabling technologies for these products.

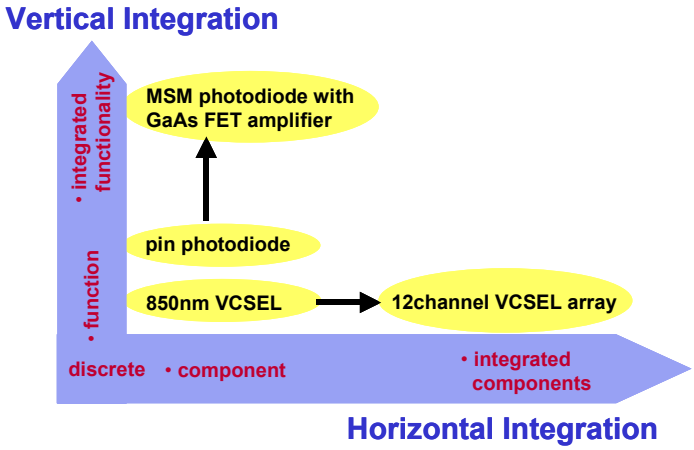

Figure 4: Integration schemes. Horizontal integration: from discrete component to many integrated components of the same functionality. Vertical integration: from discrete components to integrated elements combing different functionality.

Figure 4 summarizes the different integration schemes. Horizontal integration combines many elements of the same functionality, like laser arrays and photodiode arrays for parallel optical links. Vertical integration combines different functionality into a single element. Examples are the integration of photodetector – preamplifier, laser – modulator, and laser – driver chip.

3. EVALUATION OF INTEGRATION SCHEMES

In the last chapter we have addressed the different integration schemes. Now, we will discuss the implementation of integration and evaluate the benefits and drawbacks.

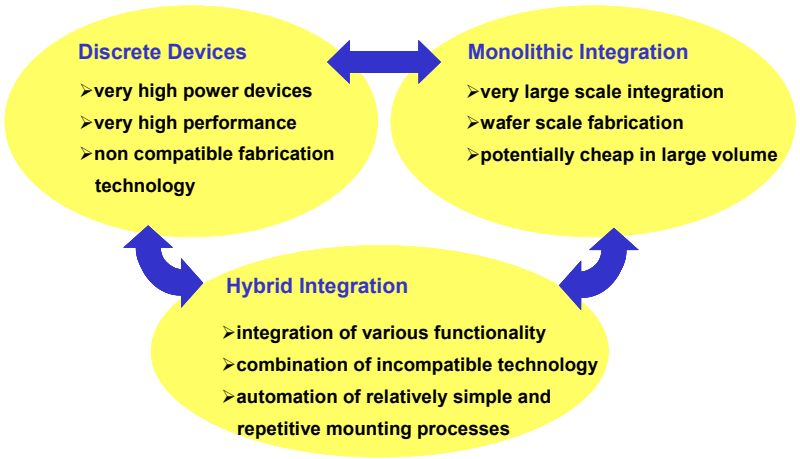

Figure 5: Implementation of integration: monolithic versus hybrid compared to discrete solutions.

3.1 Implementation of integration

Integration can be realized as monolithic integration where a single semiconductor chip integrates all the elements employed in a particular design. This is the predominant way of electronic integration, but other schemes are used as well. The other form of integration is hybrid integration where different chips are combined in a subassembly to achieve similar benefits as monolithic integration. The one characteristics of monolithic integration is that it enables large-scale integration, like millions of transistor elements. Monolithic integration is a wafer-scale fabrication process. Since all the elements go through the same fabrication process, all process steps need to be compatible to each other. Monolithic integration can be very low cost in large volume, because of the wafer-scale fabrication process.

Hybrid integration is predominantly used to combine elements of different functionality. It is the best choice if monolithic integration is not possible, because of incompatible technology. An example are bulk optic elements like lenses combined with laser diodes chips. Hybrid integration requires the automation of relatively simple and repetitive mounting processes to be advantageous. Sometimes wafer batch processing can be applied.

Discrete devices are also widely used. Discretes tend to be advantageous if ultra high performance is expected out of a single element. Examples are high power devices in electronics and optoelectronics. Another advantage of discrete devices is the high flexibility in a new design.

3.2 Evaluation of integration

The main reasons for integration in general are:

- Higher performance
- New functionality
- Smaller size
- Lower power dissipation
- Higher reliability
- Lower cost

The higher performance is mainly achieved by reduction of parasitic elements, like capacitance and inductance of bond wires. This level of higher performance can lead to new functionality that would not be achievable without integration. Examples are the transistor, the microprocessor, and distributed Bragg reflector lasers (DBRs). Since most integration provides shrinkage of elements and obsolescence of additional packaging levels, the size of devices is reduced. This enables smaller footprint products. Lower parasitic elements and fewer interfaces lead to lower power consumption. This is also necessary for further integration. Fewer interfaces and fewer separate parts normally enhance reliability. The goal of integration is also to lower the cost. We will discuss this in some more detail in the next chapter. In general, cost tends to be lower if the same fabrication technology is used for all elements to be integrated. Horizontal integration is an example. In other cases it is not always the case and needs to be evaluated on an individual basis.

Table 1: Advantages and drawbacks of integration

+ PROS	- CONS
Fewer parts => lowering packaging cost	More devices => potentially lower yield. In reality: failures tend to cluster, yield (total) >> [yield (single)]^n
Higher uniformity due to same process conditions => enabling Opamps, DRAMs, VCSEL arrays	Vertical integration requires compatibility of fabrication processes => compromise or not at all possible
Smaller space requirement	More process steps typically result in lower yield
Smaller parasitics (capacitance wire bonds) => high performance, low power	Specialized design for specific application => non-flexible in development/changing requirements
Ease of fabrication and testing (fewer elements to test)	High development cost, long lead times (ASICs) => cost advantage at high volume only

Among the advantages of integration is the fact that we have to deal with fewer parts. This lowers the assembly and packaging cost and also normally enhances the reliability of a device. Since in monolithic integration all elements experience the same fabrication process and process conditions, the uniformity is improved and enables devices like operational amplifiers (Opamps), memory chips (DRAMs), and VCSEL arrays for parallel optics. With fewer elements and integration the size requirement is reduced and the smaller parasitics provide lower power consumption and higher speed levels. The fabrication and testing is eased, because we test normally on wafer level and we test only after a lot of the internal connections have been made during the fabrication process. Thus, the number of test points is drastically reduced compared to discrete devices.

On the downside, we have to recognize that more devices need to function in an integrated assembly in order to make it work. This could potentially decrease the yield of the final device. However, failures normally tend to cluster. Thus, the total yield of multiple integrated elements is far larger than just the product of the individual yield figures. This is the case for electronic circuits, but also for VCSEL arrays for example. Vertical integration normally requires more process steps. This might enforce compromises for individual process steps. It can also result in a lower overall yield, since more process steps are required.

In many cases the integration of many elements and functions leads to a highly specialized design. Special solution are not as flexible as discrete and tend to exhibit relatively large development cost and times. Thus, a cost benefit can be obtained at high volume only.

4. COST OF INTEGRATION

The cost of a manufacturing process is obviously a very complex question and involves material cost, labor cost, equipment cost, overhead cost, yield figures, material usage, efficiencies and so on [6]. Thus, we cannot discuss any cost details for all possible configurations in this paper. Instead we will just look at one example to illustrate the various scenarios.

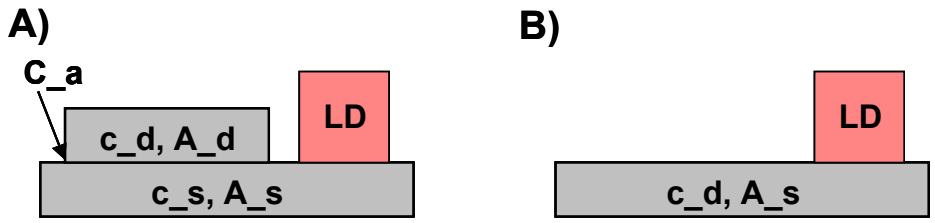

Figure 6: Optical subassembly consisting of A) laser diode (LD) mounted on a submount together with a driver IC chip. B) Integrated version with driver being the laser submount.

As an example we will examine the cost of a subassembly consisting of a mechanical submount, a laser driver IC chip, and a laser diode chip. We ask if the integration of the laser driver chip into the submount is more cost effective than the discrete solution where we need to mount the driver chip on the submount. Since the laser diode chip is the same in both cases we will not consider its cost contribution for the comparison.

For the cost calculation we consider the die cost per unit area to fabricate the laser driver chip c_d. The die area is A_d. Thus, the chip cost is C_d = c_d * A_d. The submount exhibits a different die cost per unit area of c_s which is much lower than the cost to make a high performance electronic driver IC. With the area A_s the cost of the submount is C_s = c_s * A_s. The assembly process contributes the cost C_a that is related to the equipment, labor, and so on. Therefore the total cost of the subassembly (ignoring the laser diode) is C_t = C_d + C_s + C_a.

For the integrated solution we consider that the driver chip fabrication process is now applied to the entire submount area. Thus, the die cost per unit area remains c_d, but the area is now A_s. There is no assembly cost for the integration design. The total cost is: C_I = c_d * A_s.

We compare the cost of the two versions: integrated submount chip versus two chips plus assembly process. We realize that the integrated design is only more cost effective, if the assembly cost C_a > c_d * (A_s – A_d) – c_s * A_s. Since the submount die cost per area is usually cheap, we can ignore the second term in most cases. Thus, for the integrated solution to be more cost effective, the assembly cost must be larger than the additional area cost of the larger driver chip. The equivalent expression is:
C_a > C_d * (A_s/A_d – 1) – C_s.
Therefore the submount with the integrated driver electronics is only more cost effective if the assembly cost for the two chip solution is more expensive than the driver chip multiplied by the relative ratio of the submount to driver chip area minus the submount cost. In reality, the driver chip cost dominates in most cases. Thus, from the cost point of view it does NOT make sense to integrate the driver electronics into the submount and waste expensive chip real estate to mount the laser chip on it.

In this chapter we have discussed a very specific example for cost evaluation of integrated components. It also illustrates the importance to decrease the chip real estate to reduce chip cost in general. Further cost evaluations for other integration schemes would need to be done on a case by case basis.

5. MONOLITHIC INTEGRATION

We will discuss Agility's widely tunable lasers as an example for monolithic integration of optoelectronic devices in the following chapter. As we will see the devices combine a multi-section light generating laser diode, a semiconductor optical amplifier, and an electro-absorption modulator all in the same chip. Therefore the laser is one of the most highly integrated optoelectronic devices to date.

5.1 Widely tunable laser

The high-power widely tunable laser diodes comprise a sampled grating distributed Bragg reflector (SG-DBR) laser and a semiconductor optical amplifier (SOA). The wavelength tuning range covers the entire C- or L-band. Performance characteristics of these devices meet long-haul system requirements for wavelength stability, output power (10 and 20 mW), linewidth (<5 MHz), and SMSR (>40 dB) over the entire 40 nm tuning range in C- or L-band.

At a further level of monolithic integration we combined the tunable laser and the optical amplifier with an electro-absorption modulator (EAM) on the same InP chip. This device enables the transmitter functionality for metro applications. Characteristics of the transmitter module include time-averaged powers in excess of 5 dBm and *RF* extinction ratios > 10 dB across a 40 nm tuning range. Error-free transmission at 2.5 Gb/s has been demonstrated for 350 km of standard single mode fiber. In this chapter we will discuss the design and performance of the device in detail.

5.2 Device design and fabrication

As illustrated in Fig. 7, the device consists of a SG-DBR laser, a SOA, and an EA modulator, all integrated on the same InP chip.

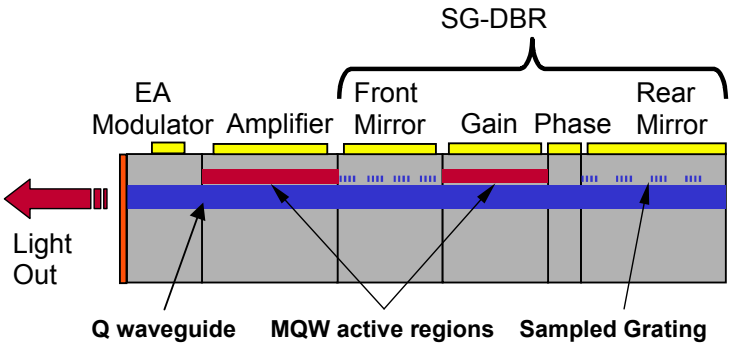

Figure 7. Schematic of SG-DBR laser integrated with SOA and EA modulator.

The SG-DBR laser [7] includes gain and phase sections positioned between two "sampled grating" distributed reflectors. By imposing additional periodicity on holographically defined Bragg grating the reflectivity spectra of the mirrors are transformed into a comb of reflectivity peaks centered at the Bragg wavelength. The spacing between adjacent peaks is inversely proportional to sampling period defined by conventional lithography. The front and back mirrors of the laser are sampled at different periods such that only one of their multiple reflection peaks can coincide at a time (this is known as the Vernier effect). Introducing a small index change in one mirror relative to the other causes adjacent reflectivity maxima to come into alignment, shifting the lasing wavelength a large amount for small index change. Continuous tuning between the reflectivity maxima is obtained by tuning both mirrors simultaneously. Biasing of the phase section fine-tunes the effective Fabry-Perot cavity mode into alignment with the maximum reflectivity of the mirrors. The tuning range of a SG-DBR laser is defined by the repeat mode spacing and can be designed to exceed the tuning range of a conventional DBR laser by a factor of ten. Optimization of the device for C- or L-band operation is accomplished by alignment of the gain spectra and Bragg wavelength of the holographically defined grating within the respective band.

The integrated SOA compensates on-state modulator loss and cavity losses caused by free carrier absorption in the tuning sections and allows wavelength independent power leveling. The integration of the laser and SOA active regions with the tuning and modulator sections of the device has been accomplished by using an offset quantum-well structure. In this simple integration technology the active region of the modulator uses the same bulk quaternary waveguide as the tuning sections of the laser. The Franz-Keldysh effect in the bulk waveguide material provides a larger spectral bandwidth as compared to the quantum-confined Stark effect. The composition of the bulk waveguide can be optimized to achieve high tuning efficiency for the laser and a target extinction ratio for the modulator over the required wide spectral bandwidth.

The laser modulator integration reduces to power consumption of the overall system compared to the discrete solution. Without integration the light output of the laser would be coupled into a fiber, transmitted a short distance, and then coupled back into the modulator chip. If we assume the coupling efficiency at the laser to be 60% and 70% at the modulator, we realize that over 50% of the light is lost. The integrated waveguide solution on the other hand exhibits only minor optical losses. Thus, the overall power efficiency is enhanced.

5.3 Packaging and control

An integrated SG-DBR-SOA-EA modulator chip and a multi-channel wavelength locker were mounted into a cooled butterfly module with a co-planar RF input. The package is integrated into a compact MSA compatible transmitter assembly as shown in Fig. 8 along with dc current sources, modulator driver circuit, control electronics, and firmware.

Fig. 8: Tunable laser assembly containing the widely tunable laser with the integrated EA modulator and the control electronics. Dimensions are 2" wide, 3.9" long, and 0.52" high. MSA pin compatible.

The reference power from the wavelength locker is fed back to the SOA current, and the etalon signal is fed back to the phase section to maintain power and wavelength control. The widely tunable transmitter assembly can be calibrated for 25 or 50 GHz channel spacing by adjusting the set points for the locker. Implementation of power control using the integrated SOA allows beam blanking to –30 dBm during wavelength switching and variable optical attenuator function with a dynamic range in excess of 10 dB.

5.4 CW performance

Under closed-loop operation 90 (180) consecutive 50 (25)-GHz spaced ITU channels with >10mW or >20mW fiber coupled output power levels and SMSR greater than 40 dB were demonstrated in the C- and L-band. The results are shown in Fig. 9. Typical operation conditions for the 20 mW cw source are I_{gain} = 150 mA, I_{FM} and I_{BM} below 30 and 50 mA, respectively, and I_{SOA} below 150 mA.

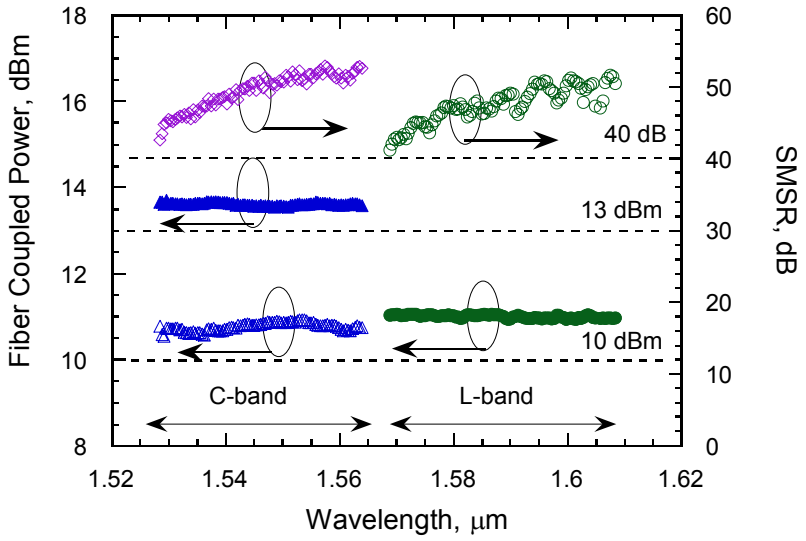

Figure 9: Fiber-coupled output power and SMSR across the C- and L-band. The two power levels are adjusted to >10dBm and >13dBm, respectively.

The linewidth of the integrated SG-DBR-SOA laser was measured using a coherent optical frequency discriminator technique [8]. Measured linewidth and relative intensity noise (RIN) are shown in Fig. 10 for 90 50-GHz spaced channels in C-band and L-band, respectively.

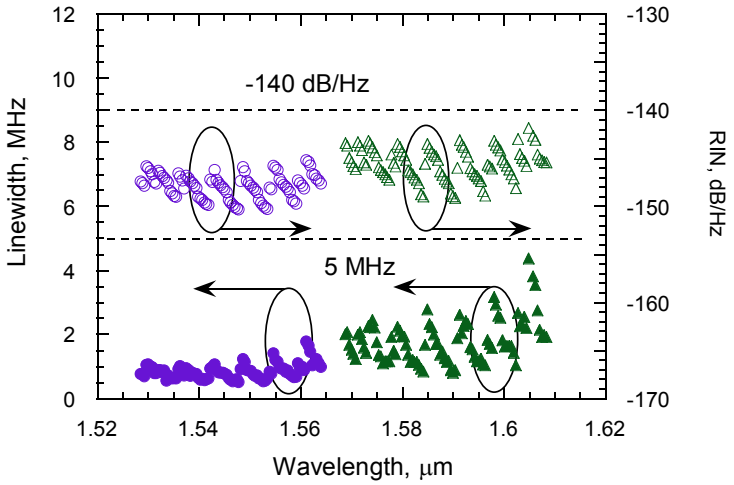

Figure 10: Linewidth and average RIN across C- and L-band for a high power, widely tunable SG-DBR laser.

The linewidth and RIN are inversely proportional to laser power and hence have periodic dependence on wavelength due to change in the mirror loss under tuning. The linewidth remains below 5MHz across the 40nm tuning range in C- and L-band, respectively. The averaged RIN within the 100MHz to 10GHz frequency range is less than –140dB/Hz.

5.5 Transmission characteristics

Maintaining a low and uniform chirp is key for achieving uniform transmission performance of the integrated transmitter over wide wavelength range. The transient chirp and extinction ratio (ER) characteristics of EA-modulators are strongly dependent on the detuning between the lasing and absorption-edge wavelengths. Previously we have demonstrated that the detuning and hence ER and chirp can be simultaneously controlled by adjusting the *dc* bias on the modulator section [2]. A uniform, high *RF* extinction ratio (>10 dB) and low chirp (<0.2 A) over a wide spectral bandwidth were achieved by calibrating the *dc* bias and the modulation voltage settings for the modulator driver. The modulator driver circuit is integrated into the tunable laser transmitter product. Under modulation a fiber-coupled time-averaged power of 5 dBm is maintained across C-band by closed loop control using the integrated SOA.

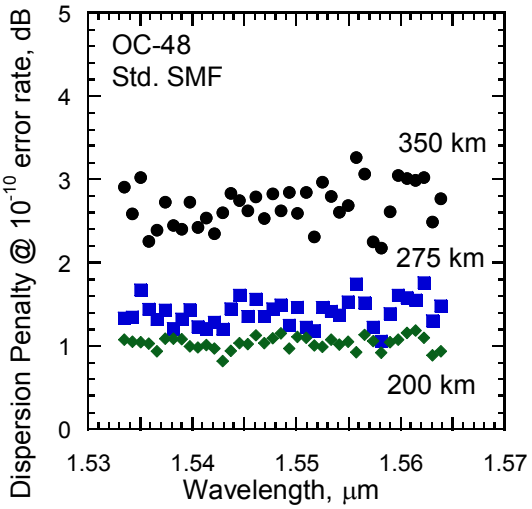

Figure 11: Dispersion penalty at 10^{-10} errors/s error rate for 200, 275, and 350 km of standard SMF for 38 ITU channels sampled across C-band.

The fiber transmission test bed consists of the SG-DBR-SOA-EA transmitter followed by spans of conventional single mode fiber (SMF). The input power into the fiber spans was 3 and 7dBm for the first and consecutive spans, respectively. A tunable band pass filter was used after the final span to remove ASE. The power and wavelength control loops were engaged during the measurements and had no effect on transmission performance. Figure 11 shows the dispersion penalty (DP) at 10^{-10} errors/s error rate for 38 ITU channels sampled across the C-band for 200, 275, and 350km of standard SMF. The short wavelength range for this measurement was limited to 1533nm by the tunable bandpass filter. The measured DP does not exhibit a significant wavelength dependence confirming the robustness of the EA-modulator chirp control over the wide tuning range.

5.6 Reliability of widely tunable lasers

In previous reports [10], [11], [12] DBR laser lifetimes were insufficient for the deployed in commercial fiber optic networks. Device lifetimes were limited by tuning section degradation, calling into question the viability of current injection tunable laser diodes. However, in this chapter we demonstrate that SG-DBR tunable lasers can operate with wear out failure rates that are comparable to or lower than those of high reliability DFB lasers currently in widespread use. In fact, the tuning section lifetime does not limit the overall device life. As the SG-DBR device is generally operated in an automatic wavelength control mode where feedback to the phase section actively fine tunes the laser wavelength, changes in wavelength during device aging are not a concern for device wear out. Moreover without any

active control on the mirror sections, accelerated aging studies have indicated that the mirror drift with time is also sufficiently small to insure that no mode-hopping will occur over life.

From a design standpoint the SG-DBR device should naturally exhibit high reliability. In DFB or standard DBR lasers a large source of the material defects that cause the device to degrade over time is the grating structure where semiconductor materials have been etched and regrown. Additionally, the rate of aging is known to be highly dependent on the current applied to the device. Compared to the DFB or standard DBR laser, the mirror sections of the SG-DBR laser have a low percentage of grating due to their periodic sampled structure. The tuning current densities applied to the mirror and phase sections of the SG-DBR are comparable to the threshold current densities (not the drive currents which are ~5-10 times the threshold current) of laser diodes made from similar materials. Therefore, the SGDBR tuning sections are expected to be at least as reliable as comparable DFB structures because they have less defect generating grating area and are driven with substantially less current.

In order to assess the reliability of the SGDBR lasers, accelerated aging experiments were conducted on greater than 150 burned-in, screened devices from the Agility manufacturing line. Several temperature and current overstresses were applied to the devices for extended periods of time to ascertain the degradation rate as a function of current and temperature. As the SGDBR device performance varies with channel, devices were calibrated at each measurement point in time, yielding the changes in the tuning currents to obtain the same channel over time. The updated calibration was then used to measure changes in other parameters such as threshold current and output power at multiple channels representing the extrema of calibrated currents and wavelength.

The failure criteria used to determine tuning section life was set conservatively to ensure mode hop free operation even in the presence of degradation processes that are not accelerated during the accelerated life test, but may nevertheless occur during field deployment of the device including high and low temperature storage or mechanical/environmental stressing.

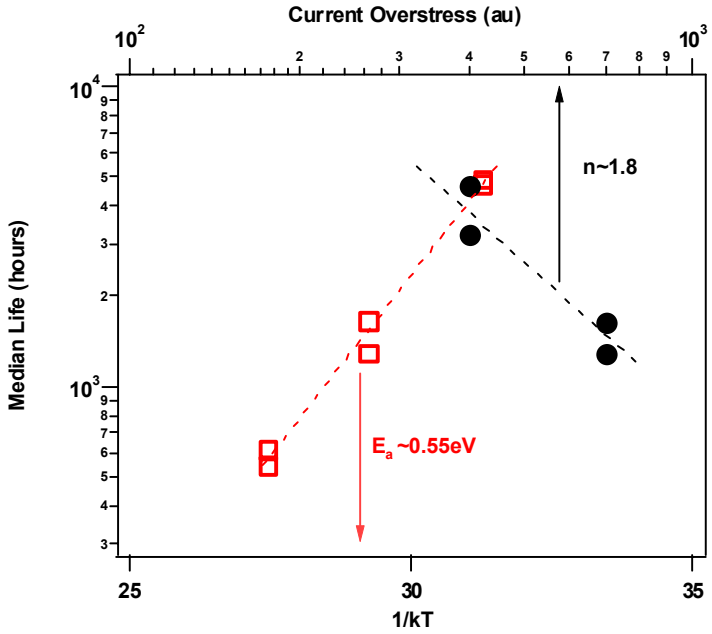

Figure 12: Determination of tuning section acceleration factors in accelerated aging experiments. Data points are the median values for all of the parts at the particular aging stress. Least squares fitting yields an activation energy of E_a ~0.55eV and current acceleration exponent of n ~1.8.

In order to predict the failure distribution at normal use conditions, the temperature and current dependent acceleration factors were determined by performing a two dimensional least squares fit to the median degradation rate at each stress condition. The aging data was fit to the following model:

$$aging\ rate \propto I^{-n} e^{\frac{-E_a}{kT}}$$

where I is the current, n the current acceleration factor, k the Boltzmann constant, T the absolute temperature, and E_a the activation enery. Figure 12 shows the median mirror aging rates, plotted versus temperature and current. A least squares fit to the data yields a thermal activation energy E_a of approximately 0.55eV and a current acceleration exponent n of approximately 1.8.

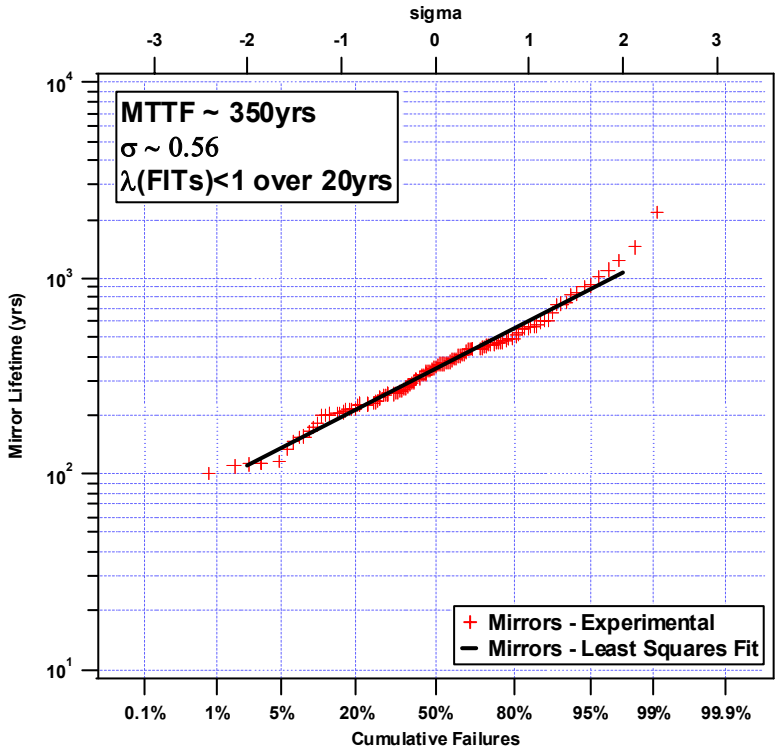

Fig. 13. Cumulative Failure Distribution (CDF) for the SG-DBR mirrors at maximum use conditions.

Using the acceleration factors to predict the lifetimes at operating conditions yields the cumulative failure distribution plotted in Fig. 13. The distribution was fit to the standard lognormal failure distribution for the purpose of calculating the instantaneous failure rate (in FITs). The failure rate due to passive tuning section wear out remains below 1 FIT over the expected useful life (~20 years).

The accelerated aging data demonstrates that SGDBR tuning sections can provide highly reliable operation over the anticipated useful life. As the lifetime of the SGDBR laser depends not only on the tuning sections but the active sections, acceleration factors and failure rates for the active sections have also been determined. The data yields activation energies and current acceleration exponents very similar to the passive sections, which is not surprising, as the different sections are made from essentially the same materials by the same processes. As the active sections are driven with higher currents than the tuning sections, the active section median life is slightly shorter than that of the tuning sections. However, adding the active and tuning failure rates results in a low total wear out failure rate that remains less than 100 FITs over the useful life of the device.

SUMMARY

We have discussed the various aspects of the integration of active optical components. Horizontal integration combines many elements of the same functionality, whereas vertical integration combines different functionality into a single element. Parallel optical links employ horizontally integrated elements: VCSEL and photodetector arrays. Most other optoelectronic integration approaches focus on combining different functionality in a single device. The modulator laser integration is an example. We discussed widely tunable laser diodes with an integrated semiconductor optical amplifier and a high speed electro absorption modulator. The monolithic integration combines the functions of high power light generation, wavelength tuning, and high speed signal modulation in a single chip. The cw output power of the packaged device is over 20mW. The optical amplifier boosts the power level and provides a convenient way of power leveling. The integrated, high speed modulator is based on the Franz-Keldysh and achieves a large extinction ratio of more than 10dB. The time averaged power is higher than 5dBm. Error free data transmission at a 2.5Gbit/s data rate (OC-48) is achieved over 350km of standard single mode fiber. Integration is key to achieve high performance, small size, low power consumption, high reliability, and low cost. Future developments will lead to more and further integrated active optical components.

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