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First Demonstration of an O-Band Coherent Link for Intra-Data Center Applications

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Abstract—We report the first demonstration of a full O-band coherent link for intra-data center applications, including custom photonic and electronic integrated circuits for the transmitter and receiver. Full-link 112 Gbps (56 Gbaud QPSK) transmission is shown with $2.1 \cdot 10^{-4}$ measured BER, and record baud rate 128 Gbps (64 Gbaud QPSK) transmission is shown for the stand-alone coherent transmitter. The link architecture is based on analog coherent detection (ACD), which improves power consumption substantially by performing functions in the analog domain that are normally implemented with power-hungry digital signal processing (DSP). Energy efficiency of 9.5 pJ/bit is demonstrated for the O-band coherent link, with 12.5 pJ/bit expected with next-generation circuits that include integrated optical gain. These results show the potential for next-generation data center networks based on low-power O-band coherent links.

Index Terms—Coherent optical link, O-Band, silicon photonics, data center, energy-efficiency.

I. INTRODUCTION

AS data center network traffic continues to increase, future intra-data center optical interconnects must scale to higher data rates while improving overall cost and power efficiency. Through in-phase and quadrature (IQ) modulation with polarization multiplexing, coherent optical link technologies provide a path to increased data rates over intensity modulation direct detection (IMDD) technologies. Short-reach O-band applications with low chromatic dispersion make power-efficient coherent links an attractive replacement for IMDD technologies for the 1.6 Tbps generation and beyond [1]. In an analog coherent detection (ACD)-based link architecture, power consumption is further reduced by performing carrier and polarization recovery in the analog domain without high-speed analog-to-digital conversion and digital signal processing (DSP). We previously reported an ACD link architecture

analysis that showed 5-10 pJ/bit energy efficiencies are possible with 13 dB of unallocated link budget [2].

The design tradeoffs for coherent links change significantly when moving from conventional longer reach long-haul, metro, and inter-data center links to shorter intra-data center ones. Power consumption and cost improvements are crucial for this high-volume application, so link performance must be sacrificed in key areas for coherent link technology to be viable. The ACD link architecture does this by eliminating the carrier and polarization recovery functions traditionally performed by the coherent DSP application specific integrated circuit (ASIC) and replacing them with an optical phase locked loop (OPLL) and analog polarization controller. DSP-based chromatic dispersion compensation is obviated by operating in the O-band, near the zero-dispersion point of single mode fiber. Long-reach coherent links have thus far operated in the C-band because it offers the lowest attenuation and chromatic dispersion can be straightforwardly compensated in DSP, but an additional 0.2 dB/km of loss is tolerable for intra-data center reaches and an O-band coherent link can omit DSP-based chromatic dispersion compensation with negligible penalties [3]. Further power savings come from using QPSK transmission, which enables power-efficient limiting electronics and removes the need for power-hungry analog-to-digital converters. Analog techniques for carrier recovery have been previously demonstrated with an OPLL in [4], and with a carrier phase synchronization chip in a polarization-multiplexed-carrier self-homodyne link, in [5].

The design requirements for intra-data center coherent links goes beyond the transceivers themselves, however. ACD links with large unallocated link budgets enable data center networks with passive arrayed waveguide grating routers (AWGRs) or active optical switches, improving overall network latency, cost, and power consumption [6]. Dynamic network reconfigurability from optical switching can optimize server and resource utilization for specific workloads, with projections of >2X energy efficiency improvement for the entire system [7]. In fact, optical switching is already deployed at scale in data centers. In [8], Google report 41% reduced power consumption and 30% reduced cost for their overall data center networks, including switches and interconnects. Furthermore, dynamically reconfigurable optical circuit switches have yielded advantages in network throughput and incremental installment. These optical switches have been widely and

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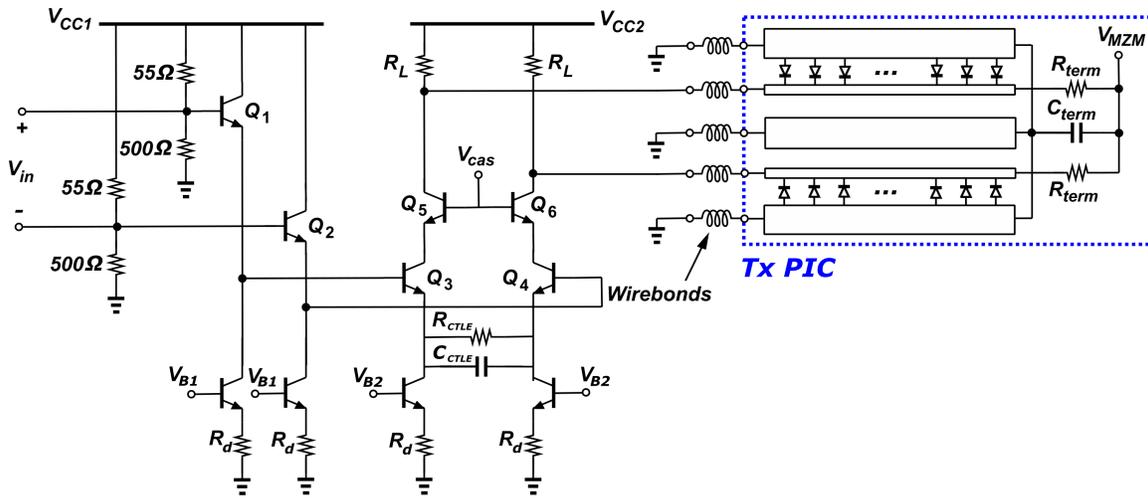


Fig. 1. Schematic of one differential driver and MZM channel. The full Tx includes 4 channels for the DP-IQ-MZM.

reliably deployed in production traffic, and are enabled by optical link technologies that support additional loss in their link budgets. As data rates scale, low-power analog coherent links are the ideal link technology to support widespread adoption of optical circuit switching across the industry.

This paper expands on the result initially published in [9]. We present here the first full-link demonstration of an O-band coherent link designed for intra-data center applications, with 56 Gbaud quadrature phase shift keying (QPSK) operation for 112 Gbps per polarization with a bit error rate (BER) of $2.1 \cdot 10^{-4}$. The achieved BER is below the threshold for KP4 forward error correction (FEC). We have designed and fabricated custom transmitter (Tx) and receiver (Rx) electronic and photonic integrated circuits (EICs and PICs) for an ACD-based link. Previously reported O-band coherent results for either high-speed Tx PICs [10] or Rx PICs and EICs [11] have relied on test equipment in the absence of integrated photonics or electronics for the full link. Our custom Tx was also measured stand-alone, resulting in record-high 64 Gbaud operation with a BER $< 10^{-4}$ for a combined O-band coherent driver and modulator. Section II will describe the design of the O-band coherent Tx and Rx, Section III will present results of component and link characterization experiments, and concluding remarks will be made in Section IV.

II. DESIGN

The Tx and Rx PICs were fabricated in Intel's silicon photonics process. The Tx and Rx EICs were fabricated in the GlobalFoundries 9HP 90 nm and 8XP 130 nm SiGe BiCMOS processes, respectively. The driver has 2 Vppd output swing and 45 GHz bandwidth across four differential channels that drive a dual-polarization (DP)-IQ travelling wave Mach-Zehnder Modulator (MZM) on the Tx PIC. The output stage load resistor R_L is 200 Ω . This quasi-open collector design maintains low power consumption while suppressing back-reflection effects from the travelling wave MZM, thereby averting the need for DSP-based equalization to recover Tx signal integrity [12]. The driver also included a continuous

time linear equalizer (CTLE) circuit in the output stage to peak the output and compensate for bandwidth degradation in the Tx PIC and receiver. The nominal design had 9.5 dB of peaking at 30 GHz, and a schematic of one channel of the driver circuit integrated with a MZM on the Tx PIC is shown in Fig. 1.

The Rx EIC design was reported previously [13], and included the data path Rx chain with transimpedance amplifiers (TIAs) and variable gain amplifiers (VGAs) as well as the phase-frequency detector (PFD) circuit required for closed-loop OPLL operation. Since the target modulation format is QPSK, the Tx and Rx both took advantage of power-efficient limiting amplifier circuits. Analog OPLL operation for this ACD-based receiver architecture does not require sampling clock information [3]. Thus, while it is not considered in detail in this work, conventional clock and data recovery (CDR) techniques can be performed on the outputs of the Rx EIC to interface with standard Serializer/Deserializer (SerDes) blocks. The Rx PIC is similar to a conventional dual-polarization coherent receiver with differential photodiodes (PDs), except that it includes an analog polarization controller formed from a series of phase shifters and 2x2 multi-mode interferometers (MMIs) after the polarization splitter rotator (PSR) in the signal path. Endless reset-free polarization control has been previously demonstrated [14], including recent demonstrations with integrated phase shifters [15]. This polarization controller is based on integrated thermal phase shifters and can perform arbitrary polarization rotation, but not in a reset-free manner. Thermal phase shifters are compact and easily integrated into the silicon photonics platform with low loss and good phase efficiency, but they have relatively low bandwidth compared to electro-optic phase shifters. However, studies performed to-date have indicated that short-reach links in data center environments would only be required to track polarization rotations on the order of roughly 100 rad/s [16], which is well within the capabilities of thermal phase shifters. In this work, in addition to an external fiber-based manual polarization controller, the integrated polarization controller was controlled by manually

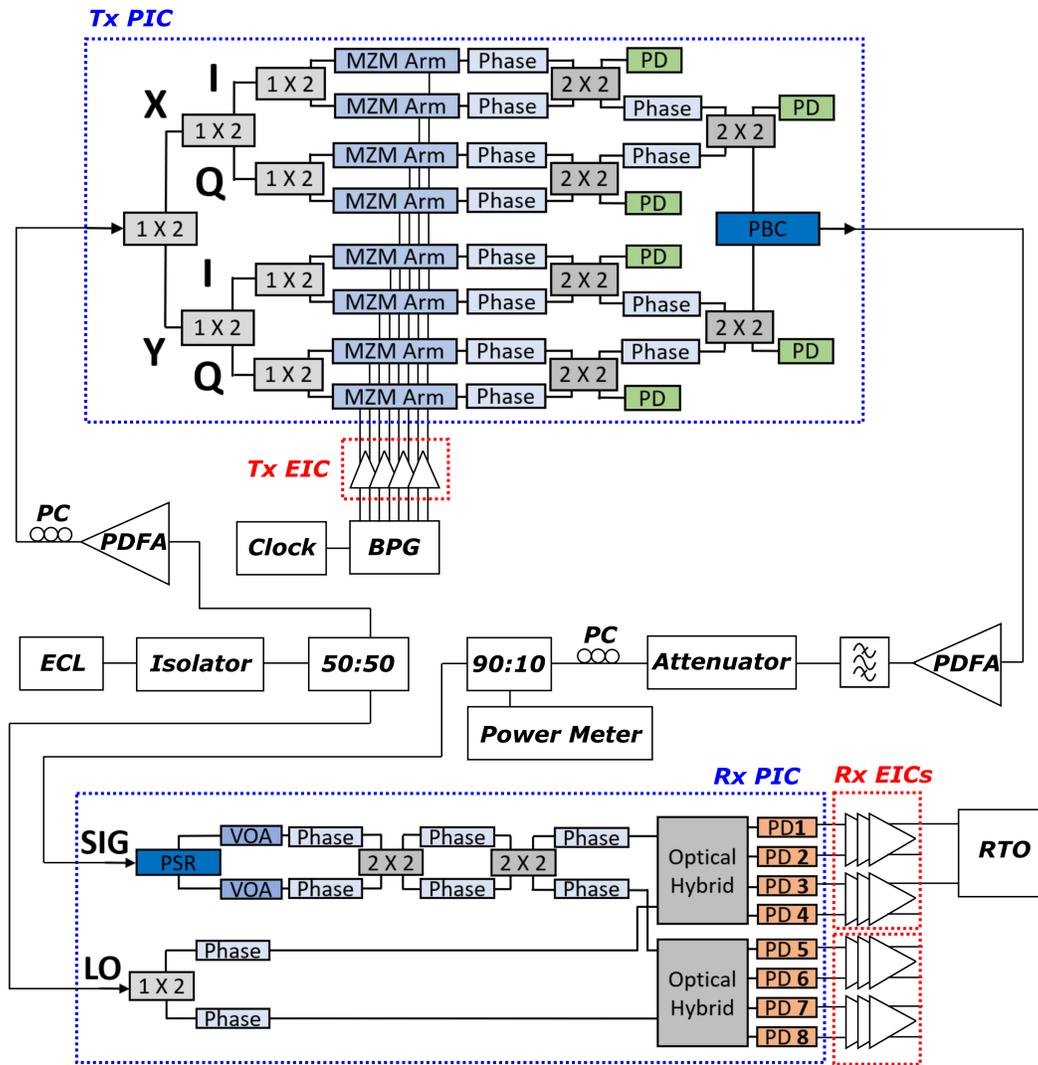


Fig. 2. Schematic of the full link measurement setup, including optical component block diagrams of Tx and Rx PICs. The integrated polarization controller in the Rx PIC, formed from cascading three pairs of phase shifters with 2x2 MMIs, was used for manual static polarization control.

applying voltages to the phase shifters to provide a static polarization rotation at the receiver. Appropriate feedback and closed loop control will be incorporated in a future ACD-based receiver PIC.

The Tx and Rx EICs and PICs were packaged with wirebonds on FR4 PCBs, with mini-SMP connectors and coaxial cables forming a high-speed interface to test equipment. Additional details of the PCB packaging platform used in this work are described in [17]. The assemblies are compatible with a permanent fiber attachment process, forming complete dual-polarization designs capable of capable of 224 Gbps/λ. During the design process, electronic and photonic circuit and component performance was optimized using full-link time-domain simulations. The link model included component losses, bandwidths, packaging parasitics, and noise contributions, and incorporated co-simulation of high-speed optoelectronic device performance with transistor-level electronic circuit simulations. In this manner, the designs were optimized with the direct goal of full-link integration. This allowed for

co-optimization of driver output stage CTLE, driver load resistor, and travelling wave MZM phase efficiency and bandwidth to minimize ISI and noise across both the Tx and Rx, and to improve the overall available link loss budget.

III. RESULTS

A. Experimental Setup

As the integrated lasers required for an OPLL were not included in these first-gen PICs, a 1310 nm external cavity laser (ECL) was split into local oscillator (LO) and signal paths in a self-homodyne link configuration. The link measurement setup is shown in Fig. 2 along with block diagrams of components of the Tx and Rx EICs. 500 mV PRBS15 differential signals from a bit pattern generator (BPG) (SHF 12105A) drove the Tx EIC, and Rx EICs outputs were detected by a real-time oscilloscope (RTO) (Keysight UXR0702A) with a 0.875 μs acquisition time at 256 GSa/s. A post-processing script corrected static constellation rotation, then sampled and counted bit errors.

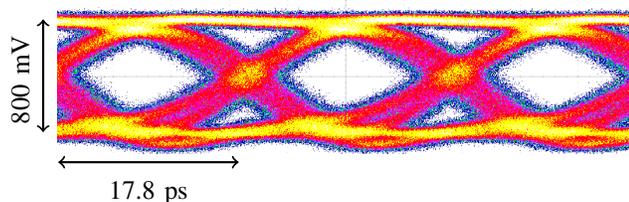


Fig. 3. Measured all-electrical eye diagram of 56 Gbaud NRZ driver operation for one single-ended output.

No external equalization or additional post-processing was performed, so the results reported in this work represent native link performance, including all ISI and packaging effects. These results are for the first Tx and Rx subsystems we have built, and due to assembly yield we are reporting dual-polarization QPSK transmission with only single-polarization 112 Gbps receiver operation. Future assemblies will be capable of full dual-polarization 224 Gbps/ λ operation. In a future full ACD-based link implementation, the OPLL would correct for time-varying and static frequency and phase errors between the Tx and LO lasers, removing the need for the constellation rotation performed in post-processing in this work. Assuming 1.3 MHz combined Tx and LO laser linewidths, as reported in [18], the OPLL locking process would give a residual phase error that would degrade the system SNR by roughly 0.5 dB [3].

B. Transmitter Characterization

The driver EIC all-electrical time-domain performance was measured by driving a single channel with 650 mVppd from the BPG and measuring the output with a 70 GHz electrical sampling module (Tektronix 80E11). The resulting 56 Gbaud eye is shown in Fig. 3 for a driver EIC variant that included output stage CTLE. This eye diagram includes bandwidth effects from the PCB packaging and coaxial cables at both the input and output.

A Tx subassembly consisting of a DP-IQ-MZM PIC and a driver EIC variant without output stage CTLE was then characterized in a standalone configuration with a reference receiver. The packaged transmitter is shown in Fig. 4. The Rx PIC and EICs in Fig. 2 were replaced by a reference optical hybrid (Kylia COH28X-FCAPC-1300nm) and balanced 70 GHz PDs (Finisar BPDV3320R), shown in Fig. 5. Resulting 56 and 64 Gbaud sampled constellations with BER $< 10^{-4}$ are shown in Fig. 6. Raw unsampled constellations are shown in 6(a) and (b), I-channel eye diagrams are shown in 6(c) and (d), and sampled constellations are shown in 6(e) and (f). BER sensitivity curves for this standalone Tx and reference Rx are shown in Fig. 7. As the unamplified output signals from the PDs were measured directly by the real-time oscilloscope, the absolute Rx input power sensitivity of this measurement does not correspond to the sensitivity of a full-link with an integrated TIA-based receiver EIC. Due to the lack of a receiver EIC and the 70 GHz PD bandwidths, however, the link inter-symbol interference (ISI) is dominated

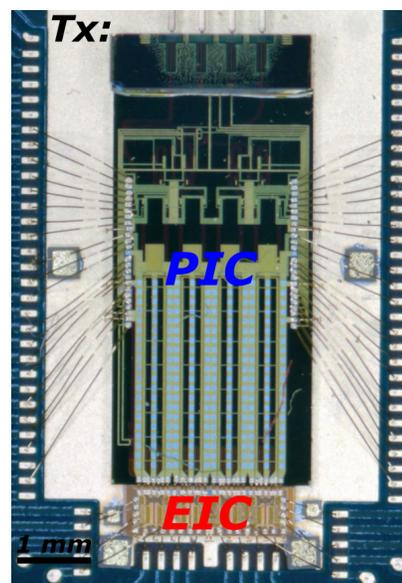


Fig. 4. Transmitter EIC and PIC, packaged on a PCB with wirebonded connections.

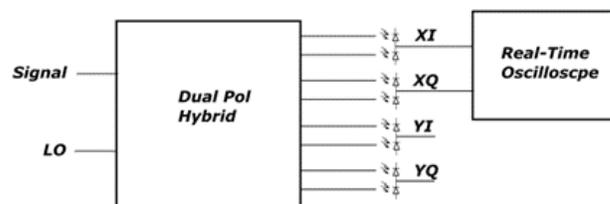


Fig. 5. Schematic of the reference receiver setup used for standalone transmitter characterization.

by bandwidth limitations in the Tx. The 28 Gbaud curve in Fig. 7 is noise-limited with negligible ISI penalty, and since no external or post-processing equalization was performed, the power-penalties shown in the 56 and 64 Gbaud curves can be attributed to the increased Tx ISI at higher symbol rates.

C. Full-Link Demonstration

Finally, the full-link performance with custom Tx and Rx EICs and PICs was characterized. The assembled transmitter is shown in Fig. 4, and the assembled receiver is shown in Fig. 8. The raw unsampled 56 Gbaud QPSK constellations for full-link transmission are shown in Fig. 9(a) and (b), the projections of each constellation onto the in-phase (I) received channel are plotted as eye diagrams in Fig. 9(c) and (d), and sampled constellations are shown in Fig. 9(e) and (f). Single-polarization transmission is shown in Fig. 9(a), (c), and (e). Dual-polarization transmission, with one polarization channel operating at the receiver, is shown in Fig. 9(b), (d), and (f). Sampled constellations for single- and dual-polarization QPSK transmission at 28 Gbaud are shown in Fig. 10. All of these constellations correspond to measured BER $< 10^{-3}$. Because no external equalization is being performed, cumulative link ISI from bandwidth limitations in the EICs, PICs, and packaging manifests in the sampled

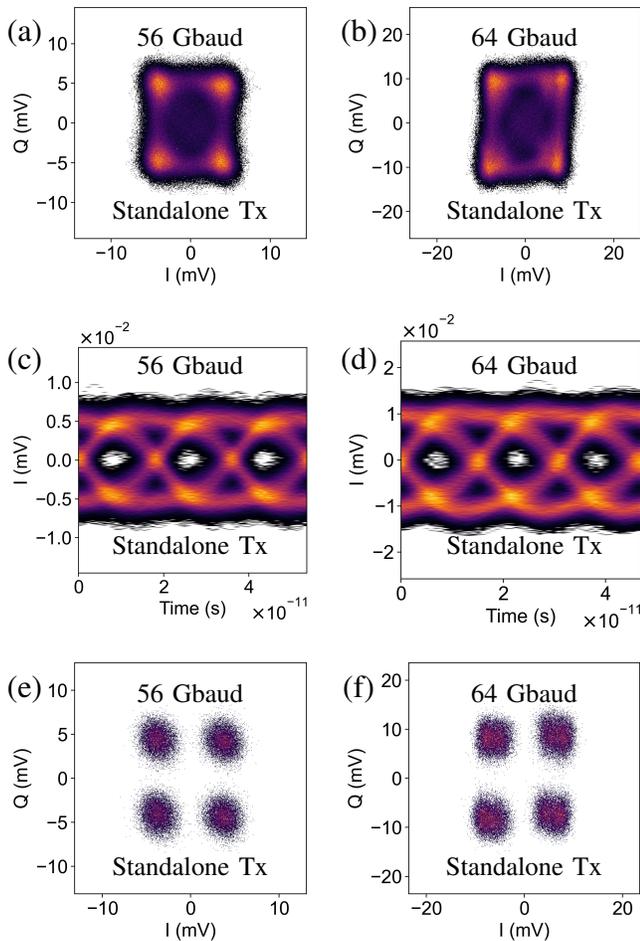


Fig. 6. Measured raw unsampled constellations (a-b), I-channel received waveforms (c-d), and sampled constellations (e-f) for standalone transmitter 56 and 64 Gbaud QPSK operation with reference receiver.

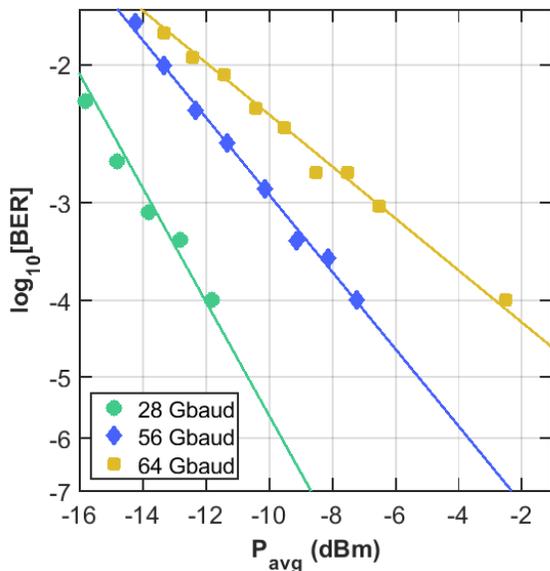


Fig. 7. Measured BER vs Rx input power for the standalone Tx with a reference receiver with -2 dBm LO power per PD.

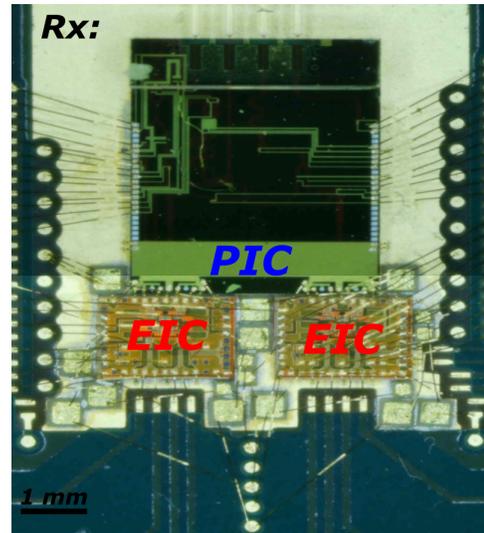


Fig. 8. Receiver EIC and PIC, packaged on a PCB with wirebonded connections.

lower baudrate transmission are noise-limited and appear as circular additive white Gaussian noise (AWGN) distributions, as in Fig. 10. Meanwhile, constellation points from higher baudrate operation appear more square, as in Fig. 6(f) and Fig. 9(e) and (f). The constellations shown in Fig. 9 and Fig. 10 are also slightly asymmetric and diverge from the ideal square QPSK constellation shape. This is likely due to instability and thermal drift in the DP-IQ-MZM biasing configuration. The thermal phase shifters used to set the bias points for the child and parent MZIs were adjusted manually, but a future practical system would incorporate active feedback control to improve the stability of the transmitted constellations.

The impact of polarization crosstalk can be seen by comparing corresponding measured constellations. BER vs average signal power at the Rx input for the full link is plotted in Fig. 11 for 28 and 56 Gbaud. The achieved BER is $2.1 \cdot 10^{-4}$ at 56 Gbaud. Rx input power is reported for a single polarization to normalize the results, and the measured power penalty from polarization crosstalk is 1 dB. The 9 dB power penalty between the 28 and 56 Gbaud sensitivity curves is a measure of the ISI from cumulative link bandwidth impairments, including PICs, EICs, and packaging.

Total power consumption with both polarization channels on was 2.1 W (9.5 pJ/bit). This includes 1.0 W (4.5 pJ/bit) from the driver, 0.2 W (1 pJ/bit) from the Tx PIC, and 0.9 W (4 pJ/bit) from the Rx EIC. Although external optical amplifiers were employed in this first demonstration, received photocurrents were kept below levels expected from next-gen PICs designed with integrated lasers and SOAs. The average LO power incident on each PD was -3.3 dBm, and the received signal power sensitivity values plotted here are expected to improve with higher LO power. Thus, the absolute receiver sensitivity values shown in Fig. 11 don't correspond directly to the sensitivity of a realistic link implementation. For reference, an ACD-based receiver with an integrated 13 dBm output power LO laser and 2 dB of on-chip excess losses would have 2 dBm LO power incident on each PD. Measurement results

constellations shown here. Constellation points resulting from

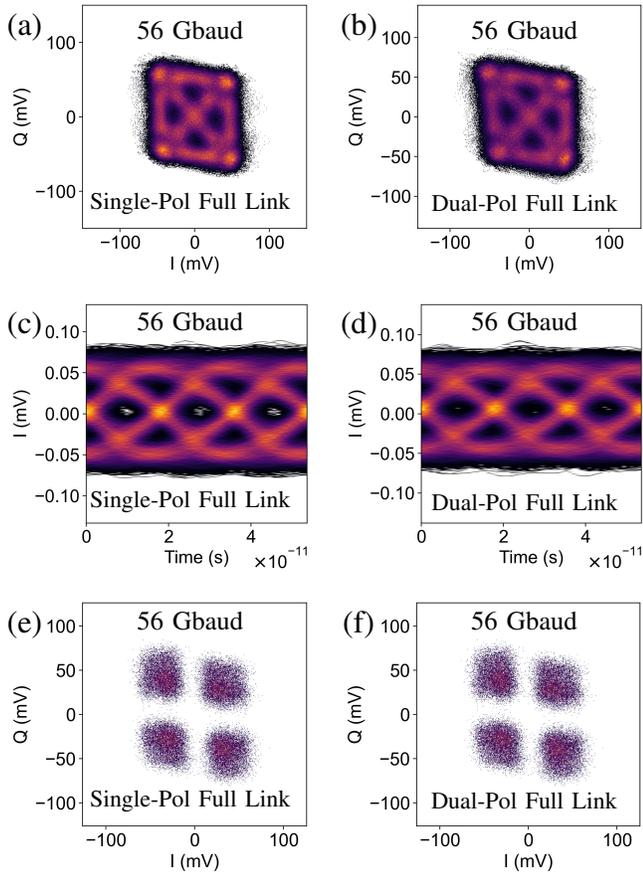


Fig. 9. Measured raw unsampled constellations (a-b), I-channel received waveforms (c-d), and sampled constellations (e-f) for single- and dual-polarization 56 Gbaud QPSK full-link transmission.

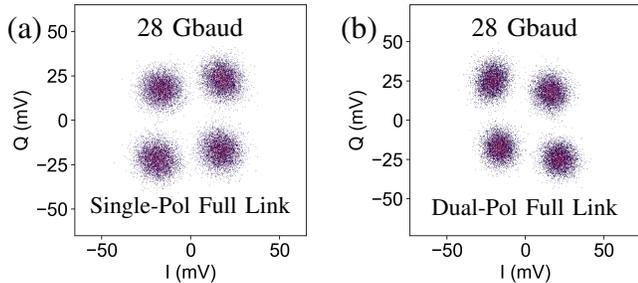


Fig. 10. Measured sampled constellations for single- and dual-polarization 28 Gbaud QPSK full-link transmission.

with next-generation Tx and Rx PICs that include integrated lasers and SOAs are forthcoming. These PICs will improve on the relatively constrained link budget demonstrated in this work by removing unneeded Tx and Rx fiber coupling as well as signal/LO splitting losses. We expect the full ACD-based link based on these PICs to operate below the KP4 FEC threshold with 13 dB of available link loss budget on the fiber, without any external amplification.

IV. CONCLUSION

We have demonstrated the first full O-band coherent link, including custom driver and receiver EICs integrated with

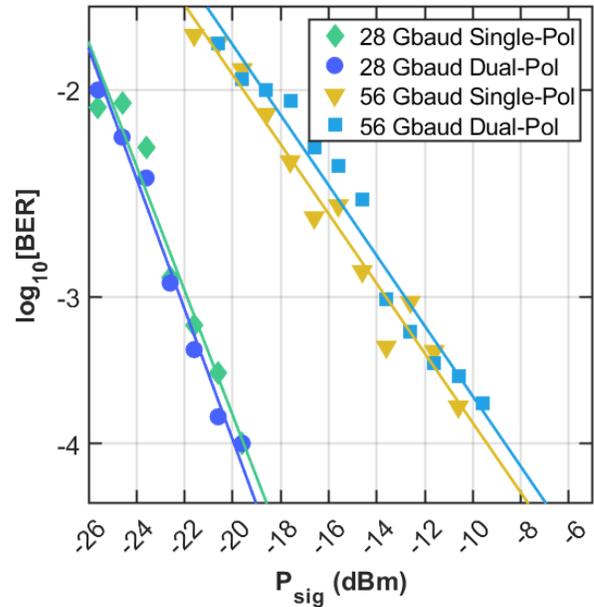


Fig. 11. Measured BER vs Rx input power (per polarization) for the full Tx + Rx link with and without polarization crosstalk.

Tx and Rx PICs. Stand-alone O-band coherent Tx operation was shown at a record 64 Gbaud. Full-link 56 Gbaud dual-polarization QPSK transmission was shown with a BER of $2.1 \cdot 10^{-4}$ with 2.1 W (9.5 pJ/bit) power consumption. We expect 2.8 W (12.5 pJ/bit) power consumption for the full 224 Gbps/ λ link, including the OPLL based on next-generation PICs with integrated optical gain. Tunable O-band lasers integrated in this silicon photonics platform were previously reported in [18]. We have also demonstrated a 224 Gbps/ λ O-band coherent link with full dual-polarization Tx and Rx operation in [19].

Coherent interconnects for intra-data center applications remain an attractive solution to meet the demands of rising data rates, but require significant redesign to achieve competitive power consumption and cost. The analog coherent approach outlined in this work aims to obviate and offload functions from the coherent DSP ASIC, which represents the dominant contribution to transceiver power consumption and cost in conventional coherent architectures. Performing polarization recovery, carrier recovery, and bandwidth equalization in the analog domain removes the need for power-hungry analog to digital converters (ADCs), and O-band operation removes the need for chromatic dispersion compensation. Perhaps the most significant benefit of intra-data center coherent link adoption would be the optical switching networks enabled by larger link budgets. Optical switching deployment has already demonstrated significant and quantifiable improvements to data center networks, and short-reach O-band coherent links will empower them by efficiently scaling links with higher data rates and expanded link budgets. While integration challenges remain, the full-link optimization, analog techniques, and new design spaces described in this work are building blocks for future low-power short-reach O-band coherent link deployment. These results show the potential of a low-power

ACD architecture and pave the way for bringing coherent links inside data centers.

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Integrated SOAs enable energy-efficient intra-data center coherent links

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Abstract: Coherent optical links are becoming increasingly attractive for intra-data center applications as data rates scale. Realizing the era of high-volume short-reach coherent links will require substantial improvements in transceiver cost and power efficiency, necessitating a reassessment of conventional architectures best-suited for longer-reach links and a review of assumptions for shorter-reach implementations. In this work, we analyze the impact of integrated semiconductor optical amplifiers (SOAs) on link performance and power consumption, and describe the optimal design spaces for low-cost and energy-efficient coherent links. Placing SOAs after the modulator provide the most energy-efficient link budget improvement, up to 6 pJ/bit for large link budgets, despite any penalties from nonlinear impairments. Increased robustness to SOA nonlinearities makes QPSK-based coherent links especially attractive, and larger supported link budgets enable the inclusion of optical switches, which could revolutionize data center networks and improve overall energy efficiency.

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1. Introduction

Fiber optic intra-data center network bandwidth has grown rapidly in recent years, and is projected to continue to do so, driving the need for continued optical transceiver performance scaling. As transceiver data rates surpass 1 Tb/s, scaling current pulse amplitude modulation (PAM) intensity modulation direct detection (IMDD) links requires increasing some combination of the baudrate, the number of PAM modulation levels, or the number of parallel fibers/wavelengths. Each of these strategies have significant challenges, and while IMDD may be able to support transceiver data rates above 1 Tb/s, it will soon become preferable to use coherent modulation and detection for high-bandwidth intra-data center links [1].

Coherent links, which can provide 4X increased data rate per wavelength relative to a comparable IMDD system due to polarization multiplexing and in-phase and quadrature (IQ) modulation, have been widely used in long haul and metro network applications, and more recently for inter-data center links below 120 km using the 400ZR standard [2]. Advances in photonic integrated circuit (PIC) technologies and continued scaling of coherent digital signal processing (DSP) application-specific integrated circuits (ASICs) implementation nodes are improving the form factor, cost, and power consumption of coherent links to rival IMDD links for short-reach intra-data center applications. In addition, our recent work has investigated the possibility of using an analog coherent detection (ACD) architecture to perform the DSP functions of carrier recovery and polarization recovery in the optical domain. This approach could remove the need for power-hungry analog-to-digital converters (ADCs) and potentially further improve coherent link power efficiency [3].

Developing coherent links for short-reach applications requires new design tradeoffs to meet the stringent power efficiency, size, cost, and interoperability requirements for intra-data center links, as opposed to the fiber capacity maximization requirements typical of longer reach coherent link implementations. Already in the 400ZR architecture, module power consumption is reduced by driving the Mach-Zehnder modulator (MZM) with an input swing well below $1 V_{\pi}$. There have been several proposals for modified DSP implementations targeted for power savings in short-reach coherent links [4,5]. Most notably, chromatic dispersion (CD) is negligible for 50 Gbaud links under 2 km, and thus CD compensation can be bypassed or omitted in the DSP [6]. Higher baudrate links may become more sensitive to CD, limiting their application to shorter reaches, or requiring the re-introduction of CD compensation. Short-reach coherent architectures using analog signal processing [7] or self-homodyne [8,9] techniques to reduce DSP power consumption have also been proposed. The trend of optimization for shorter reach applications will have to continue and be applied to other aspects of the link to enable viable intra-data center coherent links.

The power efficiency of an optical transceiver is not, however, a complete picture of its effect on overall data center power consumption. Advances in the field of optical switching have brought forward the possibility of including passive arrayed waveguide grating routers (AWGRs) or actively controlled optical switches into data center network architectures. There are proposals to replace a layer of electrical switches in current data center architectures with a layer of AWGRs or optical switches, achieving great power savings [10,11]. Additionally, data center network requirements are rapidly morphing with the rise of diverse artificial intelligence and machine learning workloads. This makes real-time network reconfiguration through optical switching especially attractive, as it has the potential to not just save power by replacing electrical switches, but also by increasing server utilization across the data center [12–14]. The potential power savings from this approach is not limited to the portion of overall data center power that is consumed by the network, but by the possible overall improvements in server utilization across the data center. Overall data center efficiency improvement of $>2X$ was projected in [15]. Thus, a critical consideration for supporting future data center growth is not just the power efficiency of the optical links themselves, but also their ability to support the inclusion of optical switches or AWGRs in the network. The available link budget of future intra-data center links is therefore crucial, since optical switches and AWGRs introduce additional losses that need to be accommodated. Coherent receivers have improved sensitivity over IMDD, and coherent links that use QPSK modulation can support greater overall link budgets than comparable IMDD links, making them attractive for optical switching applications [3].

Optical amplification is commonly used in conventional coherent links in the form of erbium doped fiber amplifiers (EDFAs) to extend link reach, and integrated semiconductor optical amplifiers (SOAs) to boost the optical power output of the transmitter (Tx), or to preamplify the signal at the receiver (Rx) [16,17]. In this paper, we present an analysis of optical amplification, namely SOAs integrated with the coherent PICs, as applied to short-reach coherent links. Design tradeoffs between Rx sensitivity, total link budget, compatibility with optical switching, inter-symbol interference (ISI), and link power consumption will be examined, with the goal of outlining short-reach coherent link architectures with optimized power efficiency and viability for implementation in data centers. Optimization for link power consumption gives rise to new design spaces for short-reach coherent links in which shot, thermal, and amplified spontaneous emission (ASE) noise can all contribute substantially to overall noise at the receiver. This hybrid regime contrasts sharply with both conventional coherent links dominated by ASE noise and IMDD links dominated by thermal noise, and thus careful design is required to optimize coherent links for short-reach applications.

Section 2 will describe the various link architectures that will be examined. Section 3 will examine the link performance penalties associated with the addition of optical amplification under

various architectures. Section 4 will present an analysis of link power efficiency incorporating optical amplification. These results will be compared to other coherent link architectures in Section 5. Concluding remarks will be made in Section 6.

2. Link architecture

The generalized coherent link architecture that will be considered in this paper is shown in Fig. 1, where 5 possible locations for SOAs have been highlighted. The optical components in this diagram can be integrated into a Tx, Rx, or combined PIC using a photonic integration platform such as [18] or [19]. The SOA in position #1 serves to directly boost the Tx laser output power with minimal impairment to the link, since a constant input power will not induce an SOA pattern effect. The principle drawback of using an SOA in this position is that the high input optical power will saturate the SOA gain. In positions #2 and #3, which come after the MZM, the attenuated input signal allows higher SOA gain, but the SOA pattern effect will introduce ISI. In these positions, the SOAs each amplify one of the two polarization channels, since SOAs are typically implemented as single-polarization devices. If wavelength division multiplexing (WDM) is used, as in the ACD-based architecture described in [3], a single pair of SOAs in position #3 can amplify all the wavelengths simultaneously after the multiplexer (MUX). Compared to position #2, this has the potential to greatly reduce power consumption in the SOAs, but will suffer from additional gain saturation, ISI, and crosstalk impairments. Similarly, SOAs in positions #4 and #5, before and after the demultiplexer (DEMUX), respectively, would act as Rx pre-amplifiers. SOAs in either of these positions would benefit from reduced nonlinear effects due to a further attenuated input signal, but would also contribute higher ASE noise at the Rx. Variations or extensions of the architectures considered in this work are also possible.

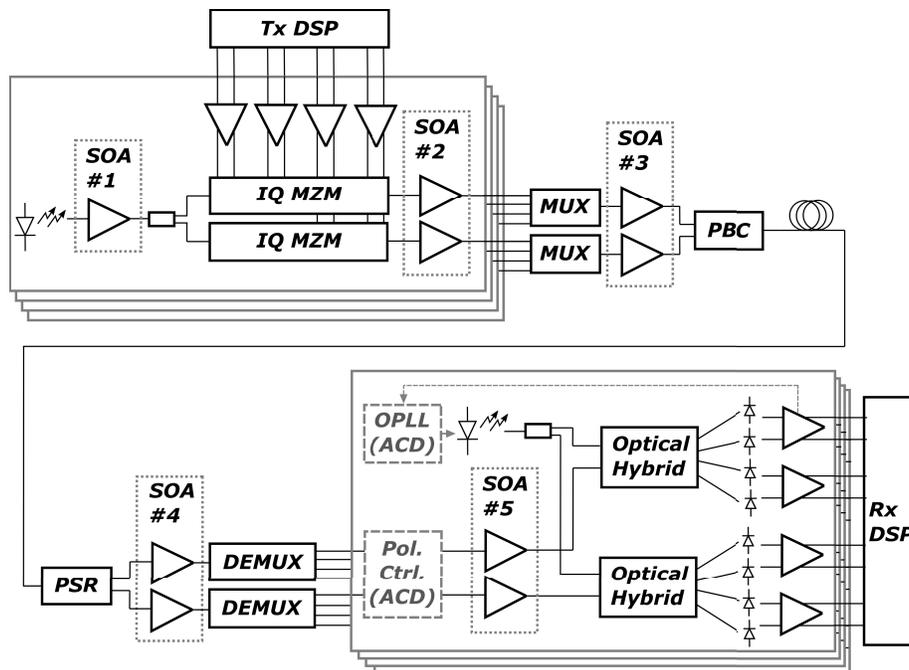


Fig. 1. General coherent link architecture. Boxes labeled SOA #1-5 indicate potential SOA insertion points throughout the link. The optical phased locked loop (OPLL) and polarization controller (Pol. Ctrl.) are used in ACD-based links, but omitted for conventional DSP-based ones.

In particular, for DSP-based coherent links, unbalanced Tx/LO laser power splitting can be employed to improve link SNR. In the cases of either equal or unequal splitting, the SOA in position #1 could be replaced by two SOA with independent bias points. This approach could improve link budgets relative to the baseline architecture, especially since gain saturation can be reduced in one of the SOAs, but for optimization parameter space simplification it is not considered in this work.

In-line fiber amplifiers are commonly included in longer reach coherent links, but are not considered in this analysis, as power and size requirements for intra-data center applications would be prohibitive compared with SOAs that can be readily integrated with transceiver PICs or packages. Moreover, as will be shown, additional in-line amplifiers are not needed to close short reach coherent links that have <1 dB of fiber losses, even for demanding link budgets that include optical switches.

3. SOA noise and gain saturation

In the architectures proposed here, the ASE noise in the SOAs introduces a current noise at the photodiodes (PDs) dominated by the beating of the LO signal with the SOA ASE noise. The ASE-induced current noise variance when detected at a PD can be expressed as

$$\sigma_{ASE}^2 = 4\mathbb{R}^2 |E_{LO}|^2 S_{ASE} \Delta f \quad (1)$$

where \mathbb{R} is the PD responsivity, E_{LO} is the normalized field from the LO, S_{ASE} is the optical power spectral density of the SOA ASE noise, and Δf is the receiver bandwidth. The ASE noise spectral density at the SOA output is calculated from

$$S_{ASE} = n_{sp} \frac{hc}{\lambda} (G - 1) \quad (2)$$

where n_{sp} is the population inversion factor of the SOA, hc/λ is the photon energy, and G is the SOA gain [20]. Due to the mixing in the optical hybrid, the ASE-induced noise currents at each differential PD pair are correlated, and the total ASE-induced RMS current noise is $\sigma_{ASE,I} = \sigma_{ASE,Q} = \sqrt{2}\sigma_{ASE}$.

In addition, SOA gain saturates with increasing input optical power, and can be written as

$$G = G_0 e^{-(G-1)P_{in}/P_{sat}} \quad (3)$$

where G is the saturated gain of the SOA, G_0 is the unsaturated or low input power gain of the SOA, P_{in} is the input optical power, and P_{sat} is the saturation power parameter [21]. P_{sat} is an internal parameter that does not correspond directly to either the input or output 3 dB gain saturation points. Static gain saturation would have the largest effect on SOA #1 in Fig. 1, since the optical input power will be the highest directly after the Tx laser.

For SOAs in positions #2-5, instantaneous changes in the power of the modulated signal at the SOA input will cause the saturated gain to fluctuate, inducing nonlinear signal distortions known as the pattern effect and nonlinear phase noise (NLPN). The pattern effect and NLPN have been well studied for IMDD applications [22,23], as well as coherent 16QAM [24,25] and RZ-QPSK [26,27]. A QPSK-modulated signal, which is used in the ACD architecture, has a quasi-constant power envelope where the only SOA input power fluctuations occur during bit transitions. Thus, it is inherently more robust to SOA nonlinearities than IMDD or higher order QAM modulation formats. Empirical characterization of SOA amplification of multi-channel QPSK links in the WDM regime was previously carried out in [28]. In this work, we experimentally investigate SOA nonlinear effects on a single-channel QPSK-modulated link. These results are then used to validate a time-domain SOA simulation model. The optical field at the SOA output is described

by

$$E_{out}(t) = E_{in}(t)e^{h(t)(1+j\alpha)/2} \quad (4)$$

where $E_{in}(t)$ is the modulated field at the SOA input, $h(t)$ is the instantaneous SOA gain parameter, and α is the SOA linewidth enhancement factor, which describes the relationship between gain fluctuation and the induced NLPN. The instantaneous SOA gain is described by

$$\frac{d}{dt}h(t) = \frac{h_0}{\tau_c} - \frac{h(t)}{\tau_c} - (e^{h(t)} - 1) \frac{|E_{in}(t)|^2}{\tau_c P_{sat}} \quad (5)$$

where h_0 is the unsaturated SOA gain parameter and τ_c is the SOA carrier lifetime [21]. The SOA gain parameter $h(t)$ is related to the total SOA gain by $G = e^{h(t)}$.

In order to confirm this model for QPSK modulation, a coherent link was tested with an SOA (Thorlabs S9FC1132P) biased at 300 mA. The measured G_0 was 23 dB and the P_{sat} was 5 dBm. Measured output constellations for a reference link operating at 10 Gbaud QPSK are shown in Fig. 2 for SOA input power levels between -10 dBm and -22 dBm. For higher SOA input power levels, the SOA NLPN contributes substantial additional phase noise. The measured link results in Fig. 2 were replicated in a simulation that modelled the SOA using the above measured parameters as well as link component bandwidths and shot, thermal, and ASE noise contributions. The SOA carrier lifetime of $\tau_c = 200$ ps and linewidth enhancement factor of $\alpha = 5$ were estimated from the literature [21]. The measured and simulated root-mean-square (RMS) phase noise characteristics are compared in Fig. 2(e), showing good agreement across SOA input power levels and validating the above SOA analytical model for application to NLPN effects on quasi-constant power envelope QPSK modulation.

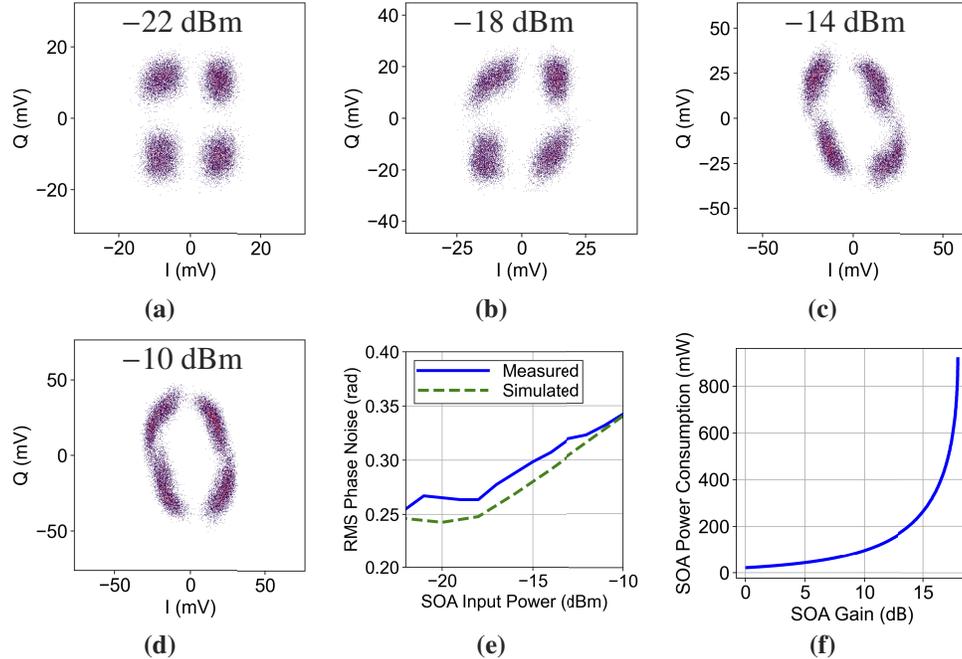


Fig. 2. Measured sampled QPSK constellations depicting the SOA pattern effect and NLPN for SOA input power levels of -22 dBm (a), -18 dBm (b), -14 dBm (c), and -10 dBm (d). (e) Measured vs modeled RMS phase error for various SOA input power levels. (f) Simulated SOA power consumption P_{soa} vs saturated gain G .

4. Power efficiency optimization

4.1. Simulation model

The performance and power efficiency of the links considered here will now be modelled and compared in simulation. The simulation model incorporates static optical losses of various components, modulation efficiency of the Tx MZM, SOA gain, time-domain simulation of BW effects and SOA nonlinearities, and various noise sources to compute the bit error rate (BER) at the receiver. All the simulations used a full PRBS15 sequence. One of the conclusions of our previous work analyzing short reach coherent links [3] was that for typical ACD links, optimal power consumption was achieved when the Tx and LO lasers were operating at high power, which is limited by laser reliability considerations. Therefore, a constant, realizable integrated laser power of 13 dBm is assumed in this work for both the Tx and LO lasers in ACD-based coherent links. For DSP-based coherent links, a 16 dBm ITLA is assumed, with equal Tx/LO splitting. All BW impairments are assumed to be single-pole low-pass filters. CD and polarization mode dispersion (PMD) are neglected. Nonlinear WDM crosstalk in each SOA is simulated in time-domain with uncorrelated aggressor signals. All of the parameters used in the simulations are shown in Table 1, for both ACD- and DSP-based coherent link configurations. These parameters represent a particular set of assumptions, and differences in actually realized device insertion loss or performance will directly affect the overall link loss budget, and potentially change SOA noise or saturation characteristics, requiring reanalysis. For the parameters and design spaces explored in this work, WDM SOA amplification was found to be an attractive and energy-efficient approach to improving coherent link performance.

The power consumption of the link is optimized by trading off driver output voltage swing and SOA gain in simulation. All other link components are assumed to have a static contribution to the overall link power consumption, which will be considered in Section 5. The driver power consumption is calculated from

$$P_{driver} = c_0 + c_1 \frac{V_{driver}}{Z_0} + c_2 \frac{V_{driver}^2}{Z_0} \quad (6)$$

where V_{driver} is the desired output swing, Z_0 is the MZM impedance, and $c_{1,2,3}$ are coefficients that depend on the driver design and process. In this work, we define the output swing of the drivers in an ACD-based link by the rail-to-rail differential voltage, since limiting electronics may be used in concert with driver output stage peaking circuits. We define the output swing of the linear drivers required for DSP-based links by the peak-to-peak differential voltage, including any peaking from linear equalization. The SOA power consumption is calculated from

$$P_{SOA} = V_d I_{SOA} + R_s I_{SOA}^2 \quad (7)$$

where V_d is the diode voltage drop and R_s is the SOA series resistance. The modeled SOA power consumption vs. saturated gain is shown in Fig. 2(f) for -11 dBm of input power.

4.2. Simulation results

The link simulation was carried out for each of the coherent architectures outlined in Section 2. For each configuration of driver output voltage and SOA gain, the link was simulated multiple times for a full PRBS word with progressively increasing unallocated link budget (ULB), modelled as additional insertion loss on the fiber. The maximum achievable ULB while meeting the target BER was thus characterized for each link configuration. The simulation results for various architectures are shown in Fig. 3, where Fig. 3(a-d) show the combined driver and SOA power consumption vs. the saturated SOA gain G . ACD-based and DSP-based link power consumption are normalized to 200 and 400 Gbps/ λ , respectively, ignoring forward error correction (FEC) overhead bits.

Table 1. Link simulation parameters.

Simulation Parameter	Value for ACD	Value for DSP	Notes
Modulation Format	QPSK	16QAM	
Baudrate	56 Gbaud	60 Gbaud	
Target BER	$3.8 \cdot 10^{-3}$	$1.25 \cdot 10^{-2}$	HD-FEC and CFEC thresholds
Rx Adaptive Equalizer Taps	1	31	No DSP equalization in ACD link
Laser Power on PIC	13 dBm	16 dBm	Integrated for ACD, ITLA for DSP
Laser Splitting	N/A	50:50	
Driver Power Coefficient c_0	0.075 W	0.1 W	Linear driver power fit to commercial driver performance. Limiting driver power fit to performance in [29].
Driver Power Coefficient c_1	0.175 V	-0.375 V	
Driver Power Coefficient c_2	1.225	1.25	
Driver CTLE Peaking	6 dB		
Driver CTLE Frequency	50 GHz		
Driver Bandwidth	40 GHz		
MZM Bandwidth	30GHz		
TIA Bandwidth	40 GHz		
MZM Phase Efficiency V_π	6.7 V		
MZM Z_0	30 Ω		
SOA Carrier Lifetime τ_c	200 ps		
SOA P_{sat}	15 dBm		Fit to performance in [30]
SOA α	5		
SOA n_{sp}	3.5		
SOA V_d	0.88		
SOA R_s	10 Ω		
Operating Wavelength	1310 nm		
Photodiode Responsivity \mathbb{R}	1 A/W		
TIA RMS Input Noise	7.2 μ A		Fit to performance in [31]
Tx Excess Losses	9 dB		
Mux+Demux Excess Losses	2 dB		Based on performance in [32]
Rx Excess Losses	5.5 dB		
LO Excess Losses	2 dB		
Fiber Loss	1 dB		

Across the simulations, power consumption is generally improved by operating at lower driver swings and higher SOA gains. Figure 3(a) shows the link design space for an ACD-based link with an SOA in position #2, where compensating for reducing driver output voltage by increasing SOA gain results in lower overall power consumption for all ULBs plotted. Further modest improvements in power consumption are achieved by moving from SOAs in position #2 to WDM amplification with SOAs in position #3, as shown in Fig. 3(b) and (d), despite increased input power and crosstalk at the SOA from three other simulated WDM channels. WDM amplification improved power efficiency by a larger amount for the ACD-based architecture than for the DSP-based architecture due to QPSK's increased tolerance to SOA NLPN.

The expected drawback of an architecture with an SOA in position #1 was that the high input power from the laser would saturate the SOA. Indeed, Fig. 3(c), shows that large SOA gains were not attainable, as they were in Fig. 3(a), (b) and (d). This limits the power efficiency of this

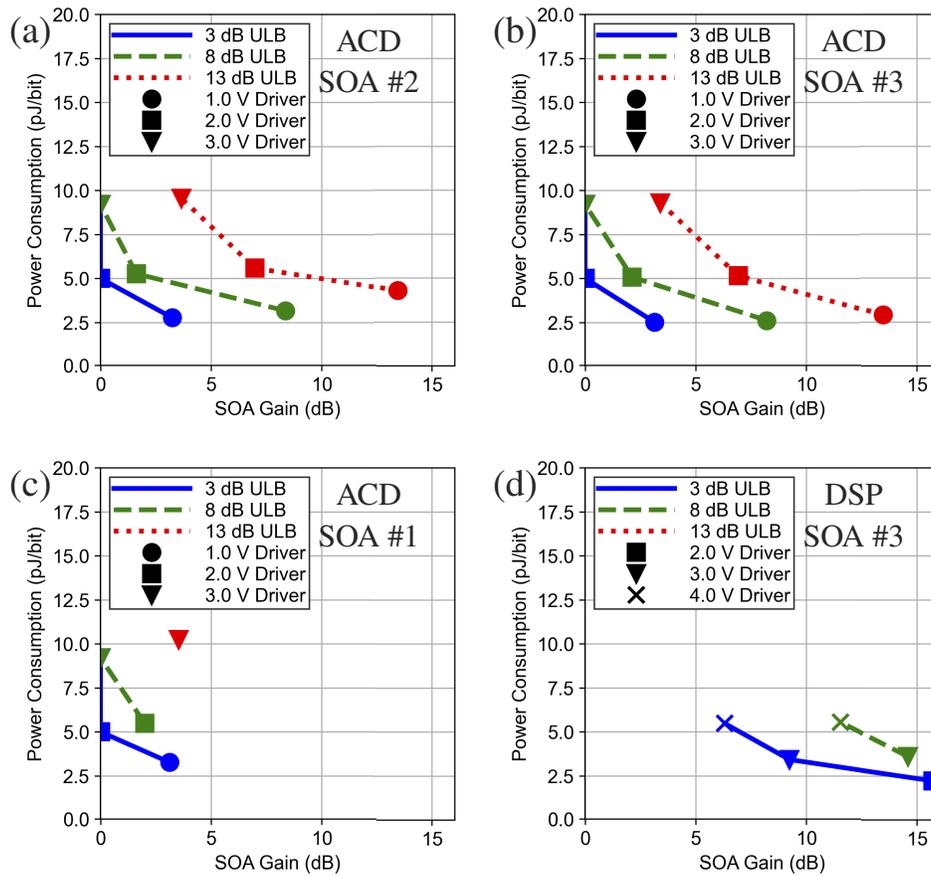


Fig. 3. Driver and SOA Power consumption vs. SOA gain for an ACD-based link with SOA in position #2 (a), #3 (b), and #1 (c), and for a DSP-based link with SOA in position #3 (d), where each curve corresponds to a particular supported ULB, and the differential peak-to-peak driver output voltages are marked.

architecture compared to one with SOAs in position #2 or #3, where the minimally saturated SOA gain enables 6 pJ/bit better power efficiency for link operation at 13 dB ULB. Links with SOAs in positions #4 or #5 were dominated by ASE noise at the receiver that was unattenuated by link losses, and did not see improved performance for the link parameters assumed here.

The shot, thermal, and ASE noise components, referred to the input of the receiver and corresponding to the plotted results in Fig. 3(b) and (d), are shown in Fig. 4(a) and (b), respectively. While the shot and thermal noise levels remain constant, the ASE noise varies strongly with SOA gain. The ASE noise in the DSP-based link simulations was comparable to the receiver shot and thermal noise levels, and the ACD-based link simulations had lower, although non-negligible ASE noise contributions. The power consumption vs SOA gain curves in Fig. 3(c-f) do not reach an optimized minimum, however, because they were limited by the 16 dB maximum gain determined by the SOA model parameters that were chosen for this analysis. A higher-gain SOA design could enable power efficiency improvement with increased ASE noise contribution at the optimal operating point. These results suggest that short-reach coherent links optimized for power efficiency will operate in a hybrid regime in which the shot, thermal, and ASE noise contributions are all appreciable. This is a notable departure from current conventional links, where long-reach coherent links are dominated by ASE noise and short-reach IMDD links

are dominated by receiver thermal noise. In describing the links that operate in this hybrid noise regime, receiver BER sensitivity can no longer be characterized solely with respect to either received optical power or OSNR, but now requires a combination of both optical power and ASE noise information.

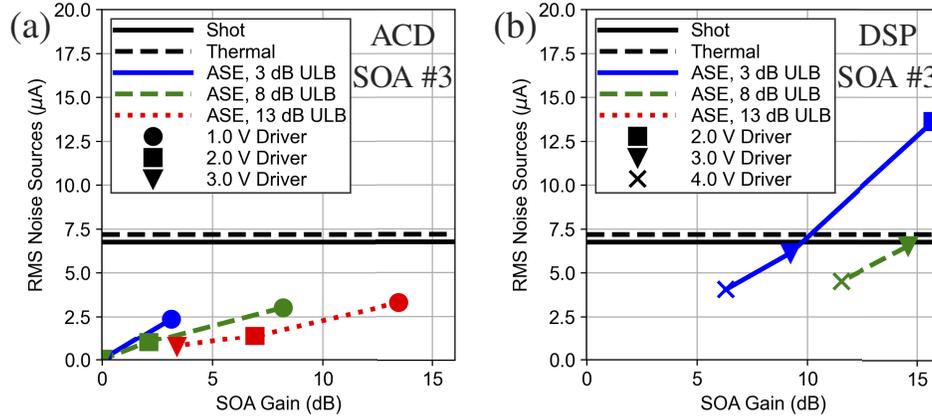


Fig. 4. RMS noise currents at the receiver vs position #3 SOA Gain for an ACD-based link (a) and a DSP-based link (b).

4.3. Optimization theory

The simulation results in Fig. 3 were carried out for discrete and somewhat arbitrary driver swing and SOA gain values. Those results showed that driver voltage and SOA gain can be traded off for improved power efficiencies and supported link budgets. Here, we will develop a theoretical model for continuous optimization by examining figures of merit (FOMs) for the driver and SOA link budget improvement per additional pJ/bit of power consumption. Optimal link operation will then be characterized by a set of driver swing and SOA gain operating points where the respective driver and SOA FOMs are equal.

For coherent modulation with an IQ-MZM, the driver swing determines the effective optical loss of the modulator, which is given by the modfactor

$$F_M = \sin\left(\frac{\pi V_{driver} L_{mod}}{4 V_{\pi} L}\right)^2 \quad (8)$$

where V_{driver} is the differential peak-to-peak driver output voltage swing, L_{mod} is the phase shifter length of one MZM arm, and $V_{\pi} L$ is the modulator phase efficiency. The modfactor describes the effective loss due to not driving a full $2V_{\pi}$ in the MZM transfer function. For 16QAM, due to the presence of lower power inner constellation points, the MZM effective loss is degraded by an additional static 2.55 dB. In this analysis, the modfactor loss directly corresponds to reduced available link budget. By defining $P_{driver}(V_{driver})$ as the driver power consumption in pJ/bit for a given driver voltage swing, converting the modfactor to dB, and differentiating, the driver figure of merit can be written as

$$\left. \frac{dF_M}{dP_{driver}} \right|_{dB} = \frac{5\pi}{\ln(10)F_M} \frac{L_{mod}}{V_{\pi} L} \sin\left(\frac{\pi V_{driver} L_{mod}}{4 V_{\pi} L}\right) \cos\left(\frac{\pi V_{driver} L_{mod}}{4 V_{\pi} L}\right) \frac{dV_{driver}}{dP_{driver}} \quad (9)$$

where the driver power consumption is modelled as shown in Eq. (6) and the differential is

$$\frac{dV_{driver}}{dP_{driver}} = \frac{1}{\sqrt{\frac{c_1^2}{Z_0^2} - \frac{4c_2(c_0 - P_d)}{Z_0}}} \quad (10)$$

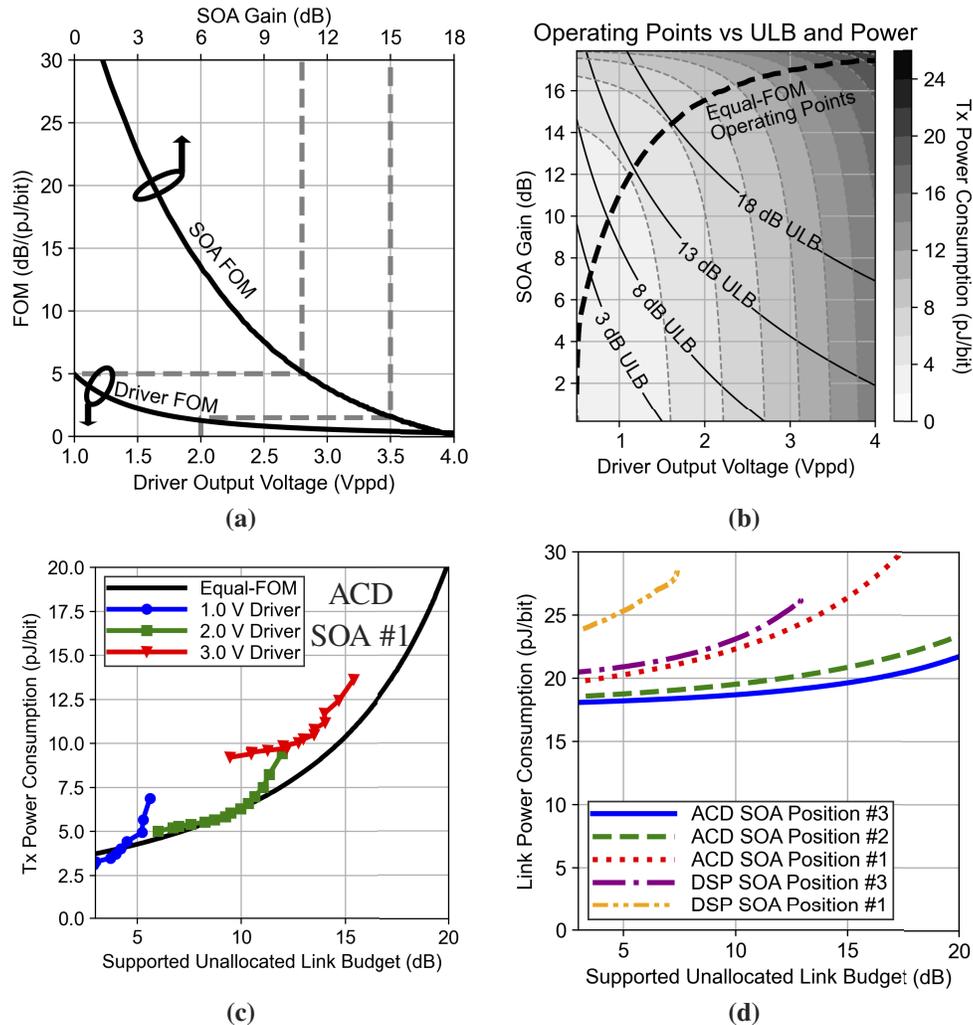


Fig. 5. Driver and SOA FOMs vs output voltage and gain operating points (a). Optimal equal-FOM operating points plotted with Tx power consumption and ULB contours for an ACD-based link with SOA in position #2 (b). Equal-FOM curve for an ACD-based link with SOA in position #1 vs. time-domain simulation results (c). Calculated full-link power consumption vs. ULB for multiple architectures (d).

A similar calculation can be carried out for an $FOM_{SOA} = dG/dP_{SOA}$, following well-known SOA gain and bias relationships [33]. The resulting power consumption and gain relationships are described by Eq. (7) and Fig. 2(f). These FOMs, with units of dB/(pJ/bit), quantify the marginal link budget improvement associated with a marginal increase in power expenditure in either the driver or SOA, enabling a comparison of the efficiency of each component. The final FOMs for the driver and SOA, plotted against the driver voltage swing and the SOA gain, for the parameters assumed in this paper for an ACD-based link, are shown in Fig. 5(a). In agreement with the simulation results in Fig. 3, it is clear that at low SOA gains, the ULB can be increased more efficiently by increasing SOA gain than by increasing driver swing. In fact, the FOM curves show that it is most efficient to raise the SOA gain to 11 dB before raising the driver swing above 1 Vppd, and again up to 15 dB before raising the driver swing past 2 Vppd.

This reasoning can be extended to form a continuous set of operating points where $FOM_{driver} = FOM_{SOA}$, yielding optimal link performance per watt. This equal-FOM curve is plotted in Fig. 5(b), along with a shaded contour map showing total driver and SOA power consumption and contour lines showing supported ULBs for each operating point. The equal-FOM operating points indeed achieve the minimum power consumption for each desired ULB. This theoretical analysis agrees well with time-domain simulation results for each of the link architectures reported above. The equal-FOM curve for an ACD-based link with and SOA in position #1 was normalized to the link receiver sensitivity and is shown in Fig. 5(c) alongside corresponding simulation results for power consumption vs. supported ULB for different driver voltages. This Equal-FOM analysis accurately describes optimally power efficient driver and SOA operating points, including SOA saturation effects.

5. Architectural comparisons

The results reported above show that integrated optical amplification in various configurations can improve short-reach coherent link power consumption, but the analysis has been confined to the power consumption changes in the drivers and SOAs alone. We will now consider the power consumption of the full link in order to compare the performance across various ACD- and DSP-based short-reach coherent links.

The estimated power consumption of all of the components of a short-reach coherent link, namely the lasers, thermo-electric coolers (TECs), transimpedance amplifiers (TIAs), biasing components, and DSP/CDR (clock data recovery) chips are shown in Table 2 for ACD-based and DSP-based links for two ULB cases. The numbers reported here do not consider any power supply overhead, which can be on the order of 10%. Driver and SOA power consumption was taken from Fig. 3, assuming SOAs in position #3. The DSP ASIC power consumption for the DSP-based coherent link is estimated from 400ZR DSP performance [34] scaled from 7 nm CMOS to 3 nm. DSP ASICs specifically tailored for short-reach applications could further improve power consumption substantially by removing CD and PMD compensation and optimizing equalizer implementations [5]. Since the ACD architecture employs limiting drivers and receivers and does not require polarization recovery or carrier recovery in DSP, power-hungry ADCs and digital-to-analog converters (DACs) can be eliminated and a greatly simplified CDR circuit can be used. Since such an ASIC tailored to ACD-based links does not yet exist, we estimate that it will consume half the power of a conventional coherent DSP chip, but have tabulated scenarios where ACD ASIC power consumption is either 1X, 0.75X, or 0.5X the conventional coherent DSP power consumption. The most aggressive scenario is based on removal of the ADCs/DACs, which account for roughly half the power consumption in the DSP ASIC for 400ZR [35], as well as the removal and simplification of dispersion compensation, equalization, carrier recovery, polarization recovery, and FEC blocks. As coherent DSPs scale to future CMOS nodes, DSP-based links will have more attractive power consumption, albeit with higher ASIC development costs. DSP-based 16QAM links also require half the quantity of lasers, modulators, and receivers as an ACD-based QPSK link with the same overall data rate, leading to cost and size advantages. DSP-based coherent links could also operate with QPSK modulation (for 200 Gbps/ λ with 50 Gbaud lanes), yielding similar link budget scaling and SOA noise tolerance as ACD-based links, with the additional improvements of DSP-based equalization. This approach would trade off power consumption, however, since it would require a full coherent DSP ASIC, including power hungry ADCs/DACs and linear drivers and TIAs, which are amortized over half as many bits, and so consume much more power. There are promising efforts to build efficient DSP-based QPSK links by leveraging higher baudrate signalling, laser sharing, and efficient limiting drivers to overcome these hurdles [35]. Full-link power consumption for several link architectures, calculated from optimal equal-FOM operating points derived in Section 4, and including the static contributions in Table 2, are shown in Fig. 5(d). An ACD-based coherent

link can improve power consumption by 2.5 and 8 pJ/bit over a DSP-based coherent link for 3 and 13 dB ULB, respectively.

Table 2. Full-link power consumption tabulation for short-reach coherent links.

Component	ACD-Based						DSP-Based	
	1X DSP Power		0.75X DSP Power		0.5X DSP Power			
DSP/CDR	10 pJ/bit		7.5 pJ/bit		5 pJ/bit		10 pJ/bit	
Lasers (with cooling)	6.5 pJ/bit						6 pJ/bit	
TIAs	1 pJ/bit						1.5 pJ/bit	
OPLL	1.5 pJ/bit						0 pJ/bit	
Biasing	2 pJ/bit						1 pJ/bit	
ULB	3 dB	13 dB	3 dB	13 dB	3 dB	13 dB	3 dB	13 dB
Drivers + SOAs	2.5 pJ/bit	3 pJ/bit	2.5 pJ/bit	3 pJ/bit	2.5 pJ/bit	3 pJ/bit	2.5 pJ/bit	8.5 pJ/bit
Total (pJ/bit)	23.5	24	21	21.5	18.5	19	21	27

Considering the power consumption of the transceivers themselves, however, does not capture their full impact on data center energy efficiency. The introduction of AWGRs or optical switches has the potential to reduce data center latency, and enable network topologies that can increase server utilization in high performance computing (HPC) and artificial intelligence (AI) clusters, and in the data center overall. These changes, which are only enabled by optical links that support higher link budgets, will directly impact overall data center efficiency. Networks with optical switching save power by reducing the total number of electrical switches and optical transceivers needed in the data center, directly improving effective transceiver energy efficiency by $>2X$ [11]. In addition, the network reconfiguration potential of optical switching is still being explored, but efficiency improvements of $>2X$ for the *overall* data center have been projected [15]. It is clear that modest increases in server utilization can lead to data center power savings greater than the total power consumption of all of the optical transceivers. Thus, optical transceivers that consume more power, but support ULBs that enable optical switching, could still bring about a more efficient overall data center.

As we have seen in Section 4, SOAs are a key enabler of efficient link operation with large ULBs. Links with SOAs in positions #2 and #3 supported higher ULBs than those with an SOA in position #1, despite any ISI penalties due to the SOA pattern effect and NLPN. Furthermore, ACD-based QPSK links are able to support higher ULBs than their DSP-based 16QAM counterparts, in part due to receiver sensitivity and SNR requirements [3], but also in part due to decreased susceptibility of QPSK signals to SOA NLPN. DSP-based SOA NLPN compensation algorithms exist, but come at the expense of additional DSP power consumption and complexity [25].

6. Conclusion

As per-wavelength data rate requirements for short-reach optical interconnects rise, coherent links will become an attractive option for intra-data center applications. The stringent power consumption and cost constraints placed on intra-data center links will require an evolution of conventional coherent link architectures and designs. SOAs integrated with coherent PICs enable link operation with reduced driver output voltages, supporting larger link budgets with reduced power consumption. Positioning SOAs after the Tx modulator results in the most improved link performance, with simulated power savings of 6 pJ/bit shown for a 13 dB ULB. Figures of merit for driver and SOA link budget improvement per additional unit of power consumption were

proposed and used to derive optimal driver and SOA operating points. For typical operating points, SOAs are more energy-efficient than drivers at increasing the link budget.

While DSP-based coherent architectures using 16QAM modulation benefit from SOA gain, their performance is hampered by SOA NLPN. Due to its quasi-constant power envelope, QPSK-based modulation is more tolerant to SOA saturation effects, making ACD-based coherent links that use power-efficient limiting drivers and TIAs especially attractive for short-reach coherent links with large ULBs. Since optical amplification can efficiently increase the supported link budget, it enables the inclusion of AWGRs or optical switches, which can revolutionize data center networks and improve overall server utilization and energy efficiency. Integrated optical amplification is the key to meeting link performance and energy efficiency targets for intra-data center coherent optical interconnects.

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Design of mode-locked semiconductor laser comb-based analog coherent links

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Abstract—Multi-wavelength analog coherent links using mode-locked laser (MLL) frequency combs as transmitter and local oscillator (LO) sources are proposed. Carrier recovery (CR) in all wavelength channels is achieved using only two optical phase-locked loops (PLLs), while polarization demultiplexing and static phase offset removal are performed using cascaded optical phase shifters. A three-section Fabry-Perot semiconductor laser structure is proposed for the comb sources. Phase-error performance in a 2.6 Tb/s system using 56-Gbaud dual-polarization quadrature phase-shift keying on 13 channels is studied. For optical and microwave beat linewidths of 2 MHz and 1 kHz, respectively, achieving phase-error penalties below 1.5 dB requires PLL delays below 400 ps. A symmetric CR scheme is shown to achieve better phase-error performance than an asymmetric CR scheme. In 13-channel analog coherent links, the MLL comb-based design is projected to consume 38% less power than a resonator-enhanced electro-optic comb-based design and 20% less power than a design using arrays of single-wavelength lasers as transmitter and LO sources, excluding modulator driver power, which is identical for the three designs.

Index Terms—Carrier phase recovery, coherent detection, data center optical links, optical frequency comb, semiconductor mode-locked laser.

I. INTRODUCTION

As data center links scale to higher bit rates, novel architectures that may improve density, spectral efficiency, receiver sensitivity and energy efficiency become important to study. In coherent optical links, a received signal is mixed with a strong local oscillator (LO), improving receiver sensitivity [1] and increasing link budget [2]. A coherent receiver can detect information encoded in all degrees of freedom of the signal field [3], enabling use of spectrally efficient modulation formats, such as dual-polarization (DP) phase-shift keying (PSK) or quadrature amplitude modulation.

Optical frequency combs obviate the need for multiple discrete lasers in wavelength-division-multiplexed (WDM) links. In addition, combs may simplify carrier recovery (CR) in coherent receivers [4]. Electro-optic (EO) transmitter and LO combs can be synchronized by transmitting a pilot tone to injection lock the LO seed laser, which is then used to generate an LO comb [5]. Using a pilot tone, however, leaves parts of the signal spectrum unmodulated, reducing overall spectral efficiency. Joint CR schemes using digital signal processing (DSP) exploiting phase coherence between comb lines have also been considered for comb-based links [6]. Employing high-speed DSP may, however, increase power consumption, which is not ideal for power-constrained data center systems.

Resonator-enhanced (RE) EO combs are promising candidates for coherent data center links with simplified carrier

recovery. RE-EO combs fabricated on thin-film lithium niobate (TFLN) offer wide, flat spectra that may support numerous wavelength channels [7]. The phase noise of the EO comb lines is completely determined by two random variables. The seed laser phase noise is common to all comb lines, while the microwave oscillator phase noise varies linearly with the comb line index [8]. An RE-EO comb-based analog WDM coherent receiver exploits these phase noise characteristics to perform CR using only two phase-locked loops (PLLs), which control the seed laser phase noise and the the microwave oscillator phase noise, respectively [9]. A potential drawback of EO comb-based coherent transceivers is the need to integrate ultra-low-loss EO materials, such as TFLN, on silicon photonics platforms. RE-EO comb generators also suffer from inefficient conversion of seed laser power to comb output power [10]. Moreover, when a RE-EO comb is used inside a PLL, its resonator-based structure adds to the round-trip delay [9].

Semiconductor mode-locked lasers (MLLs) provide another option for comb-based links. They can be realized using III-V materials, which can be heterogeneously integrated onto silicon photonics platforms [11]. Previous work has demonstrated phase synchronization of a passively MLL to a stable reference laser on an integrated platform [12]. Two independent MLLs have been synchronized by injection locking an LO MLL to two adjacent modes of a signal MLL [13]. Coherent WDM data transmission using MLLs as both transmitter and LO has been demonstrated, using offline DSP to perform CR through a blind phase search algorithm [14].

Actively and hybridly MLLs are more stable sources than passively MLLs [15], owing to the forcing effect of microwave modulation. The modulation also provides a means for synchronizing two MLLs, similar to the synchronization of two EO combs [9]. This paper studies phase synchronization between hybridly MLLs generating the transmitter and LO combs in a WDM link to enable coherent detection of all the channels. All the comb lines are synchronized using just two optical PLLs, while polarization recovery is performed using cascaded phase shifters driven by marker tone detection. The proposed scheme can be implemented using analog circuitry, obviating the need for high-speed analog-to-digital converters (ADCs), which account for a significant portion of power consumption in DSP-based coherent transceivers [16], [17]. Moreover, in multi-wavelength DSP-based coherent links, the number of ADCs required scales linearly with the number of wavelength channels. The proposed analog coherent design may therefore be preferable to DSP-based designs in power-constrained links [18]–[20].

The comb-based architecture proposed here is similar to the

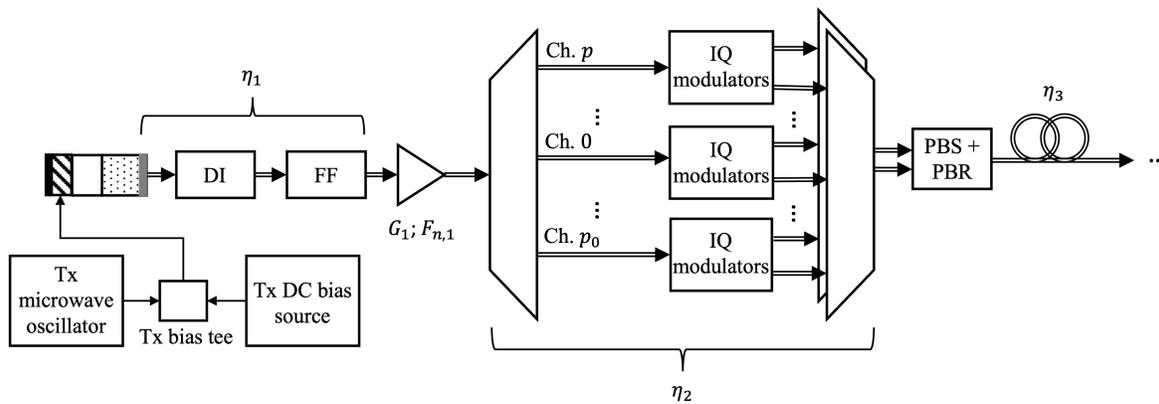


Fig. 1. MLL comb-based transmitter. A semiconductor MLL acting as a multi-wavelength source has a gain section (dotted fill), a phase-tuning section (no fill), and a saturable absorber section (striped fill). The saturable absorber section is reverse biased and modulated by a microwave source to enact hybrid mode locking. DC biases to the gain and phase-tuning sections are not shown. Tx: transmitter, DC: direct current, DI: de-interleaver, FF: flattening filter, Ch.: channel, IQ: in-phase and quadrature, PBS/R: polarization beam splitter/rotator.

RE-EO comb-based architecture proposed in [9]. This paper nevertheless makes several novel contributions: (1) it presents a hybridly MLL design based on a three-section Fabry-Perot structure appropriate for control by two PLLs in a shared CR scheme; (2) it proposes a symmetric CR configuration that achieves lower phase error between signal and LO than the asymmetric CR configuration studied in [9]; and (3) it draws detailed comparisons between MLL and RE-EO comb generators as sources in WDM analog coherent links, and compares these comb-based designs to those using arrays of single-wavelength lasers.

The remainder of this paper is organized as follows. Section II presents two semiconductor MLL comb-based analog coherent link designs using different CR schemes and analyzes their phase-error performance. It also presents a semiconductor MLL structure compatible with the proposed comb-based CR schemes. Section III studies an exemplary system, quantifying key performance metrics, including phase error, link SNR budget and the effect of chromatic dispersion. Section IV addresses third-order nonlinear effects on phase noise, compares MLL and RE-EO combs as sources for WDM analog coherent links, and studies the power consumption of such links using comb or single-wavelength laser sources. Section V presents conclusions.

II. PROPOSED TRANSCEIVER DESIGN

In this section, we provide an overview of the proposed MLL-based analog coherent transceiver and provide a framework for analyzing the system phase-noise performance.

A. Overview

Throughout this paper, the MLL comb lines are indexed by an integer p , where $-p_0 \leq p \leq p_0$. The index $p = 0$ corresponds to the central channel, while the indices $p = \pm p_0$ corresponds to the outermost channels.

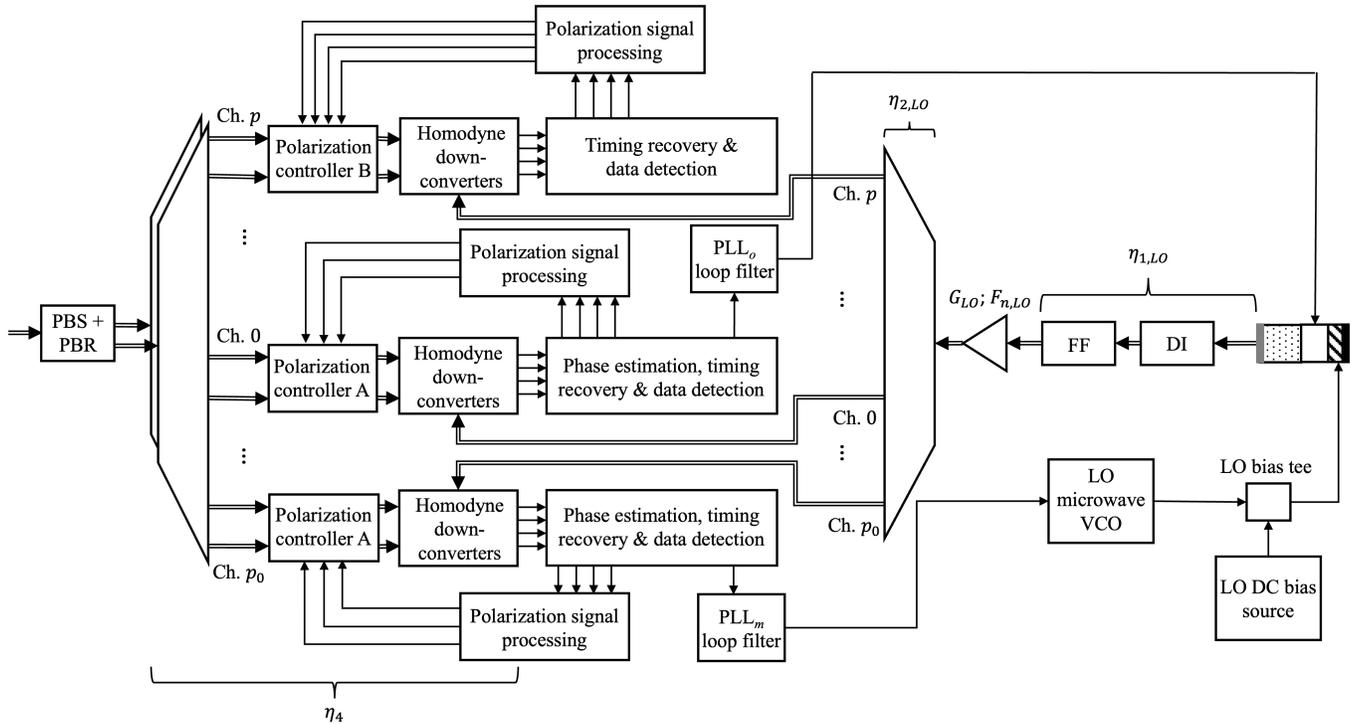
Figure 1 shows the transmitter, which uses an MLL comb as a multi-wavelength optical source. The comb may pass through a de-interleaver (DI), a flattening filter (FF), and a

semiconductor optical amplifier (SOA) before data modulation. The DI ensures a sufficiently large channel spacing when the MLL comb spacing is too small to accommodate the symbol rate.

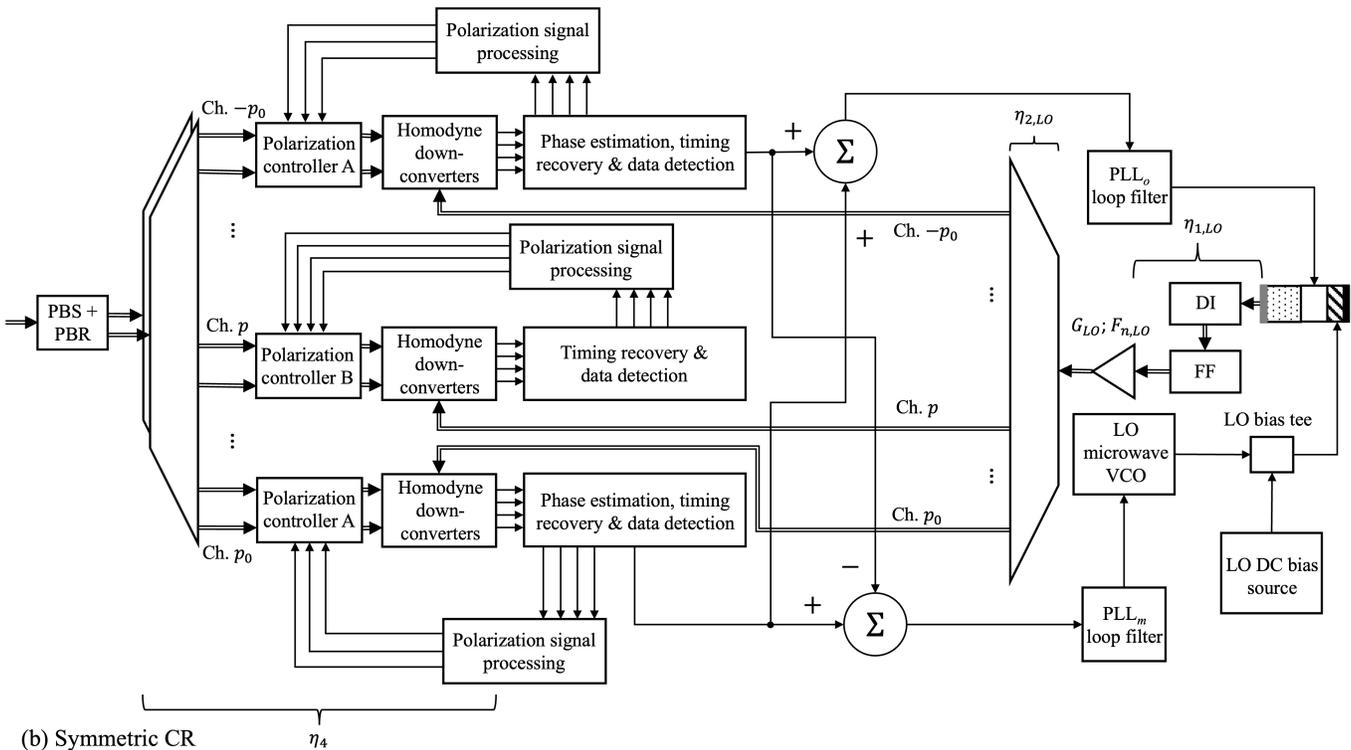
Figure 2 shows two candidate receiver designs. Each design uses an MLL comb, nominally identical to the transmitter comb, as a multi-wavelength LO source, and uses two PLLs to perform CR for all the data-bearing channels. The two designs differ in the channels on which phase estimation is performed. The asymmetric CR design in Figure 2(a) makes phase estimates on channels 0 and $+p_0$, while the symmetric CR design in Figure 2(b) makes phase estimates on channels $-p_0$ and $+p_0$. In each design, the index p corresponds to any of the channels not used for phase estimation. Both designs employ optical polarization controllers based on cascaded phase shifters [18]. In each design, the two channels used for phase estimation employ type A controllers, which compensate only for polarization changes, while the other channels employ type B controllers, which compensate for polarization changes and static phase shifts [9]. Polarization varies with a timescale of several milliseconds on link lengths of tens of kilometers [21]. This variation becomes slower with shorter link lengths [22]. Polarization signal processing can therefore be driven by low-speed circuitry [18]. The phase shifters are adjusted using a marker tone detection algorithm described in [9].

The MLL design shown in Figure 3 is proposed for the transmitter and receiver comb sources. A linear Fabry-Perot cavity has a high-reflectivity (HR) coating on one end and a low-reflectivity (LR) etched facet ($R \approx 32\%$) on the other. The cavity comprises three sections: (1) an active gain (G) section, (2) a phase-tuning (PT) section made of passive waveguide material and (3) a saturable absorber (SA) section made of reverse-biased active gain material. A microwave signal is superposed on a reverse bias to the SA section to enact hybrid mode locking [23].

The MLL output spectrum contains lines at frequencies $f_o + pf_m$ for integer values of the comb line index p . The optical frequency f_o is the frequency of the 0-th comb line, and coincides with the nominal comb center frequency. Under



(a) Asymmetric CR



(b) Symmetric CR

Fig. 2. Two configurations for the MLL comb-based analog coherent receiver. Each uses two PLLs to perform CR, and uses polarization controllers of type A or B to perform polarization recovery and remove static phase offsets [9]. The MLL has a gain section (dotted fill), a phase-tuning section (no fill) that determines the comb center frequency, and a microwave-modulated saturable absorber section (striped fill) that determines the comb spacing. A DC bias to the gain section is not shown. In the (a) asymmetric CR configuration, phase estimation is performed on channels 0 and p_0 , and the comb line index p corresponds to any of the other channels. In the (b) symmetric CR configuration, phase estimation is performed on channels $-p_0$ and p_0 , and the comb line index p corresponds to any of the other channels. PBS/R: polarization beam splitter/rotator, VCO: voltage-controlled oscillator.

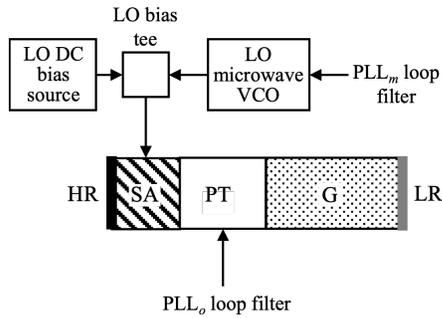


Fig. 3. Proposed MLL design (shown as used in generating the receiver LO comb). The MLL employs a three-section Fabry-Perot cavity with a high-reflectance (HR) coating and a low-reflectance (LR) etched facet ($R \approx 32\%$) on its ends. A gain (G) section comprises active gain material. A phase-tuning (PT) section comprises passive material, and receives a control current from PLL_o to lock the comb center frequency f_o . A saturable absorber (SA) section comprises active gain material. It is reverse biased and modulated by a microwave voltage-controlled oscillator (VCO) to enact hybrid mode locking. The microwave VCO receives feedback from PLL_m to lock the comb spacing f_m . A DC bias to the gain section is not shown.

hybrid mode locking, the microwave modulation frequency f_m determines the comb spacing, and should coincide approximately with the cavity free spectral range (FSR).

The MLL design in Figure 3 is designed specifically to be driven by two optical PLLs in the receiver. A first PLL, PLL_o, drives the PT section to control f_o , locking the common optical frequency and phase of the LO comb to those of the transmitter comb. The microwave modulation to the SA section is provided by a voltage controlled oscillator (VCO). A second PLL, PLL_m, drives the VCO to control f_m , locking the frequency spacings and relative phases in the LO comb lines to those in the transmitter comb.

In the following subsection, we study the phase noise of the MLL-based combs.

B. Phase Noise Analysis

The MLL in Figure 3 has a modulated SA at one end of the cavity, similar to the device studied by Ho [24]. Ho demonstrates that under hybrid mode locking, the phase noise on the p -th comb line is given by

$$\varphi_p(t) = \sum_{n=0}^{\infty} A_n(t) H_n \left(\frac{\sqrt{2}p}{P} \right), \quad (1)$$

where P is the number of locked modes (or comb lines), and $H_n(x)$ is the n -th order Hermite polynomial. The $A_n(t)$ are expansion coefficients, which are computed by solving mode-locking equations [25] under noise perturbations. As shown by Ho, $\varphi_p(t)$ can be well-approximated by the first two terms of (1):

$$\begin{aligned} \varphi_p(t) &\approx A_0(t) + A_1(t) \cdot \frac{2\sqrt{2}p}{P} \\ &= \varphi_o(t) + p\varphi_m(t). \end{aligned} \quad (2)$$

In the second line of (2), we have defined an optical phase noise $\varphi_o(t) = A_0(t)$, which is common to all the comb lines, and a microwave phase noise $\varphi_m(t) = \frac{2\sqrt{2}}{P}A_1(t)$, whose

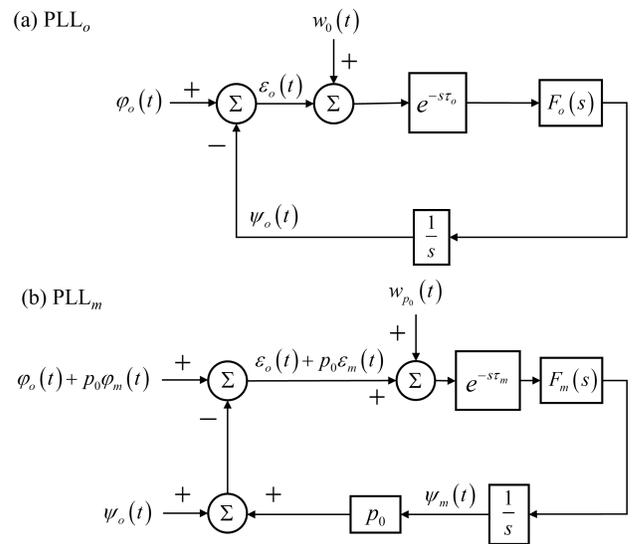


Fig. 4. Asymmetric CR receiver configuration: linearized models of (a) PLL_o and (b) PLL_m.

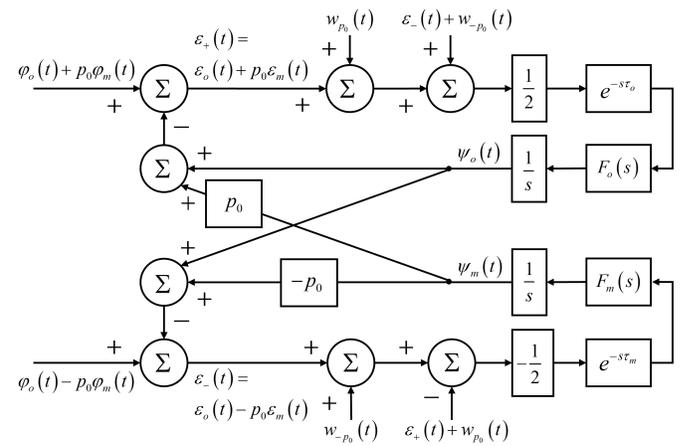


Fig. 5. Symmetric CR receiver configuration: linearized models of PLL_o and PLL_m.

contribution to the total phase noise (2) varies linearly with comb line index p .

The optical phase noise $\varphi_o(t)$ is a Wiener process [26], which we characterize by an optical linewidth $\Delta\nu_o$. In hybridly and passively MLLs, the microwave phase noise $\varphi_m(t)$ is also a Wiener process [27], which we characterize by a microwave linewidth $\Delta\nu_m$. The p -th comb line has a linewidth $\Delta\nu_p = \Delta\nu_o + p^2\Delta\nu_m$, which varies quadratically with comb line index p [28]. The phase noise model (2), containing a common term and a term varying linearly with comb line index, giving rise to a linewidth varying quadratically with comb line index, is consistent with other work [26], [29].

The two phase noise processes, $\varphi_o(t)$ and $\varphi_m(t)$, motivate the use of two PLLs, PLL_o and PLL_m, in the MLL-based analog coherent receiver, as shown in Figure 2. The PLLs in Figures 2(a) and 2(b) can be studied using the linear models in Figures 4 and 5, respectively.

The models employ the following notation:

- 1) $\varphi_o(t)$ and $\varphi_m(t)$ now denote the combined optical

and microwave phases noises of the transmitter and LO combs, which are Wiener processes. $\Delta\nu_o$ and $\Delta\nu_m$ now denote the beat linewidths of these combined phase noises.

- 2) $\psi_o(t)$ is the optical control phase of the LO MLL, induced by the PLL_o loop filter driving its PT section. $\psi_m(t)$ is the microwave control phase of the LO MLL, induced by the PLL_m loop filter driving the VCO modulating its SA section. The total control phase on the p -th LO comb line is $\psi_p(t) = \psi_o(t) + p\psi_m(t)$.
- 3) $w_i(t)$ are the additive white Gaussian noise (AWGN) components on the channels from which the PLLs derive their phase estimates. For QPSK, they have two-sided power spectral densities

$$S_{w_i w_i}(\omega) = \frac{T_s}{2\gamma_i} \quad \text{for } i \in \{0, \pm p_0\}, \quad (3)$$

where γ_i is the symbol signal-to-noise ratio (SNR) on the i -th channel and T_s is the symbol interval [3].

- 4) τ_o and τ_m are the path delays of PLL_o and PLL_m, respectively.
- 5) $F_o(\omega)$ and $F_m(\omega)$ are the second-order loop filter transfer functions for PLL_o and PLL_m, respectively. They are defined as

$$F_i(\omega) = 2\zeta\omega_{n,i} + \frac{\omega_{n,i}^2}{j\omega} \quad \text{for } i \in \{o, m\}, \quad (4)$$

where $\omega_{n,o}$ and $\omega_{n,m}$ are the natural frequencies of their associated PLLs, and $\zeta = 1/\sqrt{2}$.

- 6) $\varepsilon_o(t) = \varphi_o(t) - \psi_o(t)$ and $\varepsilon_m(t) = \varphi_m(t) - \psi_m(t)$ are, respectively, the optical and microwave phase errors between the transmitter and LO MLL combs. The total phase error on the p -th channel is $\varepsilon_o(t) + p\varepsilon_m(t)$.

The phase-error standard deviation on the p -th channel can be written as $\sqrt{\sigma_{\varepsilon_o}^2 + p^2\sigma_{\varepsilon_m}^2}$, where $\sigma_{\varepsilon_o}^2$ and $\sigma_{\varepsilon_m}^2$ are the variances of $\varepsilon_o(t)$ and $\varepsilon_m(t)$, respectively. Using the linear models in Figures 4 and 5, we can find expressions for $\sigma_{\varepsilon_o}^2$ and $\sigma_{\varepsilon_m}^2$ for the asymmetric and symmetric CR configurations. Assuming all the channels used for phase estimation have the same SNR (i.e., $\gamma_0 = \gamma_{\pm p_0}$), we can express the optical phase-error variance as

$$\sigma_{\varepsilon_o}^2 = \frac{\pi\Delta\nu_o}{2\zeta\omega_{n,o}}\Gamma_o^{\text{PN}}(\omega_{n,o}\tau_o) + \frac{(1+4\zeta^2)\omega_{n,o}T_s}{4\zeta} \frac{1}{2n_{\text{PE}}n_c\gamma_0}\Gamma_o^{\text{AWGN}}(\omega_{n,o}\tau_o). \quad (5)$$

In (5), n_{PE} is the number of polarizations used in phase estimation [18]. We assume $n_{\text{PE}} = 2$. The variable n_c captures the difference between the two receiver CR configurations. In the asymmetric CR scheme, $n_c = 1$, while in the symmetric CR scheme, $n_c = 2$. $\Gamma_o^{\text{PN}}(\omega_n\tau)$ and $\Gamma_o^{\text{AWGN}}(\omega_n\tau)$ are given by

$$\Gamma_o^{\text{PN}}(\omega_n\tau) = \frac{2\zeta\omega_n}{\pi} \int_{-\infty}^{\infty} |j\omega + e^{-j\omega\tau}F_o(\omega)|^{-2} d\omega \quad (6)$$

$$\Gamma_o^{\text{AWGN}}(\omega_n\tau) = \frac{2\zeta}{\pi(1+4\zeta^2)\omega_n} \int_{-\infty}^{\infty} \left| \frac{F_o(\omega)}{j\omega + e^{-j\omega\tau}F_o(\omega)} \right|^2 d\omega \quad (7)$$

The microwave phase-error variance $\sigma_{\varepsilon_m}^2$ can likewise be found using the linear models in Figures 4 and 5:

$$\sigma_{\varepsilon_m}^2 = \frac{\pi\Delta\nu_m}{2\zeta\omega_{n,m}}\Gamma_m^{\text{PN}}(\omega_{n,m}\tau_m) + \frac{(1+4\zeta^2)\omega_{n,m}T_s}{4\zeta} \frac{1}{2n_{\text{PE}}n_c\gamma_0}\Gamma_m^{\text{AWGN}}(\omega_{n,m}\tau_m) \quad (8)$$

where $\Gamma_m^{\text{PN}}(\omega_n\tau)$ and $\Gamma_m^{\text{AWGN}}(\omega_n\tau)$ are given by

$$\Gamma_m^{\text{PN}}(\omega_n\tau) = \frac{2\zeta\omega_n}{\pi} \int_{-\infty}^{\infty} |j\omega + p_0e^{-j\omega\tau}F_m(\omega)|^{-2} d\omega \quad (9)$$

$$\Gamma_m^{\text{AWGN}}(\omega_n\tau) = \frac{2\zeta}{\pi(1+4\zeta^2)\omega_n} \int_{-\infty}^{\infty} \left| \frac{F_m(\omega)}{j\omega + p_0e^{-j\omega\tau}F_m(\omega)} \right|^2 d\omega \quad (10)$$

In the following section, we study the performance of the MLL-based analog coherent receiver with a design example.

III. DESIGN EXAMPLE

In this section, we study a multi-wavelength system operating in the O-band, using dual-polarization quadrature phase-shift keying (DP-QPSK) at 56 GBaud symbol rate. The comb spans of integrated semiconductor MLLs are typically limited to tens of nanometers by gain bandwidth and waveguide dispersion [30]. For instance, [31] reports a span of roughly 13 nm for an InGaAsP/InP quantum well device. We conservatively assume a comb span of 1 THz (about 6 nm) and a comb spacing of 40 GHz for the transmitter and LO MLLs. Using DIs to keep only even-indexed comb lines, the system provides 13 data-modulated channels at a channel spacing of 80 GHz. The outermost channels correspond to comb line indices of $\pm p_0 = \pm 12$.

We assume a pre-forward error correction (FEC) bit-error ratio (BER) of 2.4×10^{-4} , which applies to FEC codes including RS(544, 514). Achieving the target BER requires an SNR per symbol of 10.6 dB for QPSK on an ideal AWGN channel [3]. Considering overhead, the system provides a net bit rate of 2.6 Tb/s.

A. Phase Error

To keep the SNR penalty due to phase error below 1.5 dB, the phase-error standard deviation on each channel should not exceed 7.4° for QPSK [32]. We assume the beat optical linewidth of the transmitter and LO combs is $\Delta\nu_o = 2$ MHz. This is achievable using the linear cavity design shown in Figure 3 [12]. Similar linewidths have been reported for InAs/InP Fabry-Perot devices [33]. The microwave linewidth

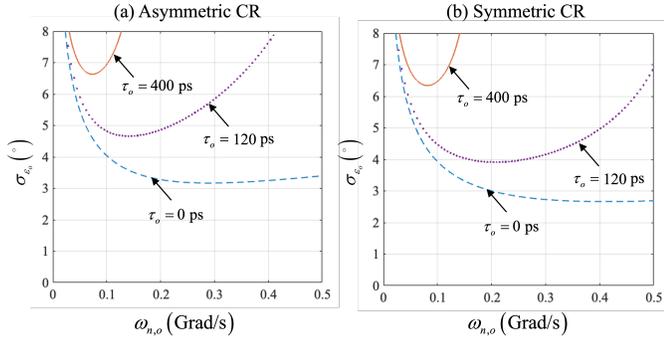


Fig. 6. Optical phase-error standard deviation σ_{ε_o} versus PLL_o natural frequency $\omega_{n,o}$ at two values of the loop delay τ_o . The beat optical linewidth is $\Delta\nu_o = 2$ MHz and the SNR per symbol is $\gamma_o = 10.6$ dB. When $\tau_o = 120$ ps, at the optimal $\omega_{n,o}$, σ_{ε_o} is 4.66° for the asymmetric CR scheme and 3.91° for the symmetric CR scheme. When $\tau_o = 400$ ps, at the optimal $\omega_{n,o}$, σ_{ε_o} is 6.62° for the asymmetric CR scheme and 6.34° for the symmetric CR scheme.

of actively or hybridly MLLs can be lower than 100 Hz [34], [35]. We assume the beat microwave linewidth of the transmitter and LO combs is $\Delta\nu_m = 1$ kHz. The corresponding microwave phase noise of each comb exceeds that of a low-power monolithic VCO in a similar frequency range [36]. We consider two choices for the delays, τ_o and τ_m . The first choice, $\tau_o = \tau_m = 120$ ps, corresponds to the minimum delay achieved in a single-wavelength PLL in photonic integrated circuits (PICs) [37], and represents a lower bound for comb-based integrated PLLs. The second choice, $\tau_o = \tau_m = 400$ ps, corresponds to the maximum value for which the comb-based analog coherent receiver can achieve a phase-error penalty below 1.5 dB, as explained below.

Figure 6 shows the optical phase-error standard deviation σ_{ε_o} against $\omega_{n,o}$, the natural frequency of PLL_o, for different values of the loop delay τ_o , for the asymmetric and symmetric CR designs at $\gamma_o = 10.6$ dB. For $\tau_o = 120$ ps, at the respective optimal values of $\omega_{n,o}$, the asymmetric scheme achieves an optical phase-error standard deviation of $\sigma_{\varepsilon_o} = 4.66^\circ$, while the symmetric scheme achieves $\sigma_{\varepsilon_o} = 3.91^\circ$. For $\tau_o = 400$ ps, the asymmetric scheme achieves an optical phase-error standard deviation of $\sigma_{\varepsilon_o} = 6.62^\circ$, while the symmetric scheme achieves $\sigma_{\varepsilon_o} = 6.34^\circ$. Figure 7 shows received DP-QPSK signal constellations in the central channel ($p = 0$) without and with CR by PLL_o.

Figure 8 shows the microwave phase-error standard deviation on the p_0 -th channel, $p_0\sigma_{\varepsilon_m}$, against $\omega_{n,m}$, the natural frequency of PLL_m, for different values of the loop delay τ_m , for the asymmetric and symmetric CR designs at $\gamma_o = 10.6$ dB. In Figure 8, for $\tau_m = 120$ ps, at the respective optimal values of $\omega_{n,m}$, the asymmetric scheme achieves $p_0\sigma_{\varepsilon_m} = 1.90^\circ$, while the symmetric scheme achieves $p_0\sigma_{\varepsilon_m} = 1.41^\circ$. For $\tau_m = 400$ ps, the asymmetric scheme achieves $p_0\sigma_{\varepsilon_m} = 2.12^\circ$, while the symmetric scheme achieves $p_0\sigma_{\varepsilon_m} = 1.72^\circ$.

We will choose p_0 to be an outermost channel, i.e., $|p| \leq |p_0|$ for all p . In that case, the total phase-error standard deviation on the p -th channel, $\sqrt{\sigma_{\varepsilon_o}^2 + p^2\sigma_{\varepsilon_m}^2}$, will not exceed that on the p_0 -th channel, which is $\sqrt{\sigma_{\varepsilon_o}^2 + p_0^2\sigma_{\varepsilon_m}^2}$. Assuming

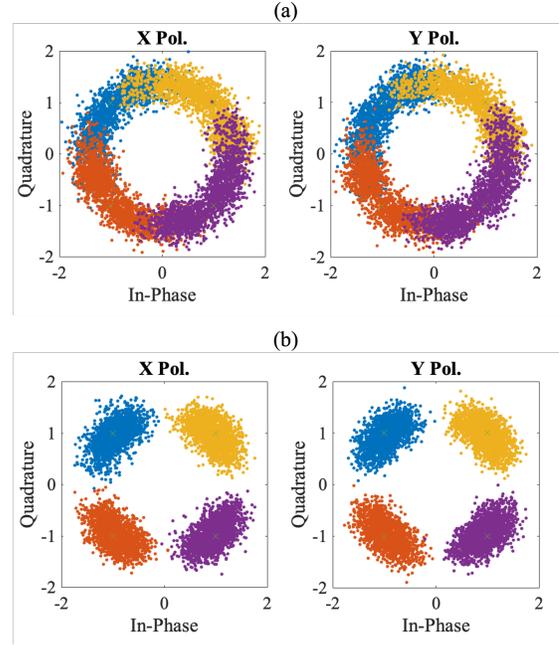


Fig. 7. Received DP-QPSK constellation diagrams in the central channel ($p = 0$) (a) without and (b) with CR by PLL_o, over an interval of 8192 symbol periods.

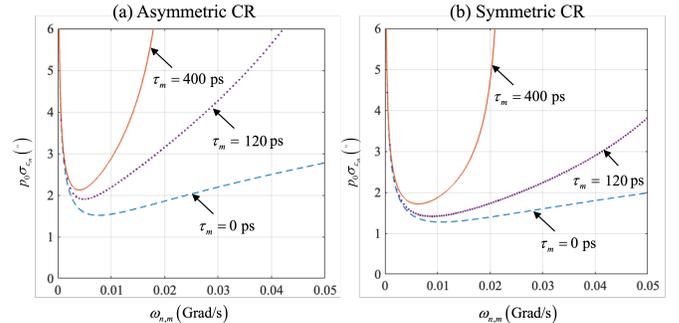


Fig. 8. Microwave phase-error standard deviation $p_0\sigma_{\varepsilon_m}$ on the p_0 -th channel versus PLL_m natural frequency $\omega_{n,m}$ at two values of the loop delay τ_m . The beat microwave linewidth is $\Delta\nu_m = 1$ kHz and the SNR per symbol is $\gamma_o = 10.6$ dB. When $\tau_m = 120$ ps, at the optimal $\omega_{n,m}$, $p_0\sigma_{\varepsilon_m}$ is 1.90° for the asymmetric CR scheme and 1.41° for the symmetric CR scheme. When $\tau_m = 400$ ps, at the optimal $\omega_{n,m}$, $p_0\sigma_{\varepsilon_m}$ is 2.12° for the asymmetric CR scheme and 1.72° for the symmetric CR scheme.

the loop delays are $\tau_o = \tau_m = 400$ ps, the total phase-error standard deviation on any channel will not exceed 7.0° in the asymmetric receiver configuration and 6.6° in the symmetric receiver configuration. Both the asymmetric and symmetric CR schemes yield phase-error SNR penalties below 1.5 dB.

To maintain low phase-error standard deviation, both schemes require the loop delays, τ_o and τ_m , to not exceed 400 ps. Optical PLLs on PICs locking independent lasers have achieved loop delays as low as 120 ps [37]. The PLLs in the MLL comb-based receiver contain similar components, with the addition of an arrayed waveguide grating (AWG) for demultiplexing the LO comb. Calculations based on optical path length suggest that compact SiN AWGs can have delays of roughly 100 ps [38]. This suggests that loop delays as small

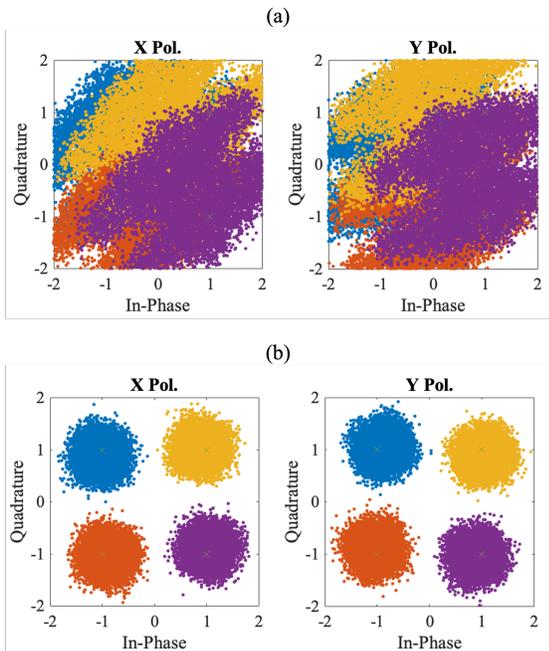


Fig. 9. Received DP-QPSK constellation diagrams (a) without and (b) with polarization recovery and phase offset removal by a type B polarization controller.

as about 220 ps are achievable with MLL comb-based systems.

As explained in Section II-A, polarization recovery and compensation of static phase offsets are achieved using phase shifter-based polarization controllers [9]. Figure 9 shows the received DP-QPSK constellations without and with polarization control and static phase offset removal by a type B controller.

B. Chromatic Dispersion

Monte Carlo link simulations assuming 5-th order Bessel transmitter and receiver responses with bandwidths equal to 0.7 times the baud rate are performed to determine the tolerable dispersion for QPSK. For a penalty less than 1 dB with a target BER of 2.4×10^{-4} , the accumulated dispersion must be limited to $|DL| \leq 25$ ps/nm. In standard single-mode fiber with 13 channels with 80-GHz spacing centered at 1310 nm, this corresponds to a dispersion-limited transmission distance of about 100 km.

C. Signal-to-Noise Ratio

The target BER of 2.4×10^{-4} requires an SNR per symbol of 10.6 dB on an ideal AWGN channel. Allowing penalties for phase error, chromatic dispersion, polarization recovery [9] and linear crosstalk at 80-GHz channel spacing of 1.5 dB, 1.0 dB, 0.5 dB and 0.5 dB, respectively, we desire to operate at an SNR per symbol of 14.1 dB. Additive noises in the comb-based link include thermal noise, shot noise, noise arising from the LO beating with amplified spontaneous emission (ASE) on the signal, and noise arising from the signal beating with ASE on the LO [9].

Table I lists link parameters used to compute SNR per symbol. Values are taken from the references listed in the

TABLE I
LOSS, GAIN AND POWER VALUES FOR EXEMPLARY MLL COMB-BASED SYSTEM.

Laser-to-PIC coupling loss, DI IL, and FF IL ($\eta_1, \eta_{1,LO}$)	5.5 dB	[39], [40]
Tx (de-)multiplexing, and DP-IQ modulation loss (η_2)	8 dB	[16], [41]
LO de-multiplexing, and downconversion loss ($\eta_{2,LO}$)	7.5 dB	[16]
Channel loss (η_3)	10 dB	[42]
Rx de-multiplexing, polarization controller, and downconversion loss (η_4)	10 dB	[16]
Booster amplifier 1 gain (G_1)	16 dB	N/A
LO booster amplifier gain (G_{LO})	14 dB	N/A
Booster amplifier noise figure ($F_{n,1}, F_{n,LO}$)	7 dB	[43]
Lowest Tx MLL output comb line	-2 dBm	N/A
Lowest LO MLL output comb line	0 dBm	N/A

rightmost column of Table I. For instance, the first row assumes insertion losses (ILs) or coupling losses of 3 dB, 0.5 dB, and 2 dB for the DI, FF, and MLL-to-PIC coupling. The fourth row assumes a channel loss of 10 dB, corresponding to a fiber length of about 28 km. Link performance is limited by the channel using the comb line with the lowest power. The last two rows of Table I therefore use the lowest comb line powers of the respective combs.

The SOA gain values are picked to ensure sufficient SNR to meet the target BER. Both SOAs in the transceiver are operated in saturation. The impact of SOA saturation is discussed in Section IV-A. The values from Table I result in a worst-case SNR per symbol of 17.8 dB. The net unallocated link margin is 3.7 dB.

IV. DISCUSSION

In the first subsection below, we discuss the effects of nonlinearities induced by gain saturation in the SOAs. Then, in the next three subsections, we compare MLL and RE-EO comb-based links in terms of comb span, optical linewidth and power consumption. These comparisons refer to Table II, which summarizes high-level differences between the two comb generators. In the final subsection, we compare asymmetric and symmetric CR schemes.

A. Semiconductor Optical Amplifier Saturation

Saturated operation of an SOA causes nonlinear effects [1]. In particular, four-wave mixing (FWM) generates components at the nominal comb frequencies $\omega_o + p\omega_m$, which may include $|p| > p_0$, corresponding to frequencies not present in the MLL output. The comb spectrum at the SOA output can be computed accurately using the model in [44], informing the design of the FFs shown in Figures 2(a) and (b).

Under FWM, the model (2) for the phase noise on the p -th comb line remains valid. If comb lines at frequencies $\omega_i = \omega_o + p_i\omega_m$, $\omega_j = \omega_o + p_j\omega_m$, and $\omega_k = \omega_o + p_k\omega_m$ undergo FWM, components are generated at frequencies $\omega_{ijk+} = \omega_i + \omega_j - \omega_k = \omega_o + (p_{ijk+})\omega_m$ and $\omega_{ijk-} = \omega_i - \omega_j + \omega_k = \omega_o + (p_{ijk-})\omega_m$, where $p_{ijk+} = p_i + p_j - p_k$ and

TABLE II
COMPARISON OF MLL AND RE-EO COMBS FOR WDM ANALOG COHERENT LINKS

Comb Type	Span	Material	Optical Linewidth	Power Consumption
MLL	About 1 THz	III-V semiconductor	Hundreds of kHz to MHz	32.5 (8.6) W
RE-EO	More than 1 THz	TFLN	Follows seed laser	37.9 (14.0) W

* Power consumptions are quoted for 13-channel links at 56 GBaud using DP-QPSK modulation. Values in parentheses exclude modulator driver power consumption, which is identical for the two link designs.

$p_{ijk-} = p_i - p_j + p_k$ are the comb line indices of the FWM-generated components. These components will have phase noises $\varphi_o(t) + (p_{ijk+})\varphi_m(t)$ and $\varphi_o(t) + (p_{ijk-})\varphi_m(t)$, respectively, matching the predictions of the phase noise model (2).

B. Comb Span

The comb span of semiconductor MLLs is limited by the active material gain bandwidth and by cavity dispersion effects. The MLL design proposed in Figure 3 has a comb span of approximately 1 THz in the O-band [45]. The comb span could be broadened by inserting a gain-flattening filter and/or dispersion-compensating filter in the cavity [45], [46]. Inserting these devices, however, would increase the round-trip cavity loss, increasing the phase noise. The gain bandwidth might alternatively be widened by using quantum-dot or quantum-dash active materials [47].

RE-EO comb generators also have output spectra that roll off away from the central comb line, but can achieve larger comb spans up to several THz [48]. Furthermore, such devices can be designed with the resonator FSR slightly detuned from the modulation frequency defining the comb spacing, such that the output spectrum only spans the desired comb lines [49]. For example, if only 25 comb lines are desired, the resonator FSR can be chosen so the output spectrum is concentrated in lines with indices $-12 \leq p \leq 12$.

While the wider bandwidth of an RE-EO comb may accommodate more data channels than an MLL comb, with either comb type, the number of data channels may be constrained by a limited total comb output power, or by the saturation output power of the SOA amplifying the comb output [9].

C. Optical Linewidth

The optical linewidth $\Delta\nu_o$ is a key parameter governing the phase-error performance of analog coherent receivers.

Semiconductor MLL combs can achieve optical linewidths in the hundreds of kHz to MHz range [30], but the optical linewidth depends on the cavity losses and other characteristics of the MLL comb-generating structure. As observed in the previous subsection, intracavity gain flattening or dispersion compensation may widen the comb span, but the consequent increased loss is likely to broaden the optical linewidth.

The optical linewidth of an RE-EO comb is determined by the linewidth of the seed laser [8], decoupling the optical linewidth from the design of the comb-generating structure. At the transmitter, an RE-EO comb can be seeded by an external cavity laser [50] having a linewidth as narrow as required. At the receiver, the LO comb seed laser should have a sufficiently narrow linewidth, while also having a

frequency modulation (FM) bandwidth sufficient to achieve low loop delay in the receiver optical PLL [9]. A two-electrode distributed-feedback laser [51], with a linewidth of hundreds of kHz and FM bandwidth of hundreds of MHz, is a good candidate to satisfy these requirements [9]. This decoupling of the optical linewidth from the comb-generating structure makes the RE-EO comb a strong candidate for scaling to higher-order modulation formats, such as 16-QAM [9].

D. Power Consumption

In this subsection, we compare the power consumption of MLL and RE-EO comb-based analog coherent links to their counterparts employing arrays of separate lasers. All three link designs support 13 channels modulated at 56 GBaud by DP-QPSK, as assumed in Section III above. The analysis assumes equal power per channel at the Tx demultiplexer outputs in all three link designs, and at the Rx demultiplexer outputs in all three link designs.

Link power consumption is divided into four categories: (1) transmitter (Tx) optics, (2) Tx electronics, (3) receiver (Rx) optics, and (4) Rx electronics. In the comb-based designs, Tx optics includes the power required for the Tx MLL or seed laser and the Tx booster SOA, Tx electronics includes power required for the comb microwave modulation and data modulator driver circuits, and Rx optics includes power required for the LO MLL or seed laser and the LO booster SOA. In all three designs, Rx electronics includes the power required for the PLLs.

The power consumptions of the three link types are summarized in Table III. Details on the power consumption of the various components are provided in Appendix A. In Table III, the columns ‘‘Tx Optics Cooling’’ and ‘‘Rx Optics Cooling’’ assume electrical power not converted to optical power is dissipated locally as heat. Assuming thermoelectric cooling of optical components, the dissipated power P_d is related to the thermoelectric cooler (TEC) power consumption P_{TEC} by the TEC coefficient of performance $\eta_{TEC} = P_d/P_{TEC}$, where a value $\eta_{TEC} = 1$ is assumed. Tracking power consumption throughout the link indicates that cooling roughly doubles the overall power consumption of optical components, consistent with thermal management observations in data centers [52].

As observed in Table III, the power consumed by the Tx and Rx optics and cooling in the MLL comb-based link (0.8 W + 0.8 W + 0.8 W + 0.8 W = 3.2 W) is less than in the RE-EO comb-based link (1.1 W + 1.4 W + 1.1 W + 1.4 W = 5.0 W), because in the RE-EO comb generator, conversion of seed light to usable comb lines is lossy and requires a high seed laser power. Moreover, the power consumed by the Tx electronics is lower in the MLL comb-based link than in the RE-EO comb-

TABLE III
POWER CONSUMPTION SUMMARY

Source	Tx Optics	Rx Optics	Tx Optics Cooling	Rx Optics Cooling	Tx Electronics	Rx Electronics	Total
MLL Comb	0.8	0.8	0.8	0.8	24.1 (0.2)	5.2	32.5 (8.6)
RE-EO Comb	1.1	1.4	1.1	1.4	25.9 (2.0)	7.0	37.9 (14.0)
Laser Array	0.4	0.4	0.4	0.4	23.9 (0.0)	9.1	34.6 (10.7)

* Power values are in units of W. Values in parentheses exclude modulator driver power consumption, which is identical for the three designs.

based link, because the SA in the MLL comb requires lower microwave drive power than the phase modulator in the RE-EO comb.

The laser array-based link consumes less power in its Tx and Rx optics and cooling (0.4 W + 0.4 W + 0.4 W + 0.4 W = 1.6 W) than the MLL or RE-EO comb-based links, as seen in Table III. Separate lasers can emit at higher power per wavelength than a frequency comb [50], and power is not lost from comb generation, de-interleaving, and flattening, so the laser array-based link avoids the power consumption associated with booster SOAs. Nevertheless, the MLL comb-based link has lower total power consumption (32.5 W) than the laser array-based link (34.6 W). Excluding modulator driver power, which is identical for the three link designs, the MLL comb-based link power consumption (8.6 W) is substantially lower than that for the laser array-based link (10.7 W). The MLL comb-based link saves power by a reduction in receiver complexity enabled by the phase-coherent combs. The comb-based analog coherent receivers use only two PLLs to achieve CR for 13 channels, while the laser array-based link needs 13 PLLs. This power savings in the MLL-comb-based link more than compensates for the power consumed by comb modulation and booster SOAs. The RE-EO comb-based link consumes more total power than the other two designs, owing especially to the high comb modulation power needed.

The power consumption of the comb-based analog coherent transceiver may be further reduced by decreasing losses associated with de-interleaving and flattening, as well as coupling and insertion losses. These improvements may be enabled by future progress in semiconductor MLL and PIC technologies. Progress in low-drive-power integrated modulators [53] can decrease the power consumption of all three link designs, increasing the fractional power savings for both MLL and RE-EO comb-based links.

E. Carrier Recovery Scheme

In Section III.A, the symmetric CR scheme was shown to achieve a lower phase-error standard deviation than the asymmetric CR scheme considering the optical and microwave phase noises in (2). As explained here, the symmetric CR scheme is also more robust to phase noise contributions that vary with higher powers of p , which are predicted by the infinite summation (1) derived by Ho [24]. For example, including terms up to $n = 2$ in (1), the combined phase noise of the transmitter and LO combs on the p -th comb line has the form

$$\varphi_p(t) = \varphi_o(t) + p\varphi_m(t) + p^2\varphi_2(t), \quad (11)$$

where $\varphi_2(t)$ is a higher-order phase noise term and the optical phase noise $\varphi_o(t)$ now includes a contribution from the $n = 2$ term in (1).

We neglect the AWGN $w_i(t)$ and loop path delays τ_o and τ_m for simplicity. Although the PLL phase detectors make noiseless measurements of the phase errors, the PT section and the microwave VCO driving the SA section in the LO MLL are constrained to effect a control phase of the form $\psi_p(t) = \psi_o(t) + p\psi_m(t)$, which varies only linearly with the comb line index p . In the symmetric CR scheme, the total LO control phase on the p -th comb line will be $\psi_p(t) = (\varphi_o + p_0^2\varphi_2) + p\varphi_m$, while in the asymmetric CR scheme, the total LO control phase will be $\psi_p(t) = \varphi_o + p(\varphi_m + p_0\varphi_2)$. We find that for $p \in [-p_0, p_0]$, the maximum absolute deviation of the symmetric CR control phase from the true phase noise is $\varphi_2 p_0^2$ at $p = 0$, while the maximum absolute deviation of the asymmetric CR control phase from the true phase noise is $2\varphi_2 p_0^2$ at $p = -p_0$, which is twice that for the symmetric CR scheme.

While the symmetric CR scheme is superior to the asymmetric CR scheme in use with the MLL comb generator, it may typically not be well-suited for use with the RE-EO comb generator. In the symmetric CR scheme, the loop delay τ_o in PLL_o includes any time needed for changes in injection current to be seen by the outermost comb lines with indices $p = \pm p_0$. In the MLL comb, adjustments to the PT section injection current affect the frequencies of all comb lines simultaneously. By contrast, in the RE-EO comb, the time delay in frequency shifting seed laser light to the p -th comb line scales as pT , where T is the resonator round-trip time, since the p -th comb line corresponds to light that has traveled p times around the phase-modulated resonator [9]. In the design example of [9], where $T = 20$ ps and $p_0 = 16$, the symmetric CR design would add over 300 ps to the loop delay τ_o , degrading the PLL phase-error performance.

V. CONCLUSION

Multi-wavelength analog coherent transceivers using three-section Fabry-Perot MLLs as transmitter and LO comb sources, enabling CR for all wavelengths to be achieved using two optical PLLs, have been proposed. A symmetric CR scheme outperforms an asymmetric CR scheme in tolerance to optical and microwave phase noises, as well as possible higher-order phase noise.

MLL comb-based links have been compared to analog coherent links using RE-EO combs or arrays of single-wavelength lasers as transmitter and LO sources. The MLL comb-based design offers the lowest overall power consump-

TABLE IV
TX OPTICS POWER TRACKING

Element	Source	Input Optical Power	Input Electrical Power	Output Optical Power
Laser ($\eta_{laser}=15\%$)	MLL Comb	0	150	23
	RE-EO Comb	0	520	78
	Laser Array	0	430	65
SOA ($G_1 = 20$ dB; $\eta_{SOA}=15\%$)	MLL Comb	2.3	600	92
	RE-EO Comb	2.3	600	92
	Laser Array	N/A	N/A	N/A
Total	MLL Comb		750	
	RE-EO Comb		1100	
	Laser Array		430	

* Power values are in units of mW.

TABLE V
RX OPTICS POWER TRACKING

Element	Source	Input Optical Power	Input Electrical Power	Output Optical Power
Laser ($\eta_{laser}=15\%$)	MLL Comb	0	250	37
	RE-EO Comb	0	820	120
	Laser Array	0	430	65
SOA ($G_{LO}=14$ dB; $\eta_{SOA}=15\%$)	MLL Comb	3.7	590	92
	RE-EO Comb	3.7	590	92
	Laser Array	N/A	N/A	N/A
Total	MLL Comb		840	
	RE-EO Comb		1400	
	Laser Array		430	

* Power values are in units of mW.

tion, owing to its requirement for only two PLLs and the higher efficiency of the MLL comb compared to the RE-EO comb.

MLL comb-based transceivers are promising candidates for integration in silicon photonics, exploiting rapid advances in heterogeneous integration technologies. Reduced passive optical losses and improved MLL comb flatness may further reduce power consumption. Scaling MLL comb-based links to higher channel counts and higher-order modulation formats will likely require novel solutions to increase the MLL comb span without increasing its optical linewidth.

RE-EO combs, by contrast, benefit from a decoupling of the optical linewidth from the comb-generating structure, facilitating a simultaneous scaling to higher channel counts and higher-order modulation formats. Nevertheless, the power consumption of RE-EO comb-based links is increased by requirements for high microwave modulation power and high seed laser power. Their low-cost implementation will likely require advances in integration of ultra-low-loss EO materials, such as TFLN, in silicon photonics platforms.

APPENDIX A POWER CONSUMPTION ANALYSIS

The power consumed by active optical components in the Tx and Rx in the three link designs is detailed in Tables IV and V, respectively. Each active optical element receives input optical and/or electrical power, and outputs optical power. In the rows labeled “Laser”, the seed laser of the RE-EO comb has a wall-plug efficiency (WPE) of 15% [54]. The conversion of seed laser light to the central 25 comb lines has an efficiency of about 30% [49]. Power loss associated with de-interleaving, flattening, and coupling before amplification is estimated as 9.9%. This results in 2.3 mW of optical power at the Tx SOA

input and 3.7 mW at the Rx SOA input for the RE-EO comb link, as indicated. The WPE of the MLL laser is estimated as 15% [30]. The power loss associated with de-interleaving, flattening, and coupling before amplification is estimated as 9.9%, similar to the RE-EO comb link. This results in 2.3 mW of optical power at the Tx SOA input and 3.7 mW at the Rx SOA input for the MLL comb link, as indicated. In the laser array-based link, the total laser output power is 65 mW at both the Tx and Rx so the power per channel at the output of the Tx and Rx demultiplexers is the same for all three link designs. The Tx and Rx SOAs are assumed similar to the device in [44], which has an estimated a WPE of 15%. Link losses used to compute the power input and output at each active optical component are consistent with values stated in Table I and used in the SNR calculation in Section III-C.

TABLE VI
TX ELECTRONICS POWER TRACKING

Element	Source	Power Consumed	Reference
Comb Modulation	MLL Comb	0.20	[35]
	RE-EO Comb	2	[48]
	Laser Array	N/A	
Data Modulation	MLL Comb	23.9	[55]
	RE-EO Comb	23.9	
	Laser Array	23.9	
Total	MLL Comb	24.1	
	RE-EO Comb	25.9	
	Laser Array	23.9	

* Power values are in units of W.

The power consumed by electrical components in the Tx and Rx in the three link designs is detailed in Tables VI and VII, respectively. In the rows labeled “Comb Modulation”, the microwave power needed to phase modulate the RE-EO

TABLE VII
RX ELECTRONICS POWER TRACKING

Element	Source	Power Consumed	Reference
Comb Modulation	MLL Comb	0.20	[35]
	RE-EO Comb	2	[48]
	Laser Array	N/A	
Receiver Chip	MLL Comb	5.0	[20]
	RE-EO Comb	5.0	
	Laser Array	9.1	
Total	MLL Comb	5.2	
	RE-EO Comb	7.0	
	Laser Array	9.1	

* Power values are in units of W.

comb is estimated to be 2 W [48]. The microwave power needed to modulate the SA section of the MLL comb in hybrid mode locking is estimated to be 200 mW [12]. In the row labeled “Data Modulation” in Table VI, the IQ modulator is assumed to consume about 8.2 pJ/bit [55], corresponding to 23.9 W for 13 channels employing DP-QPSK modulation at 56 GBaud. The row labeled “Receiver Chip” in Table VII includes the receiver chain, comprising a transimpedance amplifier (TIA), a variable-gain amplifier (VGA), and an output buffer (OB), as well as the PLL circuitry. Two polarizations are assumed to be used in phase estimation. The power consumption of the receiver chain is estimated to be 330 mW per channel, while that of each PLL circuit is estimated as 370 mW [56]. In comb-based links, each channel requires a receiver chain, but only two PLLs are required. This results in $(370 \text{ mW} \times 2 + 330 \text{ mW} \times 13) \approx 5.0 \text{ W}$ power consumption for the receiver chip, as indicated in Table VII. In laser array-based links, each channel requires a receiver chain and a PLL. This results in $(370 \text{ mW} \times 13 + 330 \text{ mW} \times 13) \approx 9.1 \text{ W}$ power consumption for the receiver chip.

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A 224 Gbps/ λ O-Band Coherent Link for Intra-Data Center Applications

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Abstract:

We present the first >200 Gbps/ λ O-band optical link with integrated transmitter and receiver photonic and electronic ICs. 224 Gbps/ λ DP-QPSK transmission is demonstrated below the $3.8 \cdot 10^{-3}$ HD-FEC threshold with 6.8 pJ/bit power consumption. © 2023 The Author(s)

1. Introduction

As transceiver data rates continue to rise, coherent links are becoming increasingly attractive for replacing intensity modulation direct detection (IMDD) links inside data centers [1]. However, the characteristically high power consumption and cost of coherent links impede widespread adoption for short-reach applications. We have proposed an analog coherent detection (ACD)-based architecture that enables low-power coherent link operation by removing power-hungry DSP functions that are required for longer-reach conventional coherent links [2]. Transitioning from C-band to O-band operation eliminates the need for chromatic dispersion (CD) compensation in short-reach intra-data center links. O-band coherent transmitter (Tx) PICs (photonic integrated circuits) [3] and receiver (Rx) ICs [4] have been reported, and we previously demonstrated the first full O-band coherent link with integrated Tx and Rx PICs and EICs (electronic integrated circuits) [5]. In this work, we present a 224 Gbps/ λ dual-polarization quadrature phase shift keying (DP-QPSK) link in the O-band with dual-polarization operation below the $3.8 \cdot 10^{-3}$ HD-FEC threshold. To our knowledge, this is a record single- λ data rate for an O-band link, either coherent or IMDD, that includes integrated photonics and electronics from the driver input to the Rx EIC output.

2. Design

The Tx and Rx PICs in this work were fabricated in Intel's silicon photonics process. Dual-polarization in-phase and quadrature Mach-Zehnder modulator (DP-IQ MZM) PIC operation with the DP-IQ MZM driver EIC, which was fabricated in GlobalFoundries 9HP 90 nm BiCMOS process, was previously reported in [5]. The DP coherent receiver PIC was packaged with a transimpedance amplifier (TIA) EIC fabricated in GlobalFoundries 45RFSOI 45 nm CMOS process. The PIC includes an integrated analog polarization controller circuit that allows for optical domain manipulation and demultiplexing of the received polarization channels. The Rx EIC is based on a record low-power inverter shunt-feedback TIA, and was previously reported in [6]. The total power consumptions of the Tx and Rx ICs were 1.3 W and 0.2 W, or 5.9 pJ/bit and 0.9 pJ/bit at 224 Gbps, respectively. PICs and EICs for both Tx and Rx were packaged on FR4 PCBs with wirebonded high-speed connections. In future designs, wavelength division multiplexing (WDM) can scale the transceiver data rate with 4 λ s for 800G or 8 λ s for 1.6T.

3. Results

A diagram of the link measurement setup and images of the packaged Tx and Rx are shown in Fig. 1(a) and (b), respectively. Since first-generation PICs that do not include integrated optical gain were used, a distributed feedback laser (DFB) (AeroDIODE 1310LD-4-1-1) was split into signal and local oscillator (LO) paths in a self-homodyne configuration. A bit-pattern generator (BPG) (SHF 12105A) drove the driver EIC with 500 mV PRBS15 signals, and a real-time oscilloscope (RTO) (Keysight UXR0702A) measured the receiver EIC output at 256 GSa/s with a 0.586 μ s acquisition time. Due to limited RTO channels, only one Rx polarization channel was measured at a time, and the coaxial cable connections were swapped to characterize the other polarization channel. The measured constellations were post-processed to apply static constellation rotation, equalization, and

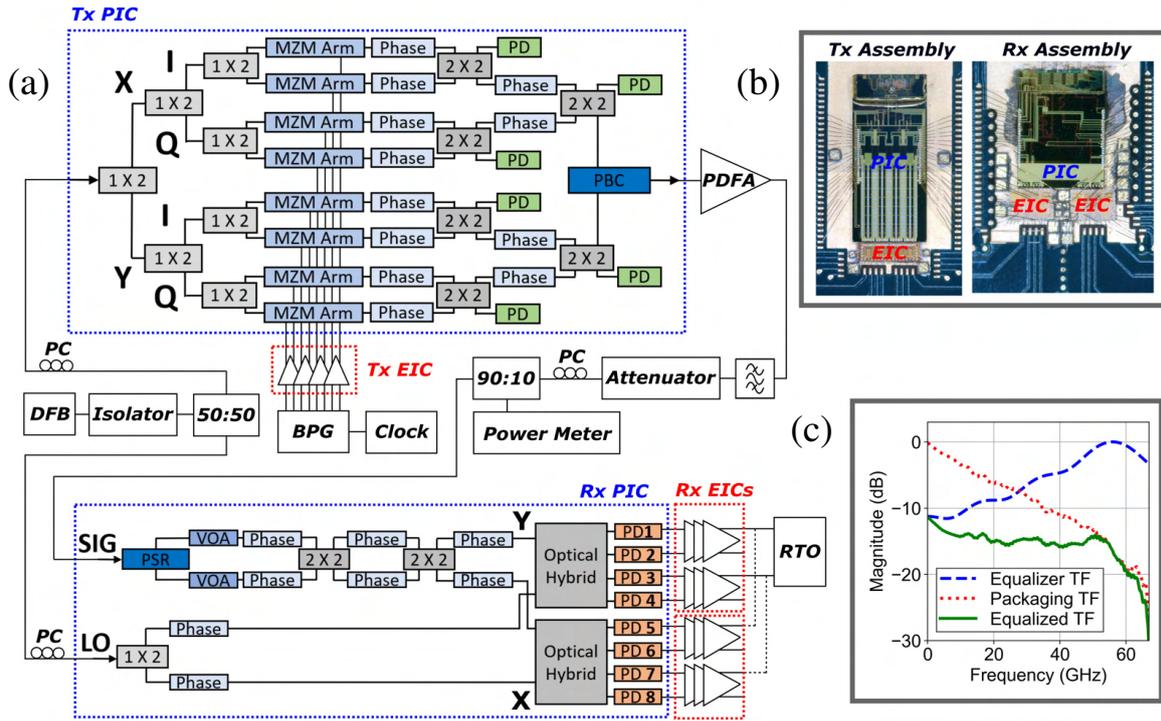


Fig. 1. (a) Block diagram of measurement setup and Tx and Rx PIC components. (b) The packaged Tx and Rx with custom EICs and PICs. (c) Measured packaging frequency response compared to post-processing equalizer and resulting equalized frequency responses.

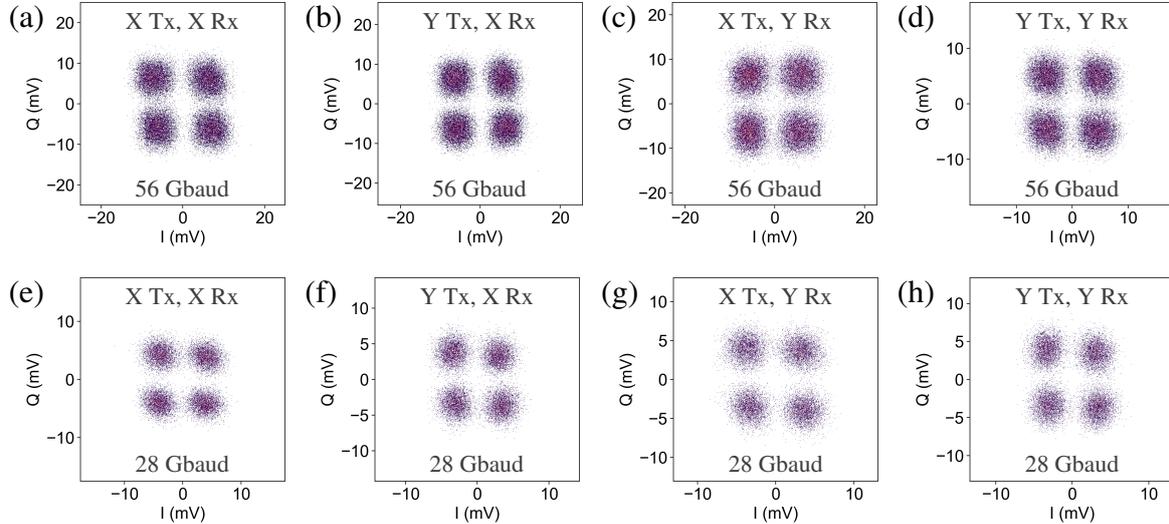


Fig. 2. Measured DP-QPSK constellations for (a-d) 56 Gbaud and (e-h) 28 Gbaud full-link operation. Individual constellations are shown for the X and Y polarization channels in the Tx and Rx.

sampling, and then to count bit errors. A 7-tap feed-forward equalizer (FFE) was used in post-processing to deembed the insertion loss due to Tx and Rx packaging. The packaging losses from the PCB microstrip transmission line, mini-SMP connector, and coaxial cables are unfortunately unavoidable for link characterization with a BPG and RTO, but they would not be present in an integrated transceiver module. As shown in Fig. 1(c), this equalizer does not compensate bandwidth impairments beyond measured off-chip packaging losses.

Constellations for full-link DP-QPSK transmission are shown in Fig. 2(a-d) for 56 Gbaud and Fig. 2(e-h) for 28 Gbaud. The on-chip polarization controller was used to switch between Rx polarization channels. A constel-

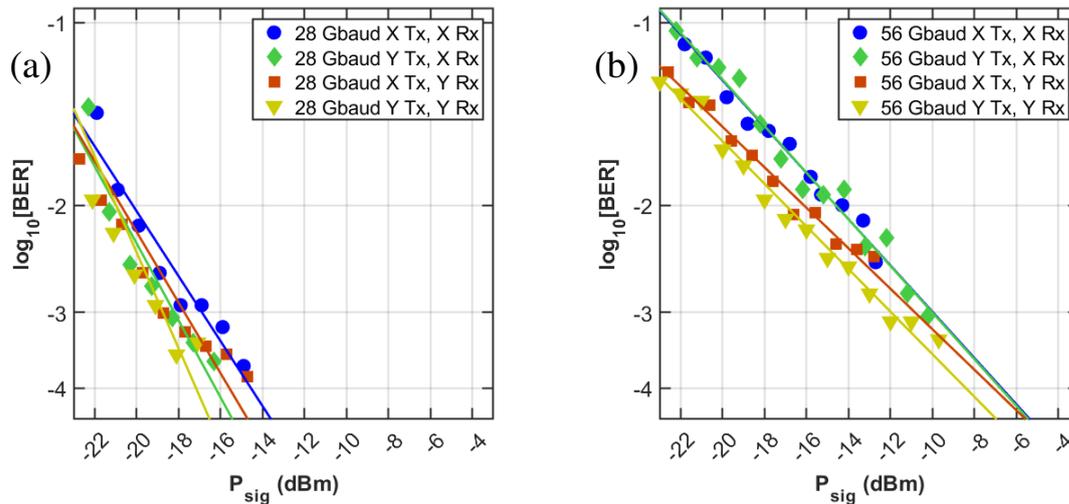


Fig. 3. Measured BER vs Rx input power for (a) 28 Gbaud and (b) 56 Gbaud DP-QPSK operation. Plotted trend lines are fit from the data.

lation is shown for each configuration of Tx and Rx X and Y polarization channels with operation below the $3.8 \cdot 10^{-3}$ HD-FEC threshold in each case. Corresponding BER sensitivity curves for each polarization configuration for 28 Gbaud and 56 Gbaud DP-QPSK are shown in Fig. 3(a) and (b), respectively. All of these measurements are for dual-polarization transmission in the presence of polarization crosstalk effects, with Rx input power reported as the power on the fiber of the polarization channel being measured and 3.8 dBm average LO power incident on each photodiode (PD).

4. Conclusion

We have demonstrated DP-QPSK link operation in the O-band at 224 Gbps/ λ (56 Gbaud) below the $3.8 \cdot 10^{-3}$ HD-FEC threshold. To our knowledge, this is the first demonstration of a >200 Gbps/ λ O-band optical link, either coherent or IMDD, that uses custom integrated electronics and photonics for the Tx and Rx. The link power consumption in this work was 1.5 W (6.8 pJ/bit), and <10 pJ/bit power consumption is expected for a next-generation link using PICs that include integrated optical gain. This result shows that O-band coherent links can support per- λ data rate scaling with attractive energy efficiency for future intra-data center networks.

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Toward GaSb-Based Monolithically Integrated Widely-Tunable Lasers for Extended Short- and Mid-Wave Infrared Wavelengths

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Abstract—A fully-functional photonic integrated circuit (PIC) platform with supporting active and passive components in the extended short- and mid-wave infrared spectral regime is of significant research interest for next-generation optical systems. Here we design offset quantum well-based photonic integrated circuits which primarily consist of four section-based widely tunable single-mode lasers emitting at 2560 nm. The platform requires the selective removal of InGaAsSb multi-quantum wells located above a GaSb-based optical waveguide layer and then subsequent single blanket GaSb regrowth. Encouraging preliminary experimental results on regrowth are also reported to confirm the feasibility of the proposed PICs. The simulation result for the tunable laser design shows that a tuning range as wide as ~ 120 nm is possible. The quasi-theoretical work performed here is an initial step towards demonstrating complex non-telecommunication PICs which could offer a comprehensive range of photonic functionalities.

Index Terms—Photonic integrated circuit, GaSb, S-MWIR, phase tuner, sampled-grating.

I. INTRODUCTION

RECENTLY, extended short- and mid-wave infrared (S-MWIR) spectral regimes have gained considerable attention to enable a whole range of emerging applica-

tions including biochemical sensing [1], [2], quantum sensing [3], industrial process control [4], and non-invasive medical diagnostics [5], [6]. The S-MWIR wavelength regime is important because it contains a number of spectral features such as strong overtones and a combination of molecular absorption bands in gas- and liquid-phase molecules for sensing applications [7], [8]. S-MWIR devices operating especially at the molecular fingerprint region, $2 \mu\text{m} < \lambda < 6 \mu\text{m}$ result in unprecedented sensitivity and selectivity when it comes to photonic sensors [9], [10]. This eye-safe spectral regime also has an atmospheric transmission window, which makes it suitable for light detection and ranging (LiDAR) or free-space communication applications [11].

Considering all these real-world applications, several discrete active [12] and passive [13], [14] photonic devices operating at the S-MWIR wavelength regime have been developed for years. However, little progress has been made in the development of PIC-compatible S-MWIR active devices, including broadband and continuously tunable lasers, and semiconductor optical amplifiers (SOAs), as well as their on-chip monolithic integration with passive devices. Highly-integrated S-MWIR PICs will not only provide low-size, -weight, -power and -cost (SWaP-C) advantages but also bring transformative changes to on-chip sensing applications.

For spectroscopy, conventional type-I diode lasers emitting at $2.2\text{--}3.4 \mu\text{m}$ [15], [16], [17] and interband cascade lasers (ICLs) at $3\text{--}6 \mu\text{m}$ [12], [18], [19], [20], [21] offer compelling SWaP-C reduction advantages over quantum cascade lasers (QCLs) that are a more mature technology for wavelengths $\lambda \geq 4.5 \mu\text{m}$ [22], [23]. In particular, type-I or ICLs in the S-MWIR regime consume nearly an order of magnitude less power than the power-hungry QCLs [24]. This is highly advantageous in handheld, battery-operated and even solar-powered photonic subsystems based on type-I lasers or ICLs. While QCLs can produce higher maximum output powers, this does not pose a problem for photonic sensors or spectrometers because typical type-I or ICL outputs on the order of mW are adequate for most absorption spectroscopy applications. Importantly, one key component of a PIC is an SOA, suggesting that the power output of a single laser is not necessarily the maximum output of the PIC.

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From the material perspective, even though gallium antimonide (GaSb) and its alloys are relatively less mature, they comprise the optimal material system for integrating 2.2-6 μm lasers on PICs. This contrasts with standard and mature material platforms such as InP, which experience a significant performance droop for gain chips at wavelengths $\geq 1.7 \mu\text{m}$. Although there are a few reports on InP-based lasers emitting up to 2.4 μm [25], [26], highly-strained type-I quantum wells as a gain medium were utilized in these studies. Hence, InP and its alloys are less attractive due to such material limitations for making high-performance PICs at the specified wavelength regime.

Widely-tunable lasers based on surface gratings are one of the basic and critical active components in realizing fully-functional PICs. Despite significant technological achievements in monolithic InP PICs with sampled-grating distributed Bragg reflector (SG-DBR)- [27] and ring resonator- [28] lasers at 1.55 μm over the past few decades, such a platform in the S-MWIR regime has not yet reached its full potential. A framework and clear roadmap for developing monolithic GaSb PICs using an ICL material system for the wavelength range of 3-6 μm has recently been reported [29]. Among basic optical passive components at S-MWIR, low-loss optical waveguides [13], [30], fiber-to-chip grating couplers [13], ring resonators [31], wavelength demultiplexers based on arrayed waveguide grating [14], [32] were developed using silicon-on-insulator (SOI) wafers that are transparent up to a wavelength of 4 μm [33]. There are also few demonstrations on heterogeneously integrated InP gain materials on silicon PICs reported around 2.3 μm wavelengths [34], [35], [36]. Recently, PICs have been demonstrated using heterogeneous integration of GaSb-active devices with SOI passive components. In particular, S-MWIR ICLs using GaSb were integrated on SOI through heterogeneous integration [37], [38], [39], [40]. Hybrid integration is another promising route, and GaSb/SOI hybrid tunable lasers with emission wavelengths up to 2.7 μm were reported [41]. Though a monolithic platform offers more flexibility and compactness, heterogenous- and hybrid- integration platforms provide several advantages, including low-loss waveguides, high-performance passives, high-coupling efficiency, and low-cost wafer-scale assembly.

By employing an InGaAsSb/AlGaAsSb/GaSb material and necessary processing steps, as well as by leveraging the technological advancement in the GaSb material system, developing S-MWIR PICs technology is possible. This paper will primarily discuss about the design of GaSb-based widely-tunable lasers by monolithically integrating functional components on the same substrate in order to have the greatest impact. SG-DBR lasers are four-section devices with four separate electrodes for controlling a gain section, a phase tuner and two mirrors which are connected by waveguides – yielding a small version of complete PICs. This will pave the way for implementing complex PICs which will simultaneously improve performance and efficiency as well as help meet low SWaP-C constraints for next-generation S-MWIR photonic technologies.

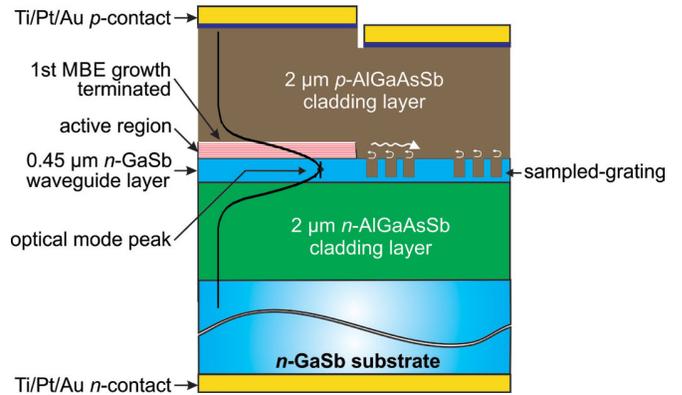


Fig. 1. Schematic cross-sectional view of an offset quantum-well SG-DBR laser cavity with an emission wavelength of 2.6 μm . The transverse-mode intensity profile is also schematically shown in the laser structure (not drawn to scale).

II. ACTIVE-PASSIVE INTEGRATION PLATFORM

Processing on the native III-V chip rather than silicon is generally more straightforward and less expensive, and likely to produce a higher yield. Several commonly used active-passive integration platforms include offset quantum well (OQW) [42], [43] and quantum well intermixing (QWI) [44] in monolithic designs, and vertical taper coupling in heterogenous designs [45]. In this study, the monolithic OQW integration platform was considered, which requires a relatively simple process. A schematic cross-sectional view of the active/passive interface within the GaSb-based SG-DBR laser is illustrated in Fig. 1. The SG-DBR lasers provide a tunable component limited to $\sim 6\%$ of the center wavelength in order to obtain a good side-mode suppression ratio using a simple cavity geometry. SG-DBR lasers are four-section devices with four separate electrodes for controlling gain section, phase modulator and two mirrors which are connected by waveguides – yielding a small version of complex PICs. Electrical isolation between the sections of the PICs can be achieved either by spatially-defined etched trenches or high-resistance ion implanted regions. Ion implantation on antimonides has recently been pursued and promising preliminary results were achieved [46], [47]. Key challenges for the successful demonstration of S-MWIR PICs include sufficient cleaning of the sample surface after patterning of the base structure, the subsequent regrowth of defect-free top cladding layers, lack of selective wet and dry etching processes, immature PIC-enabling technologies, and the fast oxidation of GaSb.

III. WAVEGUIDE STRUCTURES

A lateral waveguide architecture usually has a great impact on the design of PICs. There are four most commonly used waveguide structures including buried rib, surface ridge, buried channel, and deeply-etched ridge waveguides. All of these can be formed with a single blanket regrowth of semiconductor cladding, which does not involve any foreign masking material on the wafer surface to define epitaxial

regrowth dynamics. Among these, the surface ridge waveguide has a good current confinement, and lower loss for single-mode waveguides, which makes it uniquely suitable for lasers [48]. Hence, the surface ridge waveguide was used in the design.

IV. WIDELY TUNABLE LASERS

A. Device Structure

A base structure, containing the lower cladding, the optical waveguide and the multiple-quantum-well (MQW) layers, is required to be grown first. This allows for the selective etching removal of the MQW in regions where gain is not required, leaving a non-absorbing waveguide. Then, after removing the MQWs from regions where passive waveguides are desired, a second ‘regrowth’ is essential to apply the top cladding and the top contact in all regions. An unpatterned cladding regrowth is often performed with only a small or negligible height change between the active and passive regions [49]. For SG-DBR lasers at this long emission wavelength, the right top and bottom cladding materials with the right thickness and correct bandgap are used so that the optical mode decays fast and the highly-doped, narrower-bandgap top p -contact layer and the bottom substrate do not see the fundamental transverse mode.

In the OQW platform, the MQW active region is deliberately placed on top of the waveguide. In this configuration, the optical mode overlap with the QWs is not as high as possible and by definition, the same is true of the modal gain. However, as mentioned above, this greatly facilitates the active/passive fabrication process. The goal is to maintain sufficient optical mode overlap with QWs while reducing the overlap with the substrate and highly doped contact layer. To characterize our active and passive sections, a two-dimensional finite difference Eigenmode solver from Ansys Lumerical MODE [50] was used to perform simulations on a cross section of the waveguides. Ansys’ built-in confinement calculator was used to compute the optical confinement factors of each layer of the waveguides as listed in Table I.

Fig. 2 (top) shows the 1D and 2D intensity distribution of the fundamental transverse mode in 2.6 μm OQW SG-DBR laser structures. Despite a lower refractive index of the waveguide layer compared to the QWs, the mode overlap with the 450-nm-thick waveguide layer is substantial. This is because of the thin QWs (total 70 nm) in the active region that only add a small perturbation to the optical mode. The intensity distribution together with the refractive index profile is also shown. The optical confinement factor Γ of a semiconductor laser is of utmost importance. An increase in the confinement factor of the active QWs yields an increase in the modal gain. For low-loss optical waveguides, it is also important to simulate the transverse mode for the passive region with the MQW region removed. Fig. 2 (bottom) shows the 1D and 2D intensity distribution of the fundamental transverse mode in the passive region of the 2.6 μm laser structures. The intensity distribution together with the refractive index profile is also shown here. Table I lists the Γ values for several sections in the active and passive regions.

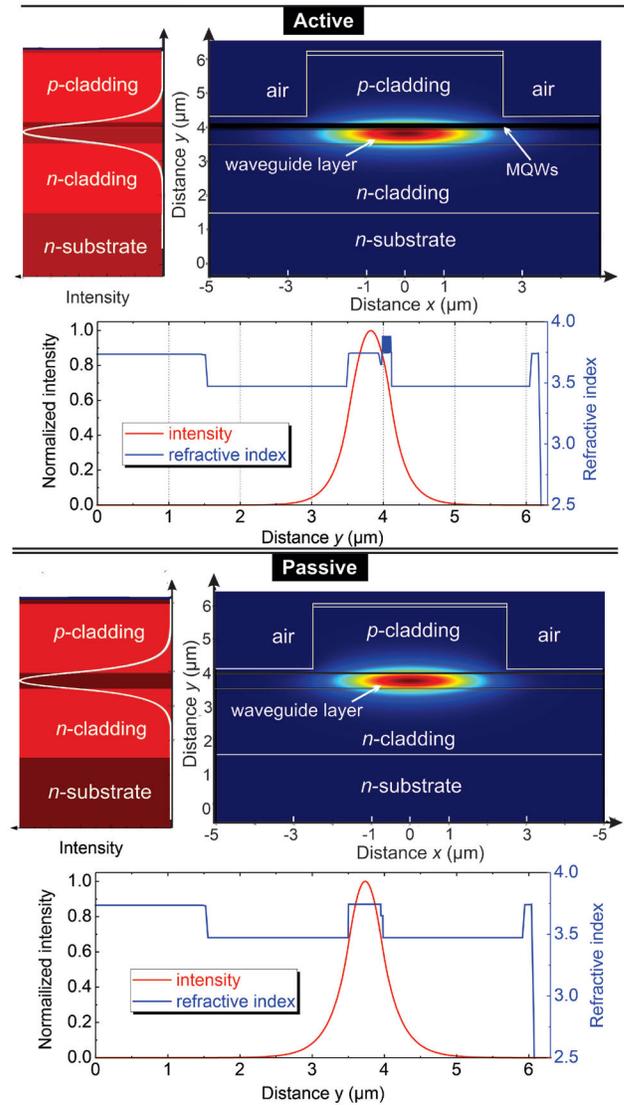


Fig. 2. Cross section of a 2.6 μm OQW SG-DBR laser structure in the active (top) and passive (bottom) regions along with 2D surface plot of the light intensity of the fundamental transverse mode, where the waveguide effective refractive index $n_{\text{eff}} = 3.61$, 1D intensity distribution of the fundamental TE-mode in the waveguide, and refractive index profile and mode intensity distribution.

B. Growth Technology

The two most popular methods available for epitaxial growth of the GaSb-based laser structures are molecular beam epitaxy (MBE) and metalorganic chemical vapor deposition (MOCVD). Although MOCVD is generally preferred for commercialization purposes, progress made to antimonide-growth has been greatly hindered due to technical challenges such as non-ideal growth conditions imposed by competing needs of typical III-Sb processes (i.e. low growth temperature) and typical precursors (i.e. inefficient pyrolysis at low temperatures). Therefore, MBE is still considered to be the preferred technology for the growth of GaSb and its alloys. GaSb as grown by MBE is known to be natively p -type due to the high number of GaSb antisite defects. In the active part, the GaSb waveguide layer has to be weakly n -doped so that it

TABLE I
CONFINEMENT FACTORS IN ACTIVE AND PASSIVE SECTIONS OF THE WAVEGUIDE

Optical mode in	Confinement factors (active)	Confinement factors (passive)
7 QWs	7.6%	N/A
Top & bottom cladding	15% + 14.3%	19.8% + 22%
Waveguide	53.8%	55.3%
<i>n</i> -substrate	0.01%	0.01%
<i>n</i> ⁺ contact layer	10 ⁻⁴ %	4 × 10 ⁻⁴ %

can conduct electrons to the MQW region. In the passive part, depletion regions of a *p-n* junction should be roughly in the middle of the structure. Placement of the *p-n* junction within the structure is important because it ensures good carrier injection into this lower bandgap waveguide region for good tuning. Considering this, it is important to weakly dope about half of the GaSb layer to be *n*-type in order to actually compensate the intrinsic disorders of GaSb.

C. Tuning Range

The spectral gain bandwidth of S-MWIR lasers in the literature as well as extrapolations of the tuning ranges of SG-DBR lasers at 1.55 μm were undertaken. From the literature, tuning range values of such lasers were estimated from the experimentally measured amplified spontaneous emission spectra of the processed Fabry Pérot lasers [51], [52], [53]. In fact, the net modal gain spectra of the device active regions for the wavelength range of 2.2-2.5 μm were measured as a function of the excitation current in these experimental studies. Although these measured GaInAsSb gain curves are more realistic, they perhaps yield conservative estimates. In this study, the tuning range of SG-DBR lasers $\Delta\lambda$ was estimated from the full width at half maximum (FWHM) of the gain material. Figure 3 shows the gain bandwidth values obtained from the literature as a function of emission wavelengths. We also considered the relative bandwidth $\Delta\lambda/\lambda$ with respect to the central wavelength that provides a convenient measure of the tuning range. Given the dependence on the central wavelength, the laser's tuning range scales with the center wavelength that the device emits at. Simple scaling of the best result from InP-based SG-DBR at 1.55 μm is probably optimistic, because optimized devices with tuning ranges as high as 72 nm were reported [27]. Considering this simple scaling, we estimated a highest tuning range scaled to the 2.56 μm spectral regime.

$$\Delta\lambda_{@2.56\mu\text{m}} = 72 \text{ nm} \times \frac{2.56 \mu\text{m}}{1.55 \mu\text{m}} \quad (1)$$

Hence, the tuning range is conservatively estimated to be 120 nm. The linear scaling is valid for the SG-DBR if the waveguide dispersion is similar. That is, the frequency response of the SG-DBR is linearly related to the Fourier transform of the spatial grating pattern and this scales inversely with grating bursts. Considering the group refractive index of the antimonide waveguide, the laser tuning range defined by FWHM envelope bandwidth (λ_{env}) of mirrors was also

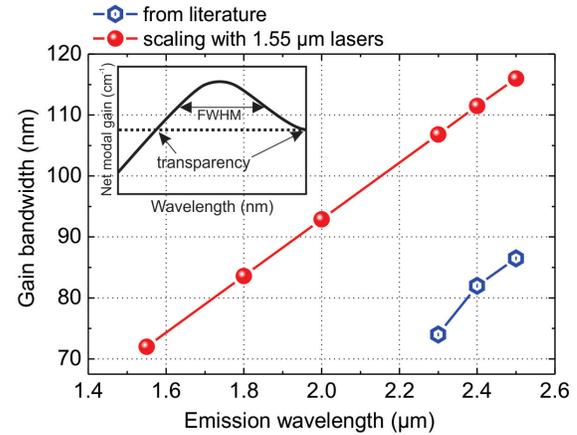


Fig. 3. Spectral gain bandwidth as a function of wavelength, where theoretical gain bandwidth values based on simple-scaling from 1.55 μm lasers (red circles), and experimentally measured values (blue hexagons) were collected from the literature.

calculated, which is in agreement with the value calculated by the linear scaling.

$$\Delta\lambda_{\text{env}} = \frac{\lambda^2}{2n_g Z_1} = 119 \text{ nm} @ 2.56 \mu\text{m}$$

where Z_1 is the grating burst length, and n_g group index. In addition, a large tuning range in such devices requires a sufficient spectral gain bandwidth from the active region.

D. Waveguide Design

1) *Thickness*: The thickness of the transverse waveguide layer plays an important role on the device performance in QW SG-DBR lasers. Thanks to the 2.56 μm design, this uses binary GaSb material as a waveguide layer. The goal is to maximize the optical mode overlap with the QWs and minimize the overlap with the substrate and contacts by optimizing the thickness and by choosing the right material. In the QW-based design, there is a trade-off between the QW overlap and the tuning efficiency in the waveguide layer. Using a thicker waveguide layer will increase the amount of index tuning that can be achieved. However, this will reduce the QW overlap and lower the available modal gain as can be seen in the left portion of Fig. 4(a). Increasing the number of QWs to compensate for the reduced overlap will increase the threshold current as well as the coupling loss between the active and passive sections due to the mode mismatch.

For the passive section, the dependence of the mode overlap with the waveguide and the doped substrate on the waveguide thickness is shown in the right portion of Fig. 4(b). As can be seen, with a 450-nm-thick waveguide layer, our design provides good optical mode overlap in the active and passive regions. Therefore, a thickness of 450 nm is chosen in this study. It should be noted that the overlap of the transverse mode with the thickness of 450-nm for the waveguide is calculated to be 55.3%. At this point, one can introduce the transverse confinement factor $\Gamma_{y,\text{waveguide}}$ for the waveguide,

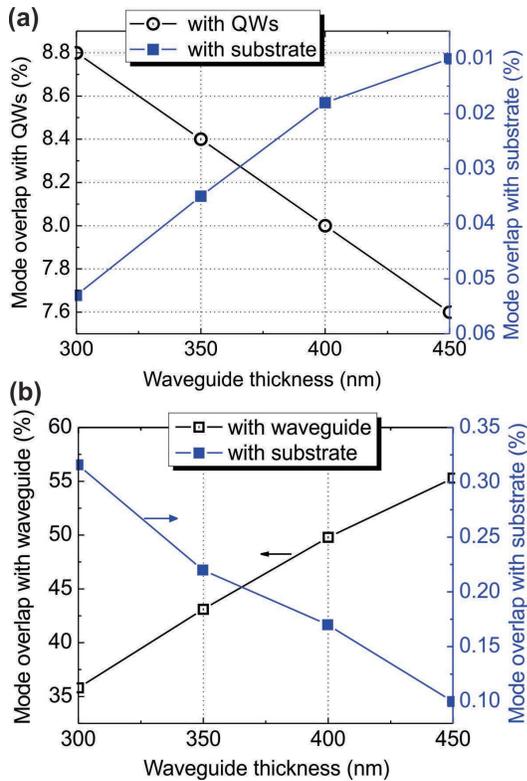


Fig. 4. Optical mode overlap as a function of waveguide thickness for offset quantum well. (a) Active region, and (b) passive region—MQW removed.

which can be written as [54],

$$\Gamma_{y,\text{waveguide}} = \frac{V_t^2}{2 + V_t^2} \quad (2)$$

where V_t is a dimensionless normalized frequency parameter for the transverse direction. Using the fundamental single-mode condition for $V = 3.14$, $\Gamma_{y,\text{waveguide}} = 83\%$. Hence, this thickness results in a single-mode waveguide and provides a safety margin from appearing the next higher order mode. However, we need to make sure $\Gamma_{y,\text{QWs}}$ does not get too small.

2) *Width*: Knowing the waveguide and cladding refractive indices, it is possible to apply single fundamental mode condition to find the maximum width of the waveguide. Again, lateral normalized frequency parameter V_l can be represented by the following relation [54].

$$V_l = \frac{2\pi}{\lambda} w \sqrt{n_{\text{eff},\text{wg}}^2 - n_{\text{eff},\text{cl}}^2} \quad (3)$$

where λ is the lasing wavelength, w the waveguide width, $n_{\text{eff},\text{wg}}$ and $n_{\text{eff},\text{cl}}$ the effective refractive indices of the surface ridge waveguide and the -etched region, respectively. Using the single-mode condition $V_l < \pi$, $n_{\text{eff},\text{wg}} = 3.57$, $n_{\text{eff},\text{cl}} = 3.5$ and assuming no optical loss, the maximum width of a surface ridge waveguide can be calculated to be $\sim 1.9 \mu\text{m}$. That means, SG-DBR lasers at $2.56 \mu\text{m}$ with $w \geq 1.9 \mu\text{m}$ are supposed to support multiple transverse modes. But experimentally, devices with larger widths (compared to the values estimated here) are observed to emit a single fundamental mode [55]. Especially, one usually ignores the first higher-order odd mode in a laser cavity because it receives very low gain due to a null

TABLE II
DESIGN PARAMETERS FOR $\sim 2.6 \mu\text{m}$ SG-DBR MIRROR

Mirror Characteristics	Value	Unit
Group index (passive)	3.93	
Center wavelength	2560	nm
Etch depth	85	nm
Grating coupling coefficient κ	300	cm^{-1}
Front Mirror	$N_{\text{FM}} = 5$ $Z_1 = 7$ $Z_0 = 80$	μm μm
Back mirror	$N_{\text{BM}} = 12$ $Z_1 = 7$ $Z_0 = 90$	μm μm
$L_{\text{eff,BM}}$	196	μm
$L_{\text{eff,FM}}$	122	μm
Tuning range based on RMS	84.5	nm
Envelope bandwidth	119	nm
$\Delta\lambda_{\text{FWHM,BM}}$	2.1	nm
$\Delta\lambda_{\text{m,cavity}}$	0.75	nm
# of cavity modes within $\Delta\lambda_{\text{FWHM,BM}}$	3	

in the center of the waveguide. Instead, one really focuses on the first higher-order even mode as the one that receives gain. Hence, the modified single-mode condition in lasers is $V = 2\pi$, yielding the maximum allowable width to be $\sim 3.8 \mu\text{m}$ at $2.56 \mu\text{m}$. Moreover, single-mode lasers may have a lateral waveguide width that supports multiple modes but only the fundamental mode lases. The reason behind this is mode-selective loss and gain in the cavity. In other words, the net losses for the higher order modes are higher, and the net gain for the fundamental mode is higher, and thus single lateral mode operation is preferred.

In summary, for a surface-ridge waveguide, single-mode operation can be expected with a $\sim 4\text{-}5 \mu\text{m}$ waveguide width, but for a deep-ridge waveguide, due to the high confinement, the ridge should be somewhat narrower, $< 3 \mu\text{m}$, at this wavelength.

E. Mirror Design

The design of the sampled-grating mirrors is critical for the SG-DBR laser operation. To this end, the design criteria of the SG-DBR mirrors that employs the Vernier effect between front and back mirrors to achieve wide tuning will be reviewed. To determine the mirror characteristics, it is very important to have the dispersion data of grating mirror materials. For $2.6 \mu\text{m}$ SG-DBR lasers, the sampled-grating mirror consists of a corrugation between the n -GaSb waveguide and the p -AlGaAsSb cladding. In addition, having knowledge of the group refractive index of the waveguide material, i.e. GaSb in this case is also very important in order to determine the physical parameters involved in SG-DBR mirror design. The wavelength-dependent refractive indices of the mirror materials as well as the group refractive index of GaSb are also used for the design. There are physical parameters, listed in Table II, that determine the reflectivity spectrum of the SG-DBR mirror. The comb-like spectrum is shown in Fig. 5.

The physical parameters are the length of the sampling period Z_0 , the burst length Z_1 , the number of periods N ,

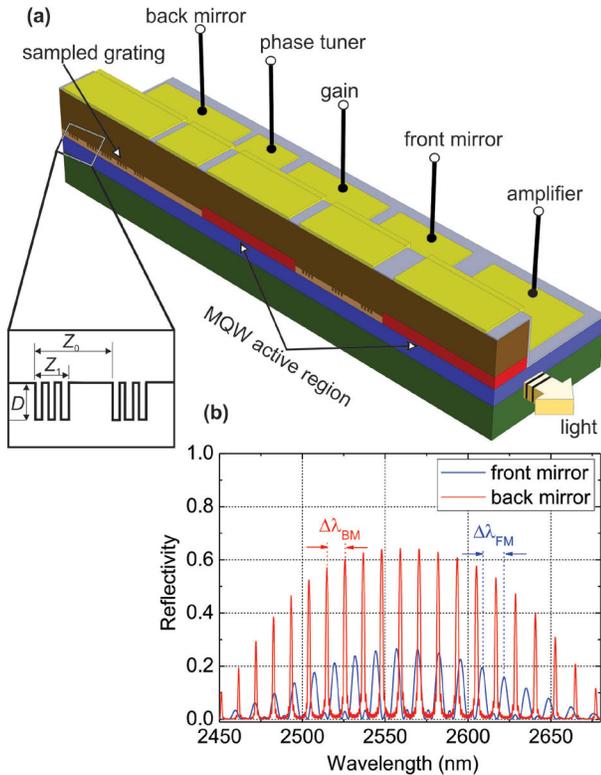


Fig. 5. (a) Schematic of the SG-DBR laser structure along with the definition of the sampled grating mirror. To boost the optical power and for PIC testing, monolithically integrated SOAs after the tunable laser are also shown, and (b) calculated front and back SG-DBR mirror spectra.

grating-coupling coefficient κ and the grating etch depth D . Table II lists parameters of an example design for an SG-DBR laser at $2.6 \mu\text{m}$. It uses numerical values of the gain material taken from [56]. Various other parameters were iterated until a reasonable design was achieved. However, further design effort will be necessary before a final design is complete.

F. Active Region Design

In an SG-DBR or other DBR structures, it is desired to first only grow up through MQW layers, remove these regions where passive waveguides, gratings, or other passive components are desired, and then finally complete the PIC by re-growing top cladding over all regions. To successfully accomplish all these GaSb-PIC technology development-related tasks, we chose a wavelength of around $2.6 \mu\text{m}$. Reasons of choosing this wavelength include knowledge availability of experimentally-proven InGaAsSb-based type-I multi-quantum well active regions, less technical difficulty of growing an active region, ease of getting a good QW/barrier interface and subsequent blanket MBE regrowth on Al-free surfaces. All these can be ensured by the well-studied InGaAsSb/GaSb active region-based lasers emitting around $2.6 \mu\text{m}$ with a record-low threshold current density at infinite lengths [56], [57], [58].

Some of the key data from the prior published work of S. Arafin on a similar quantum well gain region [56] are utilized here to obtain numerical values for the projected threshold gain and current levels. As shown in Fig. 6, the active

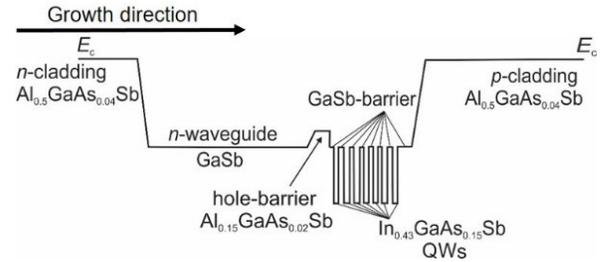


Fig. 6. Schematic band diagram of the active region used in broad-area FP laser and then SG-DBR lasers.

TABLE III
DETAILS OF THE ACTIVE REGION

Cladding	$\text{Al}_{0.5}\text{GaAs}_{0.04}\text{Sb}$
Barrier	GaSb
QWs	$\text{Ga}_{0.57}\text{In}_{0.43}\text{As}_{0.15}\text{Sb}_{0.85}$
Barrier thickness	8 nm
QWs thickness	10 nm
Compressive strain - QW (relaxed)	1.5%
QW bandgap (calculated)	446 meV
Quantization energies ($E_c + E_v$)	23 + 5 meV
Emission wavelength (calculated)	2616 nm
Band offset conduction band	212 meV
Band offset valence band	48 eV

region consists of seven QWs embedded in a GaSb separate confinement waveguide. The QWs are compressively strained and 10 nm thick and they are interfaced with lattice-matched 8 nm thick binary GaSb barriers. The outer parts of the QWs are also surrounded by undoped GaSb barriers. A 30-nm-thick n -doped $\text{Al}_{0.15}\text{GaAs}_{0.02}\text{Sb}$ layer is included as a hole barrier on the n -side to prevent hole leakage from the valence band of the QWs. Details of the active region are listed in Table III. Since there is not so much valence band offset, it is important to make the layer doped deliberately to keep most of the band offset in the valence band. Diagnostic laser structures were grown, and broad-area lasers were fabricated to de-embed numerous important material and device parameters. The test broad-area lasers exhibited near state-of-the-art threshold-current densities, as well as injection efficiencies, waveguide losses, and gain parameters, in-line with some of the reported numbers [56], [57], [58].

Gain constant (g_0) for the active region material and transparency current density J_{tr} are two important laser parameters which were determined experimentally from vertical-cavity surface emitting lasers with the same active region [56]. The gain and current density can be related by [54]

$$g_{\text{th}} = g_0 \ln \left(\frac{\eta_i J_{\text{th}}}{N_{\text{QW}} J_{\text{tr}}} \right) \quad (4)$$

where g_{th} , J_{th} , and J_{tr} are threshold gain required to reach at threshold, threshold current density and transparency current density, respectively. Considering the threshold material gain $g_{\text{th}} = 1000 \text{ cm}^{-1}$ and calculated longitudinal confinement factor $\Gamma_z = 7.6\%$, we calculate modal threshold gain 76 cm^{-1} . Table IV lists the parameters of an example design for an SG-DBR laser at $2.56 \mu\text{m}$.

TABLE IV
2.6 μm SG-DBR DEVICE PARAMETER SPECIFICATION

Property	Value	Unit
Modal threshold gain	76	cm^{-1}
g_0	1400	cm^{-1}
transparency current density / well	200	A/cm^2
Internal efficiency	0.4	%
Gain length	700	μm
Waveguide width	5	μm
# QWs	7	
Threshold current (calculated)	130	mA

G. Phase Tuner Design

The phase tuner section of GaSb-based tunable lasers exploit the carrier injection based free-carrier plasma effect. This changes refractive index that eventually changes the phase of incoming optical waves as well as makes a blueshift of resonant wavelengths. Under current injection with the injection efficiency $\eta_i = 0.6$ and tuning current $I_t = 5 \text{ mA}$ into the passive region provide a carrier density N calculated by Eqn. (5).

$$N = \sqrt{\frac{\eta_i I_t}{q V_t B}} \quad (5)$$

where V_t denotes the volume of the tuning region, the bimolecular recombination constant of GaSb $B = 1.2 \times 10^{-10} \text{ cm}^3/\text{sec}$. Considering the passive waveguide region with 450 nm thickness, 4 μm width and 80 μm length, the carrier density is calculated to be $1.2 \times 10^{18} \text{ cm}^{-3}$. Taking $\lambda = 2560 \text{ nm}$, speed of light in free-space $c = 3 \times 10^8 \text{ m/sec}$ $n_{\text{GaSb}} = 3.85$, the effective masses of electron $m_e = 0.041^*m_0$, and holes $m_h = 0.4^*m_0$, transverse confinement factor for the waveguide region $\Gamma_{\text{wg}} = 0.55$, the mobilities of electrons and holes $\mu_e = 3000 \text{ cm}^2/\text{V-sec}$ and $\mu_h = 1000 \text{ cm}^2/\text{V-sec}$, ϵ_0 is the permittivity of free-space, ambipolar injection of $N = P = 1.2 \times 10^{18} \text{ cm}^{-3}$, an index change $\Delta n = -0.025$ and an optical loss $\alpha_{\text{pl}} = 4.2 \text{ cm}^{-1}$ are obtained

$$\Delta n = -\Gamma_{\text{wg}} \frac{q^2 \lambda^2}{8\pi^2 c^2 n \epsilon_0} \left(\frac{1}{m_e^*} + \frac{1}{m_h^*} \right) N \quad (6)$$

$$\alpha_{\text{pl}} = -\Gamma_{\text{wg}} \frac{q^3 \lambda^2}{4\pi^2 c^3 n \epsilon_0} \left(\frac{1}{m_e^{*2} \mu_e} + \frac{1}{m_h^{*2} \mu_h} \right) N \quad (7)$$

Hence, a passive waveguide section of length L_p with an electronically controllable effective refractive index serves as the basic tuning element to perform the shift of the resonance wavelength. As the (single-pass) phase shift of this element $\Delta\Phi = 2\pi/\lambda^* \Delta n^* L_p$ is proportional to the product of effective refractive index and length, it is important for a strong tuning effect to extend this element over a major part of the laser cavity. Considering $L_p = 51 \mu\text{m}$, $\lambda = 2560 \text{ nm}$ and $\Delta n = -0.025$, a phase shift of π radians can be achieved. In addition to the magnitude of the index change, optical absorption losses should also be considered in the design of phase tuners.

H. Regrowth

To confirm the feasibility of the design of S-MWIR PICs, active/passive regions were defined on the MBE-grown base

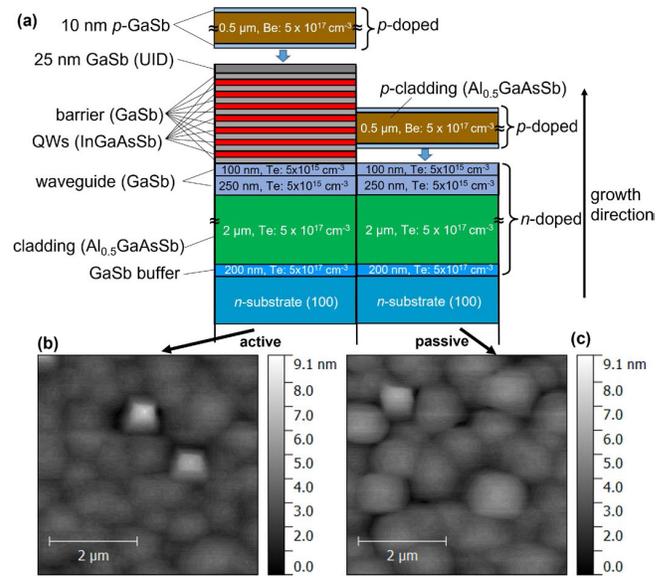


Fig. 7. (a) Schematic cross-sectional view of offset quantum-well epitaxial structure – active (left), passive (right) regions with the regrown epilayers on top. 5 $\mu\text{m} \times 5 \mu\text{m}$ AFM images of the (b) active (with MQWs) and (c) passive areas (etched MQWs) after MBE regrowth.

epitaxial structure shown in Fig. 7. Passive regions were formed by selectively removing the multiple-QW active region from the base structure. Low-temperature-based (450°C) *in situ* atomic hydrogen cleaning was employed for deoxidizing the growth surface after selectively removing the MQW region. The etch details can be found elsewhere [59]. Blanket MBE regrowth was then performed by the deposition of a thick quaternary cladding layer on Al-free surfaces. Figs. 7(b) and (c) show the AFM images of the surface morphology of both active and passive regions. Atomic steps were observed after MBE regrowth in both active and passive areas with and without MQWs, respectively. The film exhibits surface morphology with a root-mean-square (RMS) roughness value of $<0.3 \text{ nm}$, as shown in Figs. 7(b)-(c). Although the surface morphology shows coalescing mound-like structures in our first attempt, a flatter, terraced surface is desired, which will be investigated in our future studies.

V. CONCLUSION AND OUTLOOK

This study aims to transition this mature laser tuning technology to the S-MWIR by developing a GaSb PIC technology with InGaAsSb/AlGaAsSb/GaSb gain material. We have proposed GaSb-based widely-tunable laser diode which consists of an offset QW-based structure integrated with an SG-DBR monolithically. This paper focuses on developing a high-performance PIC technology for, in particular, around 2.6 μm wavelengths using type-I diode lasers, although many of the same advances will later be applicable to the 2.2-3.4 μm wavelength region using type-I and ICLs operating at 3-6 μm . The presented concepts and encouraging materials growth results pave the way for the realization of transmitter PICs covering a large SWIR wavelength range using GaSb-technology.

Beyond classical photonics, on-chip lasers in S-MWIR will also expand the range of quantum states of light generation

significantly. In an interaction-free imaging technique [60], a pair of entangled photons in telecom and MWIR are generated through nonlinear optical interactions. The MWIR photon of the pair interacts with samples while its partner telecom photon is detected by well-established and high efficiency single-photon detectors in telecom wavelength. Due to the phenomenon of entanglement, the non-interacted telecom photon provides information about the sample which interacted with the non-detected MWIR photon. An S-MWIR and tunable laser will allow generation of the pairs in higher MWIR wavelengths (limited by the material transparency), thus covering a wider sensing range [61]. The integration of this laser on-chip will allow phase stable, complex and portable version of such techniques.

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First O-band silicon coherent transmitter with integrated hybrid tunable laser and SOAs

Junqian Liu, Aaron Maharry, Aaron Wissing, Hector Andrade, Stephen Misak, et al.

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First O-band Silicon Coherent Transmitter With Integrated Hybrid Tunable Laser and SOAs

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ABSTRACT

Scaling data centers to 200 Gbps/lane with direct detection may not provide sufficient link budget for optical switches. Analog coherent detection leverages phase and polarization of optical signals to scale efficiently without requiring digital signal processing and employs integrated lasers to maximize link budgets for optical switches. We report the first O-band silicon photonics coherent transmitter integrated with hybrid semiconductor optical amplifiers and tunable lasers. The laser demonstrated >6 dBm output power with ~ 700 kHz linewidths across its 14 nm tuning spectrum. 64 Gbaud QPSK transmission was demonstrated with BER $\sim 4e-4$ and ~ 6.6 pJ/bit energy-efficiency when utilizing SiGe BiCMOS drivers.

Keywords: analog coherent detection, integrated hybrid lasers, O-band 1310 nm, Mach-Zehnder modulators, dual-polarization QPSK, silicon photonics, short-reach intra-datacenter connections, polarization multiplexed carrier

1. INTRODUCTION

To meet the demand of future data center networks, energy-efficient optical links that scale to higher data rates will be required. Coherent detection offers significant advantages over the intensity-modulation direct-detection (IMDD) links that are deployed today. By leveraging phase and polarization of optical signals, coherent detection can achieve increased data rates while also enabling a higher optical link budget by mixing the modulated signal with a local oscillator (LO) laser. Analog coherent detection schemes such as optical phase locked loops (OPLL) can be utilized to minimize power consumption by performing carrier and polarization recovery without high-speed analog-to-digital converters (ADCs) and digital signal processing (DSP). By using DP-QPSK modulation, power-efficient NRZ transmitter (TX) and receiver (RX) electronics can be utilized while maximizing link budget, which can enable optical switching.¹

Presented in this work is a silicon coherent transmitter with integrated hybrid laser meant for data center networks. This dual-polarization transmitter demonstrated 64 Gbaud QPSK constellations with bit-error ratios (BER) as low as $4e-4$ while consuming ~ 6.6 pJ/bit per channel. Photonic integrated circuits (PIC) were fabricated on Intel's silicon photonics platform while custom electronics were made in GlobalFoundries 9HP 90 nm SiGe BiCMOS process. Intel's platform that previously demonstrated 800G link applications² also includes integrated lasers and semiconductor optical amplifiers (SOA) which reduce packaging complexity and optical loss to further improve link budgets for future optical networks.

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2. TRANSMITTER DESIGN

The transmitter PIC consists of an integrated hybrid laser utilizing back reflectors based on 1 x 3 multimode interferometers (MMI) with each arm leading to tunable optical delay lines of different lengths.³ Its front output is connected to a 1 x 2 splitter leading to 4 differential travelling wave Mach-Zehnder modulators (MZMs) — two for each polarization channel. Outputs of the two channels are boosted by semiconductor optical amplifiers (SOA) then merge in a polarization beam-combiner rotator (PBCR) where half the signals are rotated to transverse magnetic (TM) polarization while the others are left in the original transverse electric (TE) orientation. Biasing of lasers and MZMs is done with thermo-optic phase shifters.

The driver utilized in this work was previously demonstrated interfacing with a similar dual polarization MZM also fabricated by Intel but without integrated lasers or SOAs.⁴ The MZM is terminated with an integrated resistor slightly less than its line impedance to peak the electro-optic response. Both driver and modulator are assembled on a custom Isola Tachyon PCB as shown in Fig. 1.

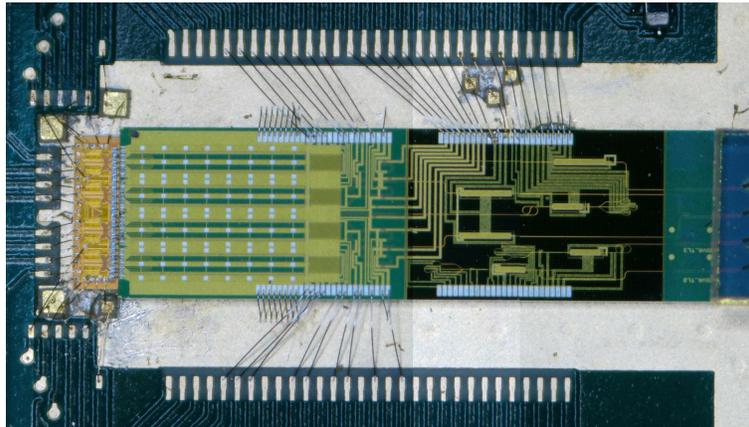


Figure 1: Micrograph of the 1.3 mm long driver on the left and 12.5 mm long PIC on the right. Both chips are 3 mm wide and had several DC traces bonded to small decoupling capacitors.

3. MEASUREMENTS AND DISCUSSION

The transmitter laser was first characterized alone without modulation. Once it was shown to have satisfactory performance, the assembly was biased and driven for QPSK transmission which was demodulated by a commercial receiver. No temperature controller was used while collecting any data so the measurement environment is assumed to be room temperature.

3.1 Integrated Hybrid III/V-Si Laser and SOAs

Laser measurements were performed with a battery box powering the gain section to minimize phase noise from AC power supplies. Lensed fiber was aligned to the edge facet with a power monitor displaying >6 dBm of output power when all MZM branches and active regions are biased for maximum transmission. The laser showed a threshold current of ~ 8 mA. A self-heterodyne setup was used to monitor 3 dB apparent linewidths which were consistently <700 kHz when optimized for single mode operation. An output tap leading to an optical spectrum analyzer (OSA) also recorded tunable wavelength ranges of 14 nm and side-mode suppression ratios >40 dB seen in Fig. 2(a) which are consistent with previously reported results.⁵ Additional sweeps were performed on each individual polarization channel's SOAs to verify channel output power symmetry in Fig. 2(b).

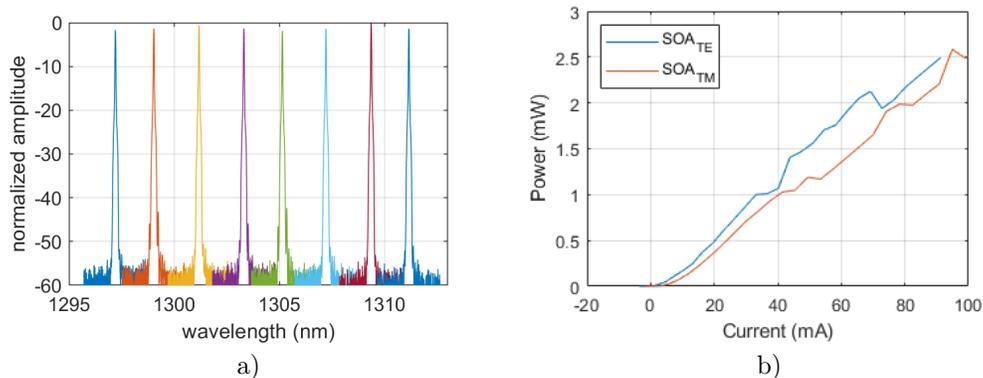


Figure 2: a) Normalized laser frequency spectrum on the OSA showing wavelength tunability across 2 nm spaced wavelength channels. b) Polarization channel SOA injection current versus output facet power. The SOA not being swept was biased at absorption in both LI measurements.

3.2 QPSK Coherent Data Link

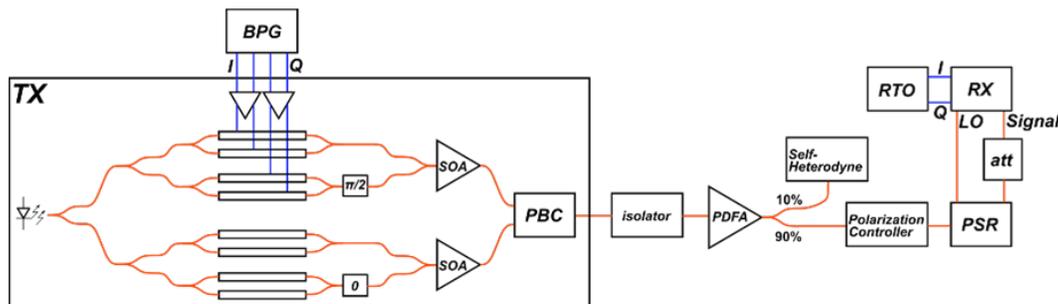


Figure 3: Block diagram of the transmitter with on-chip laser and self-homodyne test setup. Polarization carrier multiplexing was achieved by biasing the LO branch to the peak and the QPSK signal to null output power.

Intended modulation format for this transmitter is dual polarization QPSK which requires a LO laser at the receiver. To demodulate data without a receiver LO, the transmitter was biased to generate a polarization multiplexed carrier with the LO on the unmodulated polarization and the QPSK modulated signal on the other. Then the on-chip PBCR output was fiber coupled to a commercial polarization splitter rotator with linear polarizers before being fed into the reference 90-degree hybrid (Kylia COH28X-FCAPC-1300nm) connected to a pair of balanced photodetectors (Finisar BPDV3320R). Therefore only one polarization can be tested at a time with this configuration shown by Fig. 3 despite the symmetric IC design. A praseodymium-doped fiber amplifier was also introduced to compensate for additional losses introduced by using an off-chip LO for the receiver. LO path length was matched to that of the attenuator and signal to improve signal phase stability. Total output power from the facet was also reduced to <5 dBm to maintain laser stability while under additional heating when drivers were on. Overall contributions in approximate power consumption for each channel were 4.25 pJ/bit from drivers and 2.35 pJ/bit from the PIC.

RF signals from photodetectors output to a 256 GSa/s real-time oscilloscope collecting 256 kpts for BER sensitivity curves in Fig. 4 and 1.28 Mpts for constellations at the lowest BER bounds in Fig. 5. All BER sensitivity curves use a PRBS15 bit sequence while transmitted with the same LO power of 310 μ W and unattenuated signal power of 110 μ W per photodetector. QPSK constellations were sampled and rotated with no additional post-processing to modify measured points. Curves in Fig. 4 agree well with previously demonstrated results using similar platforms.⁴

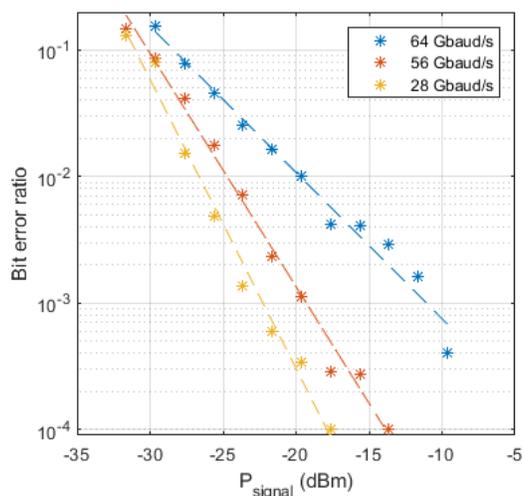


Figure 4: Sensitivity curves at 64, 56, and 28 Gbaud for received signal power per photodetector versus BER.

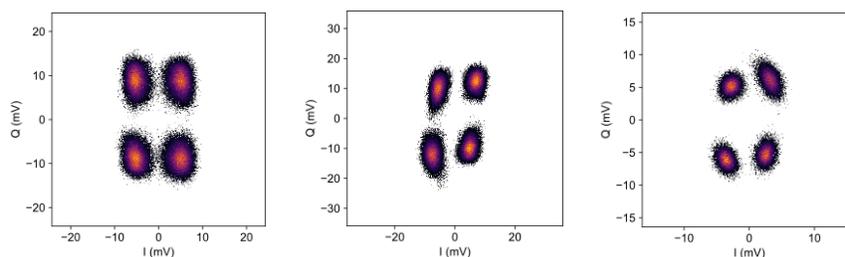


Figure 5: QPSK constellations at 64, 56, and 28 Gbaud for lowest BER of each baudrate.

4. CONCLUSION

Reported here, to the best of the authors' knowledge, is the first silicon coherent transmitter with an integrated hybrid laser operating at O-band. 64 Gbaud QPSK transmission was shown with a polarization-multiplexed carrier scheme while achieving BERs down to $4e-4$ and total power consumption of ~ 6.6 pJ/bit per channel. Future works will involve measuring both polarizations simultaneously with OPLL based optical receivers.

ACKNOWLEDGMENTS

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QPSK Transmitter Photonics Integrated Circuit (PIC) with Integrated Micro-Transfer-Printed EAMs and Custom Driver Compatible with 3D Integration

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Abstract—We present a 64 Gb/s O-band Quadrature Phase Shift Keying (QPSK) coherent transmitter, consisting of a silicon photonic transmitter (TX) integrated with micro-transfer printed (MTP) InP electro-absorption modulator (EAM) and a differential driver. We also show a co-designed flip-chip compatible electronic integrated circuit (EIC) and the photonic integrated circuit (PIC) based on the previous design.

Keywords—coherent transmitter, data center, QPSK, MTP, flip-chip

I. INTRODUCTION

With the increasing amount of network traffic within data centers, the demand for higher bandwidth and better energy efficiency is growing. Coherent technology is a promising approach to meet these requirements for intra-data center links (<2km), by introducing another degree of freedom for modulation. Additionally, it has higher spectral efficiency and improved sensitivity. A completely analog coherent scheme improves energy efficiency further by eliminating the need for analog-to-digital converters (ADC) and digital signal processing (DSP).

The silicon photonics integrated circuit (PIC) is widely used and becoming more attractive due to its mature process technique and low cost. Because of silicon's material properties, it is challenging to modulate light efficiently and reach higher speeds with low voltage swings. MTP brings the III-V coupon, which has a better modulation performance, onto the silicon platform. By taking advantage of both the III-V and Si platforms, the PIC can be more efficient with a smaller footprint. Moreover, it enables flip-chip integration between the EIC and the PIC. Therefore, these improvements can increase the bandwidth due to the reduction of parasitic capacitance and inductance and better signal integrity.

This paper presents a complete O-band coherent optical transmitter consisting of a coherent TX PIC with MTP EAMs fabricated on the Rockley platform and wirebonded to an EIC. The TX shows good performance up to 64 Gb/s. The co-design for the flip-chip EIC and PIC is then presented.

II. PLATFORM AND PACKAGING DESIGN

The design of the QPSK transmitter (TX) photonic integrated circuit (PIC) is based on the Rockley Photonics

silicon photonics technology. Key advantages of the Rockley Photonics multi-micron waveguide platform are relaxed fabrication tolerance for the silicon photonic devices with larger waveguides and integration of III-V actives achieved by attaching fully-processed known-good-die III-V devices in a recess in the silicon waveguide layer and performing edge coupling. In this work, QPSK Transmitter PICs made in the Rockley platform with MTP InP EAMS were wirebonded to GlobalFoundries EIC with current and future packaging methods including: wirebonding, flip-chip, and custom high-speed Rogers printed circuit board (PCB).

A. Multi-Micron Waveguide with integrated III-V actives

Multi-micron silicon over insulator (SOI) is used in the Rockley silicon photonics platform. The multi-micron rib waveguide enables 0.18 dB/cm propagation loss while maintaining polarization independence. Moreover, its mode size is closer to that of the III-V device, which enables low coupling loss and larger alignment tolerance. Consequently, simpler edge coupling is possible without the need for tapers and spot-size converters [1].

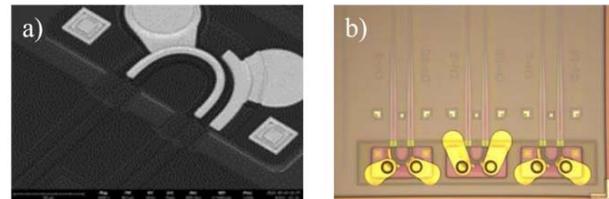


Fig. 1. a) Scanning electron microscope (SEM) image of the MTP EAM. b) MTP EAM with redistribution layer (RDL).

B. Micro-Transfer Printed EAM U-bend EAM

Previously, 106 Gb/s per channel was demonstrated on a Rockley's flip-chip-bonded U-bend EAM [2]. However, the non-planar topography after flip-chipping constrains the integration between the EIC and the PIC. Thus, Rockley developed a micro-transfer printing technique to integrate III-V devices onto a silicon substrate without substantially affecting the fabrication process flow [3]. MTP is a method of integration of III-V active devices in the form of thin coupons compatible with wafer planarization, micro-bumping, and 3D integration of electronics. This approach is particularly well suited for maximizing the high-speed performance of high-speed modulator, owing to the minimization of electrical interconnects

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and associated capacitance and parasitics. MTP also facilitates high integration densities and high throughput compared to flip-chip bonded devices. The low profile nature of the device coupons allows for tight packing, and stamp-based MTP printing process can print many coupons simultaneously [4]. The Rockley high-speed transmitter platform features InP U-bend EAMs with a 60 μm diameter. U-bend EAM coupons are bonded via micro-transfer printing into the waveguide cavity of the Si wafer, where the thin coupons sit flush with the wafer surface. Electrical connections are made after MTP in the standard wafer-level build-up process. As a result, the InP EAMs are planarized with the PIC without protrusion. Fig. 1 a) shows the planar surface topology with MTP EAM. The planar surface facilitates the flip-chip of the EIC onto the PIC. Additionally, the integration of the EAM onto the PIC allows for shorter electrical connections, thereby reducing parasitic capacitance and inductance. Fig. 1 b) shows MTP EAMs with the redistribution layer (RDL) on the silicon substrate. III-V devices transfer printed onto a silicon platform enable a smaller footprint and more efficient optical modulation compared to their silicon counter parts.

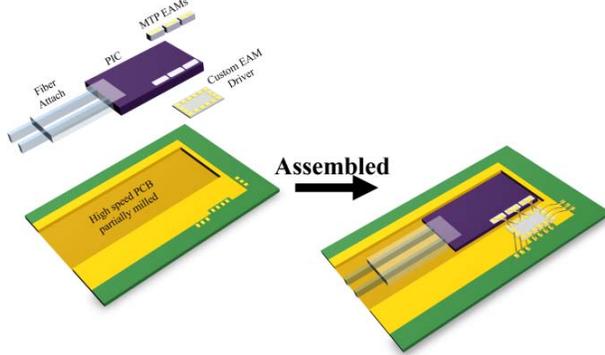


Fig. 2. The schematic of the 2D integration with wirebond.

C. 2D Integration with Wirebond

Wirebonding is a common approach for packaging. The EIC is placed next to the PIC, and electrical connections are made using pressure and ultra-sonic vibration to bond gold wires to the aluminum pads. The wire induces parasitic inductance which increases with length and can decrease the system bandwidth. To shorten the wirebond length between the EIC-PIC, as shown in Fig. 2, the carrier PCB is partially milled to match the height of the PIC and EIC. However, short wirebonds are only attainable to a single row of pads on the PIC edge adjacent to the EIC. Therefore, the number of high-speed connections on the PIC is limited by the width.

D. Flip-chip EIC on PIC for 3D integration

Flip-chipping the EIC onto the PIC provides a shorter electrical connection between the EIC and PIC compared to wirebonding. As shown in Fig. 3, further planarization and wafer-level bumping of Cu pillars (CuP) on the PIC is performed after transfer printing of the EAM coupons using Rockley's back-end-of-line wafer processing. Further details are described in Section IV-B. The EIC can then be diced and chip-level bonded to CuPs. A packaging interconnect length of ~ 100

μm , equal to the pillar bump pitch, can be assumed, resulting in a $\sim 70\%$ reduction compared to wirebonding [5]. With less parasitic inductance, higher speed can be achieved. High-speed devices can be scaled up and have more flexibility in placement. Nevertheless, the dimension for the PIC must be large enough to mechanically support the EIC. Also, additional traces are needed on the PIC to route EIC electrical signals to bondpads for wirebonding to the PCB.

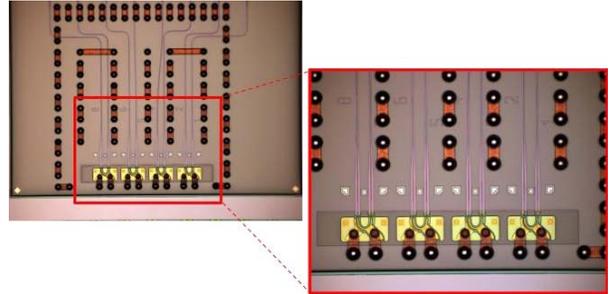


Fig. 3. MTP EAMs with backfill, RDL and CuP bump.

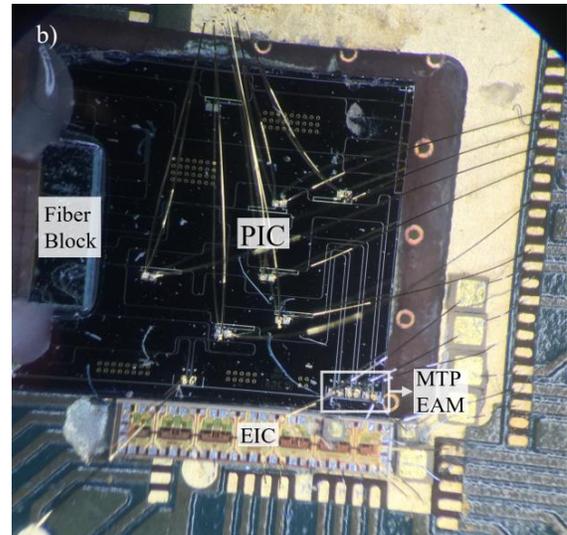
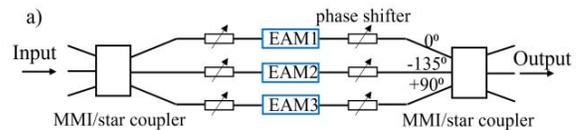


Fig. 4. a) Schematic of the PIC design. b) Assembly of the wirebond TX.

III. WIREBOND TX DESIGN AND MEASUREMENT

The O-band coherent optical TX described below has been measured up to 32Gbaud QPSK operation. The PIC was fabricated in the Rockley silicon photonics platform with three MTP EAMs in a 260- μm pitch. The EIC was fabricated in the GlobalFoundries 130 nm BiCMOS 8XP process. The EIC and PIC are packaged on a custom FR-4 PCB [6] where all electrical connections are wirebonded.

A. Coherent TX PIC Design

The TX PIC design originates from the three-arm interferometer. Two outer arms have a 90° phase difference

while the center arm has a 135° phase difference from both the outer arms. There are two phase shifters in each arm, which are biased to achieve this phase relation [7]. The three-arm design requires the outer to center power ratio to be 2:1 to achieve a symmetrical QPSK constellation. The MTP EAM in the center arm is biased by DC voltage to attain the required optical power ratio. The high-speed signal, amplified by the GlobalFoundries EIC, modulates the two EAMs on the outer arms. This results in a QPSK constellation at the output of the transmitter. Fig. 4 shows the schematic of the PIC design and a photo of the assembly.

B. Measurement

Fig. 5 shows a schematic of the measurement setup. Light from an external cavity laser (ECL) is split with 90% going to the LO port of the commercial reference receiver (RX) through a polarization controller (PC) and a 20-meter fiber. The remaining 10% goes through a semiconductor optical amplifier (SOA) and a PC, which is then coupled to the TX PIC for modulation. The modulated light is sent to the commercial reference RX after being amplified by the praseodymium-doped fiber amplifier (PDFA) and passing through a PC. The measurement is taken with 1290 nm laser wavelength to match the EAM absorption at 75°C . Two streams of PRBS15 pattern decorrelated by a bit delay were used to drive the outer two EAMs of the Rockley TX.

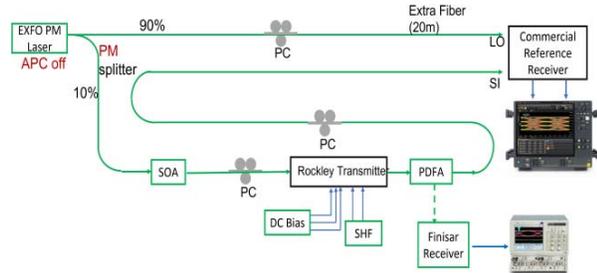


Fig. 5. Schematic of the wirebond TX measurement setup.

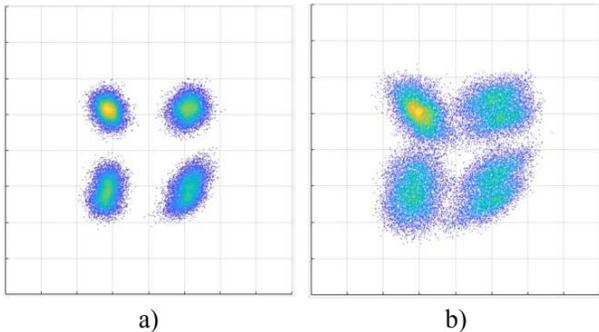


Fig. 6. Constellation diagram a) 25 GBaud, 0 errors in 65600 bits b) 32 GBaud, BER= 7.9×10^{-3} .

A MATLAB script was used to control the real-time oscilloscope and process data. To correct for random phase rotation due to the measurement setup, all the data points in an acquisition record are rotated by the same angle to produce a square QPSK constellation. Constellation diagrams were constructed using at least 32800 symbols, representing a full cycle of the PRBS15 pattern.

Constellation diagrams and BER at different bit rates are shown in Fig. 6. Fig. 6 exhibits 7.9×10^{-3} BER at 32 GBaud, which is below the SD-FEC BER limit (2×10^{-2}). The result showcases Rockley's ability to transfer III-V coupons with a tight pitch without diminishing the devices' performance. Additionally, the constellation shows that complex modulation is attainable using MTP EAM arrays and future work is focused on improving the packaging to push Rockley's MTP EAM technology to faster speeds.

IV. DRIVER CO-DESIGN AND FLIP-CHIP

Planar surface topography after MTP enables the next level of integration: flip-chip between the PIC and EIC. The design of the flip-chip can be broken into two sections: 1) driver co-design and measurement, 2) flip-chip PIC design, and 3) the assembly of the flip-chip.

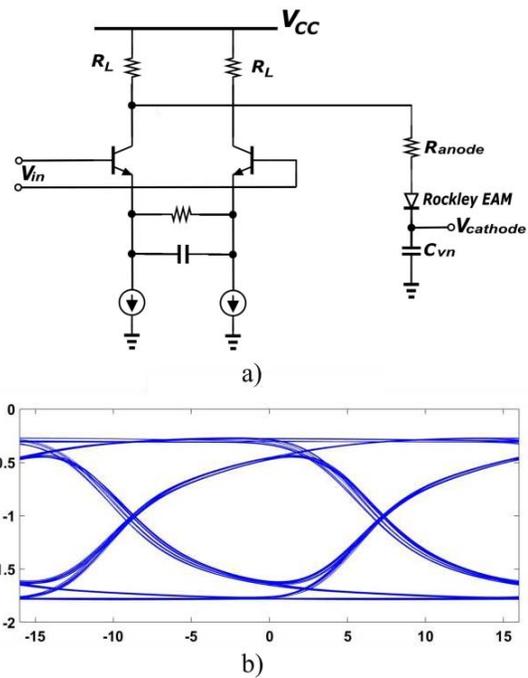


Fig. 7. a) Generalized schematic of co-designed driver b) Co-simulation eye diagram at 60 Gb/s of the driver and EAM circuit model with 50 ohm R_L and 35 ohm R_{anode} .

A. Driver Co-design and Measurement

The driver was fabricated on GlobalFoundries 90 nm BiCMOS 9HP process. Fig. 7 a) shows a generalized schematic of one channel of the co-designed driver for the Rockley InP EAM. It's a two-channel cascode differential driver with differential input and single-ended output. Power supplies and biases are shared between two channels. Each channel drives one EAM's anode. An on-chip resistor is added between the driver output and EAM anode to damp the oscillations caused by impedance mismatch and parasitic inductance. On-chip decoupling capacitors are also used for the cathode bias when co-designing the driver. Load resistance and anode resistance values were chosen, based on the co-simulation of the driver

and the EAM circuit model. Fig. 7 b) shows the eye diagram from the co-simulation at 60 Gb/s.

Fig. 9 shows the measurement setup, assembly, and eye diagram for the driver's standalone electrical-in electrical-out (EE) measurement. The driver is assembled on a test platform which operated up to 108 Gb/s [6]. Although Fig. 9 shows the measurement result of one channel, it can represent the output from both channels since the two channels are mirrored in design and should provide similar results. The driver showed good performance up to 70 Gb/s. We were able to get about 74 mV voltage swing at the single-ended output, after 20 dB of attenuation, with 500mV_{pp} differential input. Since the driver is optimized for operation with EAMs as load, we expect it to perform better with EAMs as load, we expect it to perform better with EAMs than with 50-ohm load in this measurement.

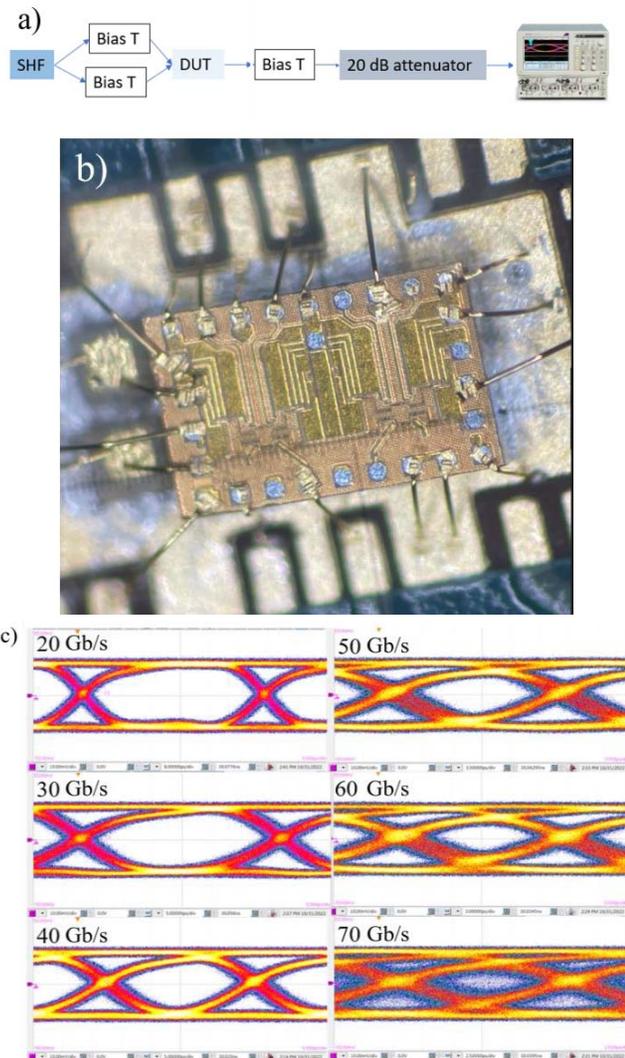


Fig. 8. a) Driver standalone EE measurement setup b) Assembly for the 50 ohm R_L , 50 ohm R_{anode} driver standalone test c) Output eye diagram of the 50 ohm R_L , 50 ohm R_{anode} driver at different bit rates.

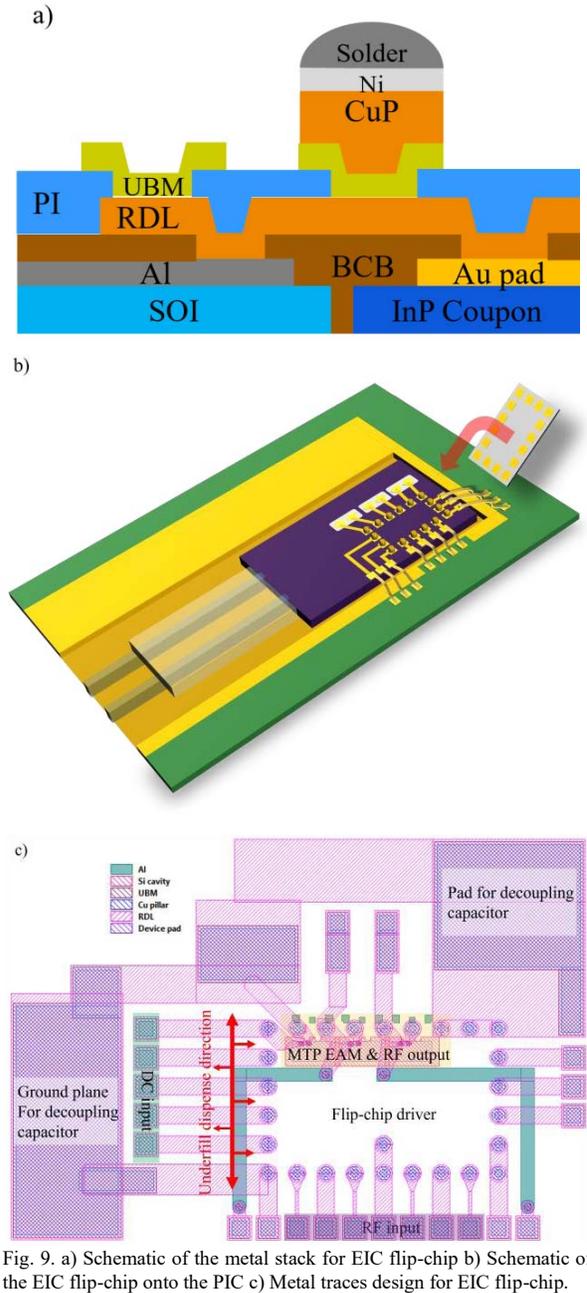


Fig. 9. a) Schematic of the metal stack for EIC flip-chip b) Schematic of the EIC flip-chip onto the PIC c) Metal traces design for EIC flip-chip.

B. Flip-chip PIC Design

In this flip-chip PIC design, we kept the photonic design consistent with the previous design seen in section III-A but added BCB planarization, metal routing, and Cu pillars using Rockley's back-end processing for flip-chip compatibility with the custom GlobalFoundries driver. Fig. 9 a) shows the metal stack for the flip-chip. Al and RDL layers were used for electrical routing. Fig. 9 b) is the schematic of the flip-chip assembly. Fig. 9 c) shows the metal routing layout for the driver flip-chip. Bondpads on the PIC, which are wirebonded to the PCB, on the PIC are routed to the driver's inputs through metal

traces. The output of the driver is connected to the EAM through the Cu pillar and short metal trace. Large pads are designed for wirebondable decoupling capacitors. Fig. 3 shows the MTP EAMs with backfill, RDL, and CuP bump. They were characterized and no degradation in DC and RF performance was observed.

C. Flip-chip Assembly Process for 3D integration

The flip-chip assembly process involves die-level bumping of the driver EIC followed by EIC dicing, then flip-chip bonding to the PIC, followed by reflow. To make the whole assembly mechanically reliable, underfill will be dispensed and cured as the final flip-chip step. The fiber block will be attached using UV epoxy to minimize misalignment during flip-chip bonding. Wirebonding will be done before the underfill dispense or after, depending on the underfill fillet. A large fillet could potentially cover the bondpads.

V. CONCLUSION

In this paper, we achieved 64Gb/s QPSK transmission with a coherent TX based on MTP EAMs fabricated in the Rockley Silicon Photonics platform. This demonstrates the capability of the Rockley platform to use MTP InP coupons for high-speed devices. Simulation and design efforts to further improve transmitter performance have been discussed, including flip-chip integration design and EIC-PIC co-simulation. EIC driver based on the co-simulation has been characterized up to 70 Gb/s.

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