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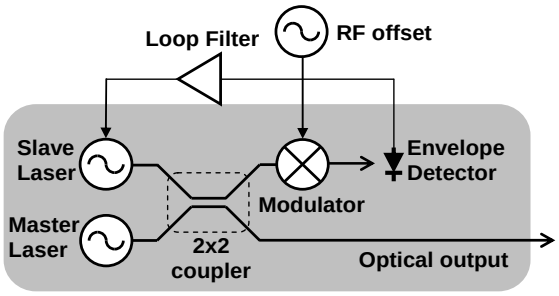

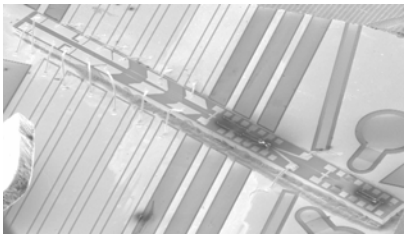

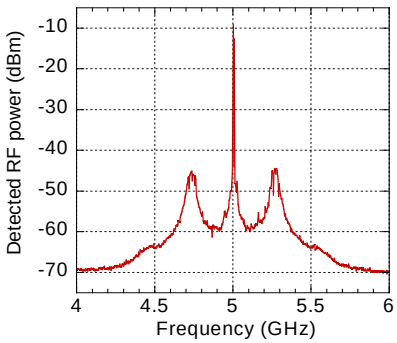

2010 Reprints of

Professor Larry A. Coldren

and Collaborators

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Research in Optoelectronics (A)

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by

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and Collaborators

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Introduction:

Articles published by Professor Coldren's group in 2010 are contained in this volume. Any journal or conference publication in which Prof. Coldren was named as a co-author is included. The majority of these works also have originated from proposals generated within Coldren's group, but a few are due to efforts that originated elsewhere and were supported by Coldren and his group members. As in recent years the work has a focus on III-V compound semiconductor materials as well as the design and creation of photonic devices using these materials—mostly diode lasers and photonic integrated circuits (PICs). The work spans efforts from basic materials and processing technology, through device physics, design, and formation, to their characterization within systems environments.

The reprints have been grouped into three areas: **I. Photonic Integrated Circuits; II. Vertical-Cavity Surface-Emitting Lasers & MBE; and III. Fabrication Technology & Photonic Crystals.** Most of the work is in the first area, which has been further subdivided into *A. High Performance PICs; B. RF-Photonics; C. Programmable Lattice Filters; and D. Optical-Phase-Locked-Loops, Mode Locking, and Injection Locking.* In nearly every project the work requires efforts in materials research, device physics, device design, process development, device fabrication, and device characterization. Most students are deeply involved in several, if not all, of these efforts, so our graduates tend to be known for their "bandwidth."

The work was performed with funding from several grants from industry and government, some gift funds from industry, and support from the Kavli Endowed Chair in Optoelectronics and Sensors. Several projects were funded by the MTO Office of DARPA, one was supported by ONR, and the industries involved included Ziva Corp. and Rockwell-Collins.

The first group of reprints (*IA.*) summarizes our work on *High-Performance PICs*. Notably all of the papers are INVITED, either directly by the journal or as invited conference talks in major international venues. All also center about the photonic integration technology we have originated, which incorporates our widely-tunable Sampled-Grating Distributed-Bragg-Reflector (SGDBR) Laser. The highlight for the past two years has been a single-chip 8 x 8 crossbar switch that uses eight wavelength converters integrated together with an arrayed-wavelength-grating-router (AWGR)—work done in collaboration with Prof. Blumenthal's group.

The Second group of papers (*IB.*) focuses on RF or analog photonics—techniques to transmit high-frequency analog information over optical fiber without distortion. Four papers, including one invited and one plenary paper, summarize results that have been obtained, primarily from our DARPA-PHORFRONT project. In this case, the objective was to demonstrate a high-dynamic-range coherent receiver for phase-modulated optical signals. Our approach involved using feedback to a tracking optical phase modulator to 'subtract out' the incoming optical modulation, thus allowing a large modulation swing as well as using a fraction of the feedback signal as the receiver output. In the final phase

of the project, flip-chip bonding to an electronic chip (EIC) and etched-trench couplers were used to reduce the feedback delay so that the modulators could better track the difference signal and increase the bandwidth of the receiver. Figure 1 illustrates a schematic of the system along with results. All-optical receivers were also developed in which the current from the detectors were sufficient to drive the tracking modulators without any electronic amplification.

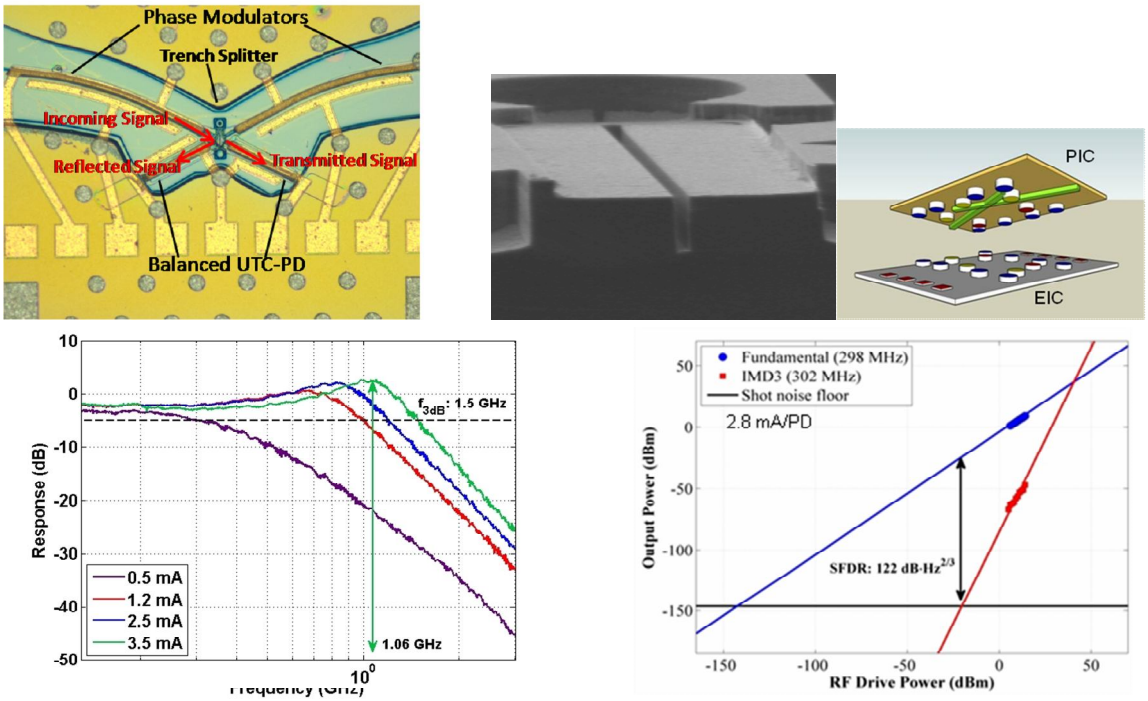


Figure 1. (top-left) Photo of PIC showing the phase modulators for the input signal and LO, the 50:50 trench splitter that combines equal portions of each to the balanced UTC-photo-detector (PD) pair; (top-center) SEM of trench; (top-right) schematic of PIC being flip-chipped to EIC. (bottom-left) Normalized rf output of PDs vs. frequency for several input powers—average photocurrent listed; (bottom-right) Two-tone distortion measurement—output power into a fundamental tone, f_1, together with IMD3: $2f_2$-f_1 level. Only 2.8 mA/PD is necessary for SFDR = 122 dB-Hz$^{2/3}$ using the feedback loop.

The work on *Programmable Lattice Filters (1C)* is summarized in five papers. Two basic approaches were pursued to build up higher order filters—(a) either cascade ring resonators using intermediate waveguides so that the resonances are uncoupled (no feedback between them), or (b) use a chain of coupled rings, in which the energy is shared amongst the rings. Figure 2 illustrates schematics of both schemes, the experimental layouts, and example results. This work was the result of work supported by the DARPA-PhASER project. As might be surmised by the placement of the various semiconductor optical amplifiers (SOAs) and phase modulators (PMs), these devices are very programmable in that many different filter configurations are possible, and the center wavelength and bandwidth are tunable. One possible application is to incorporate these in an rf photonic link to provide some adaptive pre-filtering prior to A/D conversion and Digital Signal Processing, thus enabling high-level decisions to be made rapidly and enabling more focused results with lower latency.

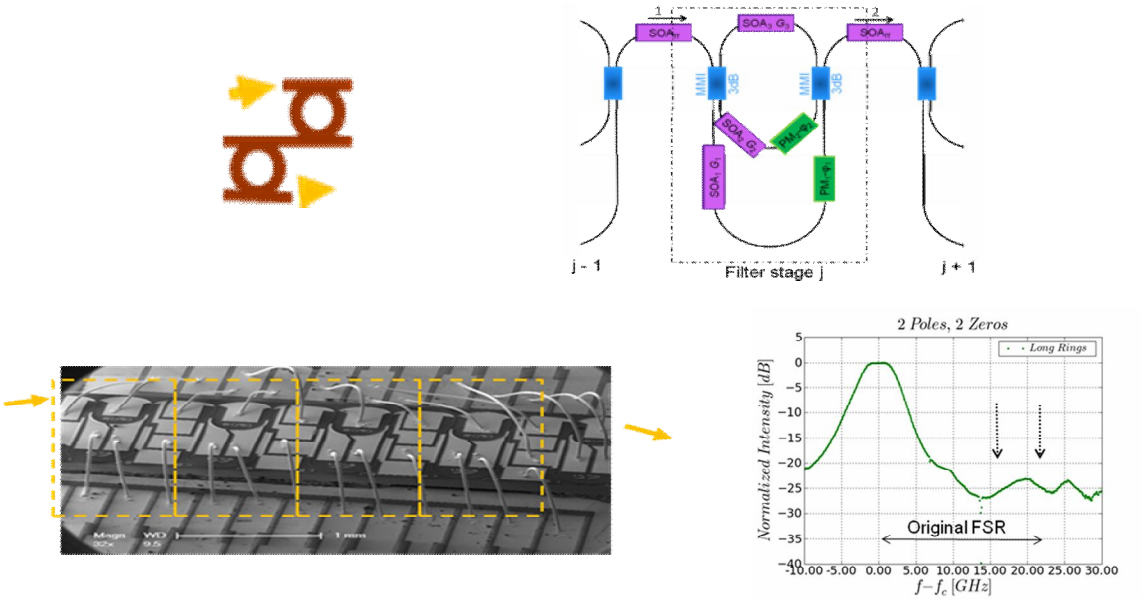


Figure 2a. (top) Concept and specific schematics of cascaded ring resonators. Top right shows element locations and indicates that rings of two different diameters are possible as well as operation in resonator or Mach-Zehnder mode. (bottom-left) SEM image of experimental chip showing four cascaded stages; (bottom-right) filter passband with two stages operated as resonators (poles or IIR mode) and two stages as Mach-Zehnders (zeros or FIR mode) .

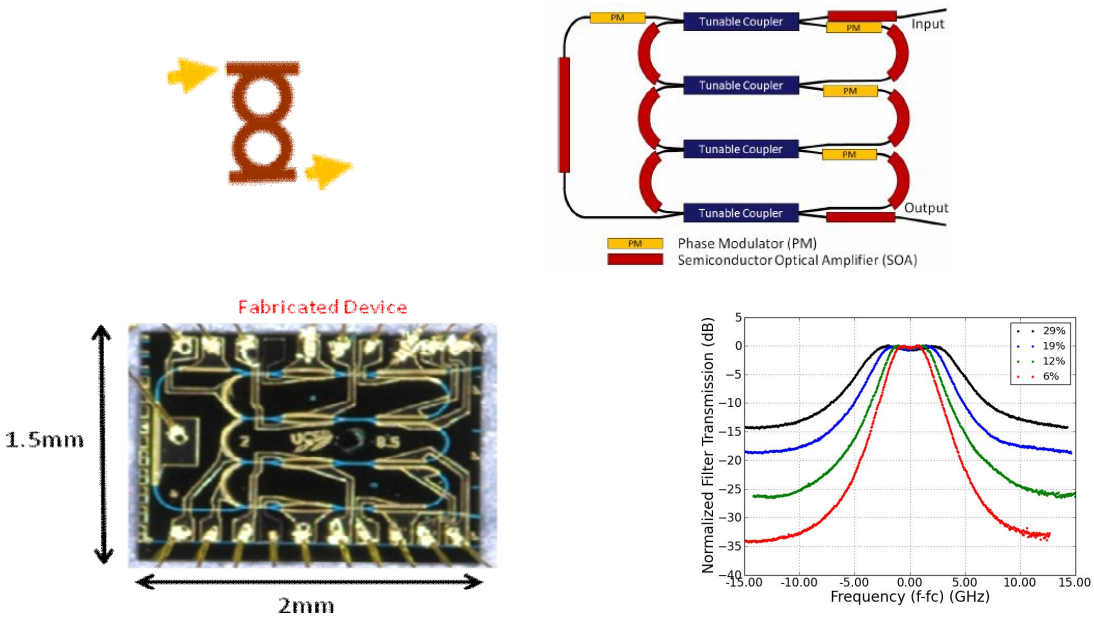


Figure 2b. (top) Concept and specific schematics of coupled ring resonators. Top right shows element locations and indicates a three-ring sub-element that also incorporates a Mach-Zehnder forward path. Variable interring couplers are key elements. (bottom-left) Photo of experimental chip; (bottom-right) filter passbands as the interring coupling is varied (inset) with Mach-Zehnder arm attenuated.

Section *1.D* contains the results of efforts on *Optical-Phase-Locked-Loops, Mode Locking, and Injection Locking.* It contains an invited paper summarizing our efforts on homodyne and offset-heterodyne-locking of two monolithically-integrated SGDBR lasers

together with all of the photonic components necessary to phase lock them together on one chip. The cover of this volume illustrates results of 5 GHz heterodyne offset-locking. As can be seen, the detected difference frequency is relatively pure. The phase error variance of 0.03 rad^2 in +/-2GHz BW is estimated from the captured spectrum. Offset locking to 20 GHz was demonstrated. This work, initially funded by a DARPA seed project, laid some of the ground work for the proposal to the DARPA-CIPhER program that is now funded as 'PICO', together with a number of industry and university partners. This relatively large program on Photonic Integration for Coherent Optics (PICO), which contains a significant component on optical phase locked loops, will be at the center of much of the group's ongoing work. This program will also contain continuing work on mode-locking, initially funded by ONR, as well as injection locking.

The publications in Section II on Vertical-Cavity Surface-Emitting Lasers (VCSELs) & MBE include recent work on high-speed VCSELs and novel three-terminal VCSELs. The invited paper summarizes our recent measurements that verify the tremendous advantages of using strained-layer quantum-well active regions because of their reduced transparency currents as well as increased differential gains. Figure 3 gives plots of gain and differential gain for various levels of strain (wavelength) vs current density to illustrate these points. The paper also references works that describe the enhanced reliability of devices with these materials. This work has been primarily funded by DARPA in the past, initially under the C2OI program. Coldren's group continues to work with highly-strained quantum-well VCSELs in the 1060 nm wavelength range for high-efficiency, high-speed data links.

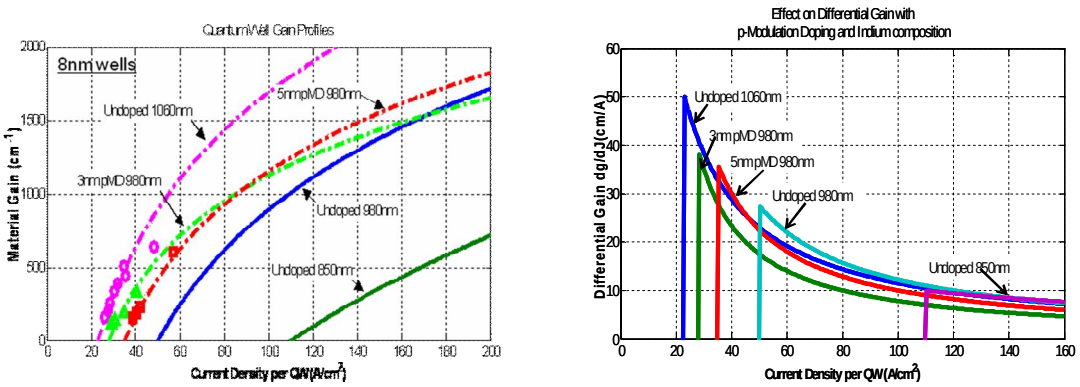


Figure 3. (left) Material gain versus current density for 8 nm In_xGaAs quantum wells clad by GaAs except in the GaAs well (x=0) case, where it is clad by $Al_{0.2}GaAs$. Peak photoluminescence is given instead of x. Also included are p-type modulation-doped (x=0.2, or 980 nm) wells. (right) Differential gain, dg/dJ; in theory the relaxation resonance frequency and potential modulation bandwidth is proportional to the square root of this. As can be seen, 1060 nm wells promise more than twice the inherent modulation bandwidth at less than a quarter of the current compared to GaAs wells (for a nominal gain ~ 300-500 cm^{-1}in each well).

Figures 4 and 5 introduce two new three-terminal VCSEL structures that have been researched in Prof. Coldren's group. The first (Fig. 4) uses a third 'field-effect' terminal to separate holes and electrons as well as modulate the confinement factor in the active region. Because it is capacitively-coupled to the charge in the active region, only displacement current flows in this modulated terminal, and in principle, the voltage swing on can be quite low (<< 1 V). The initial results verify the basic physics, although more

work is needed to obtain the hoped-for results. Modeling indicates that it may be possible to send data at much higher rates with this new device configuration without resorting to costly and high-power-consuming external modulators. Support for these efforts has been coming from DARPA, NSF, and an STTR with Ziva Corp.

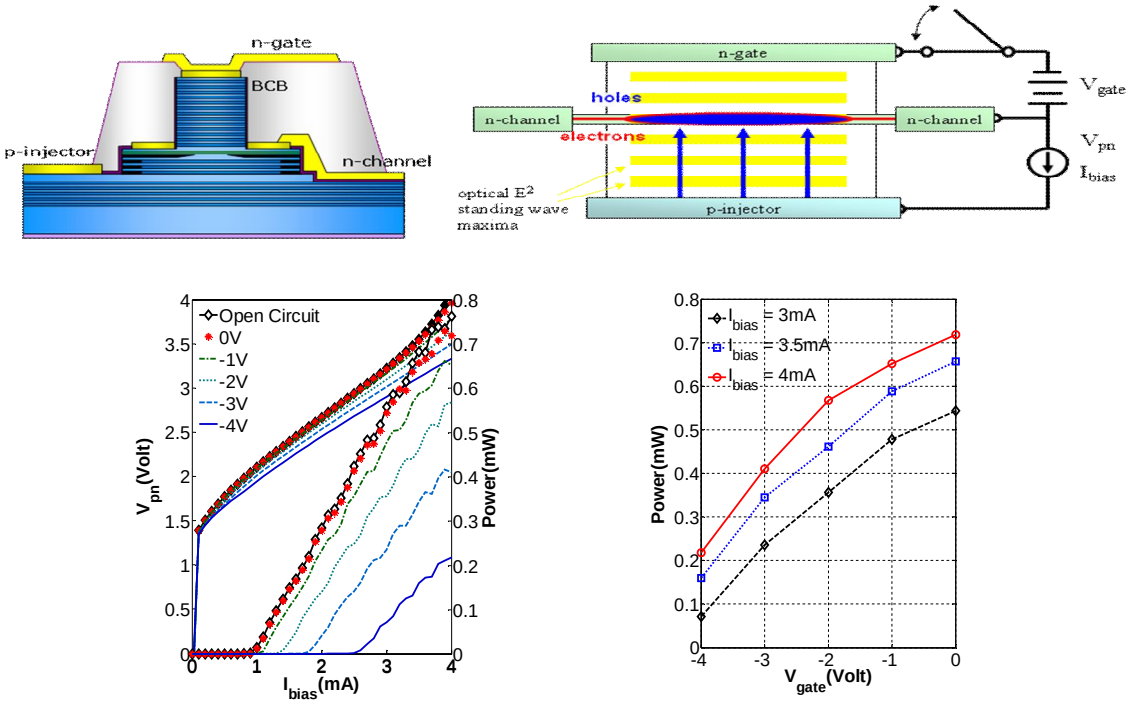


Figure 4. (top-left) Schematic of 3-terminal Field-Induced Charge-Separation Laser (FICSL) VCSEL cross section; (top-right) Equivalent circuit—dc current flows from p-injector (substrate) to n-channel, and the n-gate modulates the overlap of the holes and electrons in the channel via a field effect. No conduction gate current flows due to a quantum barrier. (bottom-left) PIV curves as a function of gate voltage—it is higher than necessary because of unnecessary resistance in the top mirror (n-gate); (bottom-right) modulation of output power at several constant channel currents.

Figure 5 shows initial results for a VCSEL that uses the third terminal to modulate polarization. Actually, the third terminal is just a second current injection terminal, but as the first, it injects current in a somewhat lateral direction, but orthogonal to the first, so that the electron momentum direction can be slightly switched. This alters the gain for one polarization mode relative to the other and promotes the observed polarization switching. Greater than 21 dB extinction is observed, and the threshold current density is relatively low. This work has been done in collaboration with and under the support of an SBIR with Ziva Corp. Use of dual polarization sources can effectively double the data rate, and they can also be used in specialized sensor applications.

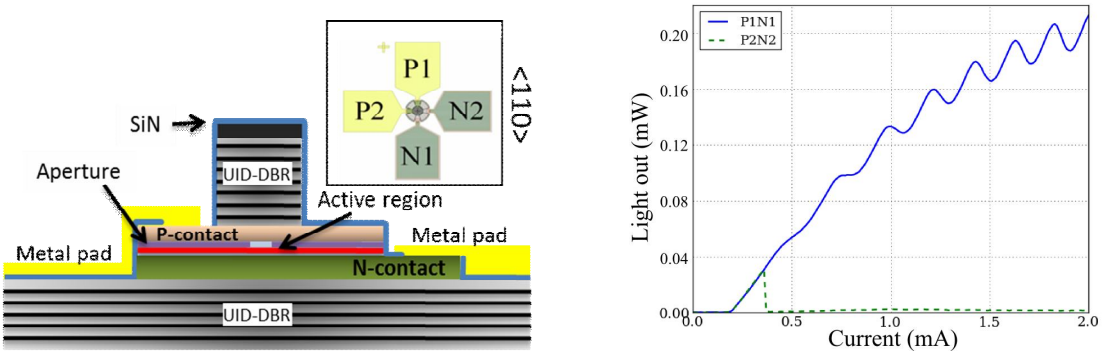
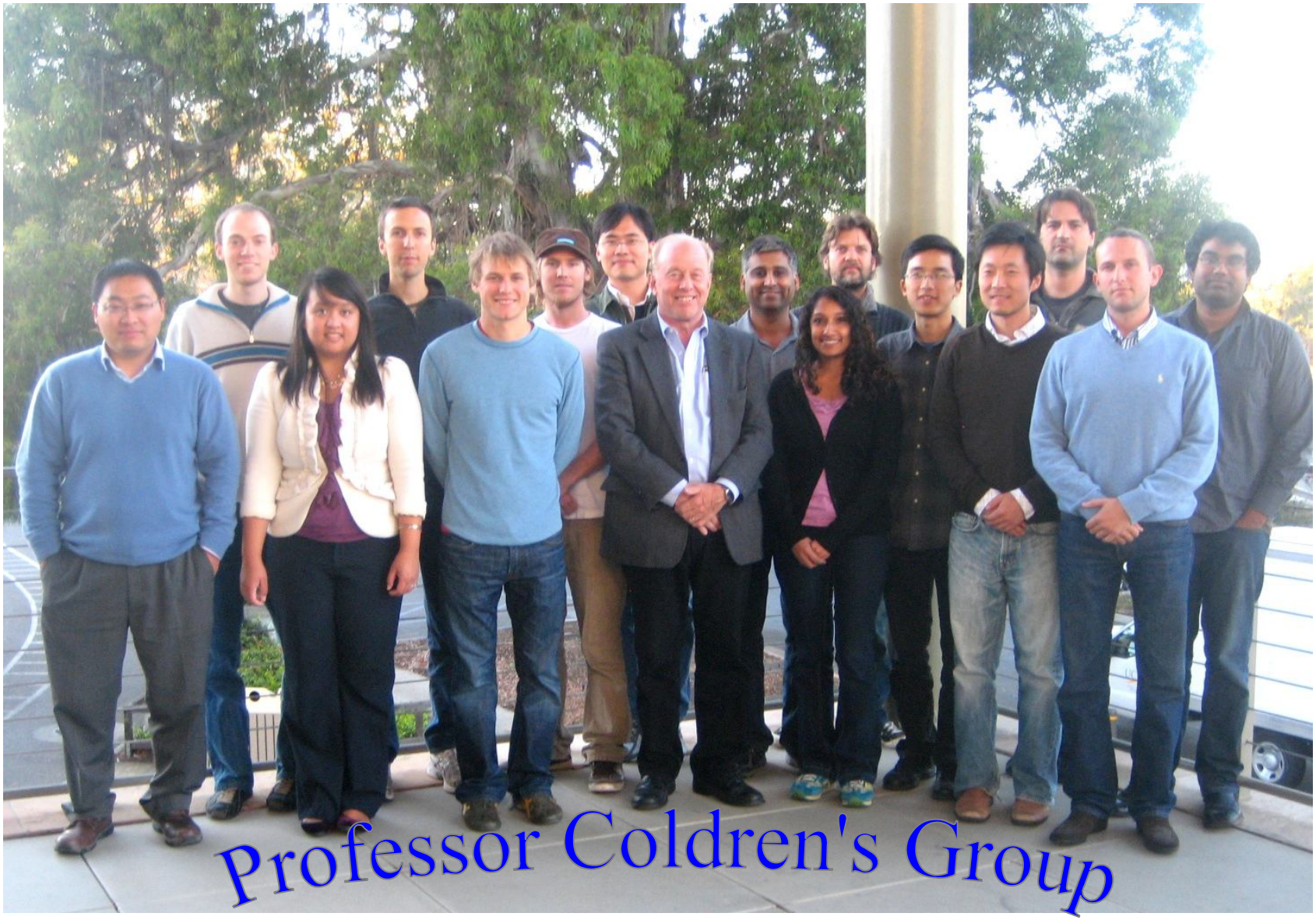


Figure 5. Schematic and results from polarization-modulated VCSEL. Current is applied either to electrodes P1-N1 or P2-N2 to force current to flow into the active region from the sides in one of two orthogonal directions. Although the electron *k*-vector is still predominately vertical near the bandedge in a quantum-well, this injection provides a slight bias on the in-plane component to be aligned preferentially along these directions, and the gain is very sensitive to this.

The publications in Section III, Fabrication Technology & Photonic Crystals, were all led by Y.-J. Hung, a visiting PhD student from Prof. S.-L. Lee's group at NTUST, Taiwan. Needless to say, Mr. Hung was a very productive and valuable addition to Prof. Coldren's group during his stay as is evidenced by the five papers he published in 2010. His work focused on developing an array of basic fabrication techniques for photonic crystals as well as many other photonic ICs. In fact, he developed several other useful technologies, such as multilayer anti-reflection coatings, that are not documented in the listed publications. It is also interesting to note that Prof. Lee was a former outstanding PhD student in Prof. Coldren's group some years ago.



Back Row: Chad Althouse, John Parker, Erik Norberg, Chin-Han Lin, Ashish Bhardwaj, Leif Johansson, Sasa Ristic, Uppili Krishnamachari
Front Row: Weihua Guo, Jeannine Roson, Rob Guzzon, Professor Larry Coldren, Abi Sivananthan, Mingzhi Lu, Yan Zheng, Pietro Binetti

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I. Photonic Integrated Circuits

A. High Performance PICs

An 8 × 8 InP Monolithic Tunable Optical Router (MOTOR) Packet Forwarding Chip

Steven C. Nicholes, Milan L. Mašanović, *Member, IEEE*, Biljana Jevremović, Erica Lively, *Student Member, IEEE*, Larry A. Coldren, *Fellow, IEEE, Fellow, OSA*, and Daniel J. Blumenthal, *Fellow, IEEE, Fellow, OSA*

***Abstract*—In this paper, we demonstrate single-channel operation of the first InP monolithic tunable optical router (MOTOR) chip designed to function as the packet forwarding engine of an all-optical router. The device has eight-input and eight-output ports and is capable of 40-Gb/s operation per port with bit-error rates below 1E-9. MOTOR integrates eight wavelength-tunable differential Mach–Zehnder semiconductor optical amplifier (SOA) wavelength converters with preamplifiers and a passive 8 × 8 arrayed-waveguide grating router. Each wavelength converter employs a widely tunable sampled-grating distributed Bragg reflector (DBR) laser for efficient wavelength switching across the C band and other functions required for 40-Gb/s wavelength conversion. Active and passive regions of the chip are defined through a robust quantum well intermixing process to optimize the gain in the wavelength converters and minimize the propagation losses in passive sections of the chip. The device is one of the most complex photonic integrated circuits (PICs) reported to date, with dimensions of 4.25 mm × 14.5 mm and more than 200 functional elements integrated on-chip. We demonstrate single-channel wavelength conversion and channel switching with this device using $2^{31} - 1$ pseudorandom bit sequence (PRBS) data at 40 Gb/s. A power penalty as low as 4.5 dB was achieved with less than 2-W drive power per channel.**

***Index Terms*—Arrayed-waveguide grating router (AWGR), photonic integrated circuits (PIC), quantum-well intermixing (QWI), wavelength converter.**

I. Introduction

ADVANCED photonic integrated circuits (PICs) in InP are a critical technology to manage the increasing bandwidth demands and core functions of next-generation optical networks [1]–[4]. The integration of many of the discrete functions required in optical networks into a single device provides a reduction in system footprint and optical losses due to the elimination of fiber coupling junctions between components, and an increase in overall reliability. Many key network components such as transceivers [5], wavelength converters [6]–[9], optical cross connects [10], add-drop multiplexers [11], and channel selectors [12] have already been realized in InP via monolithic integration. While the potential benefits of creating larger, higher functionality PICs have long been suggested, there are still very few demonstrations of PICs with more than 50 integrated components [2], [13].

Large scale integration in silicon-based integrated circuits has led to exponential growth in that industry and tremendous performance gains with a reduction in costs to the consumer. Robust design and manufacturing techniques that will enable high-yield production of large scale PICs are thus required to realize similar performance and cost improvements in the photonics industry [3]. Such efforts have been underway for several years, and the benefits of large scale integration are now being seen commercially with the recent report by Infinera of plans to deploy a 400-Gb/s PIC transmitter with more than 300 optical functions in live networks [14].

All-optical routing is a potential avenue in which large scale PICs could play a revolutionary role [15]. By moving the functions of dynamic wavelength conversion and routing to the optical layer, it may be possible to ease the increasing power consumption demands associated with scaling electronic-based routers to higher data rates [16]. For instance, discrete all-optical wavelength converters have been reported that entirely eliminate the need for power-hungry optical-to-electrical (O/E) and electrical-to-optical (E/O) data conversion [6]–[9]. While these demonstrations of wavelength conversion without O/E/O conversions are promising, the realization of a competitive all-optical alternative to electronic routers is still limited by challenges associated with optical buffering [17].

In [18], a label-switched all-optical router (LASOR) with the ability to process 40-Gb/s packets was proposed. This router architecture (Fig. 1) enables synchronization and buffering of input packets in the optical domain, and provides a means to write the input data onto a new wavelength for wavelength-selective routing. While each functional block of the router could be realized with a discrete PIC, the performance of this system in terms of reliability, optical coupling losses, and overall footprint can be significantly improved via large scale monolithic integration.

In this work, we combine the wavelength conversion and passive routing elements of LASOR shown in Fig. 1 into a single InP chip to demonstrate a monolithic tunable optical router (MOTOR) that serves as the packet-forwarding engine of an all-optical router [Fig. 2(a)]. The eight-channel InP/InGaAsP device operates at 40-Gb/s line rate per port giving a total potential data capacity of 640 Gb/s and integrates an array of eight tunable all-optical wavelength converters with a passive 8 × 8 arrayed-waveguide grating router (AWGR).

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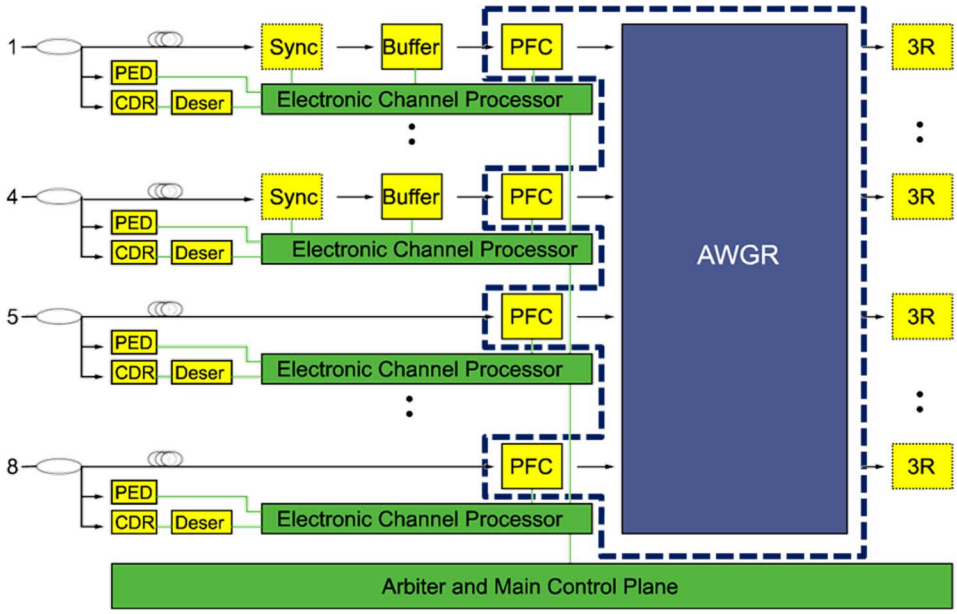

Fig. 1. Overall LASOR architecture. Key to abbreviations: PED = payload envelope detection; CDR = clock data recovery; Deser = deserializer; Sync = synchronizer; WC = wavelength converter; AWGR = arrayed-waveguide grating router; 3R = retiming, reshaping, and reamplification. The dotted region represents the elements integrated in the MOTOR chip.

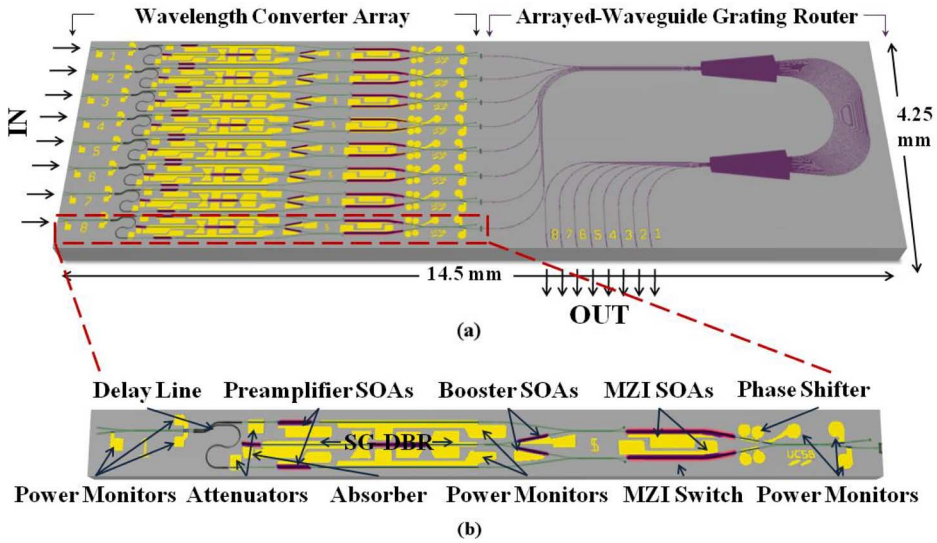

Fig. 2. (a) Schematic of overall MOTOR chip. (b) Expanded view of a single-input wavelength converter showing several key device elements.

The device represents one of the most complex InP PICs ever reported with more than 200 integrated functional elements on a single chip.

II. Device Design and Operation

A. Wavelength Converter Array

The active core of the MOTOR chip contains an array of eight wavelength converters. The technology used to implement these wavelength converters must provide: 1) error-free high-speed operation at 40 Gb/s; 2) wide tunability across the C band; 3) a small footprint; and 4) low power consumption (i.e., no O/E/O conversions). Two popular monolithic approaches to achieve these goals with 40-Gb/s data rates involve carrier-modulation effects in nonlinear semiconductor optical amplifiers (SOAs) [6], [7] or field-modulation effects with a photodiode and a modulator [9]. While each approach has inherent advantages, the design and fabrication of field-modulation-based wavelength converters tends to be more complex than that of carrier-modulation-based devices because they require integrated resistors and more complex modulator structures [9]. In order to target high device yields, we use the simpler carrier-modulation approach in the MOTOR chip.

Because our wavelength converter design exploits nonlinear SOA within a Mach–Zehnder interferometer (MZI) as in [7], both cross-phase and cross-gain modulation effects are present. However, cross-phase modulation in the MZI is the method used to shape the output pulses from the device. A detailed view of a

single-input MOTOR port is shown in Fig. 2(b). The input data signal to the chip depletes the carriers in a nonlinear SOA and changes the phase in one branch of an MZI. This phase change modulates the MZI and carves out the input data pattern onto a continuous wave (CW) source operating at the new wavelength. The overall speed of these devices is inherently limited by the carrier lifetime in the SOAs, so a differential delay line at the front end of the chip is included [7]. By time delaying the input data signal on one side of the MZI, it is possible to overcome the limitation of carrier recovery lifetime so that modulation of the MZI is governed by carrier depletion effects. The time delay is accomplished using an on-chip differential delay line before the inputs to the MZI. After the input data signal is split using a 50/50 multimode interferometer (MMI) splitter, the signals are sent to opposite branches of the MZI. The path length for one branch is increased relative to the other using a compact, tight bend radius waveguide section that adds about 11 ps of propagation delay. This delay time was chosen to simultaneously minimize the overall power penalty associated with wavelength conversion while keeping the delay line length as small as possible to minimize device footprint [19]. In general, improved performance can be achieved if the input power levels to each side of the MZI are slightly imbalanced [7], [20]. Because the path length of the inputs to the MZI differ (and hence the propagation losses differ), and because the observed splitting ratio of the fabricated MMI is sensitive to lithographic resolution, variable optical attenuators (VOAs) are included on each input line to the MZI to control the relative power levels in each branch.

The wide tunability of the wavelength converter is accomplished by incorporating a sampled-grating distributed Bragg reflector (SG-DBR) laser as the on-chip CW source. The laser consists of five sections: a 550-μm active gain section, a 470-μm front, a 910-μm back tuning mirror, a short 100-μm phase tuning pad, and a 175-μm active absorber. About 40 nm of tuning is possible through the Vernier effect [21]. By biasing both the front and back mirrors during operation, it is possible to precisely tune to any of the allowed output wavelengths of the AWGR across the C band.

The MOTOR chip also integrates SOAs with three different functions. First, 285-μm booster SOAs are used to amplify the SG-DBR output power after it is split by a 50/50 MMI splitter and before it is input into each branch of the MZI. Because the SG-DBR output power is already high, the booster SOAs are saturated but provide enough gain to overcome the halving in power from the MMI splitter. Second, nonlinear SOAs are required in the Mach–Zehnder for cross-phase and cross-gain modulation. These SOAs are >1000 μm in length in order to reduce the carrier recovery time, which tends to decrease with increasing SOA length [20]. Finally, 300-μm linear preamplifier SOAs are inserted before the input to the MZI to amplify the input data signal. It is crucial that these SOAs provide an optimal combination of high gain (to ensure that the input pulses have enough power to deplete the carriers in the MZI SOAs) and high saturation power (to avoid pattern dependent distortions that arise if the preamplifier SOAs are operated in the nonlinear regime).

One important consideration with this approach to wavelength conversion is the possibility of wavelength blocking.

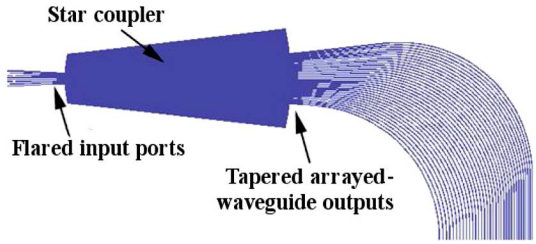

Fig. 3. Schematic view of the AWGR illustrating the flared input and tapered output waveguides.

Unlike the field-modulated wavelength converters of [9], it is not possible to convert back to the input wavelength with the differential MZI SOA wavelength converter because the input data signal exits the device from the same port as the converted signal. In a routing application, this means that the input frequency comb must be different than the output frequency comb and either a high- or low-pass filter would be required at the output to remove the original frequencies.

B. Arrayed-Waveguide Grating Router

The output of the wavelength converter is connected to an AWGR, which passively routes the wavelength converted signal based on the new wavelength of the data (as set by the SG-DBR). Our design employs an 8×8 configuration with 200-GHz channel spacing (to give a reasonable AWGR size), a center wavelength of 1550 nm, and a periodic output frequency response. The major source of loss in an AWGR is from imperfect coupling between the waveguides and the star couplers (or free propagation regions) [22]. To reduce these losses and improve coupling, our design employs flared and tapered waveguides at the star couplers (Fig. 3). The flares and tapers are 100 μm long in order to minimize the excitation of higher order modes. The 2.2-μm waveguide inputs to the star couplers are flared to 8.0 μm and are spaced by 1.0 μm. The 34 arrayed waveguides at the output of the star couplers taper from 8.25 to 2.2 μm and are spaced by only 0.8 μm. The overall size of the AWGR (not including the waveguides to the input star coupler and the waveguides from the output star coupler) is 2.84 mm $\times$ 2.60 mm.

III. Integration Platform

The integration platform used for the MOTOR chip should provide several key features: 1) high-gain regions for the SG-DBR laser and SOAs; 2) low-saturation-power (i.e., nonlinear) SOAs in the MZI; 3) high-saturation-power (i.e., linear) SOAs for preamplifiers; 4) efficient phase modulator regions for the MZI; and 5) low-loss waveguides for the AWGR and passive sections of the wavelength converters. Additionally, the integration platform should minimize the number of required regrowths and limit the overall fabrication complexity in order to maximize device yield. To meet these demands, we use an impurity-free quantum-well intermixing (QWI) process and a single, blanket p-type cladding regrowth.

The initial base epitaxial layer structure [Fig. 4(a)] is grown by MOCVD on a sulfur-doped InP substrate. It is composed of ten 6.5-nm InGaAsP quantum wells under $+0.9\%$ compressive strain and eleven 8.0-nm InGaAsP barriers under -0.2% tensile

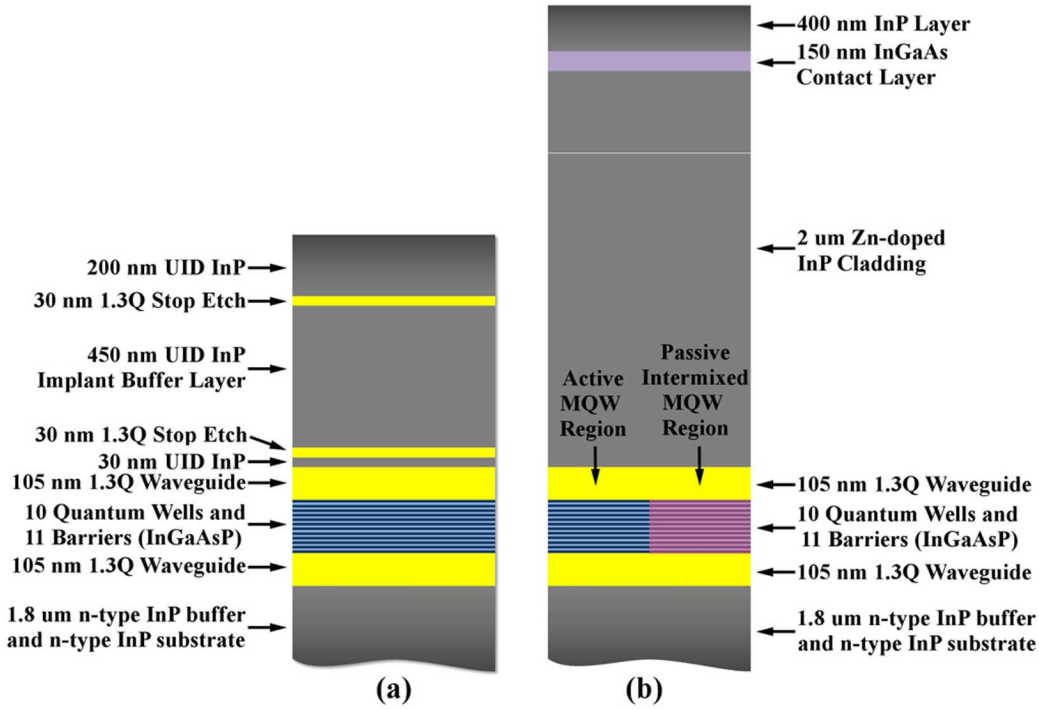

Fig. 4. (a) Initial base epitaxial growth structure. (b) Final growth structure showing both an as-grown active MQW region and an intermixed passive MQW region.

strain ($\lambda_{\mathrm{PL}} = 1545$ nm). The multiple quantum well (MQW) stack is sandwiched by a 105-nm quaternary waveguide ($\lambda_{\mathrm{PL}} = 1300$ nm) on both sides to maximize the modal overlap in the MQWs, resulting in a $\sim$13% optical confinement factor. The increased optical confinement provides high-gain regions for the booster SOAs and the gain section of the SG-DBR and low-saturation power regions for the nonlinear MZI SOAs. However, the decrease in saturation power due to high optical confinement limits the maximum possible unsaturated gain from the preamplifier SOAs. The base growth also incorporates an undoped InP buffer layer above the waveguide for QWI [23]. Passive device regions are defined by selectively implanting phosphorous into the undoped buffer layer above these regions. The implant creates point defects which are then diffused through the waveguide region using a rapid thermal anneal process in N_2 at 675 °C. These vacancies and interstitials allow diffusion of the group V elements across the metastable well and barrier boundaries to reshape the compositional profile of the MQW region and blue shift the band edge from an as-grown λ_{PL} of 1545 to 1420 nm. Because the passive regions still contain quantum wells, it is possible to realize more efficient phase shifters in the MZI region than would be available with only bulk waveguide. MQWs provide a greater refractive index change for a given injected current density than bulk material because of the step-like density of states of a 2-D system [24]. In practical terms, this means that less current (and hence a lower drive power) is required to tune the phase of the MZI to a normally closed (noninverting) or open (inverting) state.

Following QWI, the implant buffer layer is removed across most of the sample by wet etching. In the passive regions of the differential delay line and the AWGR, however, the buffer layer is not removed in order to provide an undoped setback

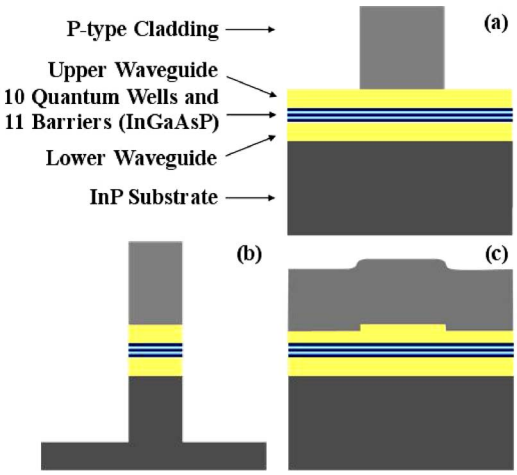

Fig. 5. Waveguide architectures used in the MOTOR chip: (a) surface ridge waveguide; (b) deeply etched waveguide; and (c) buried rib waveguide.

layer between the waveguide and the subsequent cladding. As described in [25], this helps to reduce optical loss from free carrier absorption due to the Zn dopant used in the cladding layer. The epitaxial structure is completed by a simple, blanket p-type regrowth [Fig. 4(b)]. A 150-nm heavily Zn-doped InGaAs layer is included in the regrowth for Ohmic p-type contacts. Using a single regrowth step reduces fabrication complexity and should have a positive impact on device yield. However, the Zn doping profile with this approach must be optimized to provide efficient active diode performance without detrimentally increasing passive propagation losses from free carrier absorption [26]. To address this inherent tradeoff, our cladding regrowth starts with a thin undoped InP layer followed by growth with Zn doping.

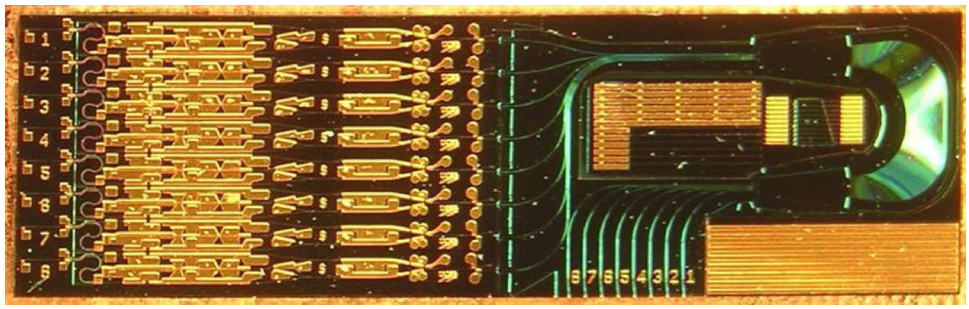

Fig. 6. Photograph of fabricated MOTOR chip. The chip is soldered to a large copper block and electrodes are directly probed. Miscellaneous test structures are contained in the center of the AWGR region, but these components are not used during the operation of the device.

Due to the elevated growth temperature, some Zn diffuses toward the waveguide, creating the desired p-i-n junctions of the device. The thickness of this undoped regrowth layer (typically ∼30–50 nm) is calibrated to ensure that the Zn doping concentrations within the waveguide are as low as possible. To reduce the loss further, additional pre- and postgrowth techniques are employed. Prior to growth as mentioned above, the undoped QWI buffer layer is left in the delay line and AWGR region to push the Zn away from the waveguide. After growth, a proton implant is utilized to passivate some of the activated Zn atoms above the waveguide, thus reducing passive losses to a more manageable level of about 1.9 cm^{-1} for a surface ridge waveguide.

Three different ridge waveguide architectures are used in MOTOR (Fig. 5). A surface ridge that stops at the top of the waveguide layer is utilized for all active components and most passive regions of the wavelength converters. This design offers a simple fabrication approach through a combination of dry and selective wet etching. Although the selective nature of the wet etch provides precise control of the etch depth, its crystallographic nature leads to detrimental undercutting of waveguides with an angle greater than about 15° off $[\bar{1}\,10]$ toward the $[110]$ direction. The device also employs a high-contrast, deeply etched waveguide region for the compact differential delay line in the wavelength converter. This region is partially defined during the dry etch step of the surface ridge waveguide to eliminate misalignment between the two sections. It is then protected with a resist mask during the wet etch of the surface ridge. An SiO_2 liftoff process is subsequently used to open the delay line region and a second dry etch through the waveguide is performed. Last, a buried rib waveguide is created in the AWGR region by dry etching through the implant buffer layer and 70 nm of the upper waveguide prior to the cladding regrowth, which consequently buries the structure. Because no selective wet etch is used, this approach can provide waveguides in the AWGR region that can be bent a full 180° to achieve a more compact structure.

IV. Experimental Setup

The fabricated MOTOR chip (shown in Fig. 6) was soldered to a copper block for testing. Because this is not an ideal heat sinking configuration, the device was maintained at 16 °C during operation using a thermoelectric cooler (TEC) to reduce thermionic emission of carriers from the MQW region of the device. Wire bonding was not practical given the size of the device so all electrodes were directly probed. Light was coupled to and from the chip using lensed fiber. The response of the AWGR was characterized using on-chip sources (i.e., MZI SOAs and the SG-DBR) and coupling the output from each port to an optical spectrum analyzer (OSA). Wavelength conversion and routing functions of the MOTOR chip were tested under single-channel operation with pseudorandom bit sequence (PRBS) $2^{31} - 1$ RZ data at 40 Gb/s. The input data signal is generated with a modulated external cavity tunable laser source, amplified with an erbium-doped fiber amplifier (EDFA) and filtered with a 5-nm filter. Because the device employs compressively strained MQWs, it is TE-polarization sensitive and a polarization controller is used to rotate the input signal to a TE orientation. Although the AWGR provides on-chip filtering at most wavelengths, the fiber-coupled output signal from the device is also filtered with an external 5-nm filter for cases in which the wavelength of the original input signal might correspond to an allowed output wavelength of the AWGR. The output was then transmitted to a preamplified receiver. Bit error rate (BER) measurements were made using a 40-Gb/s SHF BERT. A schematic of the test setup is shown in Fig. 7. Back-to-back BER measurements were made using all test elements in this setup with the MOTOR chip removed.

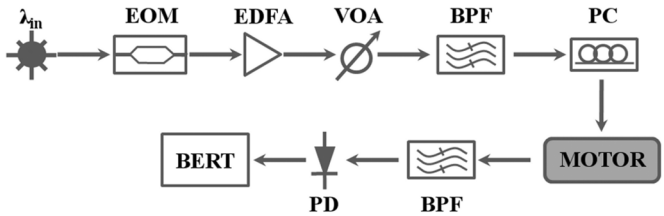

Fig. 7. Schematic of test setup. Key to abbreviations: EOM = electro-optic modulator; EDFA = erbium-doped fiber amplifier; VOA = variable optical attenuator; BPF = band-pass filter; PC = polarization controller; PD = photodiode; BERT = bit error rate tester.

V. Arrayed-Waveguide Grating Router Results

The performance of the AWGR was first characterized by forward biasing the MZI SOAs on a single-input wavelength converter to generate amplified spontaneous emission (ASE) and the spectral response from each egress port was measured. Fig. 8(a) shows a well-defined free spectral range (FSR) of approximately 11.1 nm from the AWGR and a single-channel crosstalk between −15.8 and −20.9 dB across all output ports (measured at the center wavelength of the ASE peak). Next, the pair of MZI SOAs in each input wavelength converter were

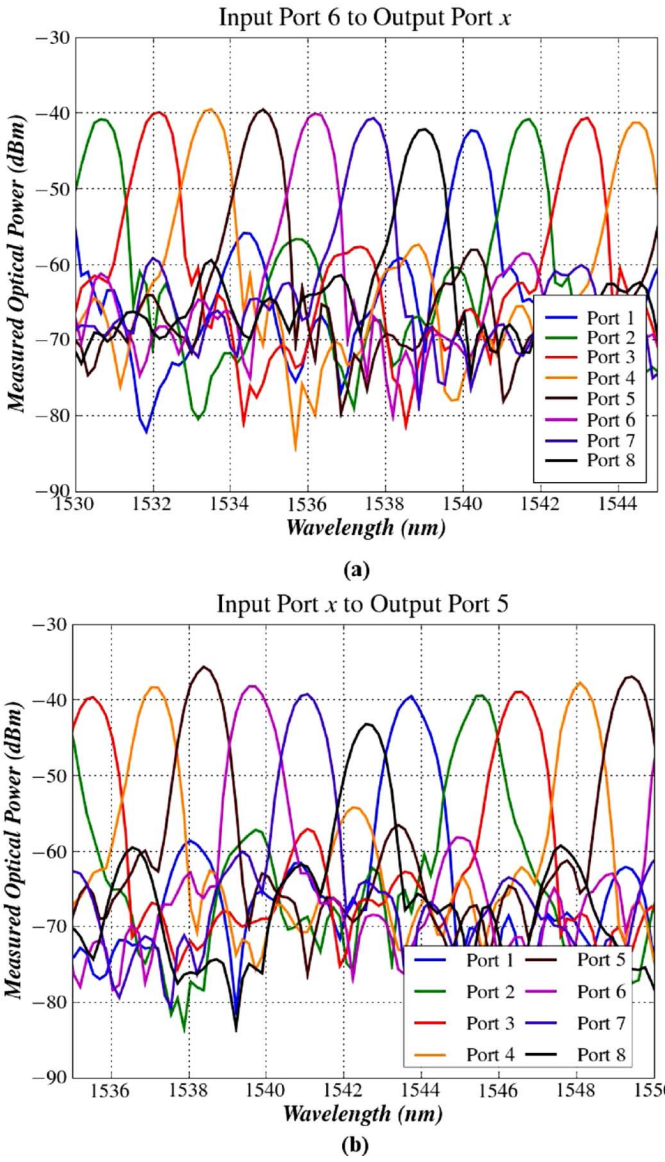

Fig. 8. Output ASE response of the integrated AWGR: (a) measured optical output from all output ports using input wavelength converter #3; (b) measured optical output from output port #2 using each input wavelength converter.

biased pair-by-pair at a constant bias level and the resulting spectra were measured from a single-output port [Fig. 8(b)]. Although some difference in power level is expected between center and outer ports of an AWGR, this figure illustrates that the performance of each input port varies, likely due to fabrication variations across the device. In general, all but one input port show crosstalk values in excess of −15.6 dB. Input port #8 only demonstrates a crosstalk of −12.3 dB, most likely due to a waveguide imperfection within this port. This will translate into a reduction in performance for port #8 relative to the other input wavelength converters.

To verify the performance of the device in terms of tunability, the SG-DBR was used in conjunction with the booster SOAs, which were forward biased to provide gain to the CW signal from the SG-DBR. Because the MZI SOAs are in the path between the SG-DBR and the AWGR, they were also biased in order to allow the signal to propagate without being absorbed.

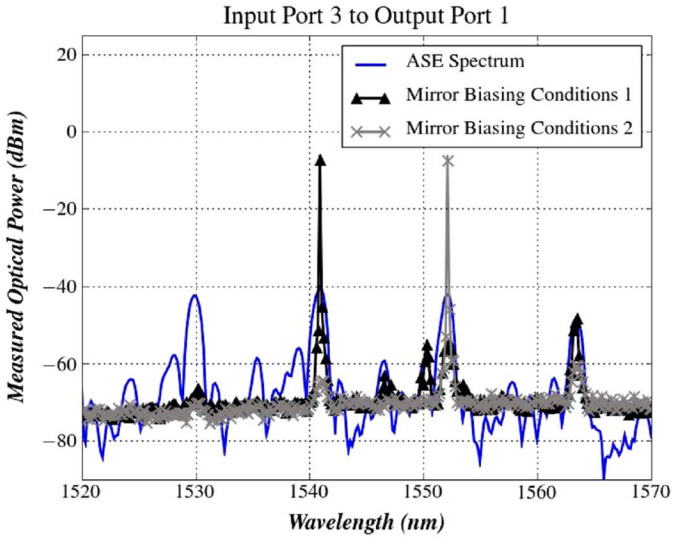

Fig. 9. Lasing spectra for different biasing conditions using the SG-DBR of input wavelength converter #3 superimposed on the ASE spectrum generated by forward biasing just the MZI SOA pair in that channel, all measured from output port #1.

By changing the biasing conditions on the front and back mirrors of the SG-DBR, the laser can be tuned to any of the allowed output wavelengths of a given port in order to achieve full channel switching. Fig. 9 shows the resulting spectra for two different mirror biasing conditions from a single-input wavelength converter to a single output. In this configuration, we measured output powers approaching −5 dBm.

Given the current architecture of our device, it is not possible to directly measure the insertion loss of the AWGR without cleaving it from the wavelength converter array. To make a reasonable estimate of the total throughput loss between the wavelength converters and the output, we measured the total power (including ASE) directly at the exit of the wavelength converter in an integrated power monitor diode with the SG-DBR, booster SOAs, and MZI SOAs forward biased at typical operating conditions. (We estimated the quantum efficiency of this power monitor by measuring the absorbed power in this pad when coupling a CW signal backward through the device from the exit of the AWGR into the wavelength converters and then comparing it to the power measured in the long MZI SOAs which should absorb all the incoming light.) The total power out of the AWGR was coupled into an output fiber and measured in an OSA. Assuming 4–5 dB of coupling loss to the fiber, the total power loss through the AWGR was estimated to be ∼8–10 dB. It is important to note that this loss also includes the loss associated with transitioning from the surface ridge waveguide of the wavelength converter to the buried rib waveguide of the AWGR, which could not be measured directly.

To improve overall device performance, the total loss in the AWGR region should be reduced. The higher than desired loss in our structure is likely due to two main factors. First, because the input and output lines and the arrayed waveguides are defined with the buried rib structure which etches into the waveguide layer, sidewall roughness created during the dry etch can result in high scattering losses. This would especially affect the input and output waveguides to and from the star couplers,

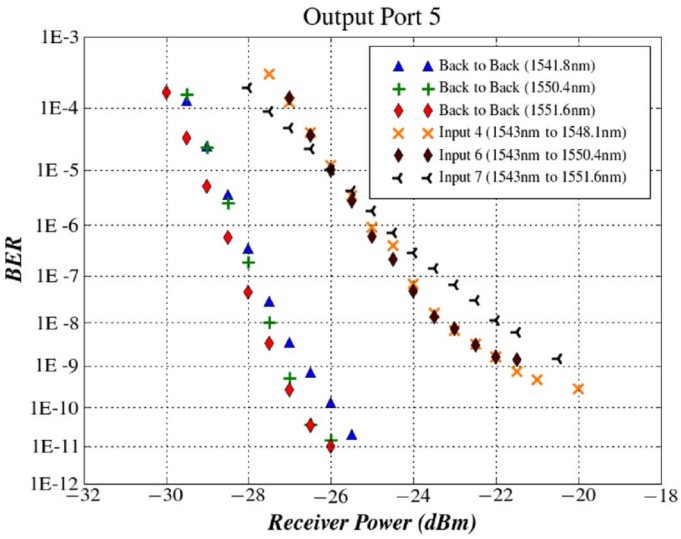

Fig. 10. BER measurements for several input wavelength converters at 40 Gb/s monitored from a constant output port. Back-to-back BER measurements are also included for the converted wavelengths.

which range in length from 6 to 10 mm. A future, more compact AWGR design similar to that of [27] could reduce these passive losses and increase the overall output power from the router. The design of [27] is also promising because it would eliminate the separate dry etch step currently used for the AWGR, thus reducing fabrication complexity. A second contribution to our AWGR loss is the coupling loss between the star couplers and the arrayed waveguide. Our lithographic capabilities should allow us to bring the waveguides separation down from their current value of 0.8 to about 0.5 μm in a future design to help reduce these coupling losses.

VI. Wavelength Converter and Routing Results and Discussion

Once the tuning characteristics of the SG-DBR are known, 40-Gb/s wavelength conversion and channel switching in the RZ data format can be achieved. Typical bias levels used for wavelength conversion are given in Table I. Figs. 10 and 11 show BER results and the associated eye diagrams for wavelength conversion from multiple-input channels through a constant output port, respectively. Eye diagrams are not shown for three of the eight wavelength converters. Although the diode yield was close to 100%, two channels did not function because of a random ridge defect in the MZI region. The other missing channel was damaged during testing. However, since the working channels have an identical structure, there are no inherent wavelength converter design issues and all channels are expected to work with an improved fabrication yield. Next, we measured the BER for wavelength conversion through different output ports using a constant input channel (Fig. 12). Open eye diagrams were also obtained for all eight output ports using a single-input channel (Fig. 13).

These results demonstrate the tunable routing ability of the MOTOR chip, as the input data to one input port can be directed to different output ports by simply changing the SG-DBR mirror biasing conditions. Figs. 10 and 12 also demonstrate that BERs

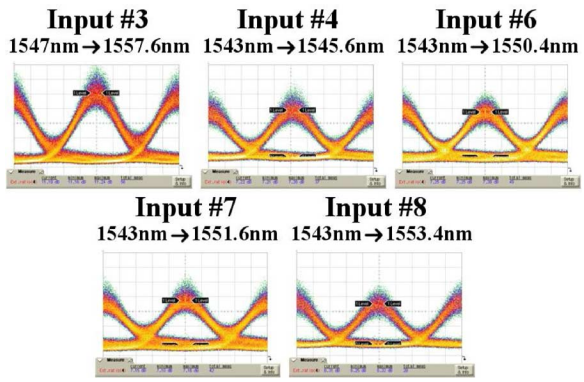

Fig. 11. Open eyes diagrams for several input wavelength converters at 40 Gb/s from a constant output port.

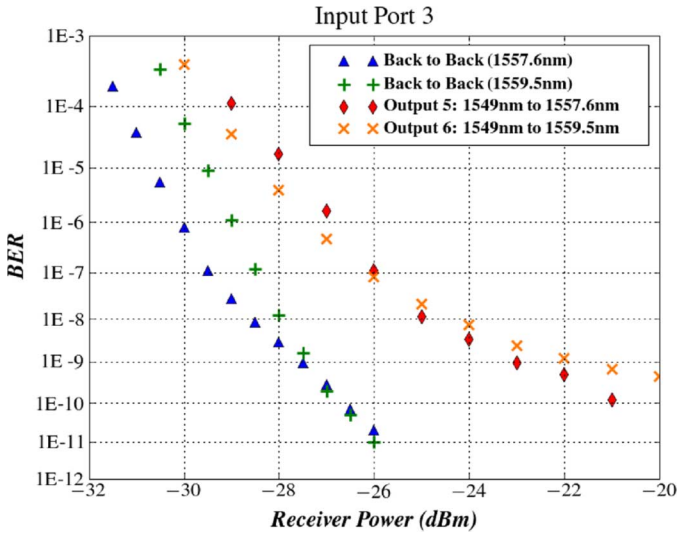

Fig. 12. BER measurements for a single-input wavelength converter at 40 Gb/s monitored from different output ports. Back-to-back BER measurements are also included for the converted wavelengths.

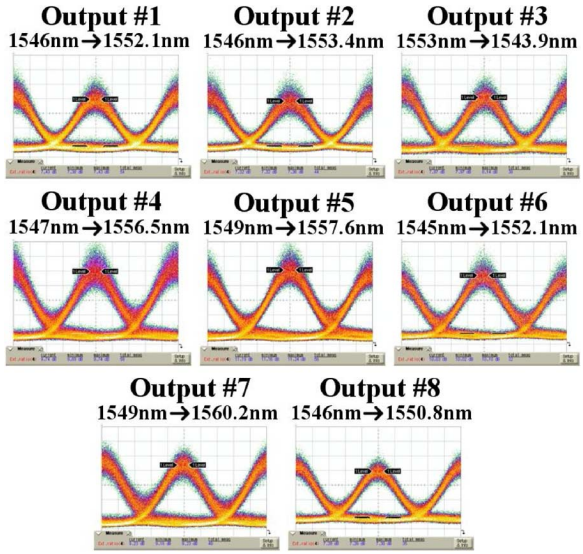

Fig. 13. Open eyes diagrams for a single-input wavelength converter at 40 Gb/s from all eight output ports.

below 1E-9 are possible for the combined wavelength conversion and routing process. The measured power penalties at this

TABLE I
WAVELENGTH CONVERTER TYPICAL BIASES

Component	*Bias (mA)*
Preamplifer SOAs	110-140
Booster SOAs	30-60
MZI SOAs	210-290
MZI Phase Modulator	0-5
SG-DBR Gain	100-110
SG-DBR Front Mirror	0-25
SG-DBR Back Mirror	0-25

BER range from approximately 4.5 to 7.0 dB (depending on the input port).

The noise floor and high-power penalty seen in these results are likely attributable to two main factors. First, the tested MOTOR chip was not antireflective (AR) coated. Additionally, given the high power of the SG-DBR, other minor reflections may exist in the device during operation. These reflections within the chip might occur at the transitions between the three different waveguide architectures. In future MOTOR designs, optimized AR coatings are planned to address this reflection issue.

Second, we measured a clear pattern dependence during wavelength conversion due to saturation in the preamplifier SOAs made from the centered MQW band edge. In order to provide enough gain to the input signal to deplete the MZI SOAs of carriers and modulate the MZI, the preamplifier SOAs had to operate in the nonlinear gain regime. This resulted in pattern distortion effects and an increased BER. In order to overcome these limitations, a more complex preamplifier structure will be required. One possible approach to increase the saturation power of the preamplifiers would involve combining the short centered MQW SOA in our device with a second MQW SOA section regrown some distance above the center of the waveguide as in [28]. This method has demonstrated SOAs with gains as high as 15 dB and output saturation powers of $>$19 dBm, but the additional regrowth could have a negative impact on device yield.

The results reported here apply only to single-channel operation. Moving to multiple-channel operation will not only require more elaborate biasing and fiber coupling schemes, but will also increase the expected power penalty for the combined process of wavelength conversion and switching. One key reason for this is expected to be the increased heating in the device with all diodes biased. This increased heating can lead to signal degradation and reduced output power due to thermal crosstalk effects in both the wavelength converters and the AWGR. Efficient heat sinking will therefore be vital to overall performance.

VII. POWER CONSUMPTION CONSIDERATIONS

The wavelength conversion and switching functions of the MOTOR chip come at a relatively low cost in terms of power consumption. Under normal operating conditions, the single-channel drive power is less than 2 W, giving an overall expected drive power of less than 16 W for eight-channel operation. However, additional power is necessary for TEC cooling. In our current testing configuration, the TEC requires $\sim$0.5 W to maintain a single channel at the 16 °C temperature used during testing. In a real application, the chip would be packaged with more efficient heat sinking (i.e., flip-chip bonding) with all channels operating simultaneously. The operating temperature would also likely be higher to match that of other system elements. Therefore, although the results reported here are promising, further work to characterize TEC demands under these conditions is needed before accurate comparisons with electronic router components can be drawn.

VIII. CONCLUSION

We report the demonstration of the first InP 8×8 MOTOR capable of 40-Gb/s operation per port with BERs below 1E-9. The device represents one of the most densely integrated InP chips ever reported, with more than 200 integrated functions and power penalty as low as 4.5 dB at 40 Gb/s. Under normal operating conditions, the per channel power consumption is less than 2 W. Improved power penalty is expected with future designs employing AR coatings and optimized preamplifier SOAs.

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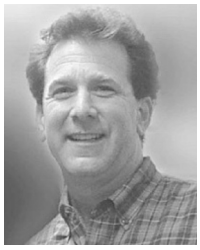
Prof. Coldren has presented dozens of invited and plenary talks at major conferences. He is a Fellow of the Optical Society of America (OSA) and the Institution of Electrical Engineers (IEE), the recipient of the 2004 John Tyndall Award, and a member of the National Academy of Engineering.



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Dr. Blumenthal was the recipient of the 1999 Presidential Early Career Award for Scientists and Engineers from the White House, the 1994 National Science Foundation Young Investigator Award, and the 1997 Office of Naval Research Young Investigator Program Award. He has served as an Associate Editor for the IEEE PHOTONICS TECHNOLOGY LETTERS and the IEEE TRANSACTIONS ON COMMUNICATIONS, as a Guest Editor for the JOURNAL OF LIGHTWAVE TECHNOLOGY special issue on photonic packet switching systems and the IEEE JOURNAL OF SELECTED AREAS IN COMMUNICATIONS special issue on high-performance optical/electronic switches/routers for high-speed Internet. He has served as the General Program Chair for the 2001 Optical Society of America (OSA) Topical Meeting on Photonics in Switching and as Program Chair for the 1999 Meeting on Photonics in Switching. He has also served on numerous other technical program committees. He is a Fellow of the Optical Society of America (OSA).

High-Performance Photonic Integrated Circuits (PICs)

Larry A. Coldren

OFC Tutorial
OWD1

March 24, 2010

Outline/Contents

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- **Motivation/the Demand for Data**
- **An Example Complex PIC: a single-chip router**
- **Integration Platforms/Technology**
  - **Indium Phosphide**
- **Serial & Parallel Integration Approaches**
  - **Transmitters/Receivers/Wavelength Converters**
- **Improved Spectral Efficiency Issues**
  - **Advanced modulation formats**
  - **Coherent techniques/Optical phase locked loops**
- **Summary**

Communication Requires a Complex Network

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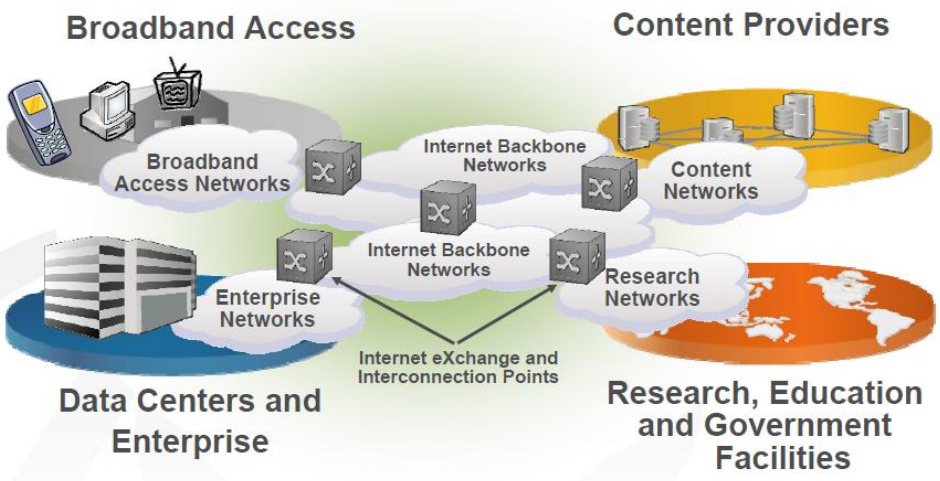
- It's nearly all optical



Data is King

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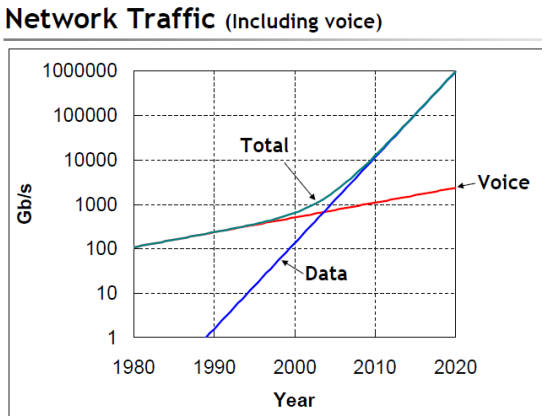
- Today traffic on the core network is nearly all data



A Typical Data Center

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- > 30 MW power requirements
- Require many Gb/s of bandwidth—justifies 100Gb-Ethernet

Electronic Routing Burns Lots of Power

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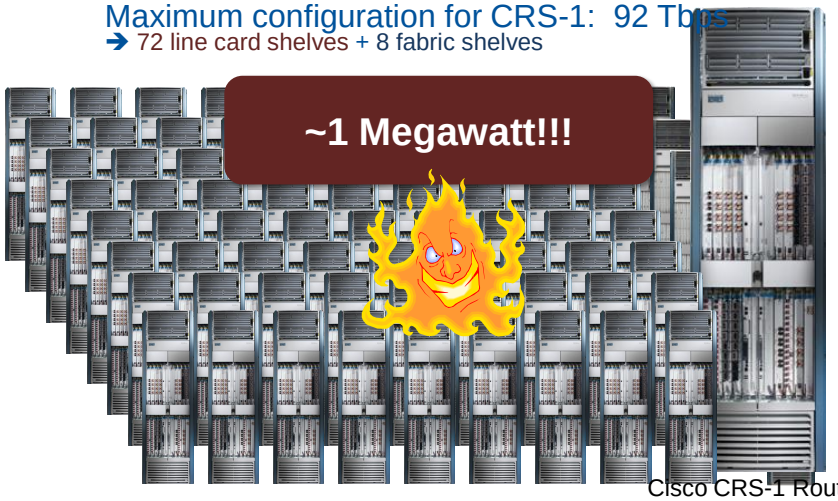
- **Problem:** Bandwidth demands scaling faster than both silicon and cooling technologies

Maximum configuration for CRS-1: 92 Tbps
➔ 72 line card shelves + 8 fabric shelves



Cisco CRS-1 Router

Optical-to-Electronic-to-Optical Switching

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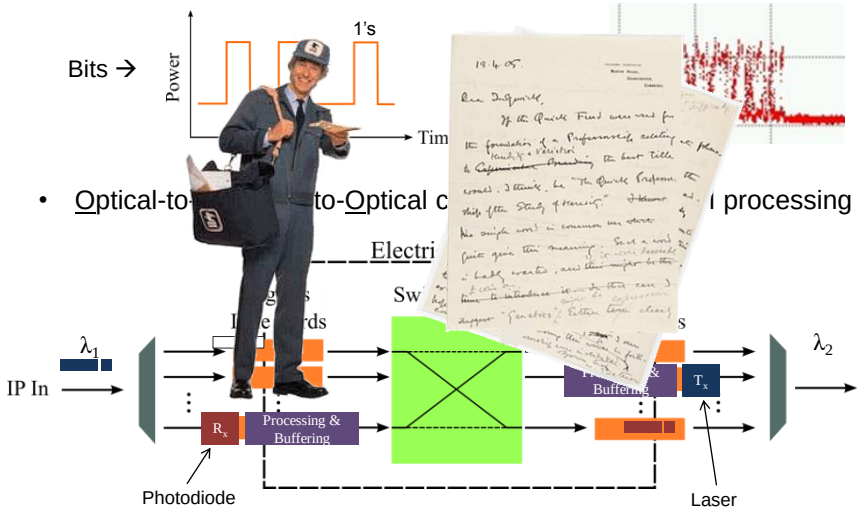
- Internet data transmitted in groups of bits = “packets”



- Optical-to- to-Optical c processing

Example of a Complex PIC: A Monolithic Tunable Optical Router (MOTOR)

A UCSB Router Solution: the MOTOR Chip

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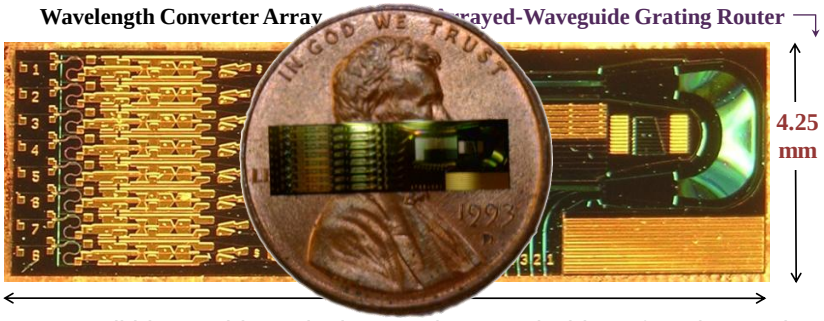

- A monolithic tunable optical router (MOTOR) chip to function as the switch fabric of an all-optical router
  - Line rate: 40 Gbps / channel
  - Total capacity: 640 Gbps
  - Error-free operation
- Photonic integration technologies designed for high-yield, large-scale applications
- World's largest and most complex Photonic IC

LASOR

Steven C. Nicholes, M. L. Mašanović, E. Lively, L. A. Coldren, and D. J. Blumenthal, *IPNRA '09*, Paper IMB1 (July, 2009); also *JLT*, (Jan. 2010) in press.

640 Gbps MOTOR

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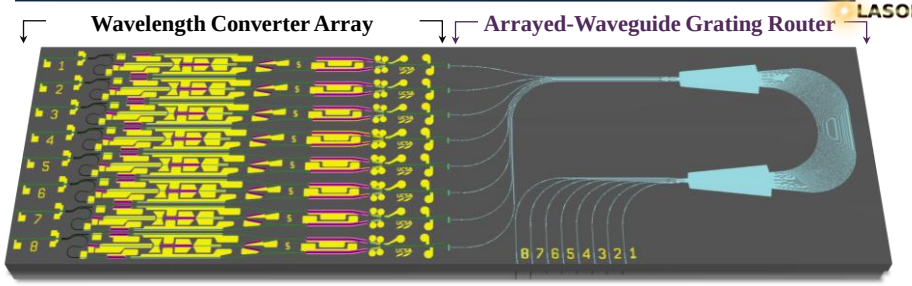
LASOR



Benefits of integrated solution:	
Size	• Smaller device footprint • Smaller rack space for increased bandwidth
Power	• No power required in passive AWGR (free switching—no transistors) • Lower power consumption with all-optical approach
Cost	• Reduced packaging and system costs • Fewer fiber alignments
Performance	• Increased reliability

Leading Edge of Monolithic Integration

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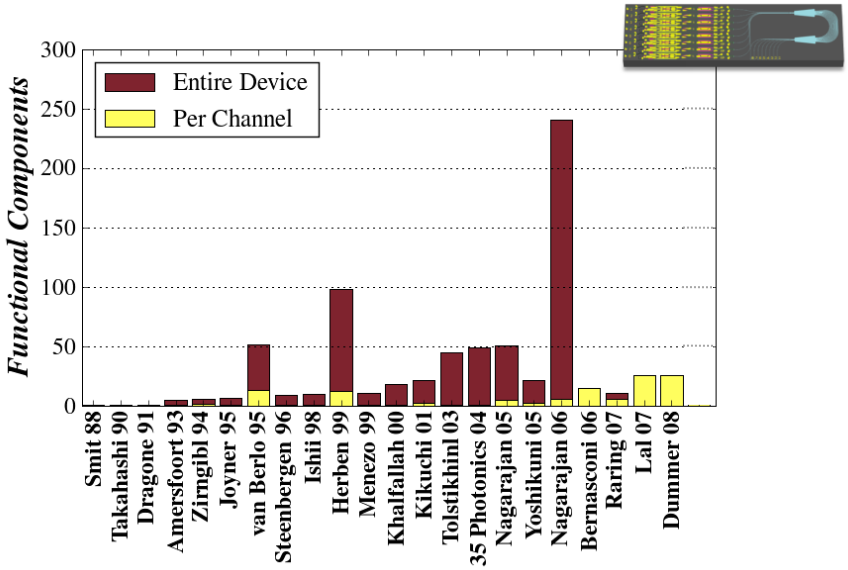

8 x 8 MOTOR Chip: (40 Gb/s per channel)

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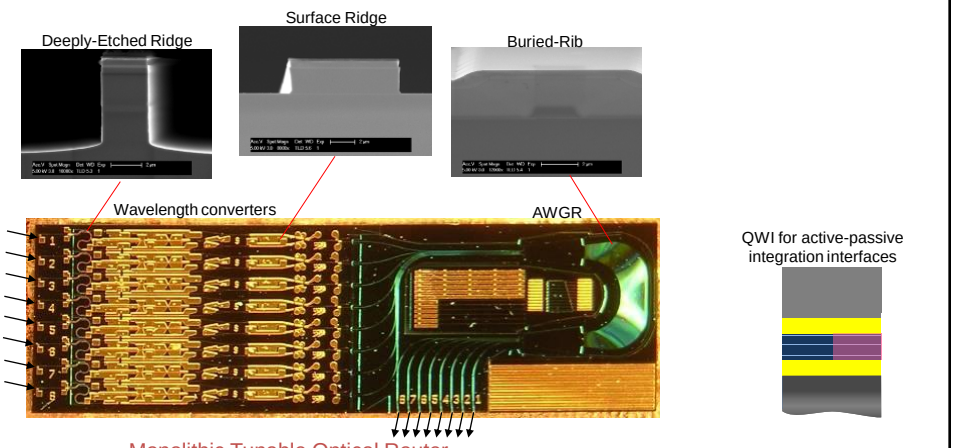
LASOR

SOA – Mach-Zehnder Wavelength Converters
Quantum-well intermixing (QWI) to shift bandedge for low absorption in passive regions
Three different lateral waveguide structures for different curve/loss requirements



Monolithic Tunable Optical Router

See S. Nicholes, et al, "Novel application of quantum-well intermixing implant buffer layer to enable high-density photonic integrated circuits in InP," *IPRM '09*, paper WB1.2, Newport Beach (May, 2009)

MOTOR Results :
Constant Input Port: 40 Gbps RZ

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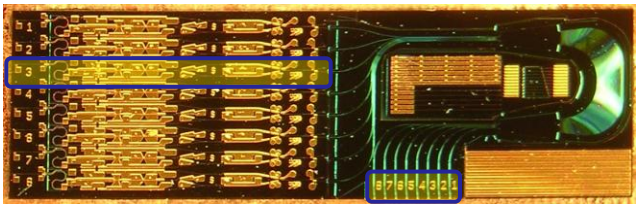
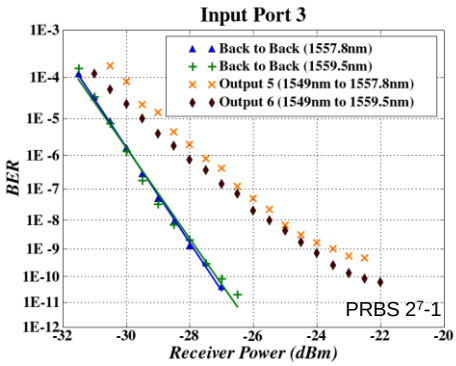
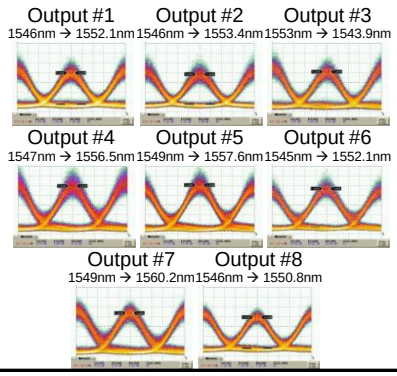
LASOR



- Power penalty at BER = 1E-9 for PRBS 2^7-1 data at 40 Gbps
  - ≥ 3.5 dB

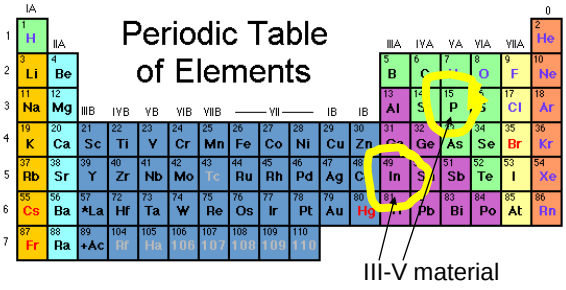
  (no AR coating)

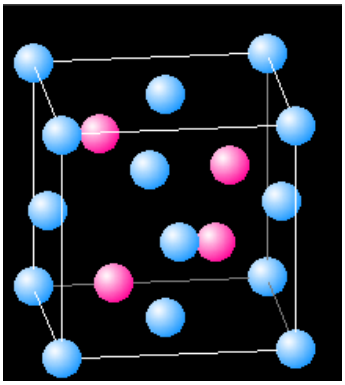




Indium Phosphide as the Materials Platform

Indium Phosphide





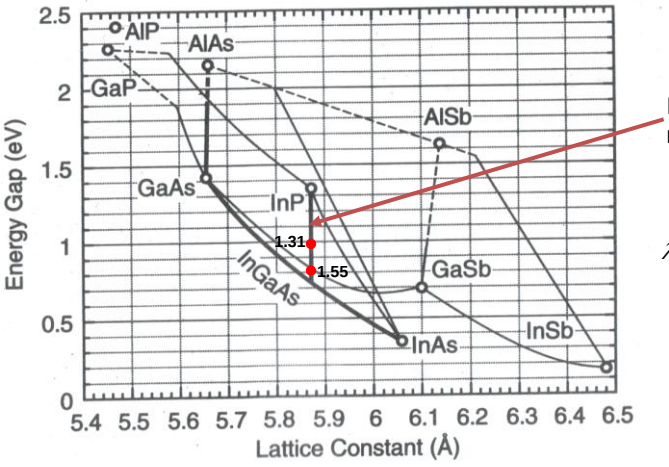
Zincblende structure

(two intersecting FCC lattices, one for In and one for P)

Lattice constant = 5.87 A at 300K

courtesy of C. Doerr

InGaAsP/InP lattice-matched alloys



InGaAsP lattice-matched to InP

$\lambda_g(\mu m) = 1.24/ E_g(eV)$

Lateral waveguides/couplers

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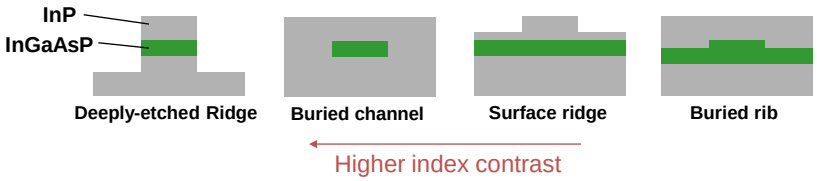
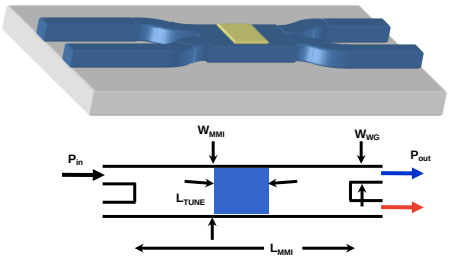
Waveguide cross sections



Higher index contrast

MMI coupler



Active-Passive (axial) Integration

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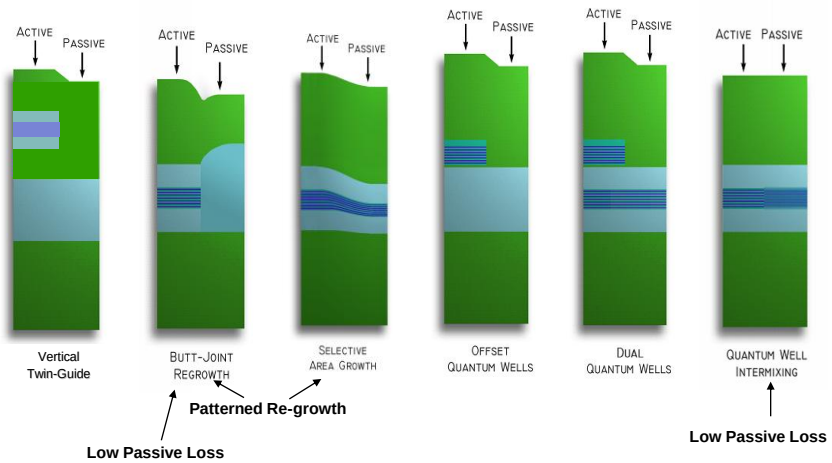
Desire lossless, reflectionless transitions between sections



3 Bandgaps usually desired

QWI For Multiple-Band Edges/Single Growth

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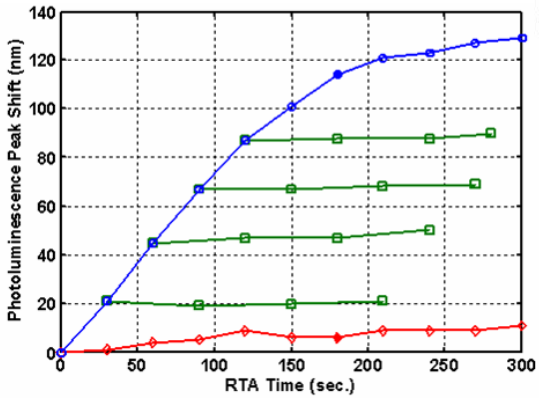
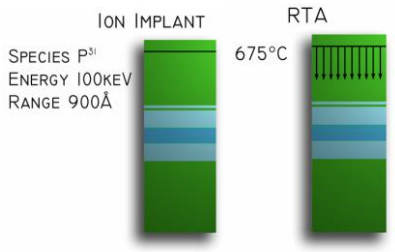
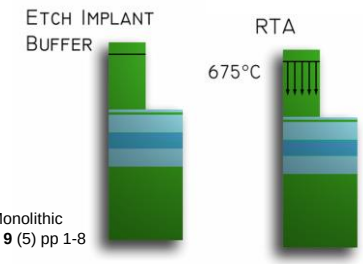
Simple/robust QWI process
- Ability to achieve multiple band edges with a single implant







E. Skogen et al, "Post-Growth Control of the Quantum-Well Band Edge for the Monolithic Integration of Widely-Tunable Lasers and Electroabsorption Modulators," *JSTQE*, **9** (5) pp 1-8 (Sept, 2003).

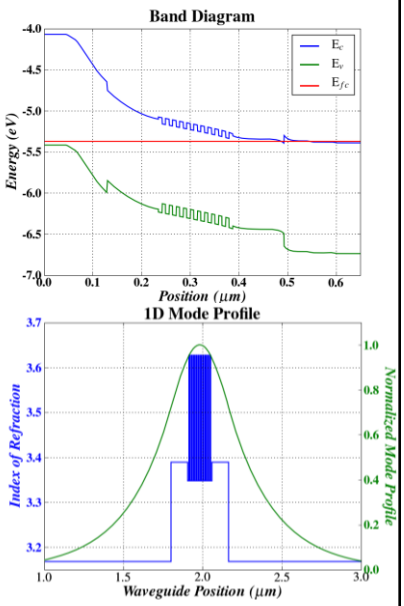
Integration Strategy: MOTOR Chip

Integration Platform for MOTOR Chip

UCSB

- Strategy:
  1. Centered MQW base structure
  2. Quantum-well intermixing for active/passive definition
  3. Single blanket cladding regrowth

- Trade-offs:
  1. Limited total number of regrowths → need multiple waveguide architectures
  2. Efficient active diodes → higher passive losses due to Zn in cladding
  3. Efficient high-gain, low-saturation power elements → nonlinear preamplifiers
  4. Polarization sensitivity

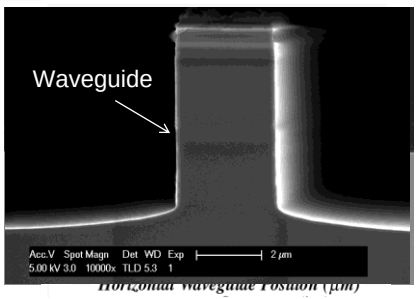


Multiple Waveguide Architectures

UCSB

- Need multiple waveguide designs to integrate diverse range of components

Waveguides



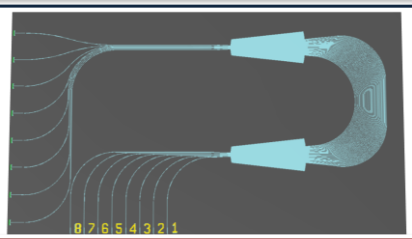
Surface Ridge

- Ridge defined through p-type cladding and stops at waveguide layer
  - Dry etch only
  - Strong lateral confinement → sharp bends possible
  - Wet etch is crystallographic → no bends over ~15°

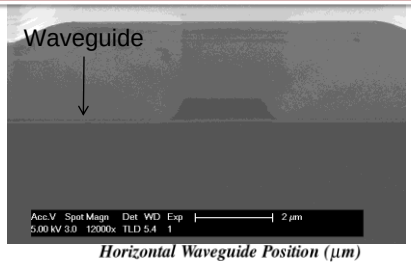
Buried Ridge

- Ridge defined through waveguide layer
  - Dry etch + selective "clean up" wet etch

Multiple Waveguide Architectures



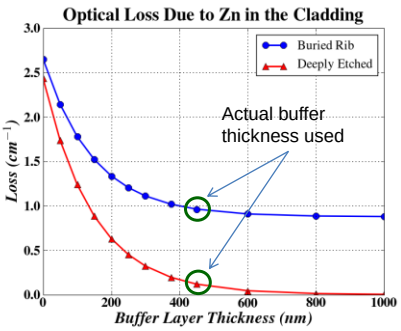
Need short mode transition elements to maximize coupling between waveguide regions



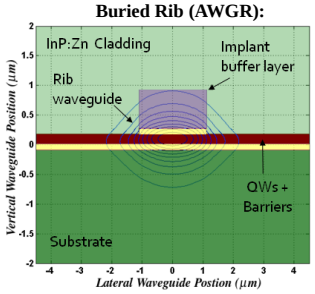
- Partial etch into upper waveguide prior to cladding regrowth, which buries it
  - Low index contrast
    - → Larger footprint
  - Dry etch due to high-angle bends

QWI Implant Buffer for Low-Loss Waveguides

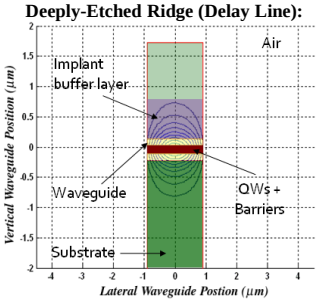
- Use QWI implant buffer to provide undoped setback layer between optical mode and Zn atoms
- Simulated *reduction* in optical loss:
  - Deeply-etched > Buried rib
  - No lateral mode interaction with Zn doped cladding



Buried Rib (AWGR):



Deeply-Etched Ridge (Delay Line):

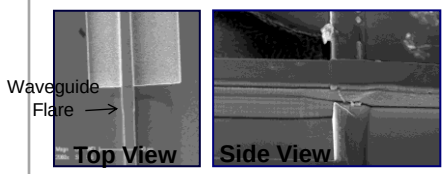


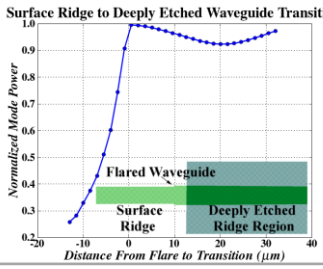
Transitions Between Waveguide Designs

UCSB

Surface-to-Deep Ridge Transition

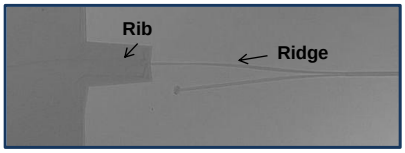
- "Mode matching" transition [1]
  - Surface ridge flares and tapers before deep ridge section
  - No lateral misalignment issues

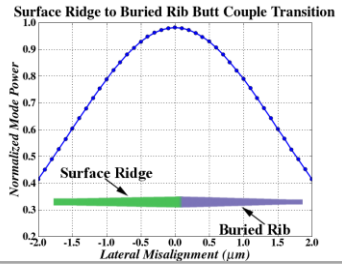




Surface-to-Buried Rib Transition

- Flared/tapered butt-couple transition
  - Surface ridges flares and butt couples to tapering rib waveguide
  - Fairly tolerant to lateral and longitudinal misalignment





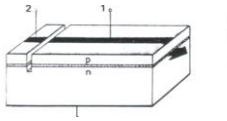
[1] *J. H. den Besten et al., Photon. Tech. Lett., vol. 14, Jan. 2002*

Widely-Tunable-X PICs
(Mostly serial integration)

Early PICs

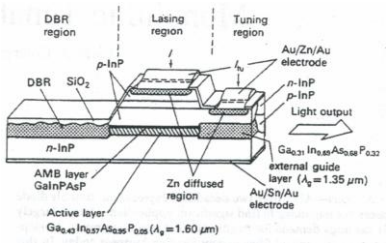
→ Etched grooves
- Tunable single frequency
- Laser-modulator
- Laser-detector

L.A. Coldren, B.I. Miller, K. Iga, and J.A. Rentschler, "Monolithic two-section GaInAsP/InP active-optical-resonator devices formed by RIE," *Appl. Phys. Letts*., 38 (5) 315-7 (March, 1981).



→ DBR gratings and vertical couplers
- Tunable single frequency
- Combined integration technologies

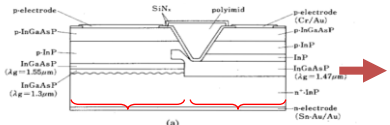
Y. Tohmori, Y. Suematsu, Y. Tushima, and S. Arai, "Wavelength tuning of GaInAsP/InP integrated laser with butt-jointed built-in DBR," *Electron. Lett*., 19 (17) 656-7 (1983).



→EML = electroabsorption-modulated laser

- Still in production today

M. Suzuki, et al., *J. Lightwave Technol.,* **LT-5**, pp. 1277-1285, 1987.

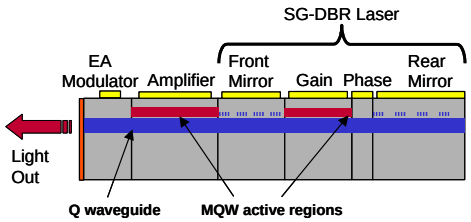


DFB laser EAM

SGDBR-SOA-Modulator PIC

SGDBR+X: Foundation of PIC work at UCSB
Heart of Wavelength Converter

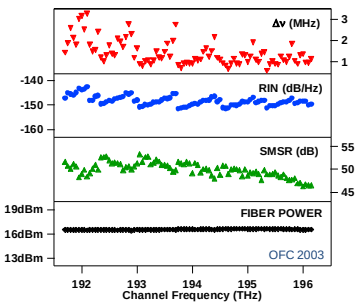
(UCSB'90-- → Agility'99-'05 → JDSU'05→)



"Multi-Section Tunable Laser with Differing Multi-Element Mirrors," US Patent # 4,896,325 (January 1990)

6 section InP chip

- SOA external to cavity provides power control
- Both EAM and MZ modulators integrated

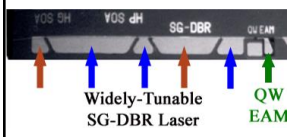


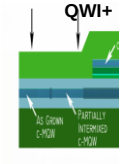
- Over a million in the field today carrying live traffic
- JDSU-ILMZ recently released as TOSA

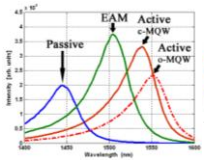
SGDBR-SOA-modulator transmitters @ 40 Gb/s

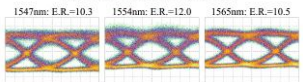
UCSB

1. QWI/EAM :







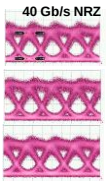


f_{3dB}=32 GHz/175µm—20dB/V (1536-1560nm)
V_{pp} = 2.5V

J.W. Raring and L.A. Coldren, *JSTQE* **13**, (1), pp. 3-14, (Jan. 2007)

2. Dual QW/TW-EAM :

LASOR

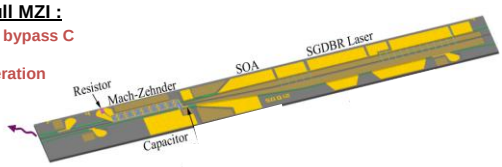


- 15 – 20 dB/V for 600 µm over range
- Open eyes for all wavelengths
  - 6 – 10 dB extinction with 2.1V

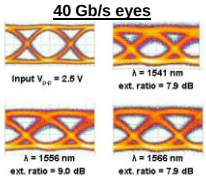
M. M. Dummer, et al, *OFC'08*, San Diego, Mar, 2008.

3. Series Push-Pull MZI :

Integrated load R and bypass C
30 GHz Bandwidth
40 Gb/s error free operation
Low/negative chirp



40 Gb/s eyes



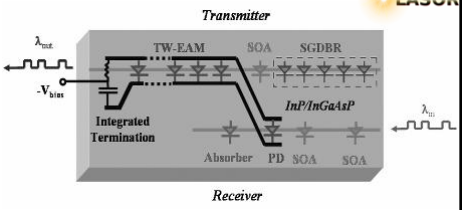
A. Tauke-Pedretti, etal, *Photon. Tech. Lett.*, **18** (18) 1922-4 (2006).

Transceiver/wavelength-converter: 2-stage-SOA-PIN & SGDBR-TW/EAM

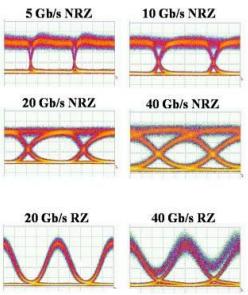
UCSB

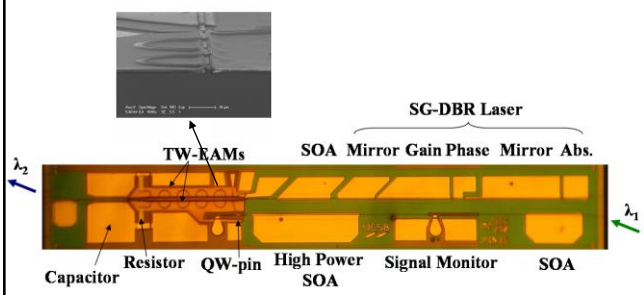
LASOR

- Data format and rate transparent 5-40Gb/s
- No filters required (same λ in and out possible)
- On-chip signal monitor
- Two-stage SOA pre-amp for high sensitivity, efficiency and linearity
- Traveling-wave EAM with on chip loads
- Only DC biases applied to chip—photocurrent
- directly drives EAM
- 40 nm wavelength tuning range



Eye Diagrams





M. Dummer et al. Invited Paper Th.2.C.1, *ECOC 2008.*

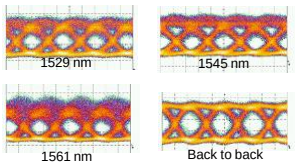
Wavelength converter/SOA-PIN receiver & SGDBR-Mach Zehnder transmitter

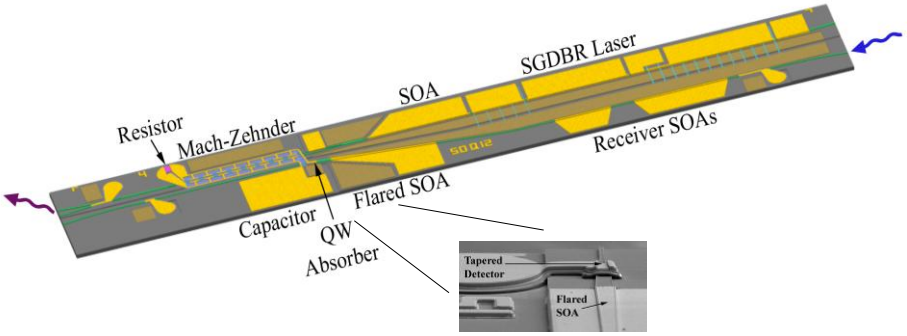
UCSB

LASOR

- Photocurrent driven
- 35 µm QW absorption region in receiver
  - Tapered for reduced capacitance
- 300 µm traveling-wave Mach-Zehnder modulation region
  - Series-push-pull design to maximize bandwidth
  - Chirp management
- Data format and rate transparent
- No optical filter required
- Integrated termination resistor and bypass Capacitor
  - No external bias tees used

40 Gb/s Eyes



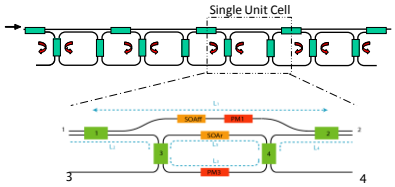


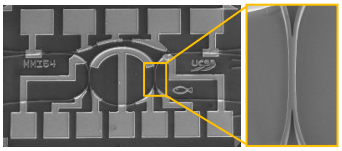
A. Tauke-Pedretti, et al, *J. Lightwave Tech.* **26** (1) pp91-98 (Jan. 2008)

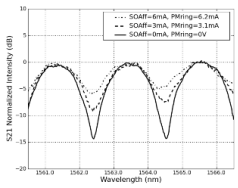
Programmable Photonic Lattice Filters

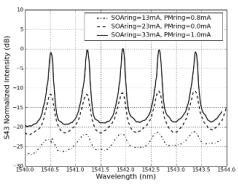
UCSB

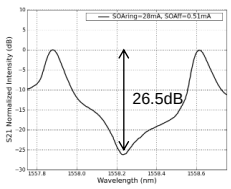
- Prefilter information, avoiding the latency and bandwidth restrictions of purely digital signal processing approaches
- Demonstrate programmable poles and zeros from a single unit cell that can be cascaded to form complex lattice filters
- Incorporate SOAs and Phase Modulators to control filter parameters





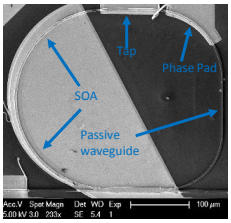






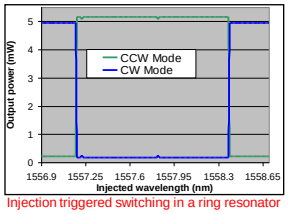
See E.J. Norberg, R.S. Guzzon, S. Nicholes, J.S. Parker, and L. A. Coldren, "Programmable photonic filters fabricated with deeply etched waveguides," *IPRM '09*, paper TuB2.1, Newport Beach (May, 2009)

Bistable Ring Resonators for Digital Logic

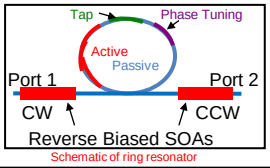


SEM image of single ring resonator

Separate gain, phase-shift, and monitoring (tap) sections added to passive waveguide in ring



Injection triggered switching in a ring resonator

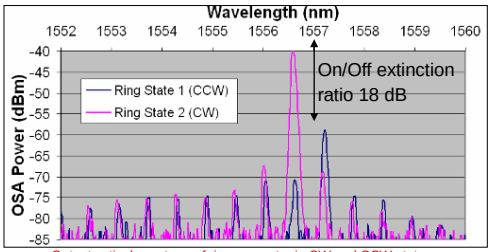


Schematic of ring resonator

Single-port injection:

- Injected tunable laser switches ring between CW / CCW lasing.
- CW mode > 98% power into Port 1.
- CCW mode > 98% power into Port 2.
- Single-port switching reduces design complexity and round trip delay.
- SMSR >25 dB.
- Injected laser -35 dB below ring lasing power.

Verifies sensitive cw-to-ccw sample-and-hold

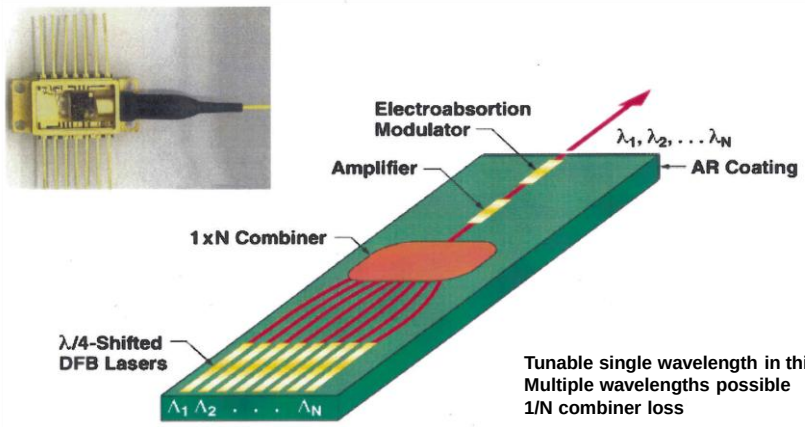


Output optical spectrum of ring resonator in CW and CCW states

J. Parker, et al, IPNRA '09, IWA2, Honolulu

Integrated Multi-Channel PICs
(Mostly parallel integration)

Early PIC with wavelength-selectable laser and EAM

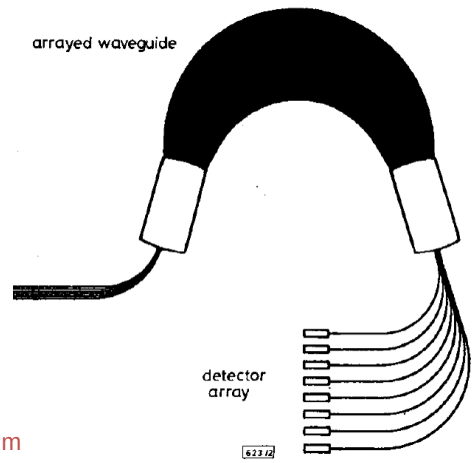


Tunable single wavelength in this case
Multiple wavelengths possible
1/N combiner loss

M. G. Young, et al., *Electron. Lett.*, **31**, pp. 1835-1836, 1995.

Early PIC multi-wavelength receiver

Wavelength Demultiplexer + Detectors



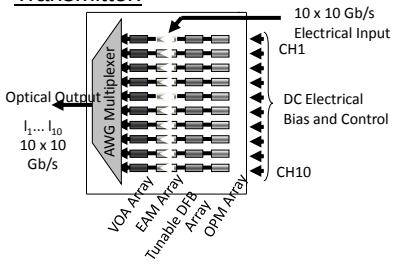
8 2 nm

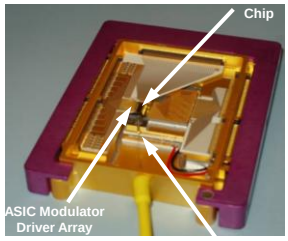
J. B. D. Soole, et. al., *Electron. Lett.*, pp. 1289-1290, 1995.

Infinera multi-channel commercial transmitter & receiver PICs: 10 x 10 Gb/s

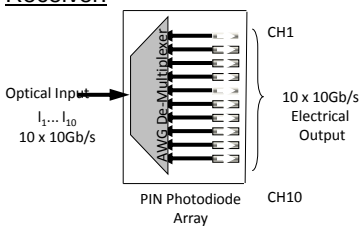
UCSB

Transmitter:



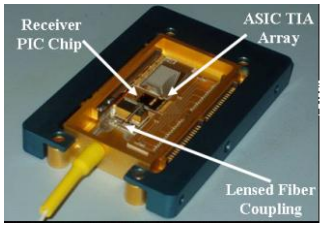


Receiver:



Low polarization dependant loss

Receiver < 0.38 dB



R. Nagarajan, et al., *Sel. Top. Quant. Electron.*, **11**, pp. 50-65, 2005.

courtesy of C. Joyner

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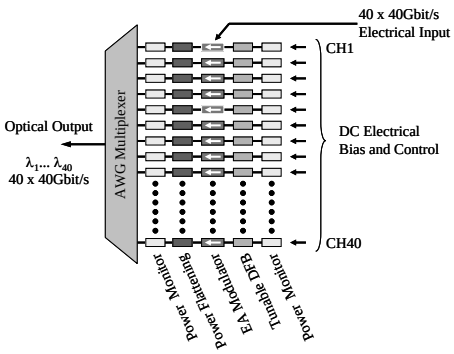
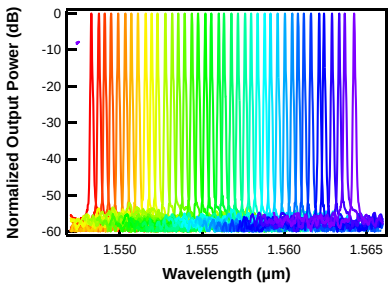
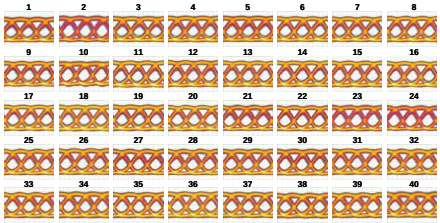
40 x 40 Gb/s results

UCSB

1.6Tbit/s DWDM Large-Scale PIC Transmitter







1.6 Tb/s single chip
40 channels
40 Gb/s modulation / channel

R. Nagarajan, et.al., *IEE Electronic Letters*, Vol. 42, no. 13, pp771-773 (2006).

courtesy of C. Joyner

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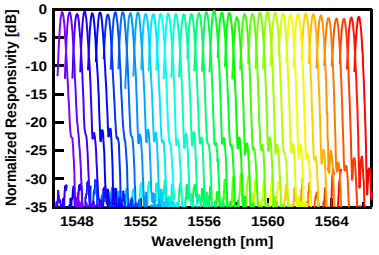
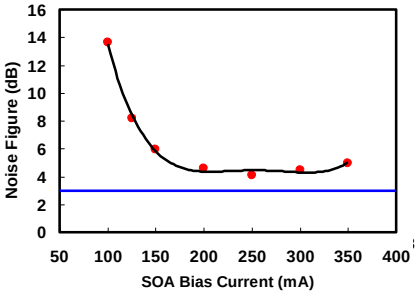
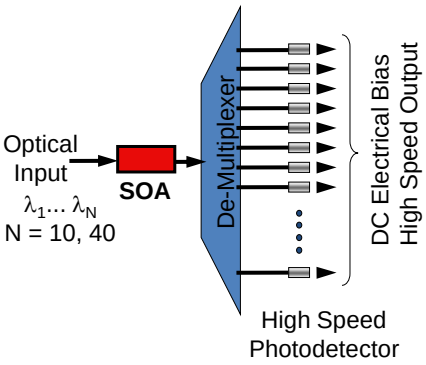
Amplified 40 channel receiver spectrum

UCSB







Nagarajan, PDP32 *OFC* 2007

courtesy of C. Joyner

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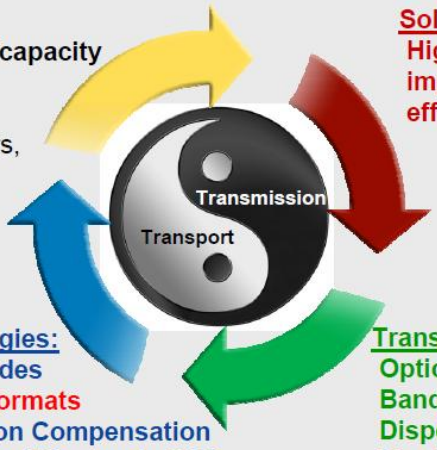
Meeting the Future Demand

UCSB

Upgrading Systems to 40 Gb/s or even 100 Gb/s Faces Serious Transport and Transmission Issues

Goal:
More bandwidth/capacity over installed infrastructure
(with existing fibers, EDFAs, DCMs, and OADMs)



Solution:
Higher data rates and improved spectral efficiency

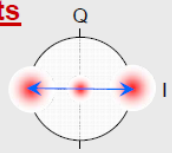
Enabling Technologies:
Advanced FEC Codes
New Modulation Formats
Adaptive Dispersion Compensation
Coherent Detection / Electronic DSP

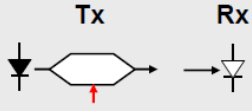
Transport Impediments:
Optical Noise (OSNR)
Bandwidth Narrowing
Dispersion (CD, PMD)
Nonlinearities (SPM, XPM)

Advanced Modulation Formats

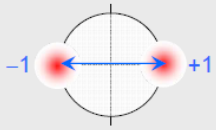
UCSB

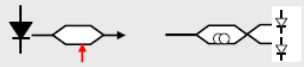
- **Binary modulation formats** (1 bit/symbol):
  - Optical duobinary / PSBT
  - NRZ- / RZ-DPSK ("bipolar" ASK)
- **Quaternary** (2 bits/symbol):
  - NRZ- / RZ-DQPSK
- **Polarization-multiplexed QPSK** (4 bits/symbol):
  - Dual-Polarization QPSK



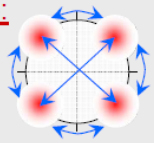


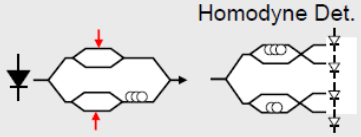
Mach-Zehnder Modulator

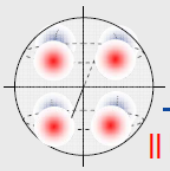




Delayed Self-Homodyne Det.







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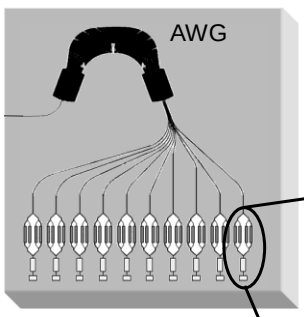
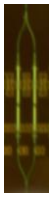
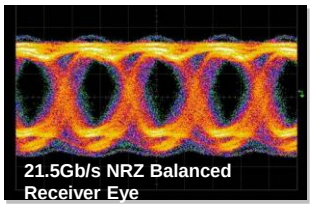
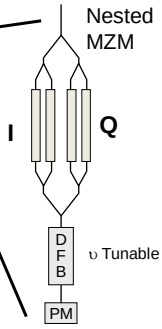
Large-scale DWDM DQPSK transmitter PIC 10 channels x 40 Gb/s

UCSB

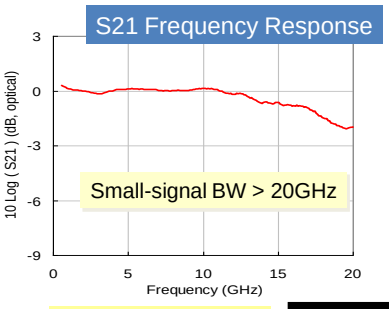








- 10 frequency-tunable DFB lasers with backside power monitors
- 10(I) + 10(Q) nested Mach-Zehnder modulator pairs
- 1 AWG
- 111 integrated elements in total on chip



S.W. Corzine, et al, *OFC'08*, PDP18, 2008

courtesy of C. Joyner

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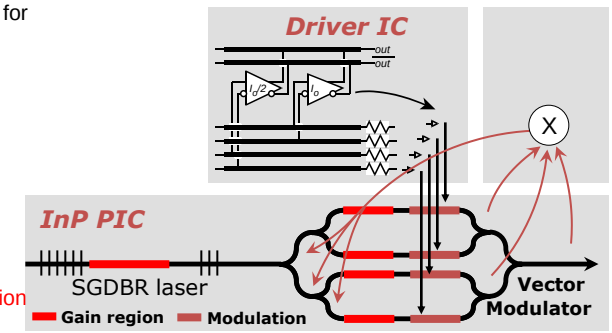
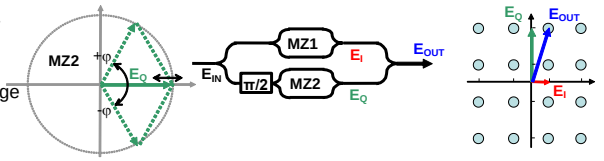
SGDBR + Multilevel Optical Modulation
(unpublished)

UCSB

- High order modulation required for high spectral density / channel rate
- Lower symbol rate – improved dispersion tolerance
- Semiconductor modulator
  - –Nonlinear response
  - –AM coupled with PM
  - –Compact, integrated with high-performance sources
- Challenge: Produce QAM modulation with required precision
  - –Improved response required, modulator nonlinearities results in ill-defined data levels.
  - –Use electronics to compensate for non-linear response → close integration electronics-photonics
  - –Capture potential of 1V drive voltage
- Integrated QAM transmitters
  - –Up to 64-QAM





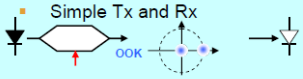
16 QAM

From Direct to Coherent Detection

UCSB

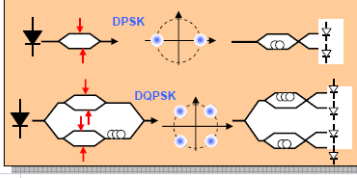
Direct Detection

- On-Off keying only
- Simple Tx and Rx



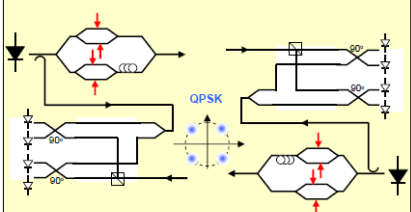
Self-Homodyne Detection

- Differential PSK encoding
- Decoding via 1-bit self-delay Mach-Zehnder interferometer
- Balanced Rx



Intradyne Coherent Detection

- Phase and polarization diversity
- Frequency-locked local oscillator
- Digital signal processing of received electrical signals
  - Electronic CD compensation
  - Electronic polarization demultiplex
  - Adaptive PMD compensation

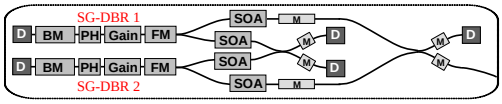


- **Use 'Intradyne' without phase-locked LOs, or do we need true Heterodyne detection?**
  - **High-speed A/Ds & DSPs require lots of power and are expensive to design if optical phase must be tracked, especially as data rate increases**
  - **Impairments can be removed with much slower, lower-power, lower-cost signal-processing circuits**

Optical Phase Locked Loops: Locking Two SGDBRs

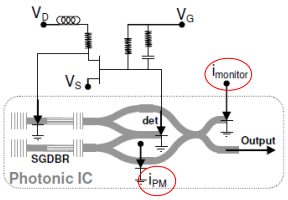
UCSB

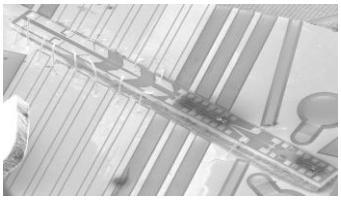
Optical phase-locked loops (OPLLs) are viable using close integration of PICs with electronics

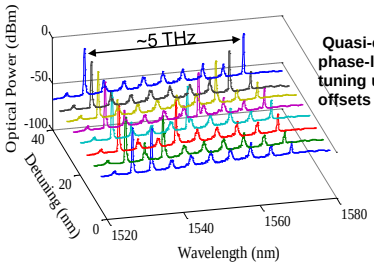


D Photodetector

M Modulator

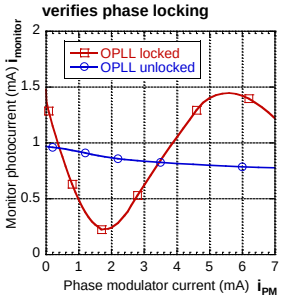






Quasi-continuous phase-locked digital tuning up to 5 THz offsets possible

Coherent interference at monitor verifies phase locking

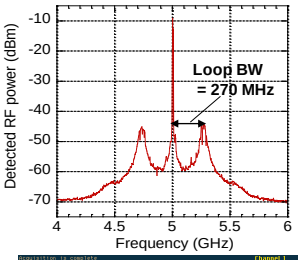


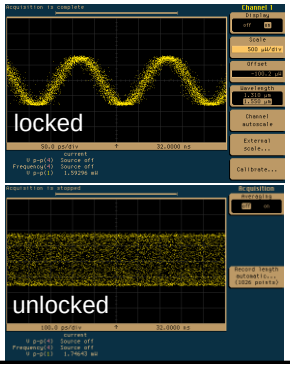
S. Ristic, et al, *OFC '09*, PDPB3, San Diego, (Mar., 2009)

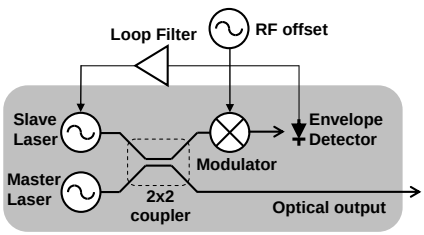
OPLL'd SGDBRs—Heterodyne

UCSB

- **EA modulator used to generate 5 GHz offset frequency**
- **Slave laser locked to modulation sideband**
- **Coherent beat observed**
  - 0.03 rad^2 phase error variance in +/-2GHz BW estimated from captured spectrum
- **Up to 20 GHz offset locking demonstrated**







Ristic et al: JLT v.28 no.4, 2010, in press, also at MWP2009, paper Th 1.5

Additional OPLL Applications/Challenges

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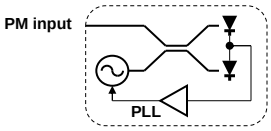
Coherent receiver



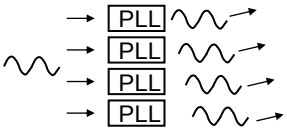
Costa's Loop for BPSK, QPSK demodulation

No requirement for complex DSP circuits

Challenge: Develop receivers for high speed (>100Gbaud) or high constellations (n-QAM)

Matched with development of coherent sources

LIDAR



Very rich/challenging area

Locking tunable lasers

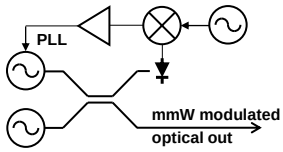
Arrays of locked OPLLs

Swept microwave reference

Time / Phase encoding of directed output

Need for rapid scanning and locking rates

mmW / THz generation



Locking of two tunable lasers

Requires Integration of high-speed UTC photodiode

Speed determined by UTC photodiode and feedback electronics: Can be very high

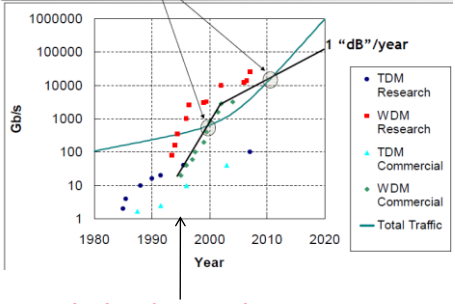
Combined with antenna designs for complete TRX links with free-space path

All require close integration of electronics with photonics

Can Spectral Efficiency Increase Enough?

UCSB

Two Special Years 2000 and 2011

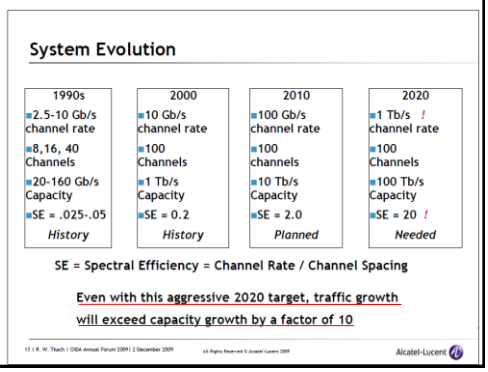


Introduction of EDFA and WDM
→ OEO repeaters vastly reduced

• Must improve Spectral Efficiency (SE)
→ Bits/Hz of bandwidth

• But vast improvements are required!

• Excess fiber capacity disappears after 2015



Fiber Capacity Estimate

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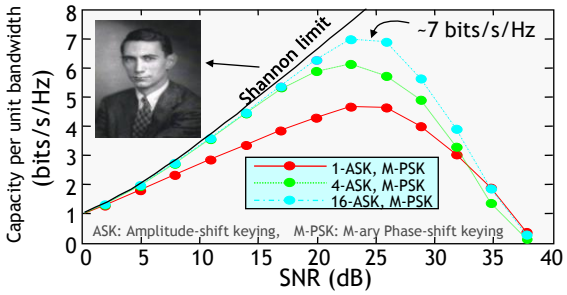
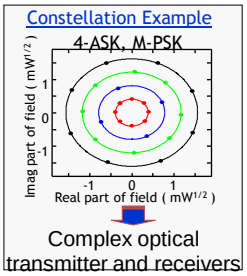
Capacity per unit bandwidth (spectral efficiency) for 2000-km transmission



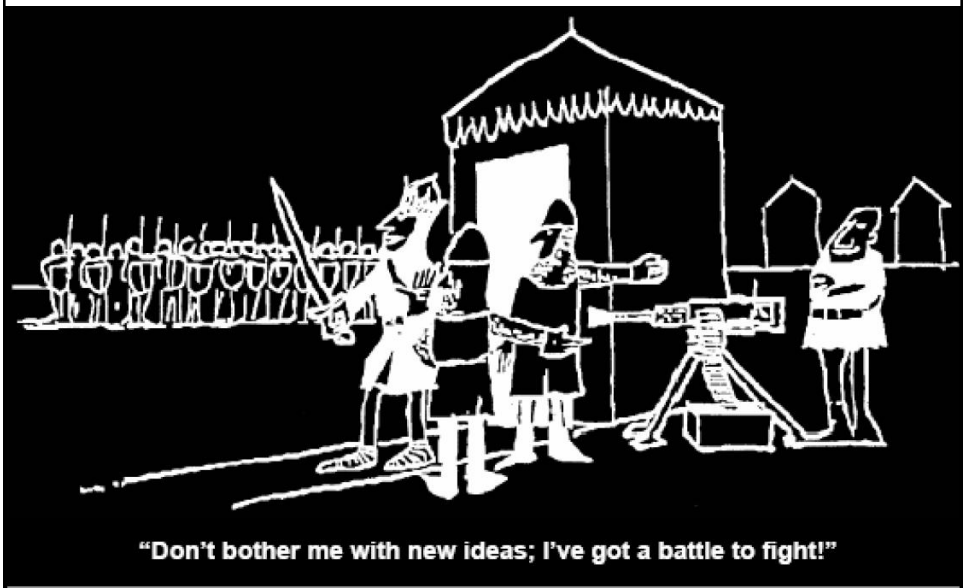


- For 2000 km, a spectral efficiency of ~7 bits/s/Hz per polarization can be achieved which corresponds to an increase of about one order of magnitude in spectral efficiency over commercial systems
- Deployed systems can transmit ~5 Tb/s over ~2000 km. For such a distance, the capacity limit of fiber is expected to be ~500 Tb/s or ~100 times the capacity of commercial systems

Courtesy: Rene Essiambre, Rod Alferness
Alcatel-Lucent

New Ideas are needed!

UCSB



Summary

UCSB

- Active InP-based photonic ICs can be created with size, weight, power and system performance metrics superior to discrete solutions in many situations. However, cost can only be less if the market size is sufficient.
- Close integration of control/feedback electronics will be desirable in many future PIC applications
- Coherent approaches will be greatly enabled by the use of photonic Integration, and numerous sensor applications may be enabled in addition to higher-spectral-efficiency communications.

Asynchronous 2x2 Optical Packet Synchronization, Buffering, and Forwarding

John P. Mack, Kimchau N. Nguyen, John M. Garcia, Emily F. Burmeister, Matt M. Dummer, Henrik N. Poulsen, Biljana Stamenic, Geza Kurczveil, Kurtis Hollar, Larry A. Coldren, John E. Bowers, and Daniel J. Blumenthal

Electrical and Computer Engineering Department, University of California, Santa Barbara

jmack@ece.ucsb.edu

Abstract: We demonstrate the first asynchronous 2x2 optical packet switch capable of synchronizing, buffering, and forwarding 10 Gb/s packets generated from independent transmitters with better than 99% packet recovery measured using a burst mode receiver.

OCIS codes: (060.1810) Buffers, couplers, routers, switches, and multiplexers; (230.4480) Optical amplifiers

1. Introduction

Optical packet switching provides a means of communication that is flexible, scalable, and high capacity [1]. Asynchronous operation of routers is the key to scaling large networks where multiple independent nodes are used, each with their own packet and bit-level clock sources. This causes inherent timing uncertainties on the clock and packet-level due to the frequency drift between plesiochronous clocks [2]. These uncertainties create unique challenges to optical technologies and switch architectures. In order to utilize synchronous buffer architectures with asynchronous packets, incoming packets must be aligned to the packet timeslots of the switch through the use of synchronizers. Packets are then synchronously loaded and unloaded from buffers to resolve temporal collisions of packets destined for the same output port [3]. Synchronous buffering is a critical component of any router as synchronization guarantees minimal uncertainty of the location of packets within buffers and allows for efficient time division multiplexing of packets onto output ports. In addition to optical buffering, the switch also requires photonic technologies to forward packets to different output ports. Optical synchronization, buffering, and forwarding approaches have been demonstrated individually with low power penalties at 40 Gb/s [4-6]. Previously, asynchronous optical forwarding of labeled optical packets was demonstrated for high bit-rate variable length 40 Gb/s payloads based on lower bit-rate 10 Gb/s labels [7]. End-to-end asynchronous optical transmission, forwarding, and detection have been shown for Internet protocol (IP) packets adapted to a labeled optical packet format for 12.5 Gb/s payloads with 3.125 Gb/s labels [8]. Asynchronous transmission, buffering, forwarding, and detection of 160 Gb/s payloads based on all-optical label processing has also been demonstrated [9]. In all of the previous work, contention of optical packets was pre-engineered using a single transmitter. The results reported here are the first demonstrations of synchronizing, buffering, and forwarding asynchronous optical packets generated by multiple independent sources.

2. Architecture

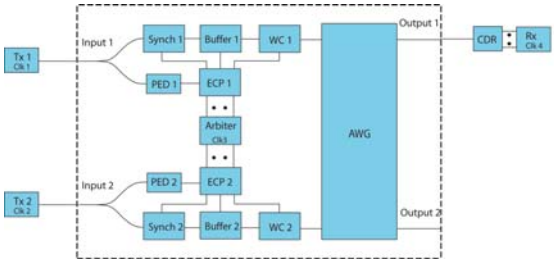


Fig. 1. Asynchronous 2x2 optical packet switch architecture.

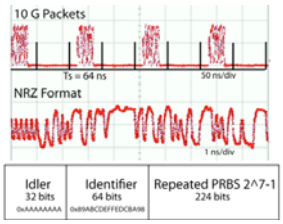


Fig. 2. Transmitted packet stream, NRZ format, and packet format.

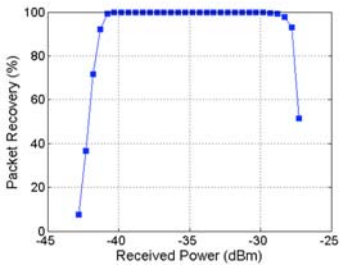


Fig. 3. Asynchronous back-to-back packet recovery measurement.

The asynchronous 2x2 optical packet switch architecture is depicted in Fig. 1. Multiple transmitters (Tx), an optically buffered switch, and a receiver (Rx) operate on independent clocks that are completely asynchronous to one another. The asynchronous FPGA based transmitters and burst mode receiver are capable of generating and detecting 10 Gb/s optical packets [10]. In the following experiments, a PC loads the transmitters with the same data

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stream, which is serialized to a 40 byte NRZ packet at 10 Gb/s with a total period of 128 ns as shown in Fig. 2. The 40-byte packets contain a 32-bit idler for clock recovery, 64-bit unique packet identifier, and repeated PRBS 2^7-1. The fixed timeslots used in the following experiments are 64 ns, which consist of a 40-byte packet and 32 ns of guard band. In this work, it is assumed packets are of fixed size due to the architecture of the implemented optical packet buffer. Packet recovery measurements were conducted for an asynchronous back-to-back experiment and are depicted in Fig. 3. Packet recovery > 99.99% was achieved for > 10 dB dynamic range of received powers. Achieving a large dynamic range for the receiver is critical when detecting incoming packets that have variations in amplitudes and signal to noise ratios.

Synchronization, buffering, and forwarding of 10 Gb/s asynchronous optical packets is performed using photonic integrated technologies. The synchronizers are a 4-stage feed forward design with binary delays based on discrete commercially available SOAs, as shown in Fig. 4 [4]. The synchronizer's resolution is 6.4 ns and the tuning range is 64 ns, as only 10 of the 16 delays are used in the following experiments. The buffers consist of packaged 2x2 InP SOA based switches and fiber delay lines equivalent to 64 ns, as shown in Fig. 5 [5]. The monolithically integrated field modulated wavelength converters consist of a high bandwidth photo detector and electro-absorption modulator (PD-EAM) and a highly tunable sampled grating distributed Bragg reflector (SG-DBR) laser, as shown in Fig. 6 [6]. Payload envelope detectors (PED), electronic channel processors (ECP), and a central arbiter are used for all synchronization, buffering, and forwarding decisions.

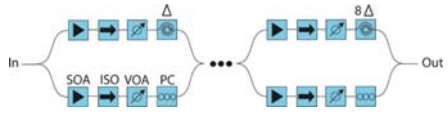

Fig. 4. Feed forward 4-stage optical packet synchronizer.

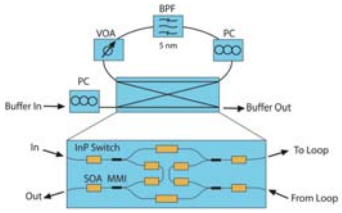

Fig. 5. Re-circulating optical packet buffer with inset of 2x2 InP switch.

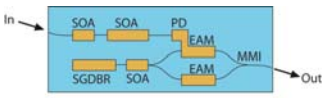

Fig. 6. Monolithically integrated field modulated wavelength converter.

3. Electronic Lookup and Arbitration

Asynchronous optical packets enter the switch fabric and the packet envelopes are extracted using the PEDs, which provide a precise time reference of the rising and falling edges of the packets. The envelopes are clocked into the electronic lookup time domain using D flip-flops in the ECPs running at 156.25 MHz. The ECPs then forward the envelopes to the arbiter for synchronization, contention, and forwarding lookup. The rising edge of the envelope is found and compared to the current count of the timeslot counter. Based on the count, the number of clock cycles needed to delay the rising edge of the packet to the next timeslot is determined. The arbiter generates SOA gating signals to select the delay of the optical synchronizer in order to align incoming optical packets to the local timeslots. The envelopes are then synchronized to the beginning count of the next timeslot and expanded to 64 ns. Next, the arbiter compares the synchronized expanded envelopes from the input ports to determine if contention is present. For this experiment, it is assumed that all packets request the same output port. The arbiter uses a round robin approach to determine which packet from the incoming ports should be buffered. Here, it is assumed that the buffers will only have to either pass a packet through or circulate a packet for one timeslot. The arbiter generates SOA gating signals to latch packets in and out of the buffers. Screenshots were taken for the outputs of the synchronizers and buffers operating asynchronously triggered by the respective transmitter and are shown in Fig. 7 and 8. The packets appear blurred because the delays needed to synchronize and buffer change over time since the transmitters and electronic lookup are asynchronous to one another. The synchronized and buffered packets are then fed into the input of the wavelength converter so that they are forwarded through the AWG. The WCs convert packets to a new wavelength using a highly tunable SG-DBR laser and an EAM that is modulated by the incoming signal. The wavelengths are mapped to the AWG to forward packets to different output ports.

4. Performance Measurements

Packet recovery measurements were conducted for various aspects and configurations of the optical switch, which were compared to the back-to-back measurements. The results of this section can be summarized using a single plot that shows power penalty versus packet recovery at 80, 90, and 99%, as depicted in Fig. 9. This includes asynchronous optical packet synchronization (S), asynchronous synchronization and buffering (SB), and asynchronous time division multiplexing (TDM) with greater than 99.99% packet recovery and minimal power penalties. Asynchronous synchronization, buffering, and forwarding (SBWC) was also demonstrated by placing a wavelength converter on each port and converting synchronized and buffered packets from 1560.5 nm to 1554.5 and

1559.5 nm with greater than 99.8% packet recovery and power penalties less than 5 dB. This also included asynchronous synchronization, buffering, TDM, and forwarding (TDM/WC) where the output of the buffers were coupled and injected into a single wavelength converter under DC biasing converting multiplexed packets from 1560.5 nm to 1554.5 nm and 1559.5 nm with greater than 99.8% packet recovery and power penalties less than 6 dB. Finally this included the asynchronous switch ports that were both TDM and WDM (TDM/WDM) where multiple synchronizers, buffers, and wavelength converters, and an AWG were implemented. Here Tx 1 and Tx 2 were tuned to 1560.5 and 1557.5 nm respectively to utilize multiple input wavelengths. Dynamically synchronized and buffered packets were forwarded to output 1 by tuning WC 1 and WC 2 to 1543.3 nm and 1553.5 nm respectively, as well as, forwarded to output 2 by tuning WC 1 and WC 2 to 1553.7 nm and 1562.9 nm respectively. Packet recovery rates greater than 99% were achieved for both outputs. The power penalties increase in both magnitude and variation as the number of cascaded devices and states increases due to variations in accumulated noise, saturation, insertion losses, and extinction ratios.

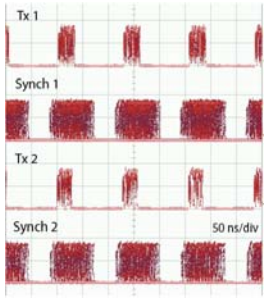

Fig. 7. Screenshots of transmitted and synchronized packets.

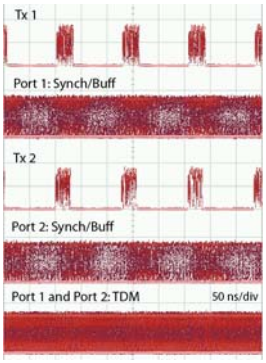

Fig. 8. Screenshots of transmitted, synchronized/buffered, and TDM packets.

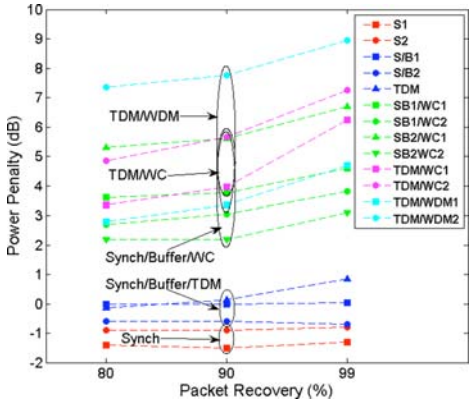

Fig. 9. Power penalty vs. packet recovery for various aspects of the asynchronous optical packet switch.

5. Conclusions

In this work, greater than 99% packet recovery was achieved for a 2x2 asynchronous 10 Gb/s optical packet switch that implemented multiple optical packet synchronizers, buffers, and wavelength converters. The demonstrated optical switch can reach 40 Gb/s with no change to the photonic devices, firmware, or power consumption. The optical switch can scale to 8x8 ports with additional photonic devices, electronics, and firmware updates.

6. Acknowledgement

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INTEGRATION TECHNOLOGIES FOR AN 8X8 INP-BASED MONOLITHIC TUNABLE OPTICAL ROUTER WITH 40GB/S LINE RATE PER PORT

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Abstract

Large-scale photonic integration depends on robust epitaxial design and fabrication techniques. This paper reviews the integration strategy we developed to demonstrate an 8x8 InP-based monolithic tunable optical router capable of 40 Gbps operation per port.

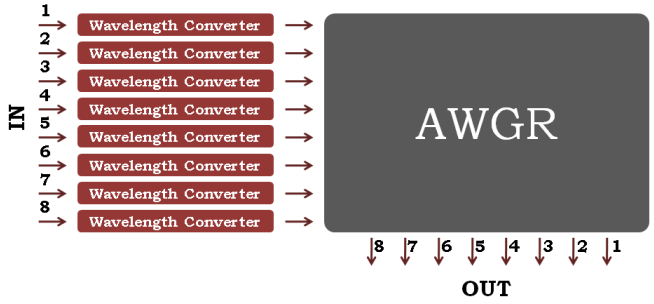
I. Introduction

Large-scale photonic integrated circuits (LS-PICs) in InP are a critical technology to manage the increasing bandwidth demands of next-generation optical networks. By integrating many of the network functions typically handled by discrete optical components into a single device, the overall system footprint can be appreciably reduced. Additionally, a compact, single-chip solution can provide performance and reliability gains along with a reduction in packaging costs. Although the promises of large-scale integration have long been known, LS-PICs have only recently emerged in the marketplace, thanks to advances in InP epitaxial growth and fabrication which have led to improved yield [1,2].

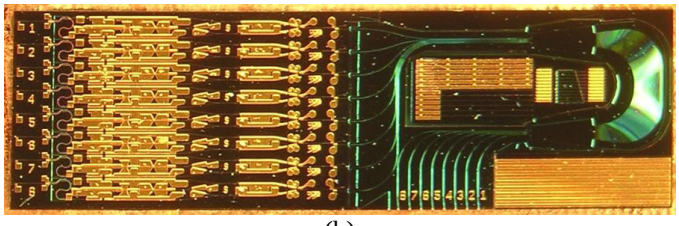
For most optical network applications, multi-channel LS-PICs that incorporate both active and passive device components on the same chip are desirable. Active/passive integration depends heavily on the epitaxial and fabrication schemes used. To this end, a number of different platform technologies have been proposed and developed in the last two decades [3-5]. Because the choice of an integration platform typically depends on the device requirements, there is not a one-size fits all integration solution. However, in general an integration strategy should be designed to limit the degree of fabrication complexity and the number epitaxial regrowth steps to provide high yield and lower cost.

All-optical packet switching at 40 Gbps is one application of interest for LS-PICs. In this approach routing of data packets is confined solely to the optical domain, potentially easing the increasing power consumption demands of electronic-based routers at high data rates. As part of the DARPA DOD-N and Army sponsored LASOR project [6], many important single-channel PIC building blocks such as wavelength converters, optical buffers and mode-locked lasers have been demonstrated [7]. Recently, however, we have advanced our integration technologies to demonstrate multi-channel PICs with even greater component densities and chip functionality.

This paper will review the integration strategy we used to demonstrate an 8x8 monolithic tunable optical router (MOTOR) chip that serves as the packet-forwarding engine of an all-optical packet-switched router (Fig 1). The 8-channel device consists of an array of 8 tunable wavelength converters and an array-waveguide grating router (AWGR). It combines more than 200 building blocks into one chip and has a potential total data capacity of 640 Gbps. Single-channel operation of the device at 10 Gbps [8] and 40 Gbps [9,10] line rates has been achieved with reasonable power penalties. Our integration approach is based on quantum-well intermixing (QWI) and leverages risk by using only a single blanket epitaxial regrowth. To provide additional component functionality, advanced InP fabrication techniques are used to define three separate waveguide architectures that provide differing levels of optical confinement.



(a)



(b)

Fig. 1. a) Schematic of MOTOR chip architecture; (b) Photograph of fabricated 8-channel device

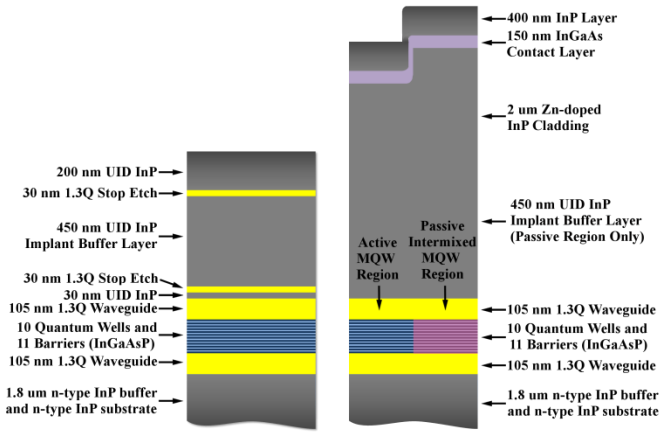
II. Device Design

Our integration strategy for the MOTOR chip was largely based on the design requirements of the WCs and AWGR. Wavelength conversion is accomplished through the use nonlinear semiconductor optical amplifiers (SOA) within a Mach-Zehnder interferometer (MZI) as in [11]. Input data pulses to these SOAs can cause a phase shift in the MZI that modulates a input CW signal, provided that the SOAs are sufficiently saturated. These SOAs necessarily require a high degree of optical confinement. In contrast to these saturated SOAs, the device also needs linear SOAs to amplify the input data signal before the MZI. Therefore, our integration approach must allow for the realization of both linear and nonlinear SOAs. To overcome the inherent limitations of slow carrier recovery time between input data pulses in the MZI SOA, each WC must also employ an integrated delay line to time-delay input pulses to one branch of the MZI relative to the other. Lastly, the device requires integration of low-loss passive waveguides, splitters and phase tuners.

The AWGR at the outputs of the WCs should have a small footprint (which constrains the channel spacing), low insertion loss and low propagation loss. The loss is mainly governed by proper design of the input and output star coupler region and the waveguide fabrication. Most notably, the etch process used should provide smooth sidewalls in order to minimize scatter loss and good uniformity across the AWGR section to minimize index variations.

III. Integration Strategy

To achieve the functionality required for the MOTOR chip, we developed a four-point integration strategy. First, an epitaxial base structure in which the MQW active region is sandwiched in the center of the passive waveguide layers is used in order to maximize optical confinement. This ensures that we can obtain the nonlinear MZI SOAs that are essential to wavelength conversion. Second, QWI is employed to blue-shift the active band edge from an as-grown PL wavelength of 1545 nm to a passive band edge of 1420 nm. This allows us to achieve low propagation loss and efficient phase tuners (due to the presence of detuned MQWs in the passive sections). Third, a single blanket p-type InP regrowth is used to clad the waveguide. Blanket regrowths have the advantage of simplicity and higher yield. However, using only one p-doped regrowth step can lead to increased propagation losses in passive regions. The technique we developed to address this issue is discussed in the next section. Finally, our device utilizes three different waveguide architectures so that components with differing optical confinement (and hence optical properties) can be realized. The specifics associated with these waveguide designs are also discussed below.



(a) (b)

Fig. 2. a) Base epitaxial structure; (b) Epitaxial structure after regrowth (the undoped buffer layer found in some passive regions of the device is also shown)

A. Passive Propagation Loss Reduction with Single Regrowth

It is well known that the interaction of an optical mode with Zn-doped InP can lead to significant loss via free-carrier absorption. In fact, this loss has been shown to be on the order of 20 cm^{-1} for every 1E18 cm^{-3} doping at a wavelength of 1.5 μm [12]. Doping of this level is required in active sections of our device to make efficient diodes. Since we limit our process to only one regrowth step, this means we would have equivalent doping in our passive sections. This problem could be addressed through an additional undoped regrowth in passive regions, but that is not ideal in terms of cost and yield.

Our base growth (Fig. 2a) contains an undoped InP buffer layer above the MQW region. Historically, this layer has been used exclusively for QWI, after which it is selectively removed via wet etching [3]. However, there is no reason that this layer must be removed after QWI, so we now deliberately leave the buffer layer in certain passive regions of the chip (Fig. 2b) [13]. This has the effect of "inserting" a unintentionally doped (UID) setback layer between the optical mode and the Zn dopant atoms in the p-type cladding, thus reducing optical scattering losses. The key advantage with this approach is that no additional regrowth is required. Simulations have shown that the net loss with this approach can be decreased by as much as much as ~2.4X, depending on the waveguide structure.

B. Waveguide Designs and Implementation

The MOTOR chip can be divided into three sections with differing ideal optical requirements. To improve the performance of components in these regions, multiple waveguide architectures are defined across the device. First, the bulk of the WC array is defined with a surface ridge waveguide (Fig. 3a,c). This design is used primarily due to its fabrication simplicity and because it provides efficient pumping in gain regions. The waveguide is fabricated by both dry and wet chemical etching. A 400-nm PECVD SiO_2 hard mask is defined above the InP cladding by lithography and then CHF_3-based inductively-coupled plasma (ICP) dry etching. The InP ridge is etched to a depth of 1.8 μm using a Cl_2:H_2:Ar-based chemistry in an ICP system. By optimizing the gas flows and power levels, straight and smooth sidewalls can be obtained [14]. The remaining 0.6 μm InP cladding

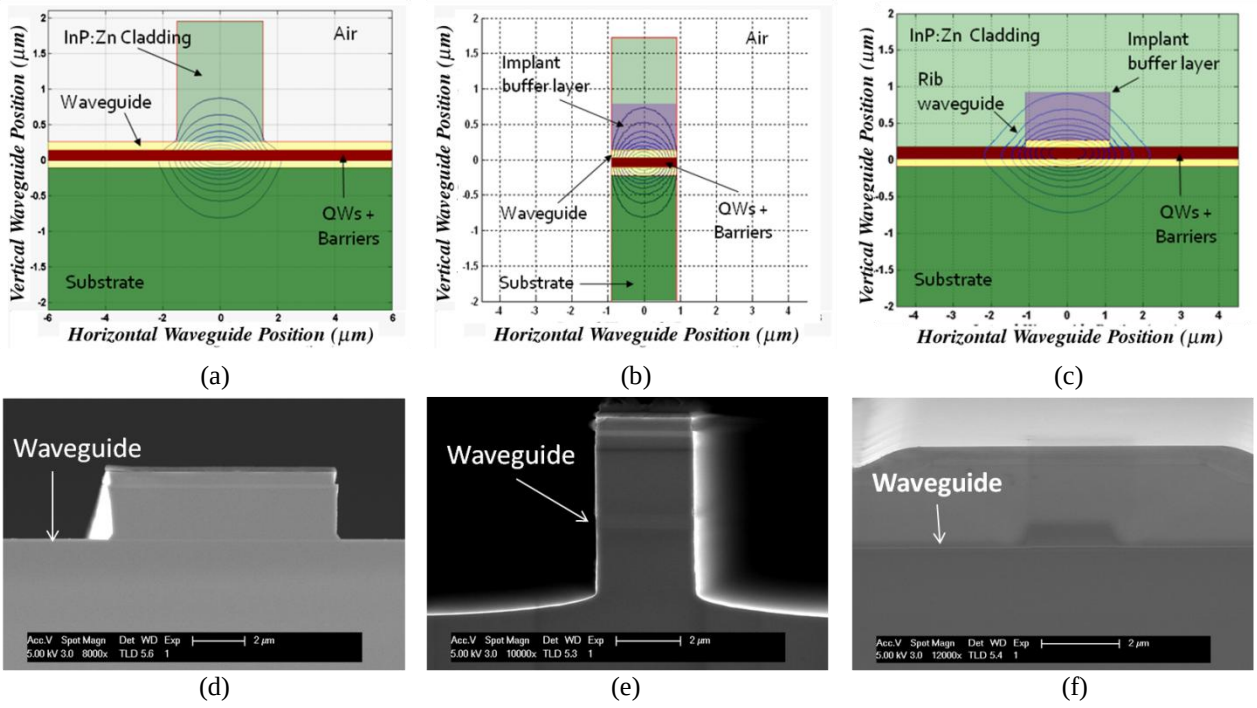


Fig 3. Waveguide architectures used in MOTOR: (a), (b), (c) show schematic cross-sections with the optical mode profile superimposed for surface ridge, deep ridge, and buried rib, respectively. (d), (e), (f) show SEM cross sections for surface ridge, deep ridge, and buried rib, respectively

of the ridge is then removed by selective wet etching in a 3:1 H_3PO_4:HCl mixture. The quaternary waveguide layer above the MQW acts as a stop-etch layer. Because the etch does not go through the MQW region, we avoid surface recombination issues. However, the wet etch is crystallographic and the structure has relatively low lateral confinement, so tight bends and high-angle structures are problematic.

Second, to achieve the differential delay in the MZI that is required for 40 Gbps operation, a compact, 11-ps delay line is needed on chip. In order to minimize the footprint of this component, a deeply-etched waveguide structure is utilized (Fig 3b,e). The delay is fabricated using two dry etch steps. The first 1.8-μm etch is performed simultaneously with the dry-etch step of the surface ridge waveguide. Precise alignment between the surface ridge and deeply-etched regions is maintained because they share the same hard mask. The delay line region is protected with photoresist during the wet etch of the surface ridge. Next, a 350 nm PECVD SiO_2 hard mask is lifted off to open the vias in the delay line region. A 2-3 μm dry etch that goes through the waveguide/MQW layers (using identical etch conditions as the first dry etch) is then performed. Since the deeply-etched waveguides are only used in passive sections, surface recombination is not relevant. However, because the optical mode can laterally interact with etched sidewalls, it is extremely important that waveguide sidewalls are not rough.

Lastly, a shallow rib waveguide with a 70-nm depth is defined in the upper waveguide layer above the MQW in the AWGR *prior* to the cladding regrowth, which subsequently buries it (Fig. 3c,f). Because a selective wet etch is avoided, this rib waveguide can be turned a full 180° to achieve a compact footprint. The insertion loss at the star couplers with this architecture is also low in comparison with that of a deeply-etched design.

IV. Results

The spectral response of AWGR to amplified spontaneous emission (ASE) generated by forward biasing the MZI SOAs was measured in an optical spectrum analyzer. Fig. 4 shows the ASE spectrum from each output port using the SOAs in input channel #3. The AWGR is well behaved with a free spectral range of 11.1 nm. Next, the wavelength-based switching capacity of the device was examined by biasing the SG-DBR of input port #3. Fig. 4 shows that with proper mirror biasing, the laser can be tuned to any of the allowed output ports. Output powers of more than -5 dBm were measured, which is reasonable given the long propagation length of the AWGR region and fiber coupling losses.

40 Gbps wavelength conversion and channel switching were then investigated by sending a modulated input data source into the chip and measuring the bit-error rate (BER) of the converted and routed data [10]. Fig. 5 shows that power penalties as low as 4.5 dB were achieved at a BER of < 1E-9 for multiple input/output port combinations.

V. Conclusion

Using an integration strategy that emphasized simplicity for the sake of yield, we have demonstrated one of the most complex LS-PICs to date. Our strategy leverages epitaxial

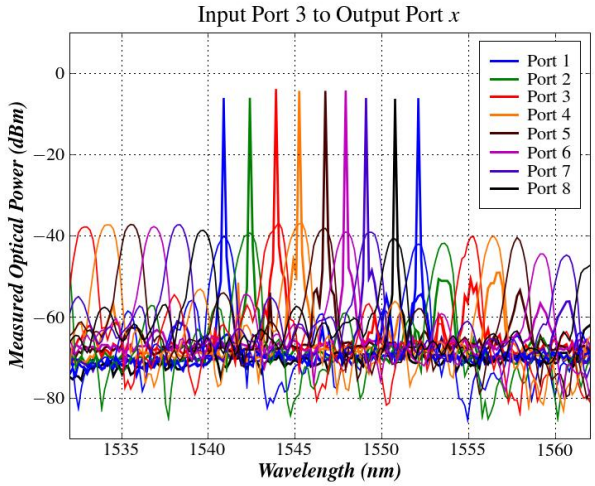


Fig. 4. Demonstration of wavelength switching capability by tuning the SG-DBR of input channel #3 to the allowed wavelength of all output port (superimposed on ASE spectra from all output ports)

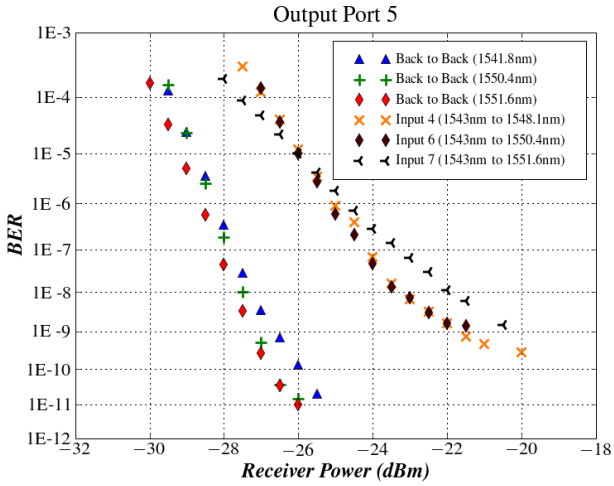


Fig. 5. BERs at 40 Gbps measured from a constant output port using multiple input ports

techniques such as QWI and simple blanket regrowths with waveguide fabrication techniques. Notably, our device employed only one p-type InP regrowth step. Because the doping profile of the cladding region was designed for active components, steps must be taken to reduce optical loss in passive regions. We selectively leave a previously sacrificial InP implant buffer layer (used for QWI) above the waveguide in passive regions to separate the optical mode from the p-type dopant in the cladding without additional regrowth steps. We have also demonstrated multiple waveguide architectures on a single-chip in order to optimize components with different optical properties. The execution of this integration strategy has led to successful demonstration of single-channel wavelength conversion and routing of data at 40 Gbps.

Acknowledgements

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Large-Scale Photonic Integration for Advanced All-Optical Routing Functions

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Abstract: We review the first InP monolithic tunable optical router chip, consisting of eight wavelength converters and an 8x8 AWGR. The device integrates more than 200 functional elements and operates at 40 Gbps per port.

OCIS codes: (250.5300) Photonic integrated circuits; (060.1155) All-optical networks

1. Introduction

Large-scale photonic integrated circuits (LS-PICs) could have a transformative influence on future-generation optical networks [1]. In general, photonic integration promises improved performance and reliability over discrete component systems because it can lead to a reduction in device footprint and the elimination of many component-to-component fiber links. Recent advances in InP-based epitaxial growth and fabrication technologies have improved component yield, such that densely-integrated multi-channel devices can now be demonstrated in single-chip form. LS-PICs can process data completely in the optical domain, thus eliminating the need for successive optical-to-electrical and electrical-to-optical conversions, common in today's electronic routers. This translates into potential energy savings through reduced power consumption.

As part of the DARPA/MTO and Army DOD-N LASOR program [ref], we have previously demonstrated several important single-channel PIC devices [2]. Recently, we have extended our integration technologies to realize the first 8-channel monolithic tunable optical router (MOTOR) chip operating at 40 Gbps per port. This multi-channel LS-PIC integrates an array of 8 tunable wavelength converters (WC) with a passive 8x8 arrayed-waveguide grating router (AWGR) and functions as a wavelength-based switching element. The MOTOR chip has a very high level of integration with more than 200 functional elements on chip.

2. Device Design and Integration Strategy

The fabricated MOTOR chip is shown in Fig. 1a. Each input port (see Fig. 1b) consists of a wavelength converter (WC) that incorporates a widely-tunable sampled-grating DBR (SG-DBR) laser. The CW-output from the laser is

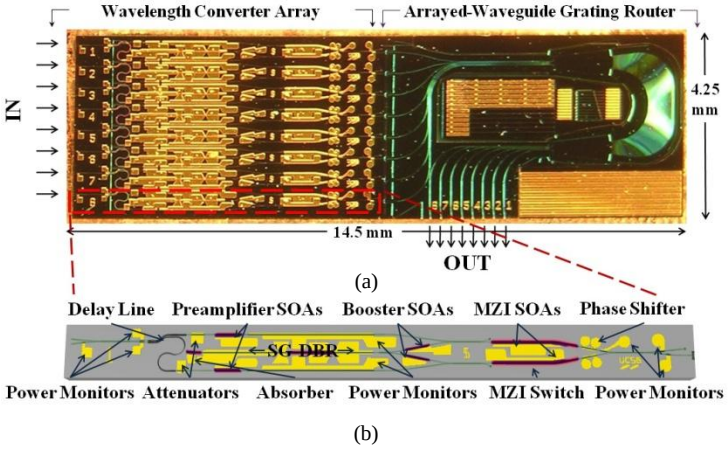


Figure 1. (a) Microscope image of fabricated MOTOR chip; (b) close-up schematic of the wavelength converter design.

modulated by an input data signal using cross-phase and cross-gain modulation effects in nonlinear semiconductor optical amplifiers (SOAs) within a Mach-Zehnder interferometer (MZI) [3]. In order to overcome the limits of carrier-recovery in these SOAs and achieve 40 Gbps operation, the input data signal in each port is split 50/50 and input into different branches of the MZI with a relative time delay. This delay is accomplished on chip through a compact, low-loss delay line. (The device can also operate at 10 Gbps line rates by bypassing the delay line and injecting the input data signal into only one branch of the MZI.) Additionally, the device incorporates two linear preamplifier SOAs before the MZI to amplify the input data signal. The original and converted data are both passed to one input of an 8x8 AWGR, which passively routes the converted signal to a desired output port based upon its new wavelength. The input and output frequency combs of the device are placed in different wavelength ranges so that a high- or low-pass filter can be placed at the output to remove the original input data signal.

To realize all of these components simultaneously, we developed an integration strategy that uses quantum-well intermixing and a single p-type cladding regrowth. The chip also has 3 waveguide architectures in different regions of the chip to optimize the optical properties of the various components. These include a surface ridge waveguide in the wavelength converter section, a high-contrast deeply etched waveguide in the delay line for compactness, and a buried rib waveguide in the AWGR region. More detail regarding this integration strategy is provided elsewhere [4]. The fabricated chip was then soldered to a copper mount and held at 16°C during operation.

3. AWGR Characterization

The performance of the AWGR was characterized using on-chip amplified spontaneous emission (ASE) generated by forward biasing the MZI SOAs of an input port and fiber coupling the output of all ports (one-by-one) to an optical spectrum analyzer (OSA) (Fig. 2a). A free spectral range (FSR) of approximately 11.1 nm and a single-channel crosstalk between -15.8 to -20.9 dB across all output ports were measured. Next, the MZI SOAs of each WC were biased and the resulting spectrum was measured from a single output port (Fig. 2b). With this measurement we see some variation in crosstalk performance between WCs, likely due to fabrication variations across the device. Lastly, Fig. 2c shows that the by changing the biasing conditions on the mirror diodes of the SG-DBR, the laser can be tuned to any of the allowed output wavelengths of a given port. A simple tuning map can made in order to achieve full channel switching from any input port to any output port.

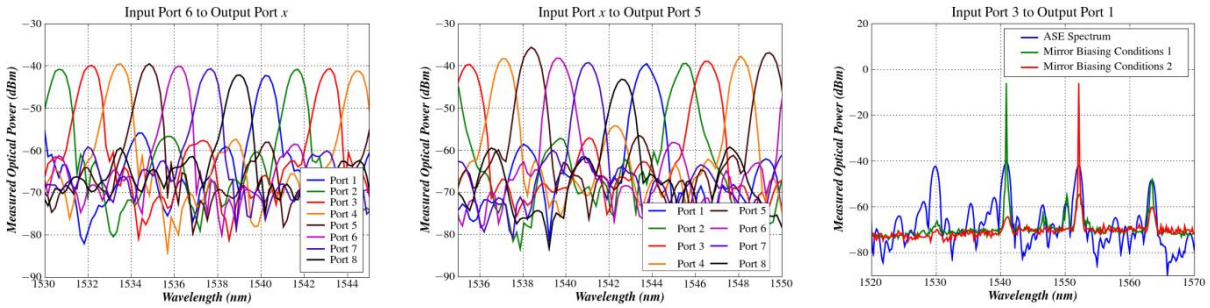


Figure 2: Output response of the AWGR: (a) measured response from input WC port #3 from each output port; (b) measured optical output from output port #5 from each input WC port; and (c) lasing spectra at different mirror biasing conditions with the SG-DBR of input WC port #3. The ASE spectrum for that channel is superimposed.

4. Wavelength Conversion and Routing Demonstration

Single-channel wavelength conversion and routing were tested under various conditions. In each case, a PRBS data was generated off-chip and amplified with an erbium doped fiber amplifier (EDFA). It was then transmitted through an optical attenuator to control the input power level, a 5-nm filter, and a polarizer to align the polarization state to TE before the signal was coupled into the chip. The fiber-coupled output was also filtered with a 5-nm passband (to ensure the original input signal was removed) and was transmitted to a preamplified receiver. Bit-error-rates (BER) were then determined using a SHF BERT.

First, 10 Gbps operation of the device was examined by inputting a PRBS 2^{31}-1 NRZ signal into only one branch of the MZI (Fig. 3) [5]. At a BER of 10^{-9} a power penalty as low as 1.3 dB was measured. Eye diagrams of the converted signal show open eyes with extinctions up to 8.79 dB. There is some distortion in the eye that can most likely be attributed to saturation in the input preamplifier SOA.

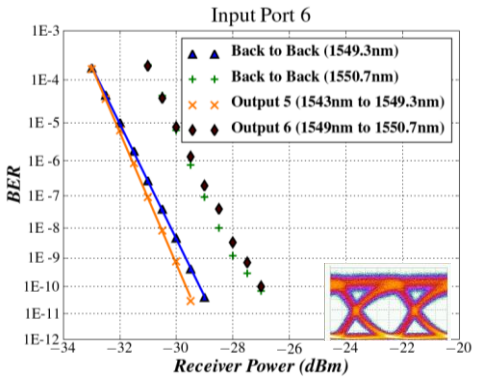
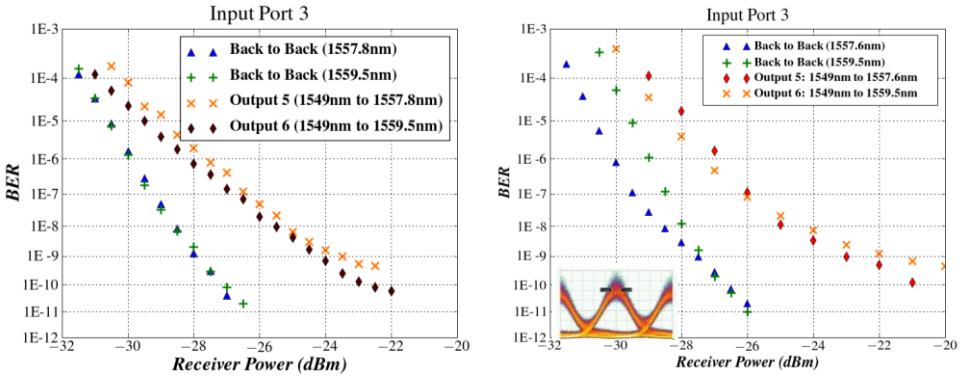


Figure 3. 10 Gbps BER measurements from multiple output ports using input WC #6.

Next, the device was tested using the differential delay approach with 40 Gbps PRBS 2^7-1 RZ data [6]. Fig. 4a shows the BER for a single input channel while monitoring a constant output port. In this configuration, power penalties as low as 3.5 dB at a BER of 10^{-9} were measured. When the pattern length was increased to 2^{31}-1 bits, there was a noticeable increase in power penalty (to 4.5 to 7 dB depending on the input/output port combination). We also saw the emergence of a noise floor at low BERs. Subsequent investigation revealed that in order to achieve sufficient input signal power to deplete the carriers in the MZI SOAs and modulate the SG-DBR signal, the preamplifier SOAs had to be operated beyond the 1-dB output saturation point. This is likely the main factor leading to the pattern length dependent power penalty. Additionally, however, it is noted that the facets of the device were not AR coated, so internal reflections could be contributing to the degradation in performance.



(a) (b)

Figure 4. 40 Gbps BER measurements for input port #3 with (a) 2^7-1 PRBS and (b) 2^{31}-1 PRBS input data signals.

5. Acknowledgements

This work was supported by the DARPA MTO and the Army under the DOD-N LASOR Project (W911NF-04-9-0001). Fabrication was done in the UCSB nanofab, part of the NSF funded NNIN network.

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I. Photonic Integrated Circuits

B. RF-Photonics

Linear Coherent Optical Receivers

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Abstract: The development of linear coherent receivers at UCSB is reviewed. The progression of the feedback receiver architecture toward closer integration, lower feedback delay and higher performance is outlined. The alternative XOR receiver approach is summarized.

OCIS codes: (250.3140) Integrated optoelectronic circuits, (060.1660) , Coherent communications (060.5060), Phase modulation, (060.2360) Fiber optics links and subsystems.

1. Introduction

Fiber optic links are attractive for remoting exposed antenna systems. In contrast to coaxial cables, they are EMI immune, lightweight and have low losses at high RF modulation frequencies. Further, if a robust optical modulator is used, the optical link can function as a buffer at the antenna unit, protecting sensitive receiver front-end electronics from large RF power surges. The traditional challenge for RF photonic links has been component limitations resulting in optical links with high noise figure and low dynamic range.

Traditionally optical intensity modulation (IM) has been considered for RF photonic links. An early result, 1994, demonstrated an optical link with 132 dB SFDR in 1 Hz bandwidth, using a carefully optimized optical modulator [1]. This result is still representative to the performance of state-of-art IM RF photonic links today, more than 15 years later. The cause of the slow advance of analog link performance is related to the modulation format. Optical intensity modulators are limited to operation between zero and full transmission. To avoid clipping, the linear RMS modulation depth is typically limited to <10% of full modulator swing. To reach higher dynamic range, the optical power must therefore be increased, but that also increases shot noise, leading only to a weak improvement in SFDR at the expense of a strong increase in detector power.

More recently, optical phase modulation has been considered for linear optical links [2,3]. Linear optical phase modulators are available, notably $LiNbO_3$ modulators which rely on the linear electro-optic effect. Further, optical phase modulators do not have any hard-limits to available modulation depth, high modulation depth can be reached through increased spectral envelope in the optical domain from modulation sidebands, as determined by the Bessel functions. Common interferometric approaches to convert optical phase modulation to intensity modulation typically have a non-linear sinusoidal response.

This paper reports on current efforts to develop coherent optical receivers for linear optical phase demodulated signals with a high modulation index. Two alternative approaches have been considered, first; a phase-feedback coherent receiver architecture, and second; optical heterodyne detection with linear RF phase detection.

2. Feedback Receiver Approach

The feedback receiver architecture is illustrated in Figure 1, left. The received optical signal is mixed with the optical LO similar to a conventional receiver. The detected differential photocurrent is then amplified and fed back into a tracking phase-modulator to form a feedback loop. For high feedback gain and using a linear tracking modulator, the drive signal to the tracking modulator is linearly related to the received optical phase. An alternative illustration of increased linearity is that with higher feedback gain and closer tracking, the received signal-LO phase difference gets smaller, allowing the interferometer to operate within its linear range. Figure 1, center illustrates this, where the predicted output from the balanced receiver compares well with measured data for increasing loop transmission gain, using a slow proof-of-concept bench-top demonstrator built from optical fiber and a $LiNbO_3$ tracking modulator [3]. Figure 1, right shows the corresponding SFDR. 124.3 $dBHz^{2/3}$ is measured for only 3mA of received photocurrent, corresponding to a respectable 131.5 $dBHz^{2/3}$ in the shot-noise limited extrapolation [3]. This initial demonstration illustrated the potential high performance of the approach is high-performance components are used.

One limitation of a fiber based, discrete-component demonstrator is that the latency in the feedback loop limits the unity-gain bandwidth. As an engineering rule, the bandwidth is limited to ~1/(10×loop delay). For this reason, the linearity data had to taken at around 150 kHz to ensure sufficiently high loop gain for linear operation.

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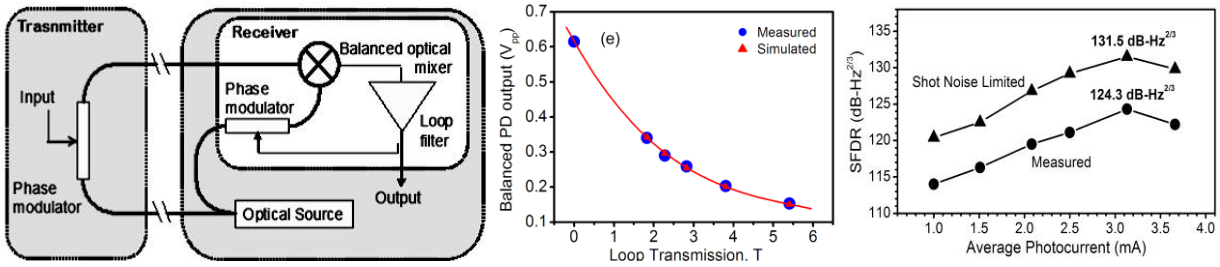

Figure 1. Left: Schematic of feedback coherent receiver approach. Center: Relation between loop transmission gain and suppression of detected differential phase. Right: Measured SFDR using discrete component proof-of-concept demonstrator.

Generation I integrated receiver: To reach higher operating frequencies, the loop latency must be reduced. Figure 2, left shows an SEM of the generation I integrated receiver IC, containing a high power balanced uni-traveling-carrier photodiode (UTC-PD), a 2x2 multimode interference (MMI) coupler, shown in Figure 2, center, and multi-quantum well tracking phase modulators [4]. This PIC is wirebonded to an electronic integrated circuit (EIC) that provides transconductance amplification of the feedback signal to drive the phase modulator to close the feed-back loop.

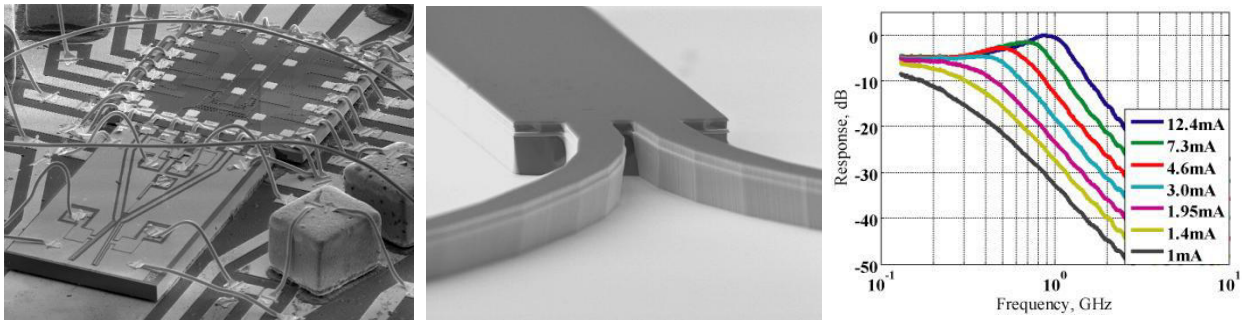

Figure 2. Left: SEM of Integrated O/E Receiver showing generation I photonic and electronic IC. Center: detail of generation I photonic IC, showing the 2x2 MMI coupler. Right: Resulting link gain at different detected photocurrent levels

The PM link response using the closed-loop receiver is shown in Figure 2, right. At high frequency, or at low photocurrents, the link gain is proportional to the photocurrent and the voltage drop over the capacitive detector load. For higher photocurrents and at lower frequencies, the loop gain is significant, and the link gain becomes proportional to the ratio of remote modulator V-pi and the V-pi of the tracking modulator. The corresponding link SFDR is as high as 125dBHz$^{2/3}$ at 300MHz frequency [5]. For this receiver, the estimated loop delay was estimated to be ~35ns, sufficient to support ~3 GHz loop bandwidth. The measured bandwidth was >1GHz.

Generation II integrated receiver: To reach further improved loop bandwidth and gain, the delay must reduced even further. This can be achieved by replacing the MMI coupler with its attributed curved input waveguides with a compact trench coupler, as shown by Figure 3, left. This coupler can be as compact as a few tens of microns in total, while allowing close integration with detectors and modulators, as shown by the fabricated device in Figure 3, center, showing input waveguides with tracking phase modulators, the 2x2 slot coupler, and a balanced UTC detector pair. Further reduction of the loop delay can be reached by a more compact integration of photonics and feed-back electronics by replacing wire-bonds and RF lines on the photonic IC by direct flip-chip bonding between photonics and electronics, as shown by Figure 3, right. It is expected that this will lead to a loop delay <10ps and lower insertion losses, with a corresponding improvement in receiver performance.

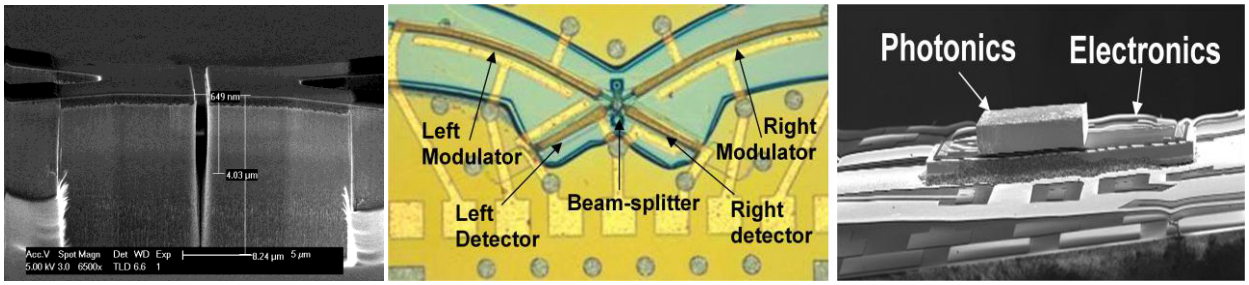

Figure 3. Left: Detail of compact optical trench coupler. Center: Generation II photonic IC incorporating detectors, coupler and modulators. Right: Generation II photonic IC flip-chip bonded on to feedback electronic IC.

3. Linear XOR Receiver

One limitation of the feedback receiver approach is that the bandwidth is delay restricted and given available integration technology, the high-gain low distortion operating frequency will remain a few GHz. To address operating frequencies up to 20 GHz, an alternative approach has been investigated based on a linear RF phase detector. Figure 4, right shows a schematic of the linear XOR optical receiver. Here, the received optical signal is downconverted to an RF signal, transferring the optical phase modulation to the RF domain. Now, a wider tool-box for linear RF phase detection can be utilized. In this approach, the RF signal is limited to form a square-wave. The phase information is now contained only in the timing of zero-crossings. The limited signal is compared to a clock-reference in an XOR-gate and the output is then low-pass filtered to remove the RF carrier. This receiver has a linear response over a $\pm\pi/2$ range. By inserting an N-times digital frequency divider before the clock, phase modulation becomes linear over a $\pm N\times\pi/2$ range. Figure 4, left shows two-tone experimental results at 0.5 GHz signal frequency and 4 GHz RF carrier, using the proposed phase demodulator [6]. It is observed that the XOR generated intermodulation products suppressed by 20 dB compared to a standard sinusoidal phase detector. Further, it is observed that implementing the frequency division, two-tone modulation depth exceeding π rad p-p phase swing is possible without resulting in clipping.

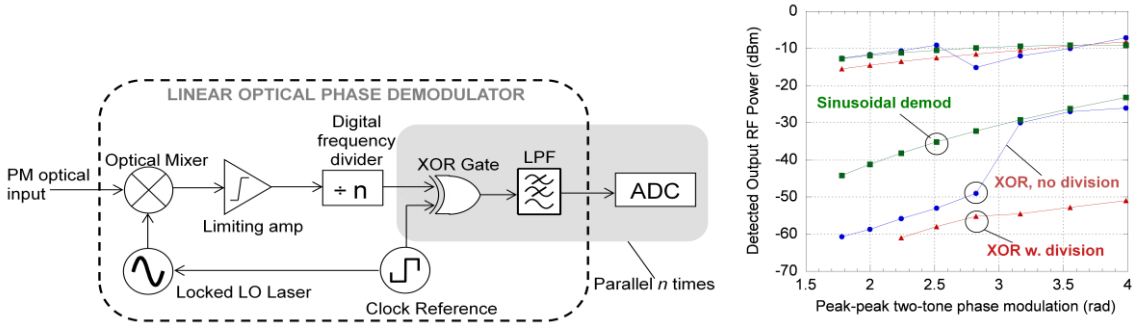

Figure 4. Left: Schematic of the linear XOR receiver architecture. Right: Resulting intermodulation performance with and without digital frequency division, and compared to conventional sinusoidal demodulation.

One advantage of the XOR receiver is that the output signal frequency is scaled down by the frequency division factor, N. With sufficient division, high performance, lower sampling rate ADCs can be used to digitize broad-band high-frequency received RF signals. The different Nyquist bands are separated by implementing a factor-of-N frequency divider with N outputs such that each zero transition is captured. Using the digitized data, the full broadband RF signal can then be fully reconstructed.

4. Conclusions

In this paper, the development of linear integrated coherent receivers at UCSB is reviewed. The first approach relies on a closed-loop feedback architecture to a closely integrated tracking modulator. The progression toward closer integration, lower feedback delay and higher performance has been outlined. The second approach relies on heterodyne detection, frequency division and linear RF phase detection. Results from a proof-of-concept demonstration are shown.

5. Acknowledgement

The authors acknowledge Northrop Grumman Space Technology for providing the EIC. This work was supported by the DARPA PHOR-FRONT program under USAF contract FA8750-05-C-0265.

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Highly Linear InP Phase Modulator for High Dynamic Range RF/Photonic Links

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***Abstract* — The optical phase locked loop (OPLL) photonic integrated circuit (PIC) is a key element for the emerging linear coherent RF-photonic links. One of the main challenges for the OPLL-PIC is the nonlinearity of the Indium Phosphide (InP)-based phase modulator. In this paper, we report the experimental results from a multi-quantum well phase modulator fabricated on an InP substrate that is specially designed for the OPLL-PIC. The phase modulator shows low optical loss and good linearity performance. In particular, at a reverse bias voltage of 5.6 V, its phase IP3 and insertion loss per unit length are ~2.8π/mm and 1.2 dB/mm, respectively.**

***Index Terms* —optical phase locked loop, dynamic range, quantum wells, linear phase modulator.**

I. Introduction

Analog fiber-optic links are attractive for Radar front-end applications in which they connect the antennas to a signal processing unit. The conventional IM-DD fiber-optic links have inadequate spurious free dynamic range (SFDR) due to their intrinsic nonlinearity [1-2]. A novel coherent phase modulated (PM) optical link employing an attenuation-counter-propagating (ACP) optical phase locked loop (OPLL) linear phase demodulator has been proposed for solving the problem arising from the limited dynamic range [3-4]. As shown in Fig. 1, the ACP-OPLL contains an ACP-optical phase modulator, a 3 dB coupler and a pair of balanced high power photodiodes. Using feedback, the ACP-OPLL forces the photodiode output to be a scaled replica of the RF signal driving the phase modulator at the transmitter side. This new optical link aims to achieve a spurious free dynamic range (SFDR) nearing 140 dB·Hz$^{2/3}$, significantly surpassing the present state-of-the-art.

In order to implement a high bandwidth ACP-OPLL, the ACP-OPLL must be implemented as compact photonic integrated circuit (PIC), where its loop propagation delay is kept at a minimum. An appropriate choice for implementing the local phase modulator inside the ACP-OPLL PIC is an $In_xGa_{1-x}As_yP_{1-y}$-based multi-quantum well (MQW) phase modulator that can be monolithically integrated with low-loss waveguides and photodetectors on an Indium Phosphide (InP)-based material platform.

The major disadvantage with using InP phase modulators is their nonlinearity. The linear modulation range of the phase modulator is characterized by its phase IP3 [6,7], which is defined as the intercept point of the linear phase modulation response and the third order spurious response in its output phase. Although in theory the phase IP3 of the phase modulator scales linearly with the device length, the high optical loss of existing InP-based optical phase modulators sets a practical constraint on the modulator length and consequently limits the phase IP3 in the range of a couple of π [6]. However, to achieve an SFDR over 140 dB·Hz$^{2/3}$, a phase IP3 of 10π or larger is required for the phase modulator. In this paper, we present a novel InP-based MQW phase modulator design with a deep ridge optical waveguide which shows a very low optical loss and a good phase IP3 value. This MQW phase modulator design enables an ACP local phase modulator with a phase IP3 of 10π and a 4.3 dB optical loss. In the following sections, we first present the design of the InP-based MQW phase modulator, and then report experimental results from the phase modulator.

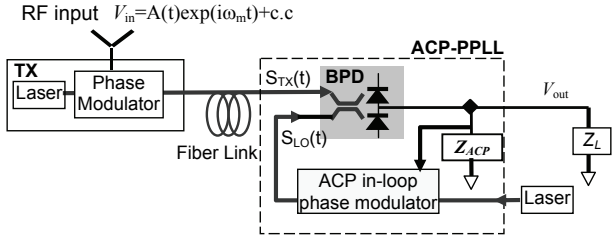

Fig. 1: PM fiber-optic link with ACP-OPLL phase demodulator/detector.

II. InP MQW Phase Modulator Design

InP-based MQW optical phase modulator devices are inherently nonlinear. In order to enhance its linear phase modulation range, the most straightforward approach is to increase the modulator length. This, however, increases the optical propagation loss through the device. For mitigation, we selected a quantum well design [5] where the operating wavelength (~1550 nm) is far from the quantum well absorption peak. A schematic of the device cross-section is shown in Fig. 2 along with an SEM image of the device. The phase modulator has a p-i-n diode configuration and is fabricated on a semi-insulating InP substrate. The p-doped layers of the device above the intrinsic MQW region consists of a highly doped (2×10^{19} cm^{-3}) p-InGaAs contact layer and three subsequent p-InP layers with doping levels of 1×10^{18}cm^{-}

^{3}, 7×10^{17} cm^{-3} and 5×10^{17} cm^{-3}, respectively from top to bottom. To further reduce the optical loss, a 0.15 um thick undoped InP layer is inserted between the QWs and the p-doped InP to separate the optical mode from the absorptive p-doped InP. Simulation shows that this reduces the optical loss by 0.7 dB/mm. While introducing this undoped InP layer reduces the phase modulation sensitivity, it can be compensated for by increasing the device length. The intrinsic MQW region contains twenty-five periods of 12 nm wide $In_{0.64}Ga_{0.36}As_{0.76}P_{0.24}$ quantum wells and 8 nm thick InP barriers. The photoluminescence (PL) peak of the QW is at 1370 nm. Below the MQW region is an n-doped InP (1×10^{18} cm^{-3}) layer followed by a 0.1 um thick n^{+}-InGaAsP contact layer. To enhance the optical confinement factor, a deep ridge optical waveguide structure is employed by dry-etching through the MQW region. Then, a mesa structure is formed under the ridge using a selective wet-etch that stops on the 0.1 um thick n^{+}-InGaAsP contact layer.

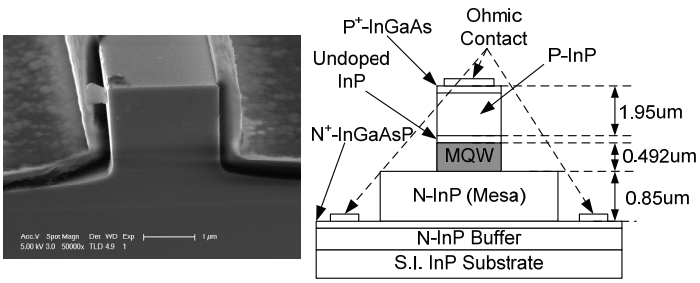

Fig. 2: SEM image and schematic diagram of the cross-section of the InP-based phase modulator.

III. Experimental Results

A. Optical Loss Measurement

The optical loss of the InP MQW phase modulator is measured using an integrated device with two identical 1 mm long phase modulators in series (see Fig. 3). In this measurement, the InP MQW phase modulators are used as photodetectors, where light is launched into one of the phase modulators. Each modulator is reverse-biased at the same voltage, and the photocurrent from each modulator is monitored using two current meters. When the input optical power is sufficiently low, we assume that the photocurrent is proportional to the optical power entering each phase modulator. Since each phase modulator is 1 mm long, the optical loss, α, of the first InP MQW phase modulator is given by:

$$\alpha = 10 \bullet \log_{10}\left(\frac{I_{M1}}{I_{M2}}\right) \quad (1)$$

where I_{M1} and I_{M2} are the photocurrent of the two modulators, and α is expressed in dB/mm. Fig. 4 shows the optical loss versus bias voltage when the wavelength of the input light is 1546 nm and the optical power from the laser source is 6 mW. The optical losses result from the sidewall roughness of the waveguide and absorption arising in the QWs, free-carrier absorption and the Franz-Keldysh effect. The measured optical loss is very small at low bias voltage (~0.5 dB/mm). It increases to ~2 dB/mm as the reverse bias voltage is raised to 6 V.

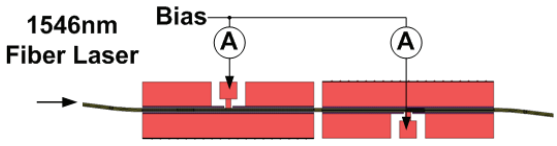

Fig. 3: Experimental setup for measuring the phase modulator loss.

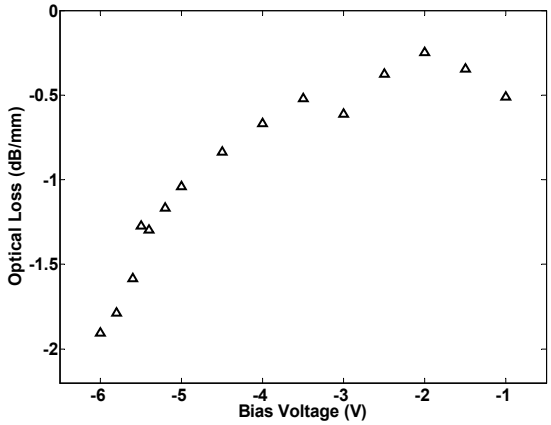

Fig. 4: Insertion loss versus bias voltage.

B. Dynamic V_π Measurement

Since the InP MQW phase modulator has a nonlinear phase modulation response where the PM sensitivity is a nonlinear function of bias voltage. Therefore, the conventional V_π measurement is not suitable to characterize the modulator. In this work, we use dynamic V_π measurement to characterize its PM sensitivity. The dynamic V_π is defined as the ratio between π and the small signal PM sensitivity. The experimental setup is shown in Fig. 5. It consists of a fiber-optic Mach-Zehnder Interferometer (MZI). An InP MQW phase modulator is placed in one arm of the MZI and a commercial $LiNbO_3$ phase modulator (by EO Space) is placed in the other arm. The small signal PM sensitivity is determined by comparing the InP MQW phase modulator with the known $LiNbO_3$ phase modulator (V_π~1.2 V). The laser source is a 1546 nm single mode narrow linewidth fiber laser (Orbits Ethernal 2800A-30-PM). A high power erbium doped fiber amplifier (EDFA) (IPG Photonics EAR-3K-C-LP-SF) is used to boost the optical power before it is launched into the MZ interferometer. In the upper arm, the light is coupled to the InP MQW phase modulator waveguide by a tapered fiber with spot size of 2 um. The output from the modulator is coupled back into a single mode fiber. The fiber-to-fiber insertion loss is ~12 dB. Thus, a second EDFA is used to amplify the optical power. Three fiber-optic polarization rotators are used in this setup to ensure that light with the correct polarization states are launched into the InP phase

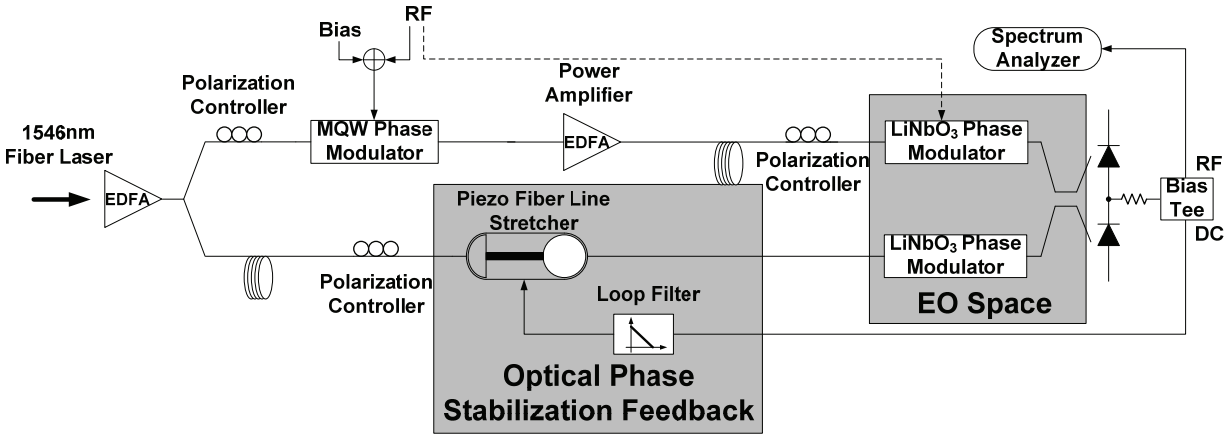

Fig. 5: Experimental setup for dynamic V_π measurement.

modulator, the $LiNbO_3$ phase modulator and the balanced photodiodes (CC-UTC PD supplied by Photodigm Inc). An HP 8593A spectrum analyzer is used to monitor the RF component of the output from the RF port of the bias tee.

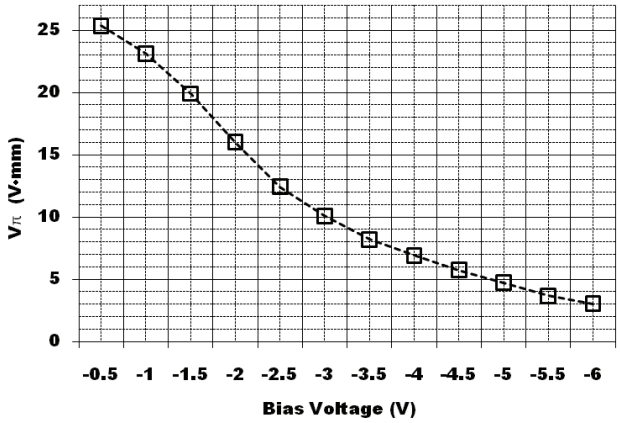

Fig. 6: Dynamic V_π vs. bias voltage.

Because of the temperature fluctuations and mechanical vibrations from the environment, the phase difference between the two interferometer paths suffer from a slow but appreciable drift. Therefore, an optical phase stabilization feedback is implemented. From the DC port of the bias tee, the low frequency spectral components from the output of the photodiodes is extracted and fed into a piezoelectric fiber line stretcher through a loop filter (with a unity gain bandwidth of ~100 Hz). This feedback locks the interferometer at its quadrature point.

To determine the PM sensitivity, a small signal RF tone (11 MHz) is first applied to the $LiNbO_3$ phase modulator and then applied to the InP MQW phase modulator. For each case, the RF power is monitored at the output of the balanced photodiodes. The RF input power is kept sufficiently low so that the entire interferometer operates in the linear region. The dynamic V_π of the QW modulator is given by:

$$V_\pi^{QW} = V_\pi^{LiNbO_3} \times \sqrt{\frac{P_{out}^{LiNbO_3}}{P_{out}^{QW}}} \qquad (2)$$

where V_π^{QW} and $V_\pi^{LiNbO_3}$ are the V_π of the QW modulator and the $LiNbO_3$ standard, P_{out}^{QW} and $P_{out}^{LiNbO_3}$ are the output RF power from the balanced photodiodes when the same RF input signal is applied to the InP MQW modulator and the $LiNbO_3$ modulator, respectively. Fig. 6 shows the measured dynamic V_π of the InP MQW phase modulator. The PM sensitivity increases with bias voltage which is consistent with the optical loss measurement, for large absorption change engender large index change according to the Kramers-Kronig relation. When the reverse bias is above 4.7 V, the dynamic V_π is below 5 V for 1 mm long device. With a 3 mm long device, this implies $V_\pi \sim 1.6$ V, which is very efficient when compared to typical $LiNbO_3$ modulators.

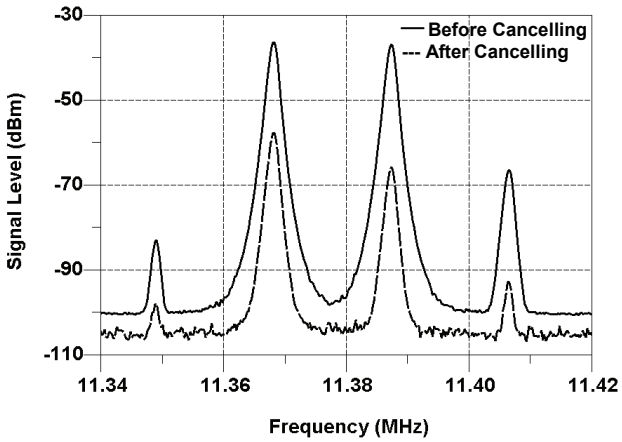

Fig. 7: Spectrum of the MZ interferometer output before and after cancellation.

C. *Phase IP3 Measurement*

The phase IP3 of the InP MQW phase modulator is determined using the approach reported in [7]. The experimental setup used is similar to that shown in Fig. 5 but with minor modifications. The RF signal is split into two paths using an RF balun (Mini-Circuits ADTL 1-12+). One path is directly applied to the InP MQW modulator placed in one arm of the MZI, while the other is fed to the $LiNbO_3$ modulator in the other arm of the MZI after passing through a

variable RF attenuator (Mini-Circuits ZX73-2500+). The RF signal contains two tones separated by 20 kHz with a center frequency of 11.38 MHz. By adjusting the attenuation of the signal applied to the $LiNbO_3$ modulator, we cancel the linear response of the phase modulators. Thus, the third order inter-modulation products measured at the output of the balanced photodiodes are solely due to the nonlinearity of the InP MQW phase modulator.

Fig. 7 shows the spectrum of the interferometer output before and after cancelling. The InP MQW modulator is biased at 5.5 V, and the level of the applied two tone signal is -3 dBm at the RF balun.

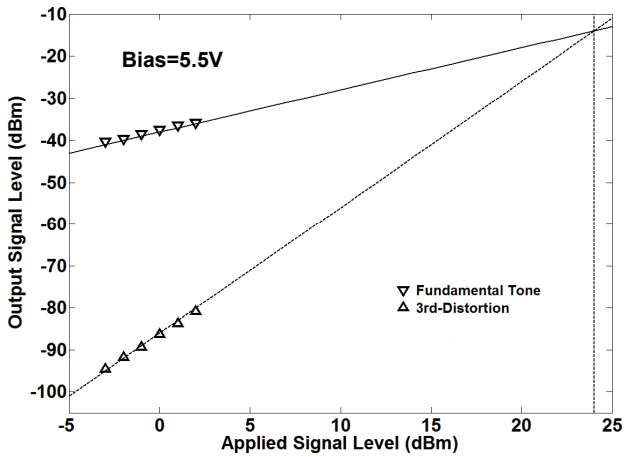

Fig. 8: Input IP3 measurement.

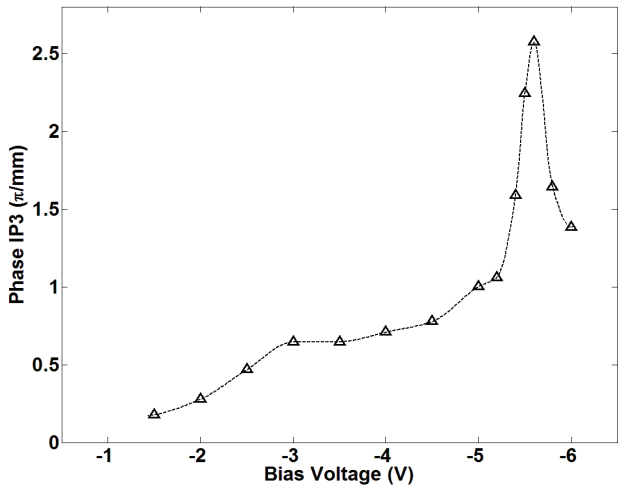

Fig. 9: Measured phase IP3 versus bias voltage.

The linear response of the output is cancelled by more than 20 dB. By applying the same method, the input IP3 of the InP MQW modulator is measured at different reverse bias voltages by sweeping the applied RF signal power. Fig. 8 shows a sample IP3 measurement. The measured Phase IP3 is also plotted as a function of the reverse bias voltage and is shown in Fig. 9. The phase IP3 of the device shows a peak at a reverse bias voltage of 5.6 V. The peak value is ~2.8π which implies that the phase IP3 of a 3 mm long device is 8.4π. This should support a link with an SFDR nearing 140 $dB{\cdot}Hz^{2/3}$. The mechanism behind the sharp peak observed in the phase IP3 as a function of reverse bias voltage is still unclear. However, the results are repeatable for the MQW modulators with the same quantum-well design.

IV. Conclusion

We have presented the design and experimental studies of an InP-based MQW phase modulator designed for implementing an ACP-OPLL PIC. The measurement shows that the MQW InP phase modulator has a small optical loss and a good phase IP3 value. Specifically, at a reverse bias voltage of 5.6 V its phase IP3 and the optical loss are 2.8π/mm and 1.2 dB/mm, respectively. For a 3 mm long device, the modulator design would show a phase IP3 of 8.4π with a tolerable optical loss of 3.6 dB. This is significantly better than the previous reported InP phase modulators [6,7]. This phase IP3 value should enable an RF/photonic link with an SFDR nearing 140 $dB{\cdot}Hz^{2/3}$.

Acknowledgement

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Photonic Integrated Circuits for Microwave Photonics

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***Abstract*—InP-based Photonic Integrated Circuits (PICs) have found applications in the telecommunication and sensing arena because they have offered improvements in cost and function as well as size, weight and power. For microwave photonics applications, it has been found that some analog functions such as optical-phase locked loops (OPLLs) can be greatly improved and enabled with PIC technology. Primary reasons are significantly reduced path lengths that enable much higher loop bandwidths and very stable optical paths enabling low noise coherent summing of optical signals.**

In this paper significant advances in PIC technology will be summarized. Integrated PIC coherent receivers and phase-locked transmitter arrays using OPLLs will be reviewed. Progammable PIC microwave photonic filters will also be briefly discussed.

I. Introduction

Photonic integration provides a reduction in system footprint, inter-element coupling losses, packaging cost, and usually power dissipation, as a single cooler can be used for multiple functions. Although yield issues must be addressed, overall reliability appears to improve, once such issues have been.

In the past decade the complexity of photonic integrated circuits (PICs) has steadily increased. At the turn of the century an integrated widely-tunable laser transmitter chip as illustrated in Fig. 1 represented a fairly advanced PIC [1]. As can be seen, it contained a widely tunable sampled-grating distributed-Bragg-reflector (SGDBR) laser, a semiconductor-optical-amplifier (SOA), and an electro-absorption modulator (EAM) all along a common waveguide.

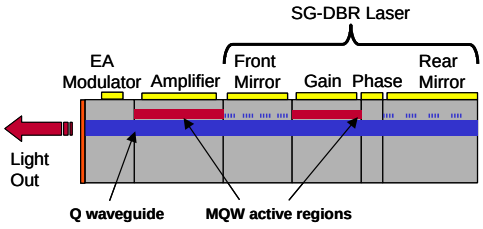

Fig. 1. SGDBR/SOA/EAM widely-tunable transmitter.

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By the end of the current decade, PICs such as that shown in Fig. 2 have been demonstrated. This chip contains over 200 functional elements. This is an 8x8 optical router chip that uses 8 wavelength converters, which each contain an SGDBR followed by an SOA, and an optically-controlled modulator [2]. The wavelength converters then feed an arrayed waveguide grating router (AWGR), which is a dispersive element that directs different wavelengths to different outputs, thus providing the desired space switching.

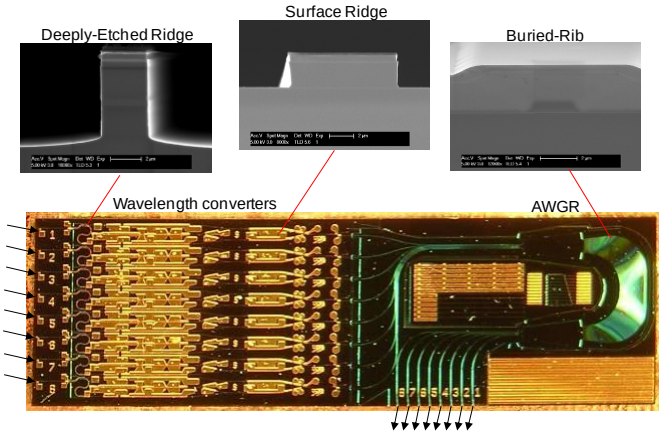

Fig. 2. Monolithic Tunable Optical Router (MOTOR) photo together with SEM cross sections of waveguides at various locations.

The MOTOR chip shown in Fig. 2 operates at 40Gb/s with RZ data, and although all of its inner workings are analog, it really is only intended to function with digital data. It has a fairly limited dynamic range ~10 dB for inputs in the -10 dBm range, a signal insertion loss ~10 dB, but it can switch digital data error-free with these limitations.

Other PICs of similar complexity to that of Fig. 2 are being manufactured and are carrying live telecom traffic. The most significant player in the commercial arena is Infinera. They are selling commercial systems that contain transmitter and receiver PICs together with all of the drive, receive, and control electronics [3]. Their PICs generally consist of a number of parallel transmit or receive channels together with

an AWG multiplexer or de-multiplexer for the transmitter or receiver, respectively [4]. 100 Gb/s systems containing 10 parallel transmit or receive channels of 10Gb/s each have been in the market for several years.

II. OPTICAL-PHASE-LOCKED-LOOPS

A. *Coherent Receiver*

The first example microwave PIC to be discussed is a coherent receiver for phase-modulated signals. The receiver circuit is outlined in Fig. 3 [5]. Microwave photonic links using intensity modulation tend to limited in dynamic range by the transmitter [6]. For direct modulation of a laser the modulation speed must be kept significantly lower than the relaxation resonance frequency of the laser, or nonlinearities result for any modest modulation depth as the carrier density becomes unclamped. For higher frequencies external modulation must be used. Unfortunately, there are no intensity modulators that inherently have a linear relationship between drive voltage and the optical output.

If phase modulation is used, then linear modulators do exist with the basic linear electro-optic effect. Also, an effectively much deeper modulation can be imparted to the optical signal because one is not limited to simple on/off, which might be viewed as a 180˚ modulation, but one in principle could modulate to many times this level to enhance the potential signal/noise. However, now the problem of linearity in the link has been switched to the receiver, and this is the problem we address with the circuit of Fig. 3.

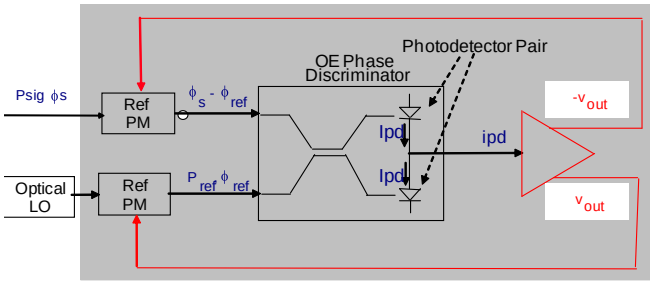

Fig. 3. Coherent receiver for phase-modulated input. Feedback from balanced photodetector is directed to tracking modulator pair.

In Fig. 3 the negative feedback signal to the tracking modulator pair reduces the level of the interference signal on the detectors so that the output is reduced to the linear range. The differential pair also suppresses even order distortions that may exist in the semiconductor modulators as well as amplitude modulation. This approach also enables the use of >> π-modulation depth since the signals leaving the differential tracking modulators are made to be almost in-phase even if hugely out of phase because of a large phase modulation prior to them.

One major issue with this approach is that the tracking phase modulators must nearly instantly track the phase deviation detected in the diode pair. Thus, the delay must be very small. In fact, for the circuit to work in the GHz range, it has been found that delays > 10ps are unacceptable. This not only calls for monolithic integration of both the electronics and photonics, it also demands the elimination of any unwanted signal paths between the two. Figure 4 illustrates the flip-chip bonding configuration that has been implemented to eliminate all additional delays in the practical implementation of the circuit of Fig. 3. The coupler has also been implemented as a beam-splitter to further eliminate propagation delay in a directional coupler embodiment, which was first explored.

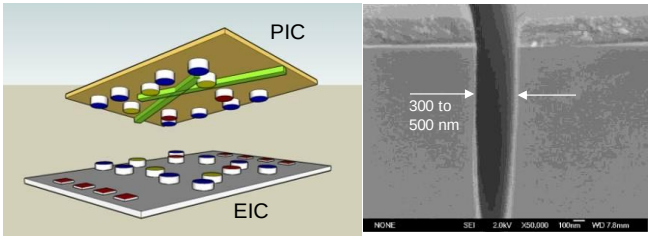

Fig. 4. Schematic of flip-chipping of electronic and photonic ICs together with SEM of etched slot beam splitter.

Initial results using this configuration will be reported in other papers [7,8], but to summarize briefly, a link gain of – 2 dB and a spur-free dynamic range (SFDR) of 122dB·Hz$^{2/3}$ was demonstrated with a transmitter V_π = 4.4 V and only 2.8 mA on each photodetector. Also, a peak-to-peak phase modulation depth of 1.62 π was used for these results, demonstrating the ability to employ a significant modulation depth.

B. *Phase-locked tunable lasers*

Loop delay is also important for phase locking lasers together. Figure 5 shows a chart of initial laser linewidth vs. loop delay for various levels of phase error. Explicitly shown are lines that represent the phase error allowed for different types of digital multilevel phase and amplitude coding. The corresponding SNRs in the signal bandwidth are 9.5dB (PSK), 12.5dB (QPSK), 20dB (16 QAM), and 26.2dB (64 QAM).

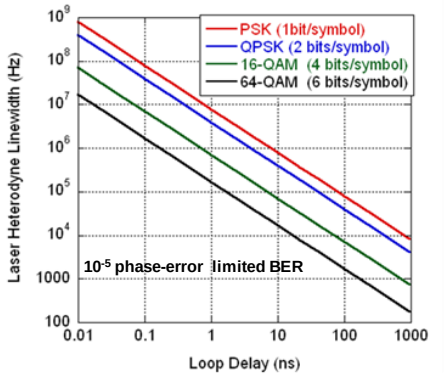

Fig. 5. Laser linewidth vs. OPLL loop delay to enable 10^{-5} error rate for given modulation format.

Widely tunable lasers as the SGDBR shown in Fig. 1 tend to have inherent linewidths in the 1- 3 MHz range. Fig. 5 would indicate a need for OPLL loop delay < 100ps for a

correctable error rate of 10^{-5} in a 64-QAM digital system. But this would actually be a fairly distorted signal from a microwave photonics perspective. Instead of an equivalent spectral efficiency of 6 bits/symbol, we would like to see the line for 10 or 12 bits/symbol, which would again require a loop delay < 10ps in the OPLL if we started with the rather noisy SGDBR. So, again very tight integration is called for.

Phase locking of semiconductor lasers is desired in order to make inexpensive arrays of coherent sources for such applications as phased-array LIDAR and other optical-coherence-tomography (OCT) and imaging applications. It is also desired to have temperature insensitive synthesized sources that are locked to an offset from some stable reference to allow much more efficient use of the spectrum as in the rf domain. As a result, some initial experiments have been done to demonstrate integrated OPLLs formed from a pair of widely-tunable SGDBRs together with most of the required optical elements.

Figure 6 describes a heterodyne experiment in which two SGDBR lasers are offset-locked together [9]. The circuit schematic shows that an integrated modulator is used to generate sidebands on the mixed signal, so that the OPLL can lock on one of these. In this case a 5GHz fundamental offset locking is illustrated. With deep phase modulation of the on-chip modulator it is possible to generate a number of side bands and such modulators can be made with bandwidths up to ~ 100GHz, so it is anticipated that such offset locking might be possible up to the THz range without having to generate rf higher than 100 GHz.

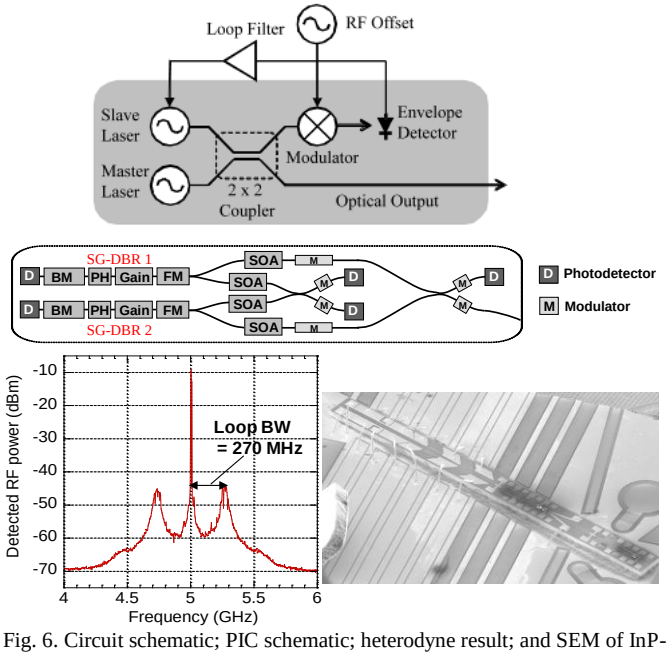

Fig. 6. Circuit schematic; PIC schematic; heterodyne result; and SEM of InP-based PIC.

Fundamental offset locking as high as 20 GHz was demonstrated with the current set up. Although a balanced detector pair was available on the chip, the electronics used only had a single-input TIA, so only a single detector was used, and this resulted in more AM and noise in the feedback loop than necessary. Nevertheless, a respectable phase error variance ~ 0.03 rad^2 was measured over the 2 GHz measurement window.

C. *Future OPLL Directions*

Figure 7 illustrates a cartoon of a futuristic LIDAR system-on-a-chip that will be one of the long-term research directions of a newly formed "Photonic Integration for Coherent Optics" (PICO) Center that involves five US universities [10]. As illustrated with OPLLs it is anticipated that both chirping of the beam in frequency as well as sweeping it in angle will be possible by rapid control of the offset locking as outlined in Fig. 6. This will involve significant developments in the control/feedback electronics as well as in the PICs themselves. As also noted, it is anticipated that much of this work may migrate to the hybrid-Si integration platform.

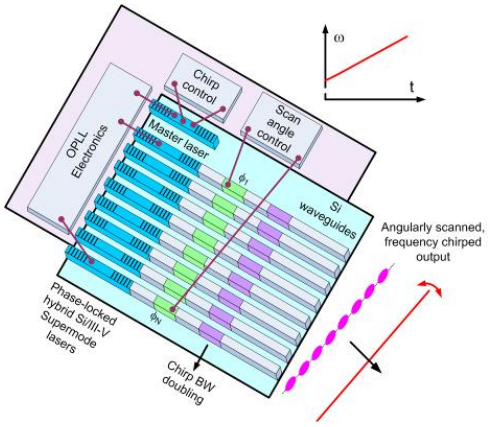

Fig. 7. Vision of future LIDAR system-on-a-chip [11].

III. PROGRAMMABLE MICROWAVE PHOTONIC FILTERS

Another area where photonic integration has potential to impact microwave photonics is in programmable optical filters. Particularly when the the rf information has already been modulated onto a lightwave carrier, it may be wise to perform some prefiltering in the optical domain prior to the receiver, where both the fractional bandwidths and the hardware are small.

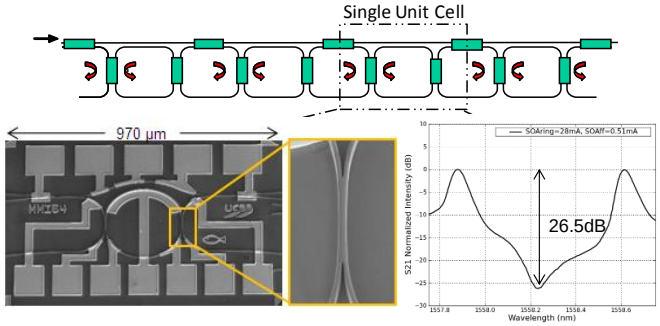

Fig. 8. Lattice filter schematic, SEM of unit cell/coupler, and combined pole/zero response [12].

Figure 8 shows some initial work in this area. The results are for a unit cell that could be an element of a more complex

lattice filter [12]. As shown, the unit cell has two forward paths, and one contains a ring resonator. By selectively biasing the various SOAs and phase modulators placed in the arms of the unit cell, filters with a single pole, a single zero, or a combination of a pole and zero (as illustrated) can be programmed. All can be tuned in frequency by ~ 100 GHz. As also illustrated, novel tapered multimode interference couplers have been employed to save space in these designs.

More complex designs incorporating multiple unit cells as well as ones with different unit cell designs are being explored [13,14]. Figure 9 shows data taken from two integrated third order filters that are cascaded to give a very good extrapolated plot. 70 dB of rejection is predicted.

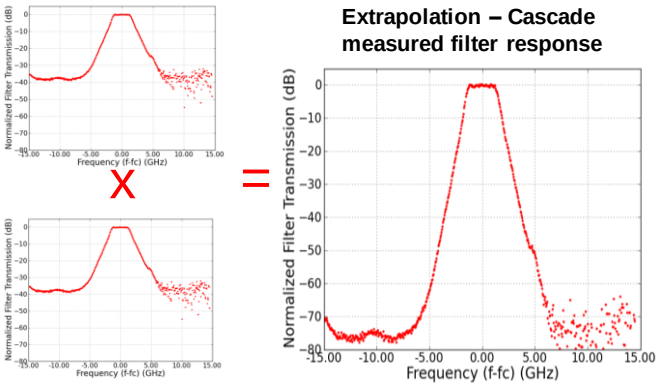

Fig. 9. Cascade of two 3-resonator filters simulated by multiplying transfer function data from the two monolithic filters.

Issues with such active filters are their noise and dynamic range properties. Some competitive designs have gone to great lengths to avoid the inclusion of SOAs because of concerns over their noise contributions and limited saturation levels. However, our simulations show, to the contrary, that some sort of amplification appears to be necessary in any realistic design because of the insertion loss that accumulates when many filter stages are cascaded.

Also, we have found that the net noise added by additional stages that contain SOAs after the first few is very small, even though the power level is just being maintained at the about same level through the cascade as at the input. This is because in a system with SOAs, the noise floor is no longer dominated by shot noise, but by added noise from the amplifiers. As a result, the effective noise figure of SOAs after a few stages in a cascade can be less than 0.5 dB, even though the measured NF for the stand-alone SOA might be ~ 4 dB.

As a result, the noise figure for a filter cascade with no amplifiers quickly goes up, directly as the insertion loss, and values of 30 or 40 dB are easily reached in a typical 8-10 stage filter. On the other hand, the cascade with SOAs, which also may have zero insertion loss, has a noise figure that saturates after a few stages, depending upon the details of the design. Typical values are in the 10 dB range.

The SFDR concern can also be managed by using low-confinement-factor designs. For confinement factors ~2%, saturation powers ~20 dBm have been demonstrated [15], which is sufficient for the current filter goals. Still higher values are possible [16], but there is a tradeoff in power dissipation, because high-saturation power designs are also low-gain designs, so more input power is required for a given gain.

IV. Conclusions

Photonic ICs are becoming important elements for microwave photonics. Low size, weight and power is fairly obvious, but additional advantages of low noise, low cost as well as high stability for a number of applications is very appealing. The possibility of simple, widely-tunable semiconductor sources being able to take the place of some of the very expensive narrow-linewidth sources of today is especially interesting.

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Ultra-Compact Integrated Coherent Receiver for High Linearity RF Photonic Links

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***Abstract*—We demonstrate a novel photonic integrated circuit(PIC) that combines an ultra compact trench beam splitter with monolithically integrated photodetectors and modulators. A coherent receiver is realized by flip chip bonding of this PIC with an electronic integrated circuit (EIC). Preliminary system results yield a third-order intermodulation distortion suppression of 46 dB at a signal frequency of 300 MHz.**

I. INTRODUCTION

Analog optical links are commonly used in the transmission of signals to and from remote antennas and electrical sensors. Since these links are designed to convey a wide range of signals, high-linearity and low-noise operation are required to retain the fidelity of the input signal. The emphasis of this work is on the receiver end of the link which currently poses the greatest challenge in terms of system linearity requirements [1].

In traditional intensity modulated direct detection (IMDD) photonic links, the dominant limitation on dynamic range is the relative intensity noise of the optical source, which is proportional to the square of the average optical power [2]. Furthermore, the modulation depth of MZM-based IMDD systems is limited to 100%. In contrast, phase modulated (PM) optical links can employ $LiNbO_3$ phase modulators that can be driven through many π phase shift, providing a clear advantage in terms of link dynamic range. Use of balanced detection in coherent systems diminishes relative intensity noise (RIN), enabling systems that approach shot noise limited performance [3].

Similar to an IMDD link, a coherent link still employs an interferometer, with an inherently non-linear, sinusoidal transfer function. To overcome this limitation, we have previously proposed a coherent optical receiver that uses negative feedback to suppress the nonlinearities inherent to the phase demodulation process [4]. The receiver architecture is shown in Figure 1. The phase modulated signal from the transmitter is mixed with the signal output of the feedback reference phase modulator. Optical mixing is achieved by using an interferometer followed by a balanced detector pair. The balanced PD produces an error signal that is amplified, filtered, and fed back to the reference phase modulator to compensate the phase difference between the signal and local oscillator. This effectively lowers the signal swing of the demodulator thereby restricting the operation of the receiver to the linear region of the response curve.

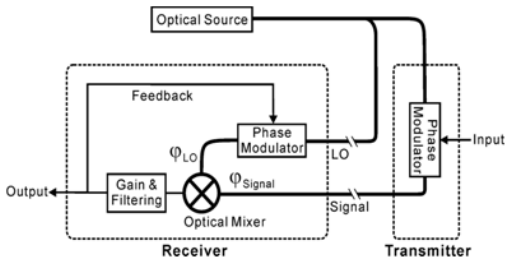

Figure 1: Architecture of coherent receiver with feedback

II. DEVICE DESIGN AND FABRICATION

Because of bandwidth limitation due to latency in the loop, the delay must be kept short for stable operation at high frequencies. Monolithic integration of the receiver components is necessary to limit the loop delay and maximize the optical power coupled to the PDs by avoiding additional coupling losses. We have designed several iterations of PICs that monolithically integrate balanced photodetector pairs, phase modulators and 2x2 combiners on an InP platform. To realize a large loop bandwidth, the capacitances of photodiodes and modulators are exploited as circuit elements to perform the desired loop integrations in the feedback path [5]. Uni-travelling-carrier photodiodes (UTC-PDs) are employed for the balanced PDs because of their high photocurrent operation made possible by reduced space charge effects [6]. The device is designed in a push pull

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Layer	In (%)	As (%)	Thickness (nm)	Doping (cm^{-3})
InP	100	0	150	1E18
InGaAs	53.2	100	75	P
InGaAs	53.2	100	8	UID
InGaAsP	75.85	52.34	16	UID
InP	100	0	6	UID
InP	100	0	7	1E18
InP collector	100	0	200	N
InP field termination	100	0	25	2E18
InGaAsP stop etch	71.14	61.12	15	UID
InP regrowth	100	0	15	UID
InGaAsP waveguide	71.14	61.12	55	1E17
InGaAsP Barrier	71.54	58.86	25	UID
14x InGaAsP Barrier	71.54	58.86	8	UID
15x InGaAsP QW	71.54	77.53	6.5	UID
InGaAsP Barrier	71.54	58.86	25	UID
InGaAsP waveguide	71.14	61.12	55	1E17
n-InP	100	0	600	1E18
n-InGaAsP contact	85.47	31.72	100	3E18
n-InP	100	0	500	1E18
SI InP substrate	100	0	350,000	8E18 - 3E19

TABLE I. Device Epitaxial Structure

configuration with symmetric tracking phase modulators used to cancel even order distortion terms [3]. In [4], a 2x2 multimode interference (MMI) coupler was used as the mixing element. That PIC was wirebonded to an external EIC that provided transconductance amplification of the feedback signal. In the present iteration, we aim to reduce the loop delay of the original design by utilizing an ultra compact trench beam splitter to reduce the footprint of the PIC. This condensed PIC is then flip chip bonded to the EIC, thereby avoiding the delay of the wirebonds and reducing the delay of the on-chip wiring.

The monolithic integration platform for the coherent receiver is realized on a semi-insulating InP substrate and requires a single regrowth step to form modulator, photodetector, and passive regions. The epitaxial structure, shown in Table 1, consists of the UTC-PD structure grown on top of unintentionally doped (UID) InGaAsP modulator QWs and barriers. The optical waveguide consists of a multiple quantum well (MQW) stack of 15 compressively strained wells and 16 tensile strained barriers [4]. The QW width is 65 Å and the barrier width is 80 Å.

Photodetection regions are formed by selectively removing the UTC-PD layers. This is followed with a p-cladding and p-contact regrowth. The optical waveguide uses a dry-etched deep ridge architecture to allow the flexibility of device geometry that the trench coupler requires. Comparatively, in surface ridge architectures, any features oriented significantly off the major plane suffer severe crystallographic undercut in the wet-etching process [7].

Waveguides and modulators are defined using a dual mask of 55 nm Cr and 500 nm SiO_2, and are deeply etched using Cl_2:H_2:Ar chemistry in an ICP-RIE system. Very low passive waveguide loss of 2.2 cm^{-1} has been reported for this deep etching process [8]. Next, mesas are etched to expose the underlying n-contact layer. The InGaAs p+ contact layer is selectively removed between contacts to provide electrical isolation, and n- and p-contacts are deposited and annealed. In order to minimize diode series resistance of the modulators and the detectors, we first deposit a pre-metal layer which is a very thin stack of Pt/Ti/Pt/Au. This liftoff is carried out in such a way that the top p-side contact layer is not exposed until just before the metal deposition. This method largely avoids contamination of the metal-semiconductor interface, which is an important factor in achieving low diode resistance. Modulators of 500 µm length are defined in the metal deposition steps.

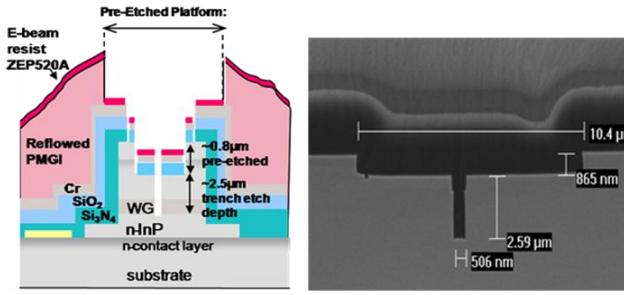

Figure 2(a). Trench planarization process. (b) Cross-sectional SEM of trench

The passive portions of the waveguide are proton implanted to reduce optical loss. To realize the balanced PD configuration, a series of high energy implants ranging from 40 keV to 1.275 MeV are used to electrically isolate the n-contact layer. Transmission line model (TLM) measurements yield an implanted sheet resistance of 4.8 MΩ/square on the n-material and 1.9 MΩ/square on the p-material. The PDs can then be connected in series with minimal electrical cross talk between the diodes.

The trench coupler is designed to act as a frustrated total internal reflection (FTIR) mirror, reflecting and transmitting equal parts to the photodetectors. The input waveguide is incident on the FTIR mirror at an angle greater than the critical angle. Normally this should result in a fully reflected wave, but designing a narrow enough trench allows evanescent coupling of the incident wave across the trench that can result in an ultra compact 50:50 beam splitter. Benzocyclobutene(BCB) with a refractive index of 1.57 is used to fill in the trench. With a calculated effective index of 3.265 for the waveguide, the critical angle is 28.5^0. Crossing angles in the range of 27^0-32^0 were fabricated, correlating to trench widths of 0.25-0.5 µm. Trenches were written using electron beam lithography (EBL). Because ZEP-520 e-beam resist is very thin (~3000 Å), the topography of the sample (which has waveguides over 3µm high) makes it very challenging to get the necessary sidewall coverage over a large step and provide a robust trench etch mask. Furthermore, the minimum thickness of the SiO_2 dielectric mask is 6000 Å, which is far too much to be etched using the thin e-beam resist. Therefore, a planarization process, using Polymethylglutarimide (PMGI) resist is employed. By reflowing the PMGI at 275^0C for 20 min, the step height is reduced from 3.1 µm to 1.2 µm, which is within the step coverage tolerance of the e-beam resist. In order to reduce the required etch depth to reach the waveguide, a wider region around the trench is pre-etched down by ~1 µm.

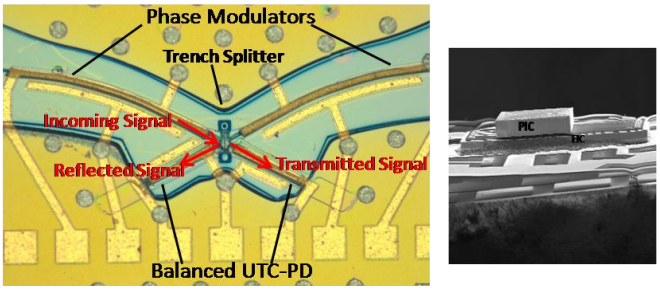

Figure 3(a): Top View of PIC. (b) Side view of flip chip bonded PIC + EIC

Simulations show that the effective index of the waveguide changes very little as a result of this pre-etching.This reduces the target etch depth to about 2 µm which is possible for the designed trench widths. A diagram of the pre-etching, planarization, and subsequent trench etch processes is shown in Figure 2(a). A dual layer mask of Cr/SiO_2 is used as the trench hard mask. Both the pre-etch and the trench etch itself utilize the Cl_2:H_2:Ar chemistry used for the waveguide etch. Gas flows, pressure, and ICP power were varied to optimize the trench for depth, sidewall straightness and smoothness, resulting in a high aspect-ratio trench coupler. A cross-sectional SEM of the optimized trench etch is shown in Figure 2(b). After the trench etch, thick pad metal is deposited using an angled, rotating stage to ensure step coverage of the metal. A top view of the completed PIC is shown in Figure 3(a).

The last step of device fabrication is the integration of the transconductance amplifier EIC to the coherent receiver PIC by flip-chip bonding. After thick pad metal is deposited for the contacts, flip chip vias are opened and 2 µm tall Indium bumps are deposited to provide the contact points between the diodes of the PIC and the EIC connections. The PIC and the EIC are carefully aligned and bonded at a force of 1000 g and a temperature of 200^0C. An SEM of the final integrated flip-chip bonded coherent receiver is shown in Figure 3(b).

III. INTEGRATED RECEIVER RESULTS

The total delay includes the delay incurred by the PIC, the EIC and the interconnections between them. In the MMI-based device reported in [4], the total loop delay was ~27 ps, where a significant portion of the delay was caused by the wirebond interconnects. In comparison, the ultra-compact trench-based flip-chip bonded approach used in this work reduces the loop delay to ~10 ps. This is expected to increase the stable open loop gain by 20 dB at 1 GHz, the target frequency of operation [9].

The pre-metal deposition process described in the previous section decreases the forward diode resistance by a factor of 6. The measured diode resistance in forward bias is ~5 Ω for 300 µm x 3 µm modulators and ~20 Ω for 50 µm x 7 µm detectors. Using a test electronic chip with direct traces to each diode contact, the PIC diode characteristics were measured before and after flip- chip bonding. In most cases, the diode series resistance improved after flip chip bonding, perhaps because the In bumps make more stable contacts than the pin probes used to test the diodes prior to bonding.

The efficiency and loss were measured for phase modulators that were separately fabricated using the same quantum well and waveguide structures used in this PIC [10]. For a 500 µm long modulator, the V_π was measured to be 3.9 V. The loss incurred between 0 V and V_π was 5.5 dB. The normalized PD response shows a 3dB bandwidth of ~5 GHz for a 7 µm x 150 µm device at -4 V bias. This bandwidth is more than satisfactory for our link experiments carried out at 300 MHz. Saturation and linearity measurements of the UTC-PDs were reported in [4]. Saturation current, defined as the photocurrent level where the RF response is compressed by 1 dB, is reported to be 80 mA at a bias of -3 V. The third order output intercept point(OIP3), which is a measure of PD linearity, was found to be 46 dBm at 60 mA of DC photocurrent. The high performance of these UTC-PDs indicates that we can achieve high open loop gain without creating nonlinearities.

The trench coupler splitting ratio was tested under illumination from a laser source emitting at 1548.51 nm. Light was fiber coupled into a phase modulator, split into reflected and transmitted waves at the trench, and detected at the UTC-PDs. A polarization controller was utilized to characterize the trench coupler for both TE and TM polarizations. For many of the trench designs implemented, the measured TE splitting ratio was very close to 50:50, with about 1.2 mA into each detector at an input power of 10 dBm at the device facet. The detected TM photocurrent for the same device was 2 mA and 0.4 mA for the reflected and transmitted waves, respectively.

To characterize the mixing efficiency, we send a local oscillator signal to both phase modulator inputs and apply phase modulation to one arm. The signal in the photodetectors will swing as the two input signals drift in and out of phase with each other. If we subtract the signals of the series connected photodetectors, we get the balanced detector signal. Following the derivation in [11], and assuming ideal balanced detection, the maximum amount of coherent mixing corresponds to a balanced detector signal swing of 4 x (average photocurrent in each detector). In the non-ideal case, there will be a coherence penalty due to imbalance in power coupled to each arm, imbalanced splitting ratio, polarization mismatch and wavefront mode mismatch between the reflected and the transmitted beam.

An oscilloscope trace of the balanced detector signal is shown in Figure 4. The voltage swing of the individual photodetector signals, $V_1(t)$ and $V_2(t)$ are shown in the top and bottom traces. The middle trace is (V_1-V_2), the balanced photodetector signal. The maximum observed signal swing for the device tested in Figure 4 was found to be 524 mV with an average I_{DC} of 3.5 mA into each detector. Considering the 50 Ω input impedance of the oscilloscope, the maximum possible signal swing is 700 mV. Thus the coherence efficiency of the mixer is ~75%.

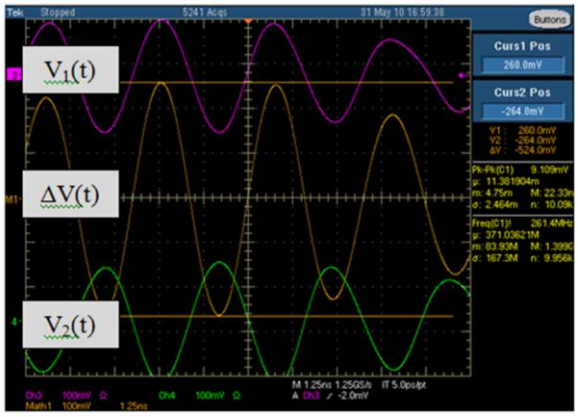

Figure 4: Measurement of Coherent Mixing in Balanced Photodetector

The suppression of the receiver nonlinearity is characterized for the full flip-chip bonded PIC + EIC. Two-tone measurements were carried out at signal frequencies of 298 MHz and 300 MHz. Output frequency spectra of the receiver with and without the use of the feedback loop are shown in Figure 5. The input power was 0 dBm per tone. The IMD3 term is suppressed by an additional 46 dB when the feedback loop is in operation, showing that the system does indeed suppress receiver nonlinearity. Assuming a shot-noise limited optical source, the calculated SFDR would be 122 $dB \cdot Hz^{2/3}$. For detailed discussion of SFDR characterization, see [9].

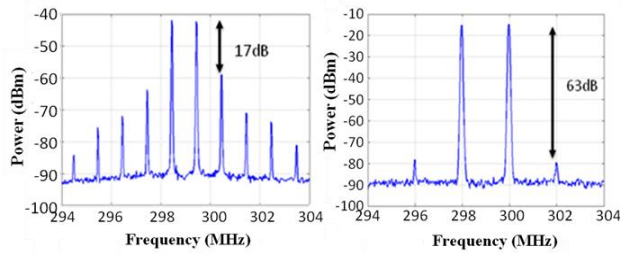

Figure 5: Measured IMD3 suppression with and without feedback loop

IV. CONCLUSION

Design and fabrication of a coherent receiver with feedback was presented. Flip chip bonding of the PIC to the EIC was used to reduce feedback latency. Trench beam splitters were developed to enable an ultra-compact PIC. We have achieved a very low latency feedback loop. Suppression of IMD3 by 46 dB was achieved.

ACKNOWLEDGMENT

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I. Photonic Integrated Circuits

C. Programmable Lattice Filters

Programmable Photonic Lattice Filters in InGaAsP–InP

Erik J. Norberg, Robert S. Guzzon, Steven C. Nicholes, John S. Parker, and Larry A. Coldren, *Fellow, IEEE*

***Abstract*—A novel monolithic programmable optical lattice filter consisting of unit cell building blocks is proposed. Single unit cells incorporating a ring resonator in one arm of a Mach–Zehnder are fabricated in an InGaAsP–InP material system. Programmable poles and zeros are demonstrated and monolithically cascaded unit cells are used to synthesize a flat passband.**

***Index Terms*—Optical filter, photonic integrated circuits (PICs), programmable filter.**

I. Introduction

PROGRAMMABLE optical filters have the potential to improve latency in real-time signal processing applications compared to entirely electronic approaches. The optical filter can be programmed to create a channelizing prefilter, quickly tunable in bandwidth and frequency. Thus, massive amounts of incoming analog data can be prefiltered in nearly real time, identifying signal bands or signatures worthy of more detailed digital signal processing. This and other applications call for a general programmable filter. The idea of programmable optical filters was suggested over two decades ago, e.g., [1]; however, their complexity, control, and stability have all been limited by the inability to integrate the optical components on a single chip. More recently, channel selection and add–drop multiplexer filters have been shown for wavelength-division-multiplexing (WDM) applications using microring resonators as well as larger ring geometries [2]–[6]. In comparison, the programmable analog filter application is very challenging in that it requires much broader frequency and bandwidth tunability than channel selection filters. We propose a lattice-based filter, monolithically integrated using the InGaAsP–InP material system. The filter architecture is an array of identical unit cells that incorporate a ring resonator within one branch of a Mach–Zehnder interferometer (MZI). In this initial work, we have fabricated and characterized the basic building blocks of these filters consisting of one and two unit cells. Preliminary fabrication results have previously been reported [7]. Here we demonstrate improved results along with a more thorough characterization and discussion of these filters.

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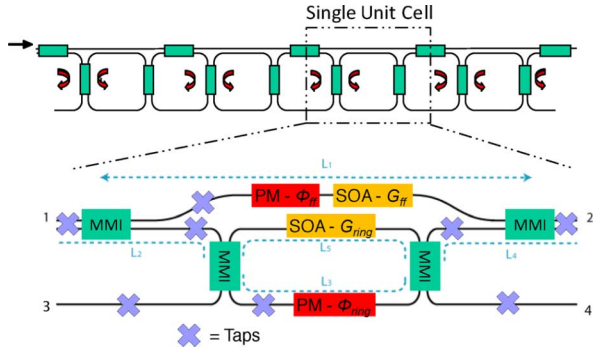

Fig. 1. Schematic drawing of the lattice filter built from unit cells. Key components in the single unit cell are highlighted: SOAs, PMs, MMIs, and Taps.

II. Filter Design

Fig. 1 shows the proposed lattice-based filter structure built from cascaded unit cells. The single unit cell itself consists of an asymmetrical MZI, in which one MZI-branch has an integrated ring resonator. Looking from port 1 to port 2, a first-order zero response is created by the MZI while a first-order pole response is provided by the resonator; these are the fundamental building blocks for both finite impulse response (FIR) and infinite impulse response (IIR) filters. The response from each single unit cell is tunable in amplitude and phase through active semiconductor optical amplifiers (SOAs) and phase modulators (PMs) incorporated in both the feed-forward MZI arm and the ring resonator. The single unit cell filter response can be described through the S_{21} scattering parameters, given here in a simplified form

$$S_{21} = AG_{\mathrm{ff}}e^{-j\beta L_1+\Phi_{\mathrm{ff}}} + \frac{Be^{-j[\beta L_2+L_3+L_4+\Phi_{\mathrm{ring}}]}}{1-CG_{\mathrm{ring}}e^{-j[\beta L_3+L_5+\Phi_{\mathrm{ring}}]}}. \tag{1}$$

The A, B, and C coefficients include the loss from various elements in the structure including waveguide, multimode interference (MMI) transmission, and MMI coupling loss. $G_{\mathrm{ff}}, \Phi_{\mathrm{ff}}$ and $G_{\mathrm{ring}}, \Phi_{\mathrm{ring}}$ are the gain and phase provided by the SOA and PM for the feed-forward and ring resonator, respectively. By reverse biasing the feed-forward SOA ($G_{\mathrm{ff}} \sim 0$) a pole response is isolated. Likewise a zero response is synthesized by reverse biasing the ring SOA ($G_{\mathrm{ring}} \sim 0$). The PMs that operate through carrier injection are used to tune the pole and zero responses in frequency. In addition to SOAs and PMs, a number of low quantum efficiency detectors (taps) are incorporated to provide real-time monitoring of the optical signal in the waveguide at many locations in the single unit cell, which, together with analog feedback circuitry and digitally implemented adaptive algorithms, can be used for control and stabilization.

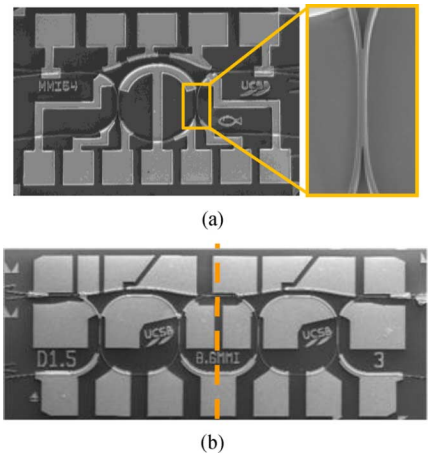

Fig. 2. (a) Scanning electron microscope (SEM) picture of the single ring unit cell with the MMI coupler highlighted. (b) Two monolithically cascaded single unit cells make up a three-ring coupled system.

The single unit cell is naturally cascaded by connecting ports 2 and 4 with ports 1 and 3 of the next cell to realize the lattice filter. The programmability of this larger lattice filter is based on the flexibility of each individual unit cell. SOAs can "turn ON" and "turn OFF" rings by applying a forward bias and reverse bias, respectively. For example, high bandwidth flat-topped bandpass filters suitable for WDM add–drop applications [3] of any order can be synthesized by turning ON the SOAs in each ring, and turning OFF the feed-forward SOAs. Coupling rings in this fashion synthesizes bandpass filters without phase tuning as the bandwidth is determined by the coupling strength between rings. Filter rolloff and extinction are enhanced by the coupling via higher order poles.

If a narrower bandwidth response is desired, rings can be cascaded without coupling by turning ON every other ring. With the rings uncoupled, no higher order poles are synthesized, and each pole location and amplitude is independently tunable. Poles can then be located at the same frequency, decreasing full-width at half-maximum (FWHM) and enhancing extinction. The MZIs created by the unit cells can be used to eliminate neighboring poles to effectively enhance the free spectral range (FSR) of the filter. Furthermore, any filter configuration can be duplicated and cascaded without back-coupling to enhance extinction and roll-off and decrease the FWHM if desired.

We have fabricated single unit cells together with two monolithically cascaded unit cells shown in Fig. 2. An offset quantum well (OQW) InGaAsP–InP integration platform was used (quantum wells placed right above the waveguide layer). Low loss passive sections were realized by selectively wet etching away quantum wells in passive regions, followed by a single blanket InP regrowth of the p-cladding. An entirely deep etched waveguide design was utilized; the specific details of the fabrication have been described elsewhere [7].

III. Experiment and Discussion

Measurements of the filters were made by fiber coupling broadband light from an amplified spontaneous emission (ASE) source into the chip and fiber coupling the output into an optical spectrum analyzer (OSA). All testing was performed continuous wave (CW) at room temperature.

An isolated MZI response is shown in Fig. 3(a), this was generated between ports 1 and 2 by reverse biasing the ring SOA at -10 V, effectively shutting off the resonator. By varying the bias on the feed-forward SOA and hence balancing the MZI branches, the zero response is tuned in amplitude. However, while changing the current on the SOA, a parasitic phase shift is introduced (through current injection and heating) which unintentionally tunes the filter response in frequency. In our device, this is addressed by simultaneously utilizing the PMs, by injecting current the zero-frequency can be fixed. Fig. 3(b) displays the isolated pole response of the single unit cell using ports 3 and 4. The pole amplitude can be adjusted by varying the ring SOA bias, again utilizing the resonator PM to fix the filter in frequency. For the SOA biased at 33 mA ($I_{\rm th} = 35$ mA), an extinction ratio of $\sim$18 dB and a pole FWHM of 0.062 nm (7.9 GHz) corresponding to a resonator Q-value of 23 800 is obtained. The pole response was also measured with a lightwave component analyzer, and this verified the expected π-phase shift across the passband of this single-pole filter. A good fit of the experimental filter shapes with the S21 parameters in (1) are demonstrated by setting $AG_{\rm ff} = 1, B = 0.68, CG_{\rm ring} = 0$ and $AG_{\rm ff} = 0, B = 1, CG_{\rm ring} = 0.75$ in Fig. 3(a) and (b), respectively.

If a further enhancement of the filter extinction ratio is desired, both zeros and poles can be utilized simultaneously (i.e., forward biasing both the feed-forward and the resonator SOA). In Fig. 3(c), a zero has been placed in between two resonator poles, resulting in a total of 26.5-dB extinction.

The frequency tunability of the of the single unit cell is demonstrated in Fig. 4; the S_{21} MZI zero is continuously tuned over a 270-GHz range by utilizing phase pads in the feed-forward and the resonator arm. The FSR of the zero is 250 GHz, thus a zero can be placed anywhere in the C-band. The resonator poles allow for a 0.4-nm continuous tuning range, using the resonator phase pads. Wavelength tuning through current injection is associated with parasitic loss through the free-carrier-absorption effect; in our device design, the filter shape is preserved by manually adjusting the SOA bias. Future work includes using the passive taps as the input signal to adaptive algorithms that automatically control SOA and PM biases to maintain filter shapes while tuning or reprogramming the filter.

Drawing on the demonstrated tunability of the single unit cell it is predicted that by cascading several unit cells, higher order and more complex filter shapes can easily be synthesized by individually controlling each single unit cell. As a proof of concept, the fabricated cascaded unit cell filter is used to demonstrate a second-order coupled pole response shown in Fig. 5. This was created by turning OFF the feed-forward waveguides and the third ring by reverse biasing their respective SOAs. The remaining two rings were tuned using PMs to create a bandpass filter with a 0.302-nm (37.7 GHz) FWHM. Given the strong 3-dB inter-ring coupling in this filter, a relatively wide-bandwidth, low-extinction passband results.

In the current device configuration, we predict that the number of unit cells that practically can be cascaded is limited by the end to end loss of the individual unit cells; currently estimated to be around 7 dB which includes the 3-dB loss in the outer MZI-MMIs when operating the filter with cascaded poles. Given a $\sim$21-dB SNR in the first filter stage, a maximum of three unit cells can be cascaded. In future work, we, therefore,

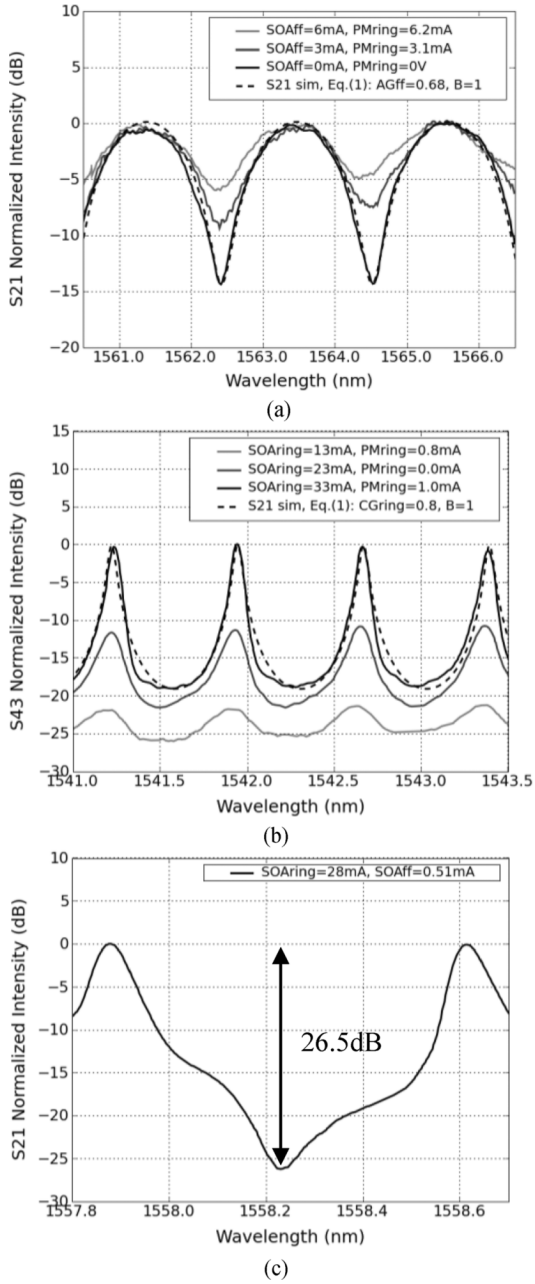

Fig. 3. (a), (b) Isolated pole and zero responses tuned in amplitude by varying bias on feed-forward SOA (SOAff) and ring SOA (SOAring), respectively, the ring PM (PMring) is used to fix the filter in frequency. (c) Zero and pole are utilizes simultaneously to enhance extinction ratio.

intend to achieve a zero insertion loss in every unit cell by incorporating an additional SOA in the ring-MZI arm (on L_2 or L_4 in Fig. 1), thus allowing a large number of filter stages to be cascaded. In addition, this also assists the balancing of the two MZI arms when a zero response is desired.

IV. Conclusion

We have proposed a novel monolithic programmable filter structure, constructed from cascaded unit cells. The single unit cells have the form of an MZI with a ring resonator integrated in one branch. Proposed programmability of the single unit cell was experimentally demonstrated through isolated zero and pole

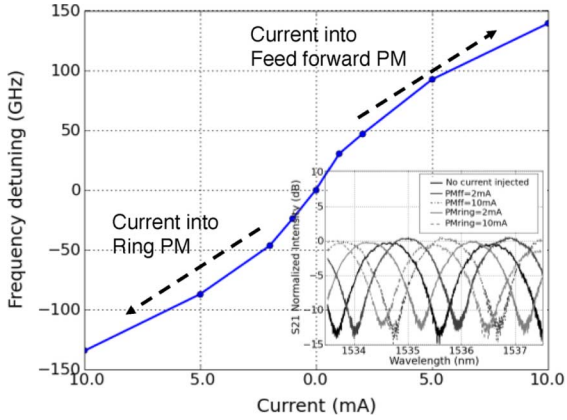

Fig. 4. Frequency detuning of the MZI zero response as a function of PM current; inset shows the actual filter response.

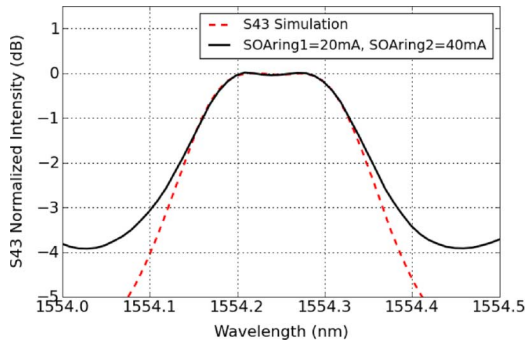

Fig. 5. Filter response from two-coupled-ring bandpass filter tuned to ∼0.1-dB ripple with a 0.302-nm (37.7 GHz) FWHM.

responses with continuous amplitude and frequency tunability. Extinction ratios of 14 and 18 dB was shown for the zero and pole, respectively, simultaneously using the pole and zero the extinction was enhanced to 26.5 dB. From cascaded unit cells, a flat passband using a second-order coupled pole response was demonstrated.

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Programmable Photonic Filters from Monolithically Cascaded Filter Stages

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Abstract: A monolithic programmable photonic filter structure is constructed from cascaded single filter stages individually capable of producing poles or zeros. Flat-topped 2nd and 3rd order filters with pass-band rejection exceeding 30 dB are demonstrated.
OCIS codes: 230.5750 Resonators, 250.5300 Photonic integrated circuits

1. Introduction

A programmable photonic filter is capable of synthesizing a variety of filter shapes and rapidly tune in both bandwidth and center frequency. Such a filter can be used as a channelizing filter to prefilter massive amounts of incoming analog data in nearly real time, thus having the potential to reduce latency in signal processing applications compared to entirely electronic approaches. The idea of this kind of filter was suggested almost three decades ago [1], however the complexity, control and stability have all been limited by the inability to integrate on a chip. Compared to channel selection and add/drop filters for WDM applications which have been successfully realized in recent years [2,3], the analog RF-filter application is more challenging as it requires much broader tunability in bandwidth and frequency. Lattice type filter structures can provide theses necessary characteristics [4]. We have previously proposed a lattice building block capable of producing both IIR (infinite-impulse-response) and FIR (finite-impulse response) filter shapes, and experimentally demonstrated it in the InP-InGaAsP material system [5]. Similar work was done in parallel on a hybrid Si-III/V platform [6]. At this time, we focus on the cascading of multiple filter stages and construction of more complex higher order filters. In order to improve the stability and control of the overall filter structure, the single filter stage has been modified to an uncoupled filter scheme.

2. Filter design and fabrication

Each filter stage consists of two nested rings of different lengths. Thus, the design also incorporates an asymmetric Mach-Zehnder interferometer (MZI), figure 1. The single stage filter response has two poles and a zero; however, the intention of the single stage design is to generate either a single pole or zero. This is achieved by utilizing the SOAs as on-off switches for different paths through the filter. Eq. (1a-c) gives the S21 scattering parameters for the single stage in the different configurations, with $G_{1,2,3}$ and $\varphi_{1,2}$ representing gain and added phase from the SOAs and the phase modulators (PM) respectively, and A,B,C representing propagation and coupling losses. By reverse biasing either SOA_1 or SOA_2 one of the poles is isolated, Eq. (1a),(1b). If SOA_2 is reversed biased, a longer resonator remains than if SOA_1 is reversed biased. A longer resonator translates into a narrower full width half max (FWHM), so depending on which ring configuration is utilized a narrower or wider bandwidth filter is synthesized. The MZI zero filter response is isolated by reverse biasing SOA_3, Eq. (1c). In each bias configuration, the filter response is tuned in amplitude by forward biasing the remaining two SOAs, providing ring gain or balancing the MZI arms in the pole or zero configurations respectively. Frequency tunability of the filter is provided through the PM.

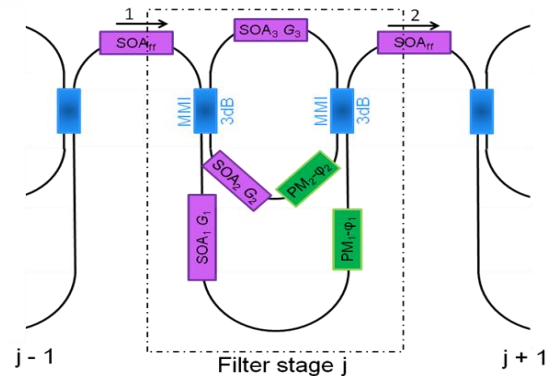

Fig.1 Schematic drawing of the filter structure highlighting the single filter stage with functional components labeled, SOAs, MMI couplers and PMs.

$$S_{21} = \frac{AG_1 e^{-j(\beta L_1+\varphi_1)}}{(1-AG_1CG_3 e^{-j(\beta(L_1+L_3)+\varphi_1)})} \quad (1a)$$

$$S_{21} = \frac{BG_2 e^{-j(\beta L_2+\varphi_2)}}{(1-BG_2CG_3 e^{-j(\beta(L_2+L_3)+\varphi_2)})} \quad (1b)$$

$$S_{21} = AG_1 e^{-j(\beta L_1+\varphi_1)} + BG_2 e^{-j(\beta L_2+\varphi_2)} \quad (1c)$$

$$\left|S_{21}^{tot}\right| = \prod_j \left|S_{21}^{j}\right|, \quad \angle(S_{21}^{tot}) = \sum_j \angle(S_{21}^{j}) \quad (2)$$

When designing cascaded filter structures, there are two main design schemes: coupled or uncoupled. In the coupled case, there is feedback between filter stages. For resonators this means that the poles are coupled and higher order poles are created. While this scheme has certain advantages in e.g. providing larger pass band rejection through the higher order poles, the inter stage couplings becomes extremely critical in order to reach the desired filter shape. In addition, a coupled system with active phase and gain controllers has more parameters and thus becomes inherently harder to control and stabilize in a real system application. This is the main reason we have in this work instead focused on a completely uncoupled approach, i.e. there is no feedback between filter stages. This is most easily seen through the single waveguide connecting neighboring stages in figure 1. This linear system approach implies that the overall transfer function of the filter is simply the product of the individual single stage transfer functions; or in S-parameters, the magnitude and phase response multiplied and added respectively, Eq. (2). With a pole or a zero synthesized by each filter stage, higher order filters are subsequently constructed by programming the individual stages with the desired pole and zero magnitudes and phases. In contrast to the coupled approach, the overall filter shape in the uncoupled scheme is completely independent of the coupler values, allowing for more fabrication tolerance and flexibility in coupler choice.

In order to monolithically integrate this type of filter we utilize the InP-InGaAsP material system, which has the advantage of providing on-chip optical gain and fast phase tuning through current injection. An offset quantum well (OQW) integration platform was employed with low loss passive waveguides realized by selectively removing quantum wells in passive regions followed by a blanket InP p-cladding regrowth. In order to avoid radiation loss from bends while keeping the fabrication complexity to a minimum, deeply etched waveguides created with a single ICP-dry etch step was used for the entire device design. For ring coupling, 3dB-2x2 restricted interference multi-mode-interference (MMI) couplers were used throughout; the insertion loss was measured to be 0.5-1dB/coupler. Specifics of the fabrication and the integration platform have been reported elsewhere [7]. In this work a total of five single filter stages were monolithically cascaded; figure 2 shows a device with four filter stages which have been wire bonded to a carrier.

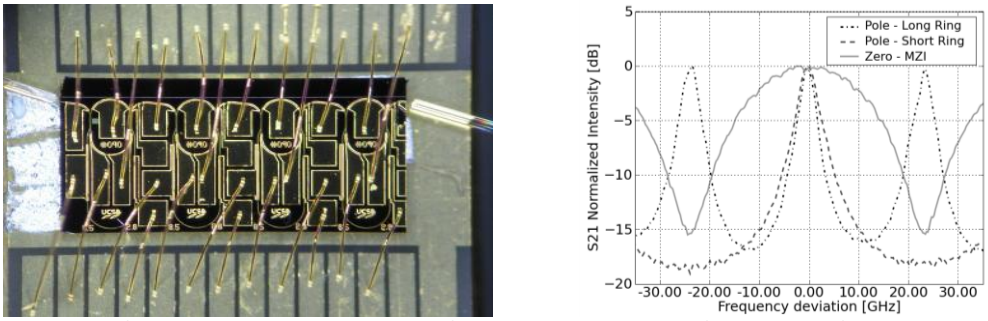

Fig.2 a) Optical image of wire bonded device with 4 cascaded filter stages. b) Experimental filter responses from a single stage filter, normalized in frequency and intensity.

3. Single filter stage

In order to construct higher order filter shapes that are useful to an application, careful consideration needs to be given to the design of the individual filter stages. The bandwidth and FSR of the overall filter is ultimately determined by the individual ring length and difference in MZI path lengths. For microwave photonic applications we are mainly interested in filters with bandwidths ~10 GHz and less, this translates into resonator lengths in the mm to cm range. In this work the two resonators lengths are 1,750 and 3,500 mm. Thus, having a relative difference in free spectral range (FSR) by a factor of two (45 and 22.5 GHz), the difference in MZI path length was designed to be 1,750 mm (45 GHz) as well. Experimental filter responses of these filter configurations are presented in figure 2. The single stage filter responses are tunable in both amplitude and frequency by tuning the SOA and PM currents. All experimental data was measured by fiber coupling broadband light from an amplified spontaneous emission (ASE) source into the chip and fiber coupling the output into an optical spectrum analyzer (OSA) with a 10 pm (1.25 GHz) resolution. All testing was performed continuous wave (CW) at room temperature.

4. Cascaded filter stages

When the single filter stages are cascaded, the transfer functions of the individual stages are multiplied together, Eq. (2). By controlling the individual filter stages separately, higher order filter shapes are easily synthesized. In order to synthesize a band-pass filter, two or more stages are programmed as poles and offset in frequency using the phase modulators. The bandwidth and ripple of the filter is set by the pole value (i.e. SOA gain) and the amount of

frequency offset between the stages. For a narrower bandwidth filter the long ring configuration is advantageous (SOA_2 reversed biased, G_2~0). In this configuration, by introducing zeros, the FSR of a band-pass filter response can effectively be doubled since the FSR of the zero is twice that of the resonator, figure 2. For wider bandwidth filters, the shorter ring configuration is utilized (SOA_1 reversed biased, G_1~0). The zero can now be used to enhance the pass-band rejection of the filter if placed half way between the pass-bands, see figure 2. In figure 3a) a 2nd order flat-top band-pass filter is experimentally demonstrated utilizing two cascaded filter stages in the short ring configuration, with the flattop achieved by injecting 0.65 mA into the PM of one stage. The filter has a 0.4 dB ripple, FWHM of 7.68 GHz and a maximum pass-band rejection of 25 dB. By adding one more filter stage, a 3rd order filter is demonstrated in figure 3b). Two poles are used to create a flat-top pass-band and a zero is placed half way in between the pass-bands to further enhance the extinction ratio. Again, the flat-top was created by injecting 0.31 mA into the PM of one stage while 5.1 mA was injected in the MZI stage PM to position the zero. The resulting filter has a 0.2 dB ripple and a FWHM of 5.5 GHz with 33 dB of maximum pass-band rejection. The reduced bandwidth for this filter is due to a slightly higher pole value (0.775 in figure 3b) versus 0.75 in figure 3a)) together with the smaller ripple.

The center frequency of the filter can be tuned continuously over one FSR using the phase modulators in each filter stage. This implies we can filter anywhere in the c-band as the filter response repeats every FSR over the gain bandwidth (~1530-1575 nm).

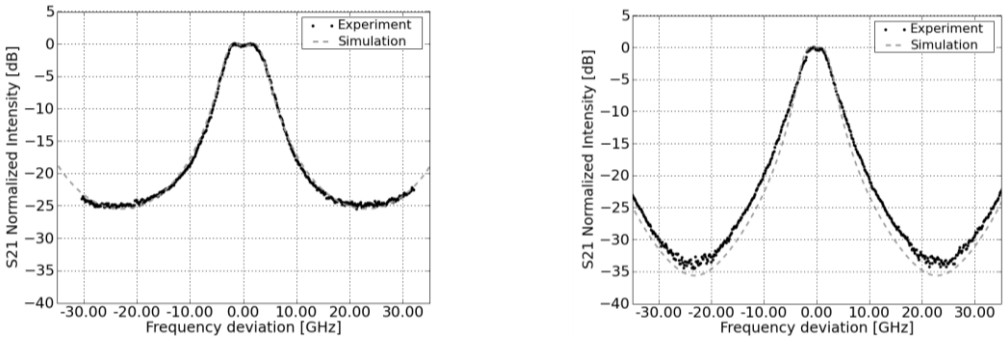

Fig.3 Experimentally measured filter responses from cascaded filter stages, simulations using Eq.(1) and (2) are superimposed. a) 2nd order flattop band-pass filter response and b) 3rd order filter - 2nd order flattop band-pass filter with a zero placed half way in between the pass-bands. Data was normalized in frequency and intensity.

5. Conclusions

A programmable photonic filter was constructed from monolithically cascaded filter stages. The single filter stages independently synthesize poles and zeros thus providing a versatile platform to create higher order filters. With increasing number of filter stages, extinction, filter roll-off, tunability in bandwidth etc., naturally improves. Band-pass filters with varied bandwidth and extinction were experimentally demonstrated utilizing two and three cascaded filter stages.

Acknowledgements

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Highly Programmable Optical Filters Integrated in InP-InGaAsP with Tunable Inter-Ring Coupling

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Abstract: A highly programmable optical filter architecture incorporating tunable inter-ring coupling is designed. The basic unit cell building block consisting of 3 coupled rings is fabricated in InP-InGaAsP, and bandpass filter results are presented.

OCIS codes: 230.5750 Resonators, 250.5300 Photonic integrated circuits

1. Introduction

The all-optical and real-time filtering of an optical signal promises to reduce the power consumption, latency, and cost of electrical filtering approaches. Much progress has been made recently in the theory of constructing such optical filters [1-3], and results have been shown for wavelength-division-multiplexing (WDM) channel selection and add-drop filtering, as well as RF signal filtering with limited tunability [4-7]. Specifically, RF channelizing filters require wide tunability in frequency, bandwidth, and extinction. We previously proposed a general integrated programmable filter lattice in the InP-InGaAsP material system consisting of a cascade of identical building blocks, or "unit cells" [8]. Work was also done on this design in the hybrid III-V/Si system [9]. By cascading unit cells, a general programmable filter architecture is possible. Here, we propose an improved unit cell design incorporating tunable couplers focused on the synthesis of flat-topped bandpass filters, which are tunable in frequency and bandwidth, and present preliminary results.

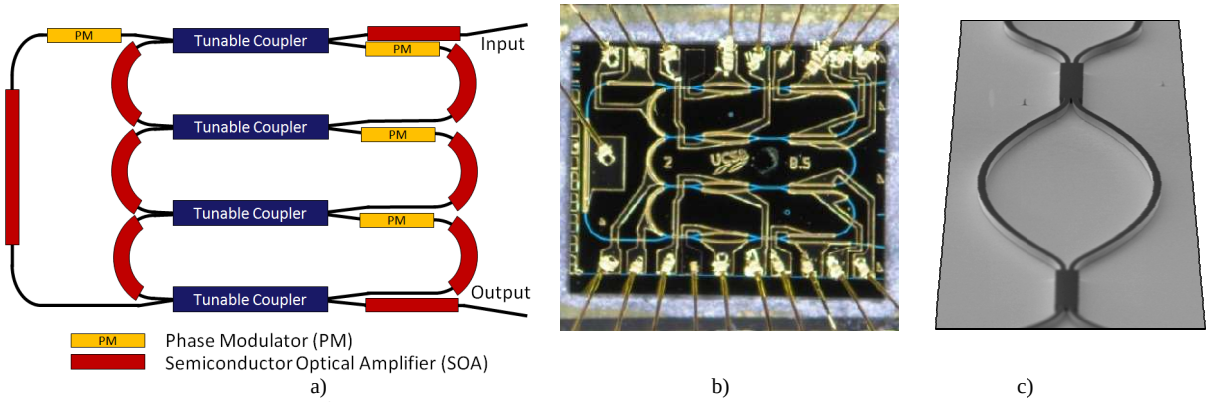


Fig. 1. a) Schematic representation of the unit cell showing SOAs, PMs, MZI Tunable Couplers, and input and output waveguides. b) Picture of fabricated and wire-bonded unit cell. c) Scanning electron microscope (SEM) image of an MZI tunable coupler without contacts.

2. Unit Cell Design and Operation

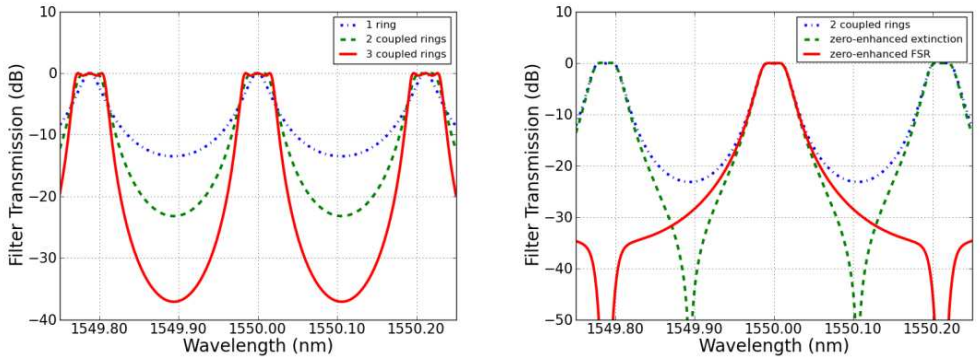
The unit cell (figure 1a) consists of three rings, each connected by a 2x2 Mach-Zehnder Interferometer (MZI) tunable coupler, and all bypassed by a secondary waveguide path. The symmetric MZI tunable coupler design consists of two 100μm long 2x2 restricted interference multi-mode-interference (MMI) couplers separated by waveguides of equal length. The full range of coupler tuning is accomplished through phase modulation of one of the 300μm long MZI waveguides, demonstrated in figure 3a. Tunable inter-ring coupling is crucial for filter bandwidth tunability. Semiconductor Optical Amplifiers (SOAs) and current injection Phase Modulators (PMs) within the unit cell provide tunability in amplitude and wavelength. Phase modulation occurs via free carrier absorption. The unit cell can be operated in two modes: the infinite-impulse-response (IIR) mode, utilizing the rings, or the finite-impulse-response (FIR) mode, utilizing the bypass waveguide.

As illustrated in figure 2a, the poles created by each of the three rings in the unit cell provide the ability to synthesize first order, second order coupled, second order uncoupled, and third order coupled IIR filters of varying bandwidth. The order of the filter is determined by the number of rings that are utilized, and the resulting response is periodically repeated every free spectral range (FSR). The FSR is determined by the ring lengths, which are in this case 3mm, giving an FSR of 0.22nm or 27.5 GHz. The IIR functionality of a unit cell is accomplished by applying a forward bias to the ring SOAs to achieve the desired extinction, and applying a forward bias to the ring PMs to tune

the poles to the desired wavelength. A reverse bias is applied to the feedback SOA in any ring that is not to be used, preventing the signal from making a round-trip. A reverse bias is also applied to the bypass waveguide in order to operate the unit cell strictly in the IIR mode. By tuning the center wavelength of the filter, and by utilizing the periodically repeated response, filter synthesis is achieved across the c-band. Filter responses were simulated with a general 4-port scattering matrix technique.

The bypass waveguide creates the ability to synthesize a finite-impulse-response (FIR) filter with a free-spectral-range (FSR) twice that of the IIR filters. Shown in figure 2, this zero filter shape can be utilized to eliminate neighboring IIR bandpass filters to essentially double the FSR of a synthesized bandpass filter, or, placed between bandpass filters, to enhance their extinction. The FIR functionality of a unit cell is accomplished by applying a forward bias to the SOA in the bypass waveguide and the SOAs in the forward path through the rings in order to equalize the output magnitudes of these two MZI arms. A forward bias is applied to the PMs in each arm to tune the wavelength location of the zero. A reverse bias is applied to the feedback SOAs in each of the rings in order to operate the unit cell strictly in the FIR mode.

Unit cells are cascaded together on-chip to facilitate synthesis of a wide range of filter shapes. IIR Bandpass filters can be cascaded in this way to increase extinction and side-band roll-off, while the FIR functionality can be utilized as mentioned above to modify IIR filters synthesized in previous unit cells.



a) b)

Fig. 2. a) Example simulation of 1 ring, 2 coupled rings, and 3 coupled rings with 15% inter-ring coupling. The poles in the 1-ring and 2-ring filters have pole values of 0.65. In the 3-ring filter, the outer rings have pole values of 0.65, and the inner ring has a pole value of 0.85. b) Simulation of 2 coupled rings with zeros placed on neighboring filter orders to effectively double the filter FSR and placed in-between filter orders to enhance extinction.

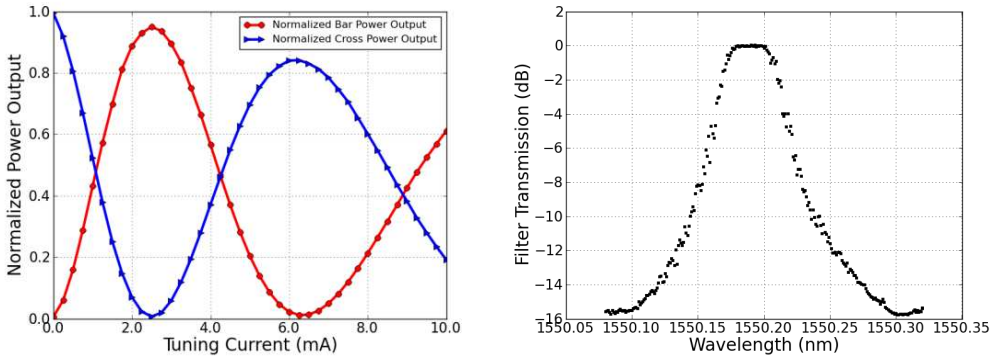
3. Fabrication

Individual unit cells were fabricated on an InP-InGaAsP offset quantum well platform, which provides a simple and robust method for active and passive material integration. The quantum wells, which are grown on top of a 1.3Q InGaAsP passive waveguide layer, are selectively wet-etched to create low-loss passive waveguide sections. A blanket InP regrowth acts as the p-cladding. In order to avoid high radiation bend loss, the waveguides are all deeply-etched structures created in an ICP dry etch. Details of this fabrication technique and results are outlined in [10]. A fabricated unit cell is shown in figure 1.

4. Results

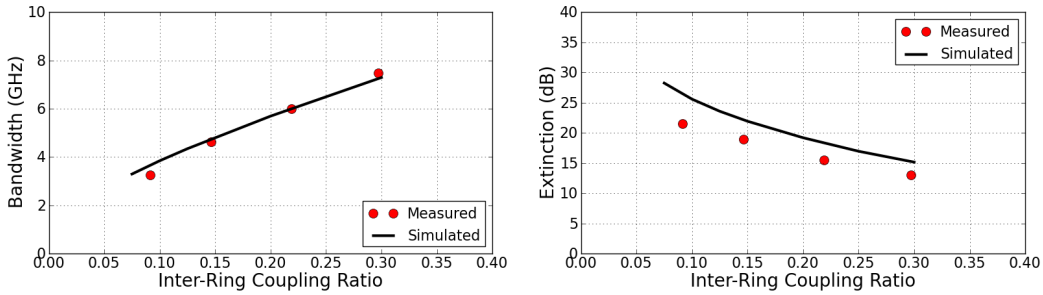
Successful operation of the MZI tunable couplers is crucial to the synthesis of coupled-pole filters. Figure 3a shows power splitting of a tunable coupler versus tuning current. Extinction of cross (inter-ring) coupling to under 1% of total output power was achieved at 2.5mA tuning current, and 2π phase tuning was achieved at 6.25mA. Insertion loss for this structure was estimated to be 1.5dB.

To confirm operation of the unit cell, 2nd order coupled pole bandpass filters of varying bandwidth were synthesized. Measurements were conducted with a locked-in tunable laser input and on-chip detection. The SOAs in the third ring were reverse biased and operated as detectors. The SOAs in the first two rings were forward biased and the PM in one ring was tuned until the poles from each ring were located at the same wavelength. The bandwidth of the filter was set by tuning the coupler between the two rings, which adjusts the inter-ring coupling ratio, and the filter pass-band ripple was optimized by adjusting the ring SOA gain. Figure 3 shows the filter transmission near 1550nm with 22% inter-ring coupling ratio providing 15.5dB extinction and a bandwidth of 0.048nm or 6.0GHz. As the coupling was decreased, the bandwidth decreased and extinction increased. Figure 4 shows the relationship between coupling value and filter bandwidth and extinction.



a) b)

Fig. 3. a) Measurement of an MZI tunable coupler splitting values vs. phase modulator tuning current. Values are normalized to total output power with zero tuning current. Additional insertion loss is estimated to be 1.5dB. Cross coupling values of less than 1% of total output power were obtained at a 2.4mA tuning current. b) Measured response of a 2nd order coupled ring bandpass filter with inter-ring coupling ratio set at 22% and gain optimized to obtain a flat-topped filter. A bandwidth of 0.048nm or 6.0GHz was obtained with an extinction of 15.5dB. The filter bandpass is normalized to 0dB.



a) b)

Fig. 4. Measured and simlulated a) bandwidth and b) extinction from 2nd order coupled ring filters vs. inter-ring coupling ratio with 1.5dB insertion loss assumed for the tunable couplers. The error in the extinction measurement is thought to be an artifact of the measurement.

5. Conclusions

A highly programmable filter architecture focused on RF channelizing filters was proposed. The basic building block, or unit cell, was designed and fabricated. Consisting of three coupled rings with tunable inter-ring coupling, the unit cell IIR response is tunable in bandwidth, frequency, and extinction. The unit cell is also capable of producing an FIR zero response in order to enhance FSR and extinction. MZI tunable couplers and unit cells were evaluated and preliminary results were obtained for 2nd order coupled ring bandpass filters.

Acknowledgements

This work was supported by DARPA through the PhASER project; a portion of the work was done in the UCSB nanofabrication facility, part of the NSF funded NNIN network.

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Monolithically Integrated Programmable Photonic Microwave Filter with Tunable Inter-Ring Coupling

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***Abstract*—The design and operation of a coupled-ring programmable photonic microwave filter architecture are described. RF measurements of coupled-ring bandpass filters tunable in bandwidth are presented.**

I. Introduction

As microwave filter applications become more demanding, the use of photonic approaches to improve latency, power consumption, and cost of implementation has gained increasing attention. A photonic filter subsystem within a microwave link promises to provide a low loss, high bandwidth, and highly tunable solution for applications such as reconfigurable microwave channelizers, programmable correlators, or dispersion compensation systems [1-2]. Furthermore, photonic integration offers to lower the cost, reduce the size, and improve the stability of such subsystems over bulk optics. Typically, photonic filters realized in bulk optics are limited to the incoherent regime, where the coherence time of the optical source is much smaller than the filter delay ($\tau_{coh} << T_{delay}$). Such systems inherently have all-positive filter coefficients, resulting in a variety of performance drawbacks [1,2]. The stability improvement of integrated systems is such that optically coherent filtering is achievable, eliminating the need for more complex approaches to attain negative filter coefficients.

Previously, we described the basic building block of a programmable microwave channelizing filter integrated in InP-InGaAsP termed a "unit cell" and demonstrated preliminary results [3,4]. Similar designs have been implemented in other material systems [5-7]. Each unit cell is capable of synthesizing up to 3rd order infinite impulse response (IIR) coupled-pole bandpass filters and first order finite impulse response (FIR) zeros. By cascading unit cells, filters with the extinction ratio and free spectral range (FSR) suitable for microwave channelizing filter applications can be obtained. Here, we review the design and operation of the unit cell and present new RF measurements of 2nd and 3rd order coupled ring filters tunable in bandwidth and frequency.

This work was supported by DARPA through the PhASER project; a portion of the work was done in the UCSB nanofabrication facility, part of the NSF funded NNIN network.

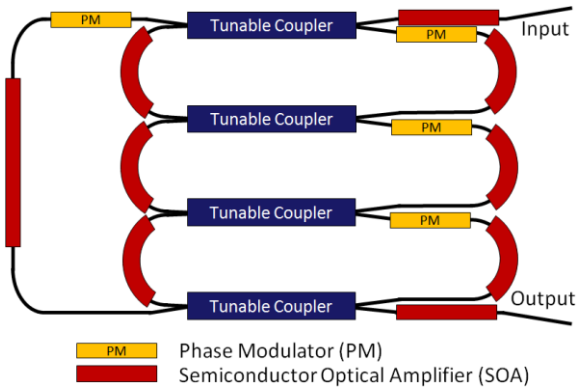


Figure 1. Schematic representation of the unit cell showing SOAs, PMs, MZI Tunable Couplers, and input and output waveguides.

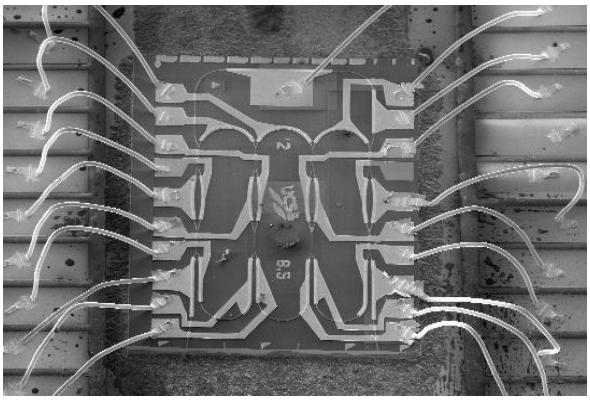


Figure 2. SEM image of a fabricated and wirebonded unit cell. The device measures 1.5 x 2.0mm. Input and output waveguides are at the bottom of the chip.

II. Design and Fabrication

A. Unit Cell Design

Shown in Fig. 1, the unit cell consists of three coupled rings and a bypass waveguide, linked by tunable couplers. An SEM image of a fabricated unit cell is shown in Fig. 2. The rings provide IIR functionality while the bypass waveguide in conjunction with the forward path through the rings supplies the FIR response. The unit cell is capable of synthesizing first order, second order coupled, second order uncoupled, and

third order coupled IIR filters. The tunable couplers consist of a symmetric Mach-Zehnder interferometer (MZI) with phase modulators (PMs) in each 300µm long waveguide. Coupling between waveguides is provided by 2x2 100µm restricted interference multi-mode interference (MMI) couplers [8]. The fabricated tunable couplers show low loss and good tunability with measured cross-coupling extinction down > 20dB from total output power [4]. The ability to attain low coupling values is crucial for synthesis of narrow bandwidth, high extinction ratio filters. Ring loop gain (i.e. pole magnitude) is set by the semiconductor optical amplifiers (SOAs), while the center frequency of each pole is set by the current-injection PMs. Filter bandwidth and pass-band ripple tunability is therefore achieved through adjustment of the coupling values, pole magnitude, and center frequency of each ring. Waveguide paths can be turned off by operating the SOAs in reverse-bias as detectors. This serves 2 purposes: to change the configuration of the unit cell, and to act as on-chip sensors for control feedback.

It is well known that in a coupled-ring system, first order resonances display a splitting caused by higher order poles. For example, in a 2-coupled-ring system, a third pole is created by the "figure 8" path. When the two coupled rings are tuned so that their independent resonances occur at the same wavelength, a splitting will occur (see [9] for a description of the transfer function of such systems). In this way, with the appropriate tuning of SOA gain, a flat-top bandpass filter response can be achieved. Alternatively, if the unit cell is operated in the uncoupled regime, a similar response can be created by tuning the individual pole locations until the desired flat-top filter is synthesized. Each of these configurations is simulated in Fig. 3. The higher order poles created by a coupled system increase roll-off and extinction compared to the uncoupled system.

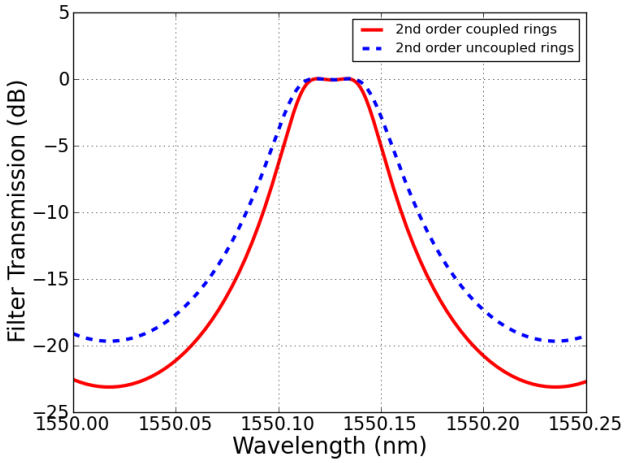


Figure 3. Simulation of 2nd order filters created with coupled and uncoupled rings. Both filters have pole magnitudes of 0.65. Inter-ring coupling of 15% creates the splitting for the coupled ring filter, while a filter displaying similar pass-band ripple with uncoupled rings is synthesized using a phase offset of 0.95 radians. Higher order poles from the coupled ring geometry provide an extra 3.5dB extinction.

The 3mm rings provide ~37ps of delay, resulting in a 27.3 GHz FSR. With reasonable pole magnitudes (0.8-0.9), this ring delay can produce flat-topped filters with bandwidths down to ~ 2GHz. The design can easily be scaled to narrower bandwidths by increasing the ring lengths. The extinction ratio of a filter can be enhanced by cascading multiple unit cells, each producing a copy of the filter, or by cascading IIR bandpass filters with FIR zeros placed in the stop-band. The FSR can be widened by using subsequent unit cells to synthesize FIR zeros, eliminating neighboring filter images [4].

B. Material Structure

The InP/InGaAsP material system provides the phase modulation and optical gain needed for a highly tunable filter architecture. Free-carrier absorption provides phase modulation through current injection, and quantum wells provide gain centered at 1550nm. While gain is crucial to reduce end-to-end loss in large systems, the dynamic range is an important consideration in system design. The system spurious free dynamic range (SFDR) is related to the linearity, and hence the saturation power of the SOAs [10]. To this end, the unit cells were fabricated on a high saturation power offset quantum well (OQW) platform. The quantum wells, which are grown on top of a 1.3Q InGaAsP passive waveguide layer, are selectively wet-etched to create low-loss passive waveguide sections. A blanket InP regrowth acts as the p-cladding. Gain and loss characteristics for this material design have been reported [11]. While offering a high 8.4dBm 1-dB saturation power, the OQW structure has reduced gain compared with a centered quantum well design. The unit cell design, however, requires much less than the 260dB/cm provided by this structure, and further improvements in saturation power can be obtained through the use of lower confinement factor designs [12].

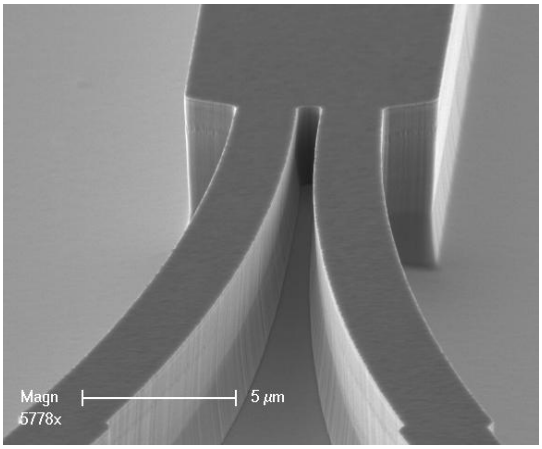


Figure 4. SEM image of the input waveguides to a deep-etched MMI coupler. The restricted interference MMI coupler is 8.5µm wide. Input waveguides are 1.8µm at the MMI coupler, tapering to 2.8µm. All waveguides are etched to a depth of approximately 5.0µm.

C. Fabrication

Fully functional unit cell devices were fabricated. All structures were defined via optical lithography. In order to avoid radiation loss from waveguide bends, high lateral optical confinement waveguides were created with an ICP-RIE "deep etch" process through the waveguide layer. The propagation loss and surface recombination current in these structures have been shown to be comparable to propagation loss and diffusion current in similar width surface ridge

structures. These results and more detail about the fabrication procedure are outlined in [11]. An SEM image of a fully fabricated and wirebonded device is shown in Fig. 2. Fig. 4 shows a close-up SEM image of an MMI coupler.

III. Results

A. Measurement Setup

In order to record filter responses in the RF domain, a single-sideband measurement was conducted using a heterodyne technique with a band-limited noise input. All measurements were conducted with continuous-wave inputs and at room temperature. A schematic representation of the measurement setup is shown in Fig. 5. A white-noise spectrum is generated with an Erbium doped amplified spontaneous emission (ASE) source, and amplified via an Erbium doped fiber amplifier (EDFA). The reflectance spectrum of a fiber grating is utilized to band-limit the input to 0.3nm (37.2GHz), with an out of band rejection of 30dB. The filter response of interest is placed within the band of the input signal, and after propagation through the integrated device the signal is combined with a local oscillator (LO) laser in a 3dB coupler and impinged upon a detector. The wavelength of the laser is chosen such that it falls at the edge of the signal band. In this way, only the lower sideband (in frequency) of the LO is occupied by the band-limited signal. With sufficient suppression, the resultant heterodyned signal measured in an electrical spectrum analyzer (ESA) is effectively single-sideband.

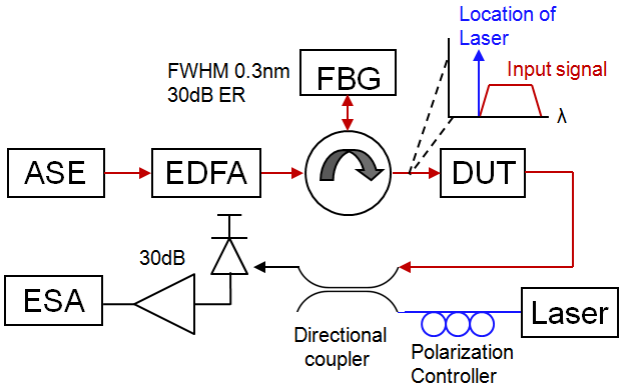
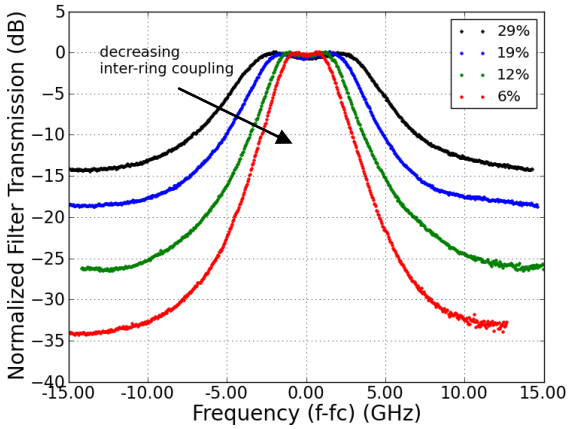


Figure 5. Schematic of the measurement setup.

B. Filter Results

IIR bandpass filters were measured on an ESA with high resolution (10MHz) using the technique outlined above. All data is normalized in frequency and amplitude; however, all filters are tunable across a full FSR – providing the ability to synthesize filters across the entire gain bandwidth and optical telecom band (~1530-1570nm). These filters were measured with a center frequency of about 25GHz. Within the filter pass-band, the signal typically sees on-chip gain of a few dB. Additional gain can be set by the inter-stage SOAs located before and after the unit cell. Maintaining zero to positive net gain would be crucial in a system with many cascaded unit cells where accumulated loss is damaging to the system dynamic range and SNR. Fig. 6 and 7 display 2nd and 3rd order coupled filter results, measured in the RF domain. Bandwidths vary from 3GHz to 7.4GHz and single-stage extinction is as high as 39.5dB. Passband ripple is on the order of 0.5dB. By cascading two stages of the narrowest 3rd order IIR bandpass filter, extinction would be increased to 79dB. If an FIR zero is cascaded with an IIR bandpass filter, the FSR would effectively be doubled to 54.6GHz.



6. Measured 2nd order coupled ring filters for various inter-ring coupling ratios. Lower coupling ratios reduce the pole splitting and result in a filter with lower bandwidth and higher extinction.

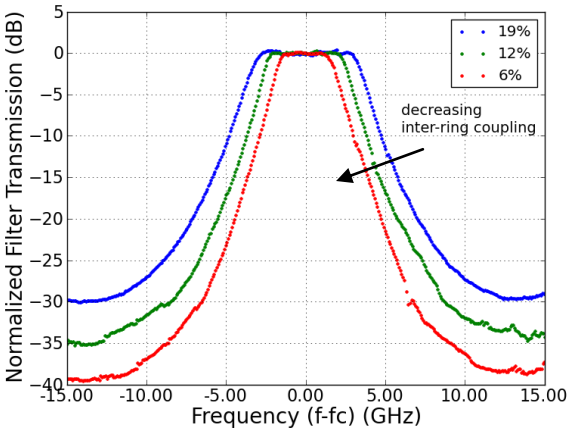


Figure 7. Measured 3rd order coupled ring filters for various inter-ring coupling ratios. For a given inter-ring coupling value, 3rd order filters have wider bandwidth, but show higher extinction and improved rolloff.

IV. Conclusion

RF measurements of programmable microwave photonic filters were presented. 2nd and 3rd order coupled ring filters were synthesized with varying inter-ring coupling to achieve tunable bandwidth. With the ability to place these filters across the full optical telecom band, the presented filter architecture is a viable building block for applications such as tunable microwave channelizing. More elaborate filter shapes, improved FSR, and increased extinction can be attained by cascading independently tunable unit cells.

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A Monolithic Programmable Optical Filter for RF-Signal Processing

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***Abstract*—A monolithic programmable optical filter suitable for dynamic pre-filtering of wide bandwidth RF signal-bands is presented. Bandpass filters have a passband tunable in bandwidth (3-14GHz) and center frequency (0-40GHz). Cascaded filter sections have stopband rejection exceeding 35dB.**

I. INTRODUCTION

All-optical signal processing has the capabilities to reduce latency, power consumption, cost and size, and overcome the inherent bandwidth limitations of its electronic counterparts [1,2]. By rapidly pre-filtering wide bandwidth analog signals in the optical domain the demand on analog-to-digital converstion (ADC) and subsequent digital signal processing (DSP) can be significantly relieved. Such a filter should ideally be highly versatile and synthesize both notch- and bandpass type filters so RF signal bands or signatures quickly can be rejected or isolated for more detailed investigation. It is also desirable that the filter passband be tunable in both bandwidth and center frequency to accommodate varying signal widths and locations in the RF domain, as well as enable tracking and sweeping abilities in the frequency domain, properties that are crucial for electronic warfare (EW) systems. A lattice type filter structure utilizing both Mach-Zehnder interferometers and ring resonators together with optical phase and amplitude control can provide these desired filter characteristics [3]. We have previously demonstrated the basic building block or unit cell of such a lattice filter, integrated in the InGaAsP material system [4]. Similar unit cells have in parallel been suggested and demonstrated on other integration platforms: gain-less silicon-on-insulator (SOI) [5,6] and SOI-IIIV hybrid [7]. More recently, we verified the ability to monolithically cascade these lattice cells to create higher order filters [8]. In this paper, we demonstrate novel functionality of such cascaded lattice filters including flat-topped bandpass filters with passbands tunable in both bandwidth and center frequency.

This work was supported by DARPA through the PhASER project; a portion of the work was done in the UCSB nanofabrication facility, part of the NSF funded NNIN network.

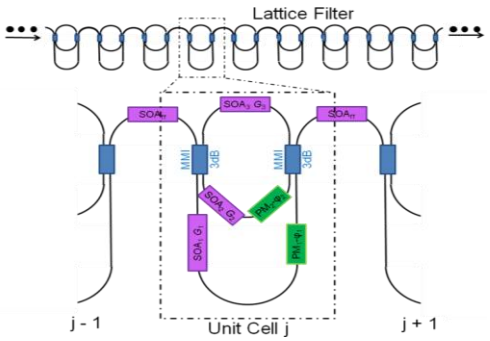

Figure 1. Schematic of the programmable lattice filter and the single unit cell; functional components, SOAs, Phase modulators and couplers have been highlighted.

II. FILTER DESIGN

A. Single Unit Cell

The fundamental filter structure is depicted in Figure 1. *N* cascaded identical filter stages or unit cells make up a one dimensional lattice structure. Every unit cell is designed to be able to synthesize either a pole or a zero. This is achieved by an asymmetrical Mach-Zendher interferometer (MZI) with a feedback path connecting the output to the input, thus creating two different resonator paths, Figure 1. Hence, the complete unit cell response consists of two poles and one zero. However, in favor of stability and control, only one pole or one zero per unit cell is utilized at any one time. The individual pole or zero is isolated by utilizing active gain/absorption elements to shut off different waveguide paths. If the top path of the unit cell is turned off, a single zero results through the remaining MZI path. Alternatively, if one of the MZI paths is shut off, one of the two poles is isolated. By designing the lengths of the different waveguide paths, desired free-spectral-range (FSR) and filter bandwidths are achieved. In this work, the two resonators have a length of 1,750 or 3,500 mm, corresponding to time delays of 21 and 42 ps, or FSRs of 48 and 24 GHz respectively. The MZI was designed with a path difference of 21 ps or FSR of 48 GHz. The pole and zero magnitudes are controlled by balancing the MZI arms or providing resonator gain respectively, while the phase (frequency) is controlled by the phase modulators located in both paths of the MZI.

B. Lattice Filter Operation

The single unit cells are cascaded in an uncoupled fashion with a single waveguide connecting the cells; there is no feedback between the unit cells and the individual unit cell transfer functions are multiplied in a linear fashion. This naturally aids in stability and control of these lattice filter structures as well as simplifying the filter synthesis since the unit cells can be controlled individually. Higher order filters are constructed by programming the unit cells with desired pole or zero magnitudes and phases. Bandpass filters are constructed by utilizing two or more poles; the passband bandwidth can be varied by changing the pole magnitude and adjusting the pole location to maintain a flat passband. Since the unit cell design incorporates two poles with different FSRs, bandpass filters with inherently wider or narrower FSR and bandwidths can be utilized for different bandwidth applications. Zeros can be added to construct elliptical bandpass designs with enhanced filter extinction and roll-off. By using only zeros, notch filters are synthesized. In the current design the FSR of the zero is twice that of the longer ring, thus the zero can also be used to enhance the FSR of the narrower bandwidth bandpass filter by canceling out the neighboring filter order on either side.

In the current design, the device does not include any on-chip modulator, laser source, or detectors. However, using the InGaAsP integration platform, these components could all be integrated together with the filter if an electrical RF-in and or out was desired. However, for many applications, the RF might already be on an optical carrier, where the filter would work as a subsystem in the RF link, e.g. in remote antenna fiber links.

C. Integration Platform

For monolithic integration of the filter structure we utilize the InP-InGaAsP material system. This has the advantage of on-chip gain through semiconductor amplifiers (SOAs) and effective and quick phase control using current injected phase modulators. Of course, utilizing on-chip gain, the impact on the spur-free dynamic range (SFDR) through saturation effects in the SOA must be considered. It can be shown that the ratio of intermodulation distortion to signal power is proportional to the inverse of the squared SOA saturation power [9]. Thus the SFDR is proportional to the squared saturation power, which in turn is proportional to the quantum well confinement factor. For this reason, we utilize an offset quantum well (OQW) integration platform which has a lower confinement factor compared to centered multi quantum well (MQW) structures. We measured the optical 3dB-saturation power of our SOAs to be 11.4 dBm; this should be compared to 15 dBm which has been calculated to have an SFDR number in the range 105-115 $dB/Hz^{2/3}$ (lower end for low frequencies) for a commercial InGaAsP QW SOA [10]. We do have the ability to push the saturation power higher by further reducing the confinement factor, 20 dBm having previously been demonstrated [11]. This suggests SFDR numbers as high as 115-125 $dB/Hz^{2/3}$, which is sufficient for most radar applications. The re-programming and tuning time of the filter is ultimately limited by the response time of the gain and phase controllers, which here are governed by the carrier lifetime suggesting extremely fast tuning speeds in the nano-second range [12]. This is crucial for fast tracking and sweeping in the RF domain which is important to many applications.

In order to avoid radiation loss from waveguide bends and keep the fabrication complexity to a minimum, deeply etched waveguides was used for the entire device. For coupling, 3dB restrictive multi-mode-interference (MMI) couplers with a measured total insertion loss of ~1.0 dB/coupler were used everywhere. More details on the fabrication and integration platform have been reported elsewhere [13]. Figure 2 shows a fabricated lattice filter with four cascaded unit cells that have been wire-bonded to a carrier; the device size measures 1.5 x 3.5 mm.

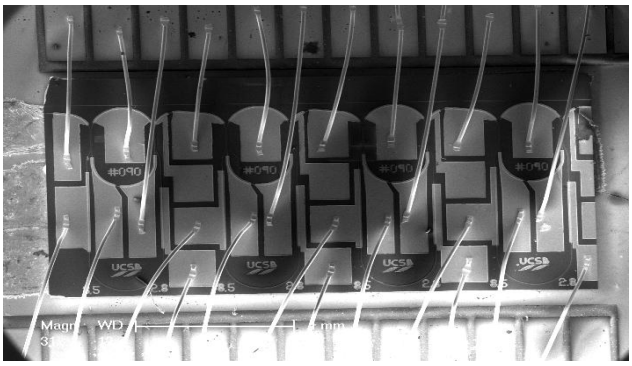

Figure 2. Scanning electron microscope image of a fabricated device containing four unit cells; device has been wirebonded to a carrier.

III. Experiment and Discussion

A. Experiment

In this work we investigated a lattice filter structure consisting of a four cascaded unit cells, Figure 2. In order to demonstrate the filtering function of our device, we input a band limited noise spectrum into the device and measure the output in high resolution (10 MHz), utilizing a heterodyne detection scheme. The band limited noise spectrum simulates a wide bandwidth single sideband RF-signal band that has been carrier suppressed. A schematic of the measurement is shown in Figure 3. The noise spectrum is generated by an amplified spontaneous emission (ASE) source and is amplified by erbium doped fiber amplifiers (EDFAs) and sent through a circulator connected to a fiber grating (FBG) that has a 44 GHz wide reflection bandwidth. The filtered signal is down converted using a tunable laser placed just to the side of the initial noise spectrum at 1553.152nm, inset Figure 3. A 40 GHz photodiode (PD), with a 38 GHz broadband amplifier and a 50 GHz electrum spectrum analyzer (ESA) is used to image the device output in the electrical domain. All data was normalized to the throughput (w/o device) in order to eliminate ripples in the FBG spectrum. The added receiver noise was subtracted from the measured data. An optical spectrum analyzer (OSA) was used in parallel to monitor the optical domain; however, the OSA does not have the resolution necessary to truthfully resolve the filter shapes. All measurements were done continuous wave (CW) in room-temperature.

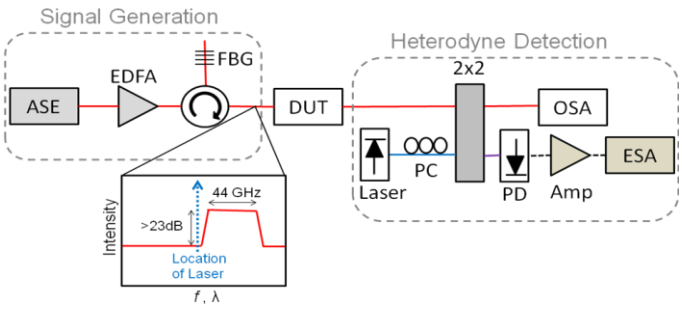

Figure 3. Schematic of experimental setup. Inset spectrum shows the generated signal and where the local oscillator laser is located in the heterodyne detection.

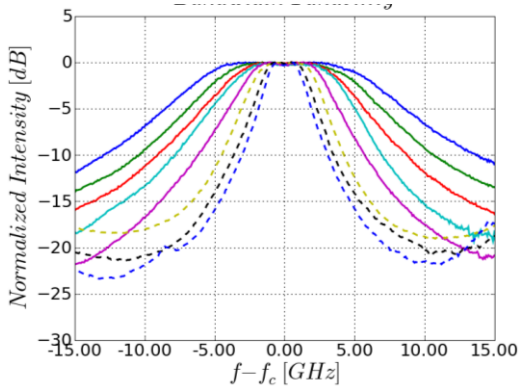

Figure 4. 2nd order bandpass filter with variable passband bandwidth. Solid and dashed lines indiate the use of the shorter or longer resonator respectivly.

B. *Results and Discussion*

Utilizing two out of four unit cells, a variable bandwidth 2nd order bandpass filter is demonstrated in Figure 4. For easy comparison, the filters have been normalized in frequency from the 20-25 GHz range down to zero. The bandwidth is varied by changing the pole magnitudes from 0.55 to 0.75 (found by fitting data to simulations) while adjusting the phase difference between the poles to maintain the flat passband. The ripple is kept less then 0.5dB for all filters. The tuning is completely continuous but illustrated with a few discrete steps for clarity. Since the pole magnitudes are varied, the filter extinction and roll-off also change accordingly. Thus, it becomes necessary to keep a lower bound on the pole magnitude to maintain sufficient filtering efficiency. The shorter resonator configuration with a FSR of 48 GHz is here utilized for filtering in the 5-14 GHz bandwidth regime (solid lines in figure 4), while the longer resonators with FSR of 24 GHz are utilized for 3-5 GHz (dashed lines in Figure 4). For many RF-applications, filter bandwidths even narrower than the 3 GHz demonstrated here are desired. This requires longer resonator and MZI delays. However, the principle of the demonstrated filter operation does not change. In this current design we have considerable excess gain, so by keeping the same SOA gain but moving to a lower loss InGaAsP integration platform (basically reducing p-cladding overlap), e.g. [14], 10 cm resonator delays with 100 MHz filter bandwidths are feasible. The shorter resonator delays will however still be crucial to achieve a broad operation range (governed by the filter FSR) by removing the narrowly spaced neighboring filter orders of the longer delays.

The second important functionality beside a variable filter bandwidth is the ability to tune the center frequency of the passband. This is demonstrated in Figure 5 using a 2nd order bandpass filter tuned from 9 to 37 GHz. The tuning can extend further but above 40 GHz the receiver noise becomes too large. In fact, all the poles and zeros have more then 2π of phase tuning, effectively meaning that the filter can work anywhere in the gain bandwidth (5 THz wide). Thus, the filter operation range is limited by the FSR, here 48 GHz. The small peaks showing in the stopband are not part of the filter but rather an artifact of the measurement. These peaks are caused by the laser beating with the neighboring filter order to the left of the laser since the FBG extinction ratio is limited; see inset Figure 3. Note that the added center frequencies of the filter passband and the peak in the stopband always equal the filter FSR, as would be expected for this phenomena.

For improved extinction and roll-off, higher order filters can be utilized. Figure 6 shows the improvement in using four instead of two unit cells. With four poles, a 2nd order bandpass filter was cascaded twice, enhancing filter roll off and stopband rejection to almost 40 dB. Again, the limitation of the measurement setup is evident; at high extinctions many low intensity peaks generated by the measurement are revealed in the stopband, e.g. the peak at -12 GHz (at 10 GHz before frequency normalization) is caused by an internal interference in the tunable laser.

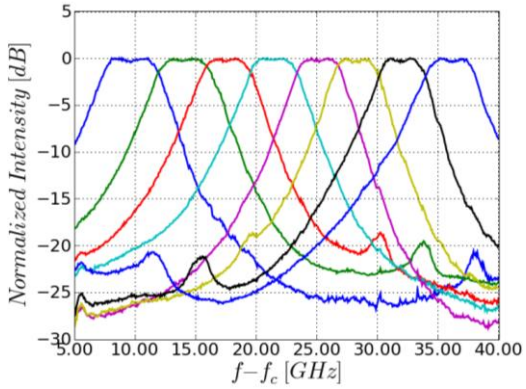

Figure 5. Frequency tunability of a 2nd order bandpass filter.

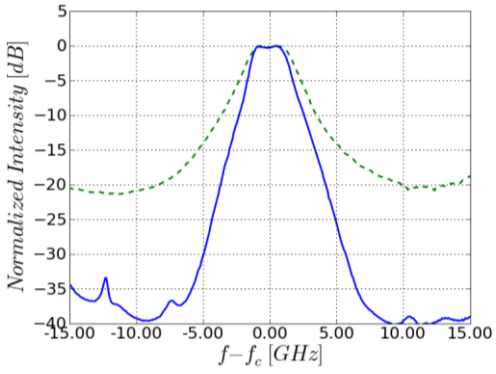

Figure 6. Comparison of bandpass filters constructed from 2 poles (dashed) and 4 poles (solid).

For the four unit cell long lattice filter investigated here, the end-to-end loss (not including fiber coupling losses) in the passband is generally zero or has slight gain. This suggests that the number of lattice cells could be increased further. For example, going of Figure 6, a lattice with only 8 unit cells would produce a stopband rejection of ~75 dB. The only limitation of longer lattices seems to lie in practical interfacing and control, since additional bias parameters are introduced with added unit cells. Thus it would be desirable to interface the lattice filter with a field-programmable gate array (FPGA) controller to ease the filter synthesis in the future.

IV. CONCLUSION

We have presented a programmable optical filter constructed as a lattice of identical unit cells. The uncoupled unit cells give rise to independently programmable zeros and poles which can freely be placed in the complex plane. We have demonstrated a 2^{nd} order bandpass filter tunable in both bandwidth and center frequency, and shown that longer lattices can be used to enhance the filter roll-off and stopband rejection. This kind of filter would be suitable for signal processing of wide bandwidths RF signal-bands in the optical domain.

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I. Photonic Integrated Circuits

D. Optical-Phase-Locked-Loop, Mode Locking, and Injection Locking

An Optical Phase-Locked Loop Photonic Integrated Circuit

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***Abstract*—We present the design, fabrication, and results from the first monolithically integrated optical phase-locked loop (OPLL) photonic integrated circuit (PIC) suitable for a variety of homodyne and offset phase locking applications. This InP-based PIC contains two sampled-grating distributed reflector (SG-DBR) lasers, semiconductor optical amplifiers (SOAs), phase modulators, balanced photodetectors, and multimode interference (MMI)-couplers and splitters. The SG-DBR lasers have more than 5 THz of frequency tuning range and can generate a coherent beat for a wide spectrum of frequencies. In addition, the SG-DBR lasers have large tuning sensitivities and do not exhibit any phase inversion over the frequency modulation bandwidths making them ideal for use as current controlled oscillators in feedback loops. These SG-DBR lasers have wide linewidths and require high feedback loop bandwidths in order to be used in OPLLs. This is made possible using photonic integration which provides low cost, easy to package compact loops with low feedback latencies. In this paper, we present two experiments to demonstrate proof-of-concept operation of the OPLL-PIC: homodyne locking and offset locking of the SG-DBR lasers.**

***Index Terms*—Coherent optical communications, integrated optoelectronics, optical phase-locked loops (OPLLs), tunable semiconductor lasers.**

I. Introduction

EVER SINCE the first demonstration of an optical phase-locked loop (OPLL) [1], a significant research effort has been invested in developing the system for a wide range of applications, as shown in [2]–[4] and references therein. In optical communications, the OPLL allows synchronous coherent receivers where mixing the received signal with a high-power local-oscillator (LO) laser provides high sensitivity and out-of-band noise suppression [5]–[7]. For carrier-suppressed modulation schemes, a Costa's loop can be used [8]. OPLLs are commonly used for optical clock recovery in digital telecommunication systems [9]. They have also been developed for generation of stable channel offsets in dense wavelength-division multiplexed (DWDM) systems [10]. In microwave photonics, an OPLL can form a microwave single-sideband optical source [2] with the potential for endless microwave phase adjustment. This is an attractive property for implementation of a phased array microwave system. OPLLs also find applications in free-space optical systems such as LIDAR systems, where they allow coherent combination of several coherent optical sources [3], potentially to form large swept optical phase arrays.

Compared to fiber lasers and solid state lasers with narrow linewidths, semiconductor lasers are generally favored because of their small sizes, low costs, and high efficiencies [2], [11]. In addition, the phase and frequency tuning of a semiconductor laser, which is necessary for the laser to be used in the negative feedback loop of an OPLL, is easily achieved by current injection. So far, the central difficulty in realizing OPLLs using semiconductor lasers has been the strict relation between laser phase noise and feedback loop bandwidth. The wide linewidths observed in semiconductor lasers, typically in the megahertz range, require sufficiently wide loop bandwidths, i.e., small loop delays. In the past, this has been addressed by using low-linewidth external cavity lasers that allow longer feedback loop delays [12], [13], or by construction of compact OPLLs using miniaturized bulk optical components to meet the delay restrictions arising from the use of standard semiconductor lasers [2], [14]. Other efforts include relaxing this restriction by combining an OPLL with optical injection locking, thereby gaining the wide locking bandwidth of optical injection, while a slow phase-locked loop with a long delay allows long-term stability [15].

Recent progress in device design and fabrication has enabled distributed-feedback (DFB) lasers to have sub-megahertz linewidths, without external cavity linewidth reduction schemes, [3], [8], [14], [16]–[18]. Consequently, the delay in fiber-based OPLLs is not the bandwidth limiting factor in locking the standard DFB lasers. Rather, the loop bandwidth is limited by the phase reversal in the FM response, which is characteristic for DFB lasers and occurs at frequencies between 0.1 and 10 MHz [2], [16], [19], [21], as explained in Section III. While this lower loop bandwidth is sufficient for locking of DFB lasers even in fiber-based OPLLs, it is still a limiting factor in achieving high-performance OPLLs with very small phase errors because the benefits of locking are constrained to the narrow bandwidth determined by the phase reversal [2], [11], [16]. In the applications such as the coherent beam combining [16], where several lasers are locked, the cumulative phase error increases with the number of lasers, and it is important to minimize it.

In order to overcome the phase-inversion-limited FM bandwidth of standard narrow-linewidth DFB lasers, new types

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of semiconductor lasers have been developed for their use in OPLLs. Complex-coupled DFB lasers have been shown to have flat FM responses without phase inversion between 10 kHz and over 20 GHz [22]. The requirement for precise control of the lasers' bias current and the fact that the FM-response uniformity and sensitivity depend on the output power level are disadvantageous for OPLL applications [19]. Multi-section tunable semiconductor lasers have been very popular in the past in OPLLs [2], [17], [19], [23], [25]. Here, the phase tuning section is separated from the gain section and the Bragg section, which minimizes the thermal tuning issues responsible for the phase inversion in DFB lasers.

Integration of an OPLL is considered to be beneficial for a wide range of applications by researchers in the field [2], [3], [10], [13], [14], [17], [25]. Monolithic integration of the optical components in an OPLL can improve its robustness to temperature and environmental variations, which can be detrimental in fiber-based systems [16]. These variations have smaller cumulative effects on light when it propagates through a robust and compact, monolithically integrated optical components. In addition, the whole photonics integrated circuit (PIC) that includes the semiconductor lasers and the optical components of the OPLL can be maintained at a constant temperature by the same temperature controller. Typical integrated optical waveguides and devices preserve the polarization of light, so that no polarization alignment between the components is necessary in order to maximize the interference between the integrated lasers in the applications where multiple lasers are being locked. Furthermore, integrated waveguides are immune to long term polarization drifts. Also, compared to the miniature bulk optics OPLLs [2], no alignment between the components needs to be performed. The compactness and ease of packaging of integrated OPLLs can improve their cost effectiveness. This is especially true for the applications where multiple lasers are locked together [3], [11], [26].

Monolithic integration of multi-section lasers is strongly motivated by two factors. First, in multi-section lasers the passive phase and Bragg sections are already integrated with the active gain section. In order to achieve this, a regrowth or some other type of post-growth bandgap engineering technique, such as quantum-well intermixing, is necessary [27], thereby facilitating integration of additional active devices, such as semiconductor optical amplifiers (SOAs) and photodetectors, and passive devices, such as modulators and multimode interference (MMI) couplers and splitters. Second, compared to DFB lasers, multi-section lasers have larger linewidths, in the several-megahertz range. Although, a state-of-the-art OPLL performance has been achieved with multi-section lasers and miniature bulk optics [2], monolithic integration can offer further performance improvement by reduction of the loop delay. Monolithic integration can also enable a variety of other types of wide-linewidth lasers to be used in OPLL applications, such as widely-tunable sampled grating distributed feedback (SG-DBR) lasers.

So far, monolithic integration has focused on the receivers and on the electronic components rather than the optical components of an OPLL [10], [28], [29]. In this paper, we demonstrate for the first time, an OPLL photonic integrated circuit (OPLL-PIC) in which all required optical components are monolithically integrated, including: lasers, passive optical waveguides, MMI couplers/splitters, high-speed photodetectors, and high-speed optical phase modulators. Moreover, the OPLL-PIC uses widely-tunable SG-DBR lasers that have a wavelength tuning range greater than 5 THz [30]. This is a key feature for several applications. First, it allows the development of homodyne coherent receivers in the form of Costa's loop, with an optical bandwidth exceeding the entire C-band. The relative simplicity of the Costa's loop also allows scaling to high data rates, exceeding 100 Gbps. Second, an OPLL with 5 THz wavelength tuning range can be used for coherent beam forming for sub-millimeter resolution LIDAR applications. Third, together with a THz photodetector and electronics, it allows optical heterodyne signal generation with a DC to 5 THz frequency range. Applying optical phase or amplitude modulation to one optical line can be used to generate a coherent phase or amplitude modulated THz signal. The rest of the paper is organized as follows: the design and fabrication of the OPLL-PIC is described in Section II, the SG-DBR laser performance is described in Section III, proof-of-concept homodyne and offset locking OPLL demonstrations are presented in Section IV, and the conclusion remarks are presented in Section V.

II. Optical Phase-Locked Loop Photonic Integrated Circuit

A. OPLL Basics

An OPLL has both parallels and fundamental differences when compared to its RF equivalents. In a microwave loop, it is a voltage-controlled oscillator that typically tracks the input signal. In an OPLL, wavelength tuning of a laser takes this role, achieved typically by current injection [3]. An RF phase-locked loop (PLL) can be built using spectrally pure oscillators, which allow stable operation in a narrowband loop to enable filtering, or it can be built using compact integrated circuits to have a substantial fractional loop bandwidth compared to the carrier frequency, allowing agile tracking of a frequency modulated signal. In contrast, an OPLL is built using less compact optical components, leading to a smaller loop bandwidth, and with a carrier frequency of $\sim$ 193 THz (1550 nm), which results in low loop bandwidth to carrier frequency ratio. As a result, acquiring locking is less straightforward in an OPLL as the slave laser must be tuned to the master laser wavelength with high accuracy.

Fig. 1 shows a simple schematic of the OPLL architecture demonstrated in this paper. Two widely tunable SG-DBR lasers are monolithically integrated on a single InP substrate along with all of the other optical components needed to form the OPLL. One laser takes the role of a master laser, while the other takes the role of a slave laser. The outputs of the two lasers are first combined using a 2×2 optical coupler. The combined beat signal is then amplitude modulated for offset-locking using an integrated optical modulator and envelope- detected using an integrated photodetector. The current output from the photode-

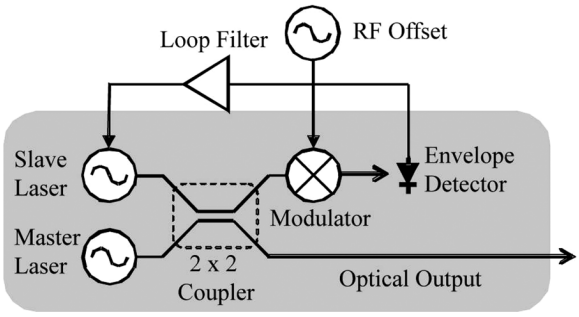


Fig. 1. Schematic of an OPLL heterodyne offset locking experiment.

tector is filtered and fed back into the salve laser. The resulting slave laser frequency tuning is then given by

$$\frac{d\varphi_s}{dt} = h_m * h_d * f_{\mathrm{LF}} * h_s * (2R\sqrt{mP_mP_s}\sin(\varphi_m - \varphi_s)) \quad (1)$$

where the terms in the convolution: $h_m, h_d, f_{\mathrm{LF}}$, and h_s are the impulse responses of modulator, detector, loop filter, and slave laser frequency tuning, respectively. R is the detector responsivity, P_m and P_s are the master and slave laser powers incident on the photodetector, and φ_m and φ_s are the phases of the master and slave laser respectively. Also, m is the relative power of the modulation sidebands used for offset locking after optical modulation. For zero offset locking, i.e., homodyne locking, no optical modulation needs to be applied and $m = 1$. Assuming locked condition and small phase error $(\varphi_m \approx \varphi_s)$, the equation can be linearized $(\sin(x) \approx x)$ and the Laplace transform applied

$$\begin{aligned}\varphi_s &= \frac{H_m H_d F_{\mathrm{LF}} H_s 2R\sqrt{mP_mP_s}}{s}(\varphi_m - \varphi_s) \\ &= G(s)(\varphi_m - \varphi_s). \end{aligned} \quad (2)$$

Here, $G(s)$ is the open-loop gain function from which stability and operation of the loop can be evaluated. It is interesting to note that offset locking of our OPLL could also be achieved without the on-chip modulation of the two laser outputs, but rather by mixing the photodetector current with an external RF reference. In our method, the generated sidebands carry only a fraction of power of the laser outputs and thus produce small interference extinction ratios when mixed together, incurring additional noise penalty. The advantage is that no RF electronics is required.

B. OPLL-PIC Design

Fig. 2(a) and (b) show schematics of our two different OPLL-PIC designs. The design shown in Fig. 2(a) is intended for locking of an on-chip tunable laser to an external laser, while the design shown in Fig. 2(b) is intended for offset locking of two on-chip tunable lasers. Each OPLL-PIC design comprises of three sections that are labeled in Fig. 2(a) and (b) as: Laser Section, Middle Section, and Output Section. We choose the SG-DBR laser because of its wide tuning range, large frequency-modulation (FM) tuning sensitivity,

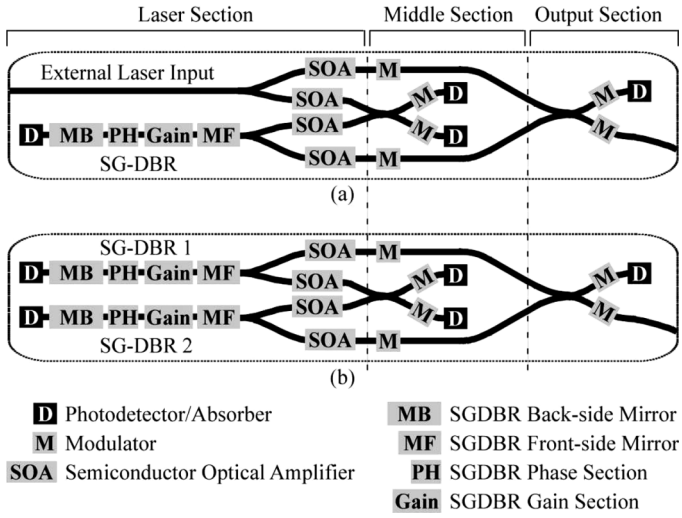


Fig. 2. Schematic of (a) an OPLL-PIC for locking to an external laser and (b) an OPLL-PIC for offset locking of two on-chip lasers.

and absence of phase inversion in the frequency response, as explained in Section III.

In Fig. 2(a) and (b), we explicitly show the constituent components of the SG-DBR laser: front-side mirror (MF), gain section, phase section (PH), back-side mirror (MB), and back-side absorber/photodetector (D). Light from each laser is first split using 1×2 MMIs into two half-power components. One of the two half-power components from each laser is directed into a 2×2 MMI, which is a part of the feedback loop, and which is located in the Middle Section of the OPLL-PIC. The remaining half-power component from each laser is directed into a 2×2 MMI in the Output Section of the OPLL-PIC. Each of the four half-power optical paths has an SOA to adjust the optical power in each path. Each optical path at the output of the 2×2 MMI coupler in the Middle Section of the OPLL-PIC contains a phase modulator (M), followed by a photodetector (D), which can be used in a balanced receiver configuration. Similarly, each optical path at the two outputs of the 2×2 MMI in the Output Section of the OPLL-PIC contains a phase modulator. One of these two output waveguides ends upon a photodetector that can be used for electrical-domain monitoring of the interference resulting from the beating of the two lasers. The other output waveguide extends to the edge of the OPLL-PIC to enable coupling into an optical fiber and can be used for optical-domain beat monitoring. The 2×2 MMI in the Output Section has phase modulators on its input waveguides as well, which can be used for additional phase control.

Fig. 3(a) shows a scanning electron microscope (SEM) image of an OPLL-PIC based on the schematic shown in Fig. 2(b), which enables offset locking, after it has been mounted on a carrier and wire-bonded. The distinct OPLL-PIC sections mentioned above are marked for identification. The OPLL-PIC is 6.6 mm long and 0.45 mm wide.

The Laser Section of the OPLL-PIC is shown in greater detail in Fig. 3(b). The abbreviations used in labeling the various components of this section are explained in Fig. 2. This section

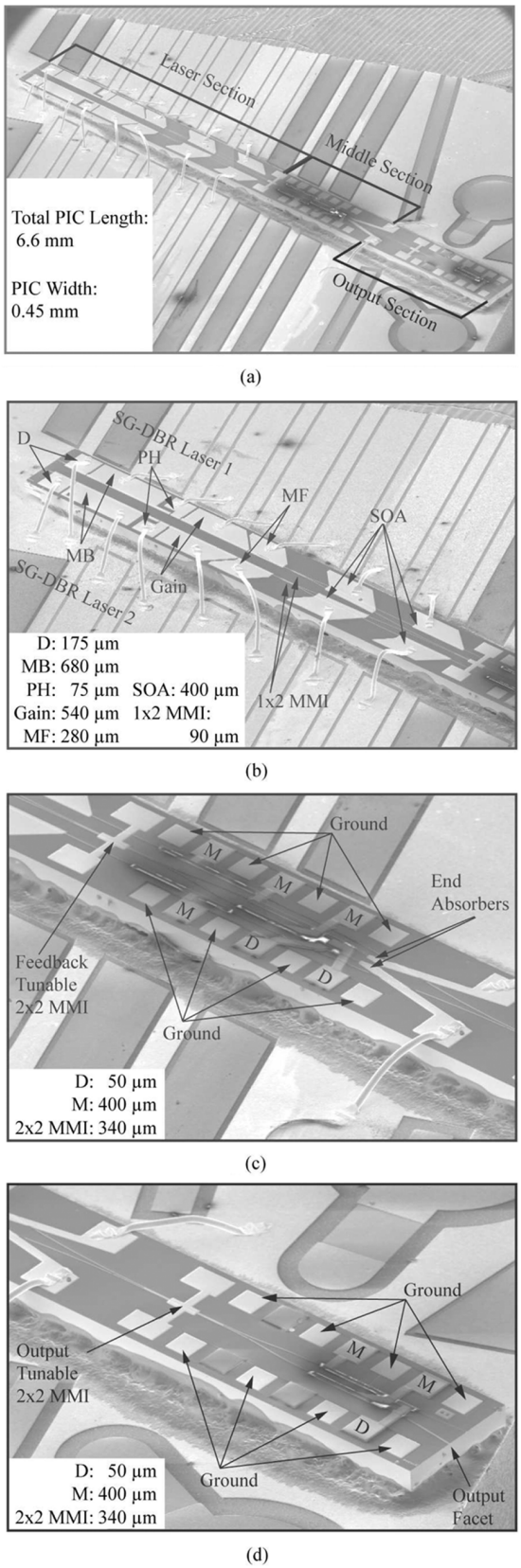


Fig. 3. SEM images of the OPLL-PIC and its various sections. (a) Whole OPLL-PIC. (b) Laser Section of the OPLL-PIC. (c) Middle Section of the OPLL-PIC. (d) Output Section of the OPLL-PIC.

also includes the two 1×2 MMI splitters and the four SOAs. As shown in Fig. 2, there are four SOAs in the PIC, one on each output of both 1×2 MMI splitters. Some variations of the PIC, approximately one third of the devices, were designed to have only two SOAs, one for each laser, placed at inputs of the 1×2 MMI splitters. Although additional biasing is required, the advantage of having four SOAs at the outputs of the 1×2 MMI splitters is that they can be used to equalize the lasers' output powers for better, more efficient interference. In this work, however, due to the test bench limitations, the SOAs were wire-bonded together to the same pad on the carrier.

Fig. 3(c) shows the Middle Section of the OPLL-PIC. The 2×2 MMI in this section can be tuned by current injection [31], [32], although we have not done it in this work. The modulator and photodetector at the output of the 2×2 MMI connect to RF pads that are arranged in a G-S-G-S-G-S-G configuration for direct probing, with 150 μm pitch and 100 μm $\times$ 100 μm surface area per pad. Two 200 μm long curved (7°) active sections with grounded pads, absorb light that is not absorbed in the two photodetectors.

Fig. 3(d) shows the Output Section of the OPLL-PIC. The two modulators and the photodetector at the outputs of the 2×2 MMI connect to RF pads that are arranged in the same way as those in the Middle Section of the OPLL-PIC, except that here there are three unused pads. The output waveguides that enable coupling into an optical fiber are angled at 7° with respect to the direction normal to the cleaved facet, and anti-reflection coatings are applied in order to minimize facet reflections.

C. OPLL-PIC Fabrication

For monolithic integration of the SG-DBR lasers with the other components of the OPLL-PIC, an integration platform that is often referred to as "Offset Quantum Well (OQW)" Platform [27] is used. In this platform, light is guided by a "passive" 1.4Q bulk layer that forms a basis for waveguiding, as well as modulation through current injection [33] or the Franz-Keldysh effect if reverse biased [34]. Above this layer, light couples evanescently to an "active" multiple-quantum-well (MQW) layered structure that is present only in the regions that form SOAs, gain sections of SG-DBR lasers, and photodetectors [27].

Fig. 4 shows details of the base epitaxial layer structure used in the OQW platform that is grown on a 2-inch S-doped InP wafer by metal-organic chemical vapor deposition (MOCVD). A 2 μm thick Si-graded-doped InP buffer is grown on the substrate to reduce the overlap of the optical mode confined to the 1.4Q waveguiding layer with the heavily doped substrate and minimize the free-carrier-induced optical propagation loss in the waveguide. The buffer doping is graded from $\sim$1e19 cm^{-3}, close to the substrate, to $\sim$1e18 cm^{-3}, close to the 1.4Q waveguide core layer. A 300 nm thick, unintentionally doped (UID), 1.4Q waveguiding layer is epitaxially grown over the graded InP buffer, followed by a 20 nm thick 1.2Q separate confinement heterostructure (SCH) layer, a 10 nm thick InP etch-stop layer, an active region comprised of multiple quantum wells (MQW) layers with a total thickness of 119 nm, another 30 nm thick 1.2Q SCH layer, a 60 nm thick UID InP spacer, and a 150 nm thick Zn-doped (1e18 cm^{-3}) InP cap. The thin InP spacer underneath the Zn-doped InP cap helps prevent diffusion of Zn

	150 nm InP, Zn (1e18 cm^{-3})
	60 nm InP, UID
	30 nm 1.2Q, UID
"active layer"	119 nm MQW, UID
	10 nm InP, UID
	20 nm 1.2Q, UID
"passive layer"	300 nm 1.4Q
	2000 nm InP, graded Si-doped
	S-doped InP substrate

Fig. 4. "OQW" base epitaxial structure.

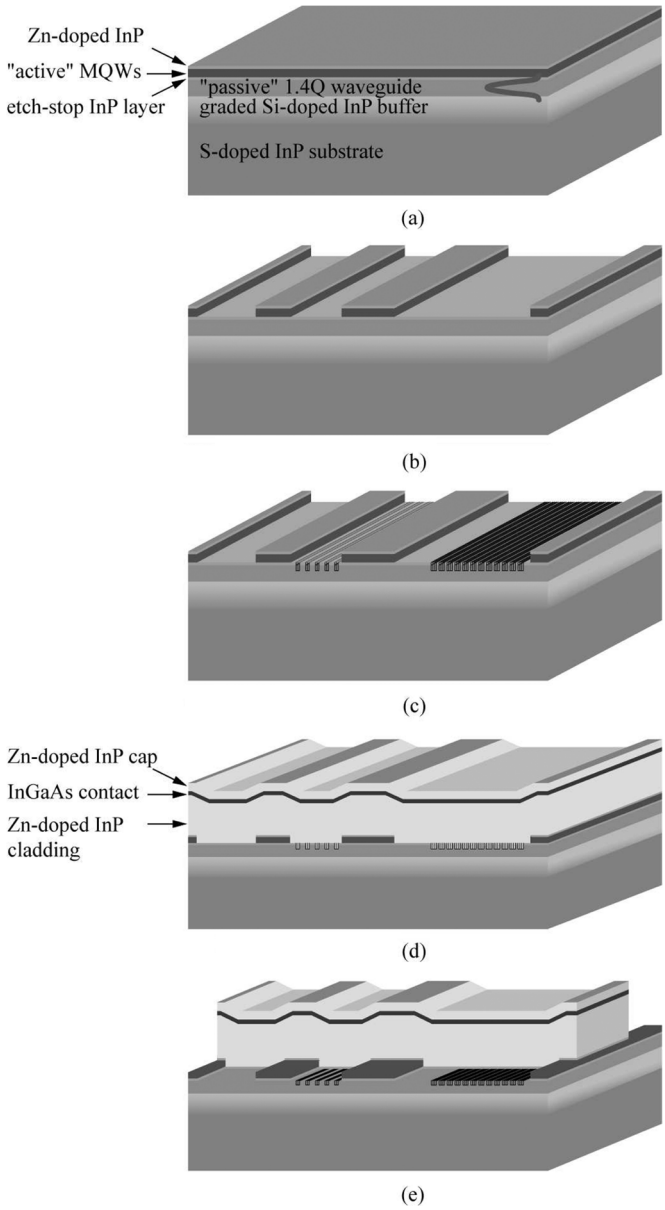


Fig. 5. "OQW Platform": schematics of the main processing steps starting with the base epitaxial structure. (a) Base epitaxial structure. (b) Active/passive wet etch. (c) Gratings etch. (d) P cladding regrowth. (e) Surface-ridge waveguide etch.

dopant into the active MQW layer, and the Zn doping in the InP cap helps in controlling the position of the p-i-n junction formed after regrowth. The photoluminescence peak of the active MQW layers was measured to be $\sim$ 1560 nm.

The 2-in wafer is cleaved into four different quarters and each quarter is processed separately. In Fig. 5(a)–(e), we illustrate the processing steps used in the fabrication of the OPLL-PIC. Starting from the base epitaxial structure shown again in Fig. 5(a), Fig. 5(b) illustrates the active/passive wet etch step, where the "active" regions are etched away everywhere on the wafer except in the areas that define the SOAs, gain sections of the SG-DBR lasers and the photodetectors. A 100 nm thick Silicon Nitride (SiN_x) layer is deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD), and 5 $\times$ Stepper Lithography is used to define the active regions by patterning photoresist that is spun on top of the SiN_x layer. All SiN_x depositions in this work are done at 250 °C. The pattern is transferred to SiN_x by CF_4/O_2-based Reactive Ion Etching (RIE). The SiN_x hard mask protects the InP cap, spacer layers at the top of the wafer, and the active MQW and SCH regions during wet etching steps that selectively remove these layers elsewhere. The SiN_x mask is subsequently removed using buffered hydrofluoric acid (BHF).

The gratings in the SG-DBR sections are defined in the passive 1.4Q layer using a Methane/Hydrogen/Argon (MHA)-based RIE, as shown in Fig. 5(c). The targeted grating depth is around 100 nm and duty cycle is 50%. The gratings are patterned onto a high-resolution photoresist using electron-beam lithography. The grating pattern is transferred to a 50 nm thick SiO_2 layer using CHF_3-based RIE, which, in turn, is used as a hard-mask for the MHA RIE step that etches the grating into the 1.4Q layer. The grating period is targeted to be $\sim$ 240 nm so that the center wavelength of the SG-DBR laser is close to 1550 nm. The sampled gratings are used in both the front-side and back-side mirrors of the SG-DBR lasers. The front-side mirror consists of 5 grating bursts, each burst being 6 μm long, that repeat periodically with an interval of 61.5 μm. The back-side mirror consists of 12 grating bursts, each burst being 4 μm long, that repeat periodically with an interval of 68.5 μm. More details about the wide wavelength tuning using the Vernier effect achievable with SG-DBR lasers can be found in [35]. The SiO_2 layer is subsequently removed using BHF, and the sample is thoroughly cleaned in UV-ozone prior to the regrowth step.

The following step is the regrowth step, as shown in Fig. 5(d). The regrowth layers comprise of a 50 nm thick UID InP spacer that helps prevent diffusion of Zn from p-doped cladding into the underlying MQW layers in the active regions and the 1.4Q layer in the passive regions of the OPLL-PIC, a 2000 nm of Zn-doped InP cladding, where the doping is 7e17 cm^{-3} in the lower half of the cladding and 1e18 cm^{-3} in the upper half of the cladding, a 100 nm thick Zn-doped (1e19 cm^{-3}) InGaAs contact layer followed by a 200 nm thick Zn-doped (1e18 cm^{-3}) sacrificial InP cap layer, on the top of the wafer, which is used to

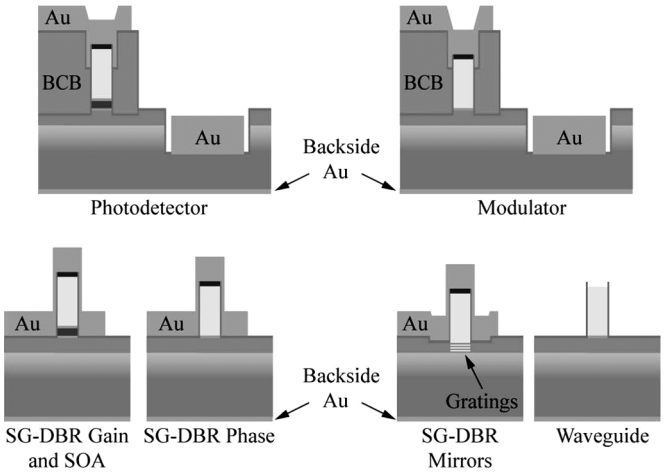


Fig. 6. Schematics showing cross sections of various components of the fully processed OPLL-PIC.

protect the thin InGaAs contact layer during the processing steps prior to metallization. The p-doping in the InP cladding layer is decreased closer to the waveguide core in order to reduce the free-carrier-induced optical loss.

Following the regrowth, surface-ridge waveguides are etched, as shown in Fig. 5(e). First, an MHA-based RIE using a 100 nm thick SiN_x hard mask is used to etch the waveguides to a depth of $\sim$1.5 μm below the regrown InGaAs layer. Following the dry etch, the surface ridge waveguide is further etched by a $HCl:H_3PO_4$ wet etch cleanup so that the rest of the p-doped InP cladding is removed. The 1.2Q layers directly above the MQW layer in the active regions and directly above the 1.4Q layer in the passive regions act as etch-stops for the selective wet-etch. All waveguides deviate less than 7° from the normal to the major plane, so that minimal undercutting of waveguide walls is observed. In one quarter of the fabricated PICs, including the PIC presented in this paper, waveguides widths are adiabatically tapered from 3 μm, starting at the outputs of the 1×2 MMI splitters to 2.3 μm at the input of the feedback loop 2×2 MMI coupler. This is done over a distance longer than 300 μm in order to minimize the radiation losses. Similar tapering is done for the waveguide sections entering the output 2×2 MMI coupler. Since our passive waveguides are weakly multimoding when they are 3 μm wide, the tapering is used to diminish the negative effect that multimoding has on the extinction ratio of interference of the two lasers' outputs in the 2×2 MMI coupler. As the wider waveguide sections have lower loss, outputs of the 2×2 MMI couplers are tapered back to 3 μm in a similar manner. Passive waveguide widths in the rest three quarters of the PICs are maintained at 3 μm. By comparing PICs with tapered waveguides to those with non-tapered waveguides, the effect of weak multimoding on the extinction ratio can be studied. Waveguide sections for input and output coupling of light are curved by 7° and their widths are tapered to 5.5 μm in order to minimize facet reflections. In addition, anti-reflection coatings are applied to the facets after the processing steps are completed. Together with the 7° waveguide curves and the 5.5-μm tapers, total facet reflectivity of less than 10^{-4} is expected, which has been shown to be necessary for similar PICs [36], [37].

The processing steps that follow the ridge waveguide etching are fairly common and not necessarily characteristic of our integration platform. Here, we summarize the remaining steps. Fig. 6, shows various sections of the OPLL-PIC after these processing steps have been completed.

First, a thick photoresist is pattered so that it covers the entire sample except $\sim$12 μm on each side of the ridge waveguides sections that form the high-speed modulators and high-speed photodetectors. The waveguides are still protected by SiN_x hard mask that was used to etch the surface ridges in the previous step. MHA-based RIE is used to remove the top 20 nm thick 1.2Q SCH layer and approximately 80 nm of the underlying 1.4Q layer. Both of these layers contain Zn atoms that diffuse from the p-doped InP cladding during regrowth. These Zn atoms can considerably increase the capacitance for the detectors and modulators, necessating the dry etching of the top 100 nm of the quaternary semiconductor.

An additional 100 nm thick SiN_x layer is deposited and patterned to provide a hard mask for MHA-based RIE that is used to etch windows for top N-contact metallization. The etch is performed until it penetrates $\sim$0.5 μm below the Si-graded-doped InP buffer into the heavily doped substrate. A thick photoresist covers the wafer everywhere except the N-contact metallization window regions. An electron-beam evaporator is used to deposit a Ni/AuGe/Ni/Au contact, which is patterned using the liftoff technique. The thickness of gold deposited during this step is only $\sim$0.5 μm as more gold is added during the P-contact metallization step. As illustrated in Fig. 6, the top N-contact is made only for fast devices, i.e., photodetectors and modulators. Top N-contacts are typically required for the PICs that are fabricated on semi-insulating substrates to provide low-loss connection to the ground plane [32], [36]. The main reason for having the top N-contacts in our proof-of-concept demonstration is the ease of direct RF probing, as discussed in Section II-B. N-contact for the remaining devices is achieved by backside metallization at the end of processing. The N-contacts are annealed at 430 °C for 30 s. After the top N-contact metallization, a thin SiN_x layer is deposit and photo-sensitive BCB is spun, developed, and cured at 250 °C. This leaves BCB in places that will be underneath the P-contact metal pads and traces running along the lengths of the high-speed photodetectors and modulators and covering the surface ridges in these regions. Along with the capacitance reduction etch, the BCB further reduces the capacitance of these devices to the extent that should enable their operation at frequencies far exceeding 10 GHz. The P-metal pads without BCB are separated from the top surface of the wafer (1.2Q stop-etch layer) by sub-micron-thick SiN_x. BCB is used to elevate the P-metal pads farther from this surface, and thus farther from the N-doped substrate, so that this increased separation combined with the small dielectric constant of BCB (2.65), provide lower capacitance compared to the P-metal pads without BCB [36]. An additional thin SiN_x layer is deposit after BCB patterning. Thus, the BCB is sandwiched between thin layers of SiN_x, shown as thin lines in Fig. 6, for better adhesion to the

semiconductor surface below as well as the P-contact metal on top.

Three different types of P-contact metal vias need to be opened in the top SiN_x layer prior to the P-contact metallization. First, vias are formed by removing the SiN_x layer above N-contact metal. This is accomplished by patterning photoresist to cover the sample everywhere except over the N-contact metal and dry etching the SiN_x layer above the N-contact metal using CF_4/O_2-based RIE. The next via is formed by removing the SiN_x layer on top of all the ridge waveguide sections except those covered with BCB. To open this via, photoresist is partly developed around the waveguides and partially etched back using O_2-based RIE until the ridge tops are exposed. CF_4/O_2-based RIE is then used to etch the SiN_x layer and expose the InP cap layer that is on top of the ridge waveguides. The remaining SiN_x over the rest of the wafer is protected by photoresist during this step. Finally, vias through the BCB layers are opened using a two-step process. A 5-μm-wide via is etched using CF_4/O_2-based RIE to expose the ridge top buried underneath 3.7-μm-thick BCB and the SiN_x layers. This etch needs to be timed in order to minimize the difference in height between the ridge top and the BCB, and, consequently, minimize the P-contact capacitance. SiN_x is then re-deposited to fill in any openings that typically develop between the waveguide sidewalls and BCB, and a new via that is narrower than the waveguide is dry etched until the BCB and SiN_x layers are completely removed thereby exposing the InP on the top of the ridge.

At this point the sacrificial InP cap layer is removed using $HCl:H_3PO_4$-based wet etch everywhere along the ridge waveguides, thus exposing the InGaAs contact layer.

Standard Ti/Pt/Au 8-μm-wide P-contact metal is deposited by electron-beam evaporation, where gold thickness is over 2 μm. During the deposition, the sample is mounted on a rotation stage tilted at $\sim 30°$ for maximum sidewall coverage. The P-contact metal is patterned using the liftoff technique. The thermal annealing is done at 400 °C for 30 s.

After the P-contact metallization is completed, the passive waveguide sections that are not covered by metal are further processed. At this point, the SiN_x layers and the sacrificial InP cap layer are missing from the top surfaces of these waveguide sections, and the InGaAs contact layer is exposed. A thick photoresist is first patterned so that it covers the entire sample, including the metalized waveguide sections, except ~ 12 μm on each side of the passive waveguide sections. The top InGaAs contact layer is then removed from the ridge tops in these sections using a $H_3PO_4:H_2O_2:H_2O$-based selective wet etch. SiN_x layers protect the top 1.4Q layer on each side of the ridge during this etch step. The same photoresist mask is subsequently re-patterned, and the wafer quarter is subjected to proton implantation. Proton implantation along with the removal of the InGaAs contact layer increase the electrical isolation between neighboring devices and reduces the free-carrier-induced optical loss. The use of proton implantation for neutralizing Zn acceptors, which dominate the carrier-induced loss, is described in [38].

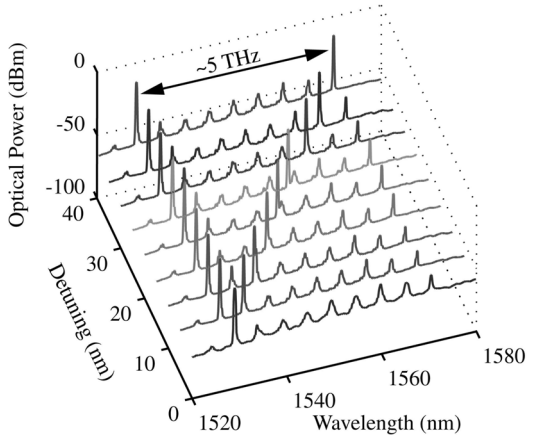


Fig. 7. Optical spectra obtained by heterodyning two integrated, unlocked widely tunable SG-DBR lasers.

Typical passive waveguide loss for this integration platform is ~ 2.5 dB/mm [37].

The wafer quarter is then thinned to a thickness of ~ 130 μm, for the ease of cleaving. Back-side Ti/Pt/Au metallization is performed using electron-beam evaporation, where the thickness of gold is around 0.3 μm. The thermal annealing is done at 380 °C for 30 s. The sample is cleaved into bars along facets that have the waveguides for input or output coupling to an optical fiber. Anti-reflection coatings are applied to these facets to further reduce reflections. Individual devices are then cleaved and mounted on carriers and wire-bonded.

III. SG-DBR Laser Performance

Besides the fact that it is a well established technology, there are at least four important characteristics of the SG-DBR laser that make it a very attractive choice for its use in an OPLL.

First, SG-DBR lasers have in excess of 40 nm of quasi-continuous wavelength tuning range, as shown in the optical spectrum analyzer spectra plotted in Fig. 7. In this figure, one of two on-chip SG-DBR lasers is tuned to a constant wavelength, while the wavelength of the other on-chip SG-DBR laser is detuned away from that wavelength in increments of ~ 5 nm. This wide wavelength tuning range enables the OPLL-PIC to generate a heterodyne beat frequency that spans from DC to over 5 THz.

Second, the FM tuning mechanism of the SG-DBR laser is very efficient. Unlike Distributed Feedback (DFB) lasers, which are tuned by current injection into the laser gain section, in SG-DBR lasers, the tuning is achieved by current injection into a small, separate, passive phase section. The DC FM sensitivity can be as high as 20 GHz/mA for this tuning mechanism, which is over an order of magnitude greater than the 1–3 GHz/mA DC FM sensitivity reported for a three-section laser optimized for use in OPLL applications [2]. The large FM sensitivity directly translates into a large feedback loop gain and thus helps improve OPLL stability.

Third, an important advantage of the SG-DBR laser is that, unlike in a typical DFB laser, there is no sign change in its FM

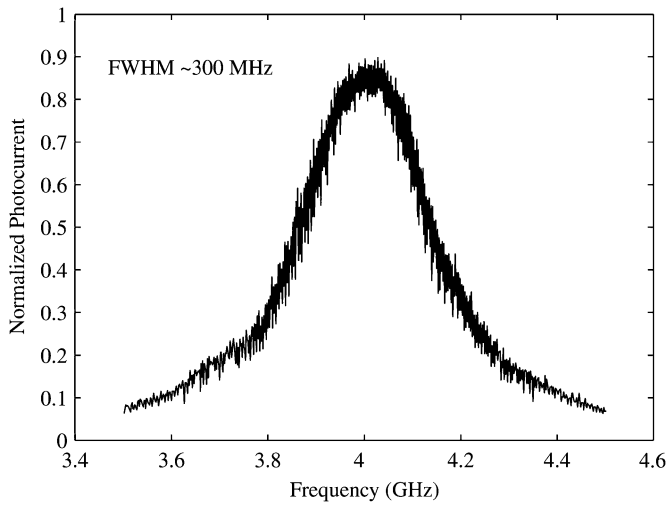


Fig. 8. Composite linewidth measured from the heterodyne beat of the two integrated, unlocked SG-DBR lasers. Resolution and video bandwidths are 2 MHz and 3 kHz, respectively.

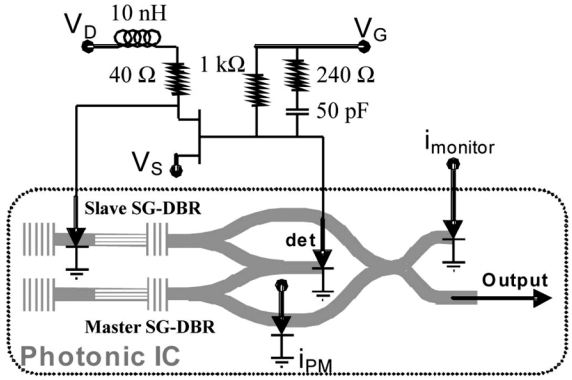


Fig. 9. Schematic of the homodyne locking experimental setup.

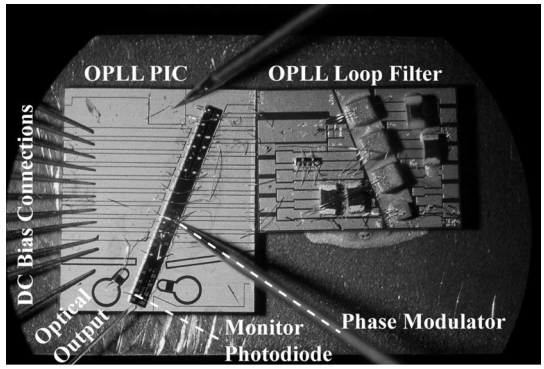


Fig. 10. Optical image of the homodyne locking experimental setup.

phase response. The FM response has a 3 dB bandwidth of ~ 70 MHz, and no phase inversion is observed below this frequency. The phase inversion in a DFB laser occurs within its bandwidth at a frequency where the thermal effect becomes too slow to dominate frequency tuning with the corresponding red shift in the FM response so that frequency tuning becomes dominated by the carrier-injection effect and the corresponding blue shift in the FM response. It is very challenging to implement an OPLL feedback electronic circuit that can compensate for this phase inversion. The absence of phase inversion in the FM phase response of an SG-DBR laser is due to the fact that: 1) the small and efficient phase tuning pads require small currents for tuning, thereby reducing the thermal effects and 2) the phase section is composed of the passive material that has a band gap larger than that of the active material so that the accumulation of carriers is very efficient as they cannot be depleted by stimulated emission.

Fourth, the linewidth of an SG-DBR laser is dominated by low-frequency jitter [39], which is not very difficult to compensate with the large bandwidth of an integrated OPLL, which as we will show below is at least 300 MHz.

We note that the Shawlow–Townes linewidth limit for a typical SG-DBR laser is below 1 MHz [39]. However, the linewidth that we measure with a 30-μs-delay self-homodyne technique is in the range between 10 and 50 MHz, varying with mirror setting, which is dominated by low-frequency jitter noise. This linewidth would be hard to compensate with an OPLL that is not integrated. Fig. 8 shows the linewidth from the heterodyne beat of two unlocked, integrated SG-DBR lasers obtained by combining their outputs at an offset frequency. The combined linewidth of ~ 300 MHz is measured using an external 20 GHz photodetector and a 20 GHz electrical spectrum analyzer. This wide linewidth is associated with low frequency current noise on the tuning port, and this is normally removed with a large capacitive load in cases where rapid tuning is not required.

IV. Proof-of-Concept Experimental Results

We perform two experiments in order to demonstrate proof-of-concept operation of the OPLL: homodyne locking and offset locking of the two monolithically integrated SG-DBR-lasers, as presented in Sections IV-B and IV-C. Before presenting the details of these two experiments, we first present the basics of the electronics used in the feedback loop in Section IV-A.

A. Feedback Loop

Fig. 9 shows the schematic of OPLL-PIC including the feedback electronic circuit when used in the homodyne locking experiment, and Fig. 10 shows the corresponding optical image. The electronic circuit is built around a field effect transistor (FET). One of the two photodetectors in the Middle Section of the OPLL-PIC is used to detect a phase error signal between the two lasers, which is converted to an amplitude error signal in the 2×2 MMI. The reverse-biased current signal generated by this photodetector is amplified by the FET and converted into a forward-biased current signal needed to control the injection of carriers into the phase section of the slave SG-DBR laser.

We design the detector load to provide a second order loop transfer function with lag compensation. The FM response of the SG-DBR laser has a 3-dB point around 70 MHz. The LR circuit that loads the laser phase section is designed to have a zero close to the laser's pole, compensating its FM response and making it a more controllable device. The RC circuit that loads

the photodetector is designed to provide the following function. The larger of the two resistors dominates at frequencies closer to DC and ensures a large locking range. The other resistor dominates at frequencies closer to the 3-dB point and provides the desired zero needed to improve the stability of the loop for the higher frequencies where the gain becomes unity. The resulting loop bandwidth that we measure is $\sim$ 300 MHz. Similar to a voltage-controlled oscillator in an RF PLL, the laser itself acts as an integrator, which means that the rest of the electronics is required to provide a single pole to realize a second-order loop. More details on the issues pertaining to the feedback loop design can be found in [40].

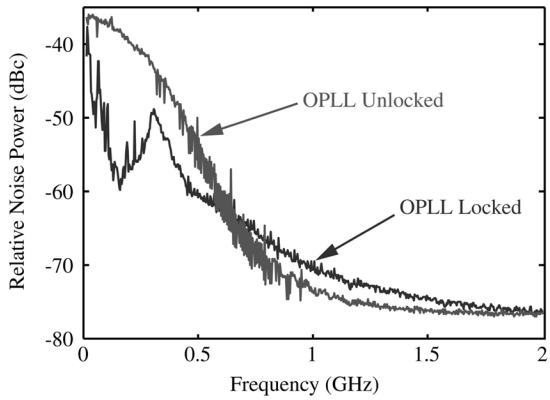


Fig. 11. Noise spectra measured at the optical output of the OPLL-PIC in the homodyne locking experiment. Resolution and video bandwidths are 2 MHz and 10 kHz, respectively.

B. Homodyne Locking

As mentioned above, the schematic and optical image corresponding to the homodyne locking experiment are shown in Figs. 9 and 10, respectively. No current is applied to the backside or the front-side mirror of the two SG-DBR lasers, so that they lase at their untuned wavelengths, which are close to 1542 nm. The random phase variation between the two lasers translates into an intensity modulated error signal at the output of the 2×2 MMI in the Middle Section of the OPLL-PIC and finally into a current error signal at the output of one of the photodetectors that is connected to the feedback loop. The error signal then passes through the electronic circuit and tunes the frequency of the slave laser so that it is matched to that of the master laser, where the slave laser effectively plays a role of a current-controlled oscillator.

In order to bring the OPLL from an unlocked state into a locked state, we inject appropriate bias currents into the phase section of the one of the SG-DBR laser until its frequency is within the feedback loop bandwidth, i.e., $\sim$ 300 MHz, to that of the second SG-DBR laser. The bias current is adjusted until the noise spectrum measured at the optical output of the OPLL-PIC changes as shown in Fig. 11, which indicates that the OPLL-PIC has become locked. Fig. 11 also reveals the expected presence of the 300 MHz resonance frequency peak, above which the OPLL provides a positive rather than negative feedback and becomes unstable. The data is acquired using an external 20 GHz photodetector and a 20 GHz electrical spectrum analyzer. The uncompensated low-frequency noise below the resonance frequency peak is mainly due to OPLL-PIC's AM noise that can be effectively cancelled using feedback from a balanced photodetector pair (implemented on the PIC, but not used here) rather than a single photodetector.

To further confirm the homodyne locking, we inject current into one of the modulators and continuously adjust the phase of the light from one of the SG-DBR lasers. This modulator is part of the waveguide that directs light toward the 2×2 MMI in the Output Section of the OPLL-PIC and is not the feedback-loop. This phase modulator allows us to independently modulate the phase of one SG-DBR laser output while leaving the phase of the second SG-DBR laser unchanged. When the OPLL is in the locked state, the two lasers are coherent with respect to each other. By changing the phase on one of the lasers, the interference between the two lasers in the 2×2 MMI in the Output Section of the OPLL-PIC shows the characteristic interference that is observed from a Mach–Zehnder Interferometer (MZI), which converts phase modulation to amplitude modulation. When the OPLL is not locked, the two lasers are not coherent with respect to each other and their interference in the 2×2 MMI does not exhibit the phase to amplitude modulation response that is characteristic of an MZI.

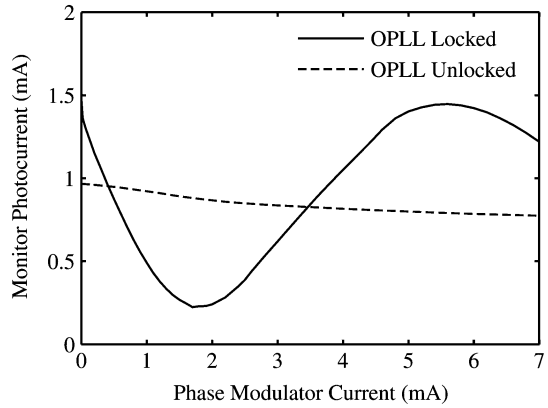


Fig. 12. Phase-to-amplitude modulation conversion observed for the locked and unlocked states of the OPLL for homodyne locking of the two SG-DBR lasers.

Fig. 12 illustrates this behavior for both locked and unlocked states of the OPLL. In both cases, we see a small intensity modulation characteristic for our modulators when operated in the forward bias. Also, the half-wave current (I_π) needed for switching the interference between "on" and "off" states is $\sim$ 4 mA, which is consistent with other measurements performed on similar phase modulators. The extinction ratio ($\sim$ 8 dB) observed for the constructive versus destructive interference is limited by unequal optical powers reaching the 2×2 MMI, phase noise of the lasers, weak multimoding in the waveguides, and polarization mismatch. Because the SG-DBR lasers emit quasi-TE-polarized light and all of the integrated optical components are designed to be polarization maintaining, the

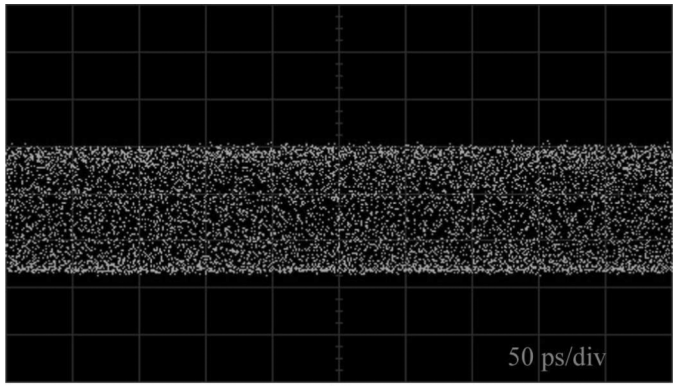
polarization mismatch is expected to have a small effect on the extinction ratio. Due to the present probing station limitations, i.e., limited number of bias controls, in this proof-of-concept study, we did not bias the SOAs independently nor did we tune the MMI splitters in order to overcome the possible optical power mismatch. This issue will be addressed more systematically in a future study.

C. Offset Locking

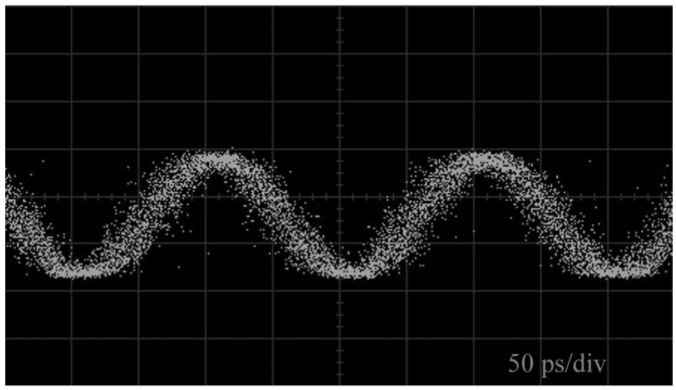
The same PIC and electronic circuit that were used in the homodyne experiment are also used in the offset locking experiment. To demonstrate offset-locking of the two monolithically integrated SG-DBR lasers, we apply a reverse bias phase modulation to one of the modulators that is connected to the output of the 2×2 MMI in the Middle Section of the OPLL-PIC and is a part of the feedback loop, as shown in Fig. 1. As this phase modulator output is only connected to the integrated detector pair used for the feedback circuit, the OPLL-PIC output signal does not contain any modulation sidebands. In this case, we use the reverse bias modulation based on the Franz–Keldysh effect because the gigahertz-range modulation frequency that we need far exceeds the bandwidth ($\sim$ 100 MHz) of the modulator in the forward-biased current-injection mode. In our offset-locking scheme, the carrier frequencies from both lasers are simultaneously modulated, which generates two modulation sidebands corresponding to either laser's carrier frequency. When the frequency separation between the two SG-DBR lasers equals the modulation frequency, the detected photocurrent will contain a phase-dependent DC component, and sideband locking of the two lasers becomes possible. Mixing of the two laser frequencies and their sidebands occurs in the photodetector, which generates a corresponding current error signal to the feedback electronics and the phase section of the slave laser whenever there is a random phase walk-off between a center frequency of one laser and a sideband of the other laser. The power in the sidebands is smaller in comparison to the power at the center frequencies of the laser. Consequently, the extinction ratio of the corresponding interference is smaller than for the homodyne OPLL, producing a weaker error signal. To compensate for this, to generate as strong modulation sidebands as possible, the power applied to the modulator used in offset locking is between 10 and 15 dBm.

Fig. 13(a) and (b) show an oscilloscope trace of the OPLL-PIC's optical output before and after 5 GHz offset locking of the two SG-DBR lasers, respectively. The oscilloscope is triggered by the 5 GHz modulating signal. Before locking, the phase of the beat varies randomly and only an envelope of the beat is observed in Fig. 13(a). After phase-locking, a coherent beat signal is generated, as observed by the oscilloscope trace in Fig. 13(b).

In addition to the time domain representation of the locked beat shown in Fig. 13(b), in Fig. 14, we plot the corresponding frequency spectrum obtained using an external 20 GHz photodetector and a 20 GHz electrical spectrum analyzer. As expected, the spectrum is centered at the 5 GHz modulation frequency, surrounded by two peaks that are offset by $\sim$ 300 MHz, corresponding to the bandwidth of the feedback loop. From



(a)



(b)

Fig. 13. Oscilloscope traces observed at the optical output of the OPLL-PIC in the heterodyne locking experiment when the OPLL is (a) unlocked and (b) locked.

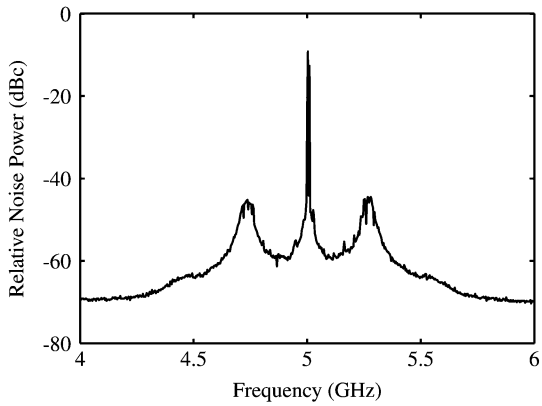


Fig. 14. Noise spectrum measured at the optical output of the OPLL-PIC in the heterodyne locking experiment. Resolution and video bandwidths are 2 MHz and 10 kHz, respectively.

the spectrum in Fig. 14, we calculated the phase error variance to be 0.03 rad^2 by dividing the noise power within the 2 GHz span by the signal power [3]. Our result is comparable to the state-of-the-art result in [2], where phase error radiance of 0.05 rad^2 in a 1 GHz bandwidth has been reported for an OPLL based on miniature bulk optics designed for use in a microwave photonic transmitter. We obtained similar results for different offset frequencies up to 15 GHz.

V. Conclusion

In this work, we have successfully demonstrated the first monolithically integrated optical phase-locked loop photonic integrated circuit in which all of the optical components are integrated on the same InP platform, including: master and slave SG-DBR lasers, high-speed modulators, high-speed photo detectors, multimode interference couples/splitters, as well as interconnecting optical waveguides. Compared to the alternatives, monolithic integration of an optical phase-locked loop is expected not only to provide a competitive performance, but also to make the technology more easily packaged and less expensive.

We have shown that, via monolithic integration, the phase-locked loop can be made sufficiently compact, and thus have a sufficiently wide bandwidth (300 MHz), to allow use of wide linewidth semiconductor lasers. We have further demonstrated suitability of SG-DBR lasers to be used as the master laser and the slave laser, i.e., current-controlled oscillator, in this application. Most importantly, unlike the DFB laser, the slave SG-DBR laser does not suffer from a phase inversion in the FM frequency response, which is not easily compensated by the loop filter electronics. In addition, the slave SG-DBR laser offers a large phase tuning sensitivity, improving the gain and stability of the phase-locked loop. We have also shown that the detuning range of the master and slave SG-DBR lasers exceeds 5 THz, which enables the phase-locked loop to generate phase-stable optical beats at very high frequencies. This beat can be modulated with on-chip high-speed modulators and also converted into an electrical signal with on-chip high-speed photodetectors.

We have performed two experiments to demonstrate the proof-of-concept operation of the monolithically integrated PLL: homodyne locking and offset (5 GHz offset) locking of the master and slave SG-DBR lasers. We have shown that a simple electronic filter is sufficient to enable locking. The future versions of optical phased-locked loop will utilize both feedback photodetectors as a balanced pair in order to reduce laser amplitude noise. In addition, integrated feedback electronics will be implemented to further increase the bandwidth of the loop. Both of the changes are expected to significantly reduce the phase noise of the PLL.

Acknowledgment

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years, for example, he has been involved in the creation of efficient all-epitaxial InP-based and high-modulation speed GaAs-based VCSELs as well as a variety of InP-based PICs incorporating numerous optical elements for widely-tunable integrated transmitters, receivers, and wavelength converters operating up to 40 Gb/s. He has has authored or coauthored over 1000 journal and conference papers, 7 book chapters, 1 textbook, and has been issued 63 U.S. patents. He has presented dozens of invited and plenary talks at major conferences.

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Direct modulation bandwidth enhancement of strongly injection-locked SG-DBR laser

A. Bhardwaj, S. Ristic, L.A. Johansson, C. Althouse and L.A. Coldren

Significant enhancement in the direct amplitude modulation bandwidth of an SG-DBR laser has been demonstrated under strong injection-locking conditions, where the wavelength detuning between the master and the free-running SG-DBR slave laser is varied from −8.58 to 13.6 nm. It is demonstrated that the relaxation resonance frequency of a strongly injection-locked SG-DBR laser increases from 1.05 GHz for the free-running case to over 20 GHz.

Introduction: It is well known that the direct modulation bandwidth of a semiconductor laser is limited by the relaxation oscillations arising from the coupled rate equations that describe the dynamics of the carrier and photon densities inside the laser cavity. It has been shown that the relaxation resonance frequency of a laser can be increased using injection-locking, resulting in an enhancement of its direct modulation bandwidth. Strong optical injection-locking has attracted attention recently for its potential for providing high-speed laser transmitters, as it improves the dynamic response of directly modulated semiconductor lasers, as well as for enhancing the relaxation oscillation frequencies, suppressing nonlinear distortions and relative intensity noise, and reducing chirp [1–3]. In the strong injection-locking regime, the optical power of the light injected from the master laser into the slave cavity is much larger than the optical power of the free-running slave laser. Recent demonstrations include enhancement of the resonance frequency beyond 100 GHz in a directly modulated strongly injection-locked vertical-cavity surface-emitting laser (VCSEL) [4].

In this Letter, we consider the injection-locking of a widely tunable sampled grating distributed Bragg reflector (SG-DBR) laser that is designed with high-speed gain and phase modulator sections. We study the direct amplitude modulation response of the SG-DBR laser when it acts as a slave laser and is strongly injection-locked to an external master laser. We demonstrate that a strongly injection-locked SG-DBR laser shows significant enhancement in its direct modulation bandwidth, even when the wavelength detuning between the master and the free-running SG-DBR slave laser is varied between −8.58 and 13.6 nm (corresponding to a frequency detuning of 1.072 and −1.68 THz, respectively). To the best of our knowledge, this is the first demonstration of direct modulation bandwidth enhancement of a strong injection-locked SG-DBR laser over a large wavelength detuning range from its free-running state.

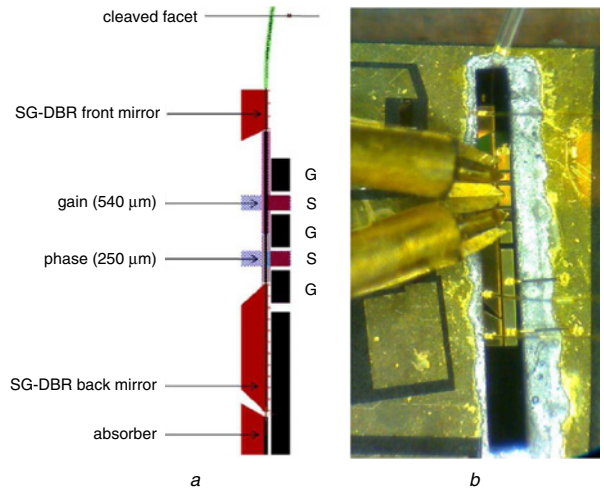

Fig. 1 *Mask layout of SG-DBR laser with high-speed gain and phase modulator sections; and photograph of SG-DBR laser probed using G-S-G-S-G probe with lensed-fibre coupled to its output*

a Mask layout of SG-DBR laser
b Photograph of SG-DBR laser

Device design and fabrication: A widely tunable SG-DBR laser [5] was designed and fabricated using a standard offset quantum well material platform on an indium phosphide (InP) substrate [6] that allows monolithic integration of active and passive waveguide sections. In this platform, light is guided by a 300 nm-thick passive $In_xGa_{1-x}As_yP_{1-y}$ based quaternary 1.4Q bulk layer (with a bandgap corresponding to the energy of a photon at 1.4 μm) that forms a basis for waveguiding, as well as modulation through current injection, or the Franz-Keldysh effect if reverse biased. Above this layer, light couples evanescently to an 'active' compressively strained $In_xGa_{1-x}As_yP_{1-y}$ based quaternary multiple-quantum-well (MQW) layered structure that is present only in the regions that form the active sections of the SG-DBR laser.

The sampled gratings define the front-side and back-side mirrors of the SG-DBR laser. The targeted grating depth is around 100 nm into the 1.4Q layer and the duty cycle is 50%. The front-side mirror consists of five grating bursts, each 6 μm long and repeats periodically with an interval of 61.5 μm. The back-side mirror consists of 12 grating bursts, each 4 μm long and repeats periodically with an interval of 68.5 μm. The width of the surface ridge waveguide is 3.5 μm. The gain section is 540 μm long and the phase section is 125 μm long. The high-speed gain and phase sections have top-side N-metal pads on either side of the corresponding P-metal pad so that they can be probed with a high-speed G-S-G-S-G RF probe. The pitch between the G-S-G-S-G pads is 150 μm. The waveguide beyond the back-mirror is flared and fed into an active region, which acts as an absorber. The access waveguide at the front facet is flared to 5 μm and angled by 7° to suppress reflections. No anti-reflection coating was applied to the front facet of the SG-DBR laser. The layout of the SG-DBR laser is shown in Fig. 1*a*.

Experiment and results: A G-S-G-S-G RF probe was used to apply bias currents to the gain and phase sections of the SG-DBR laser, as shown in Fig. 1*b*. To study the direct amplitude modulation response of the SG-DBR laser, a DC forward-bias current was combined with an RF modulation generated from a vector network analyser (VNA) using a high-speed bias-tee and applied to the gain section of the SG-DBR laser. To characterise the small-signal RF modulation response, the VNA (Agilent 8703A) was calibrated from 130 MHz to 20 GHz to normalise the RF response arising from the electrical front-end of the VNA, the RF cables and the photodetector at the optical front-end of the VNA. The response of the G-S-G-S-G probe was not calibrated and it is embedded in the measured RF response from the VNA. The output from the SG-DBR laser passed through the circulator and was sent to an optical spectrum analyser and the high-speed photodetector at the optical front-end of the VNA. The experimental setup is shown in Fig. 2.

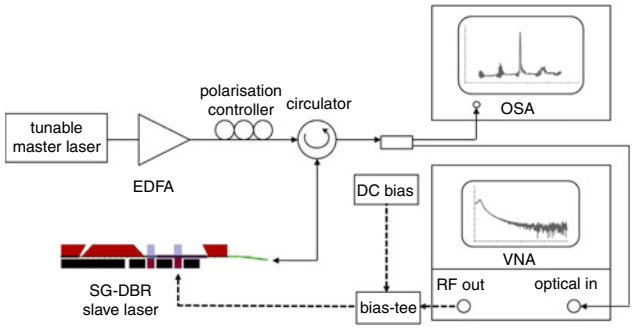

Fig. 2 *Experimental setup to study strong external injection-locking of SG-DBR laser*

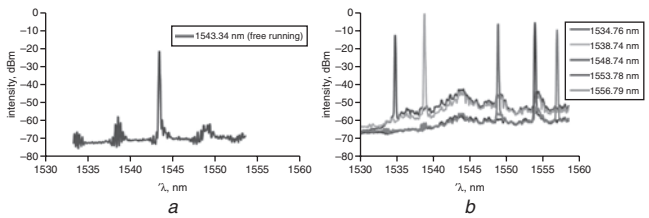

Fig. 3 *Optical spectra*

a Free-running SG-DBR laser
b SG-DBR slave laser strongly injection-locked at different wavelengths

The DC forward bias current applied to the gain section of the SG-DBR laser was 41 mA, just above its lasing threshold. In this study, no bias currents were applied to the front mirror, back mirror or the

phase section. The free-running wavelength of the SG-DBR laser was 1543.34 nm and its optical spectrum is shown in Fig. 3*a*. The output from the free-running SG-DBR laser was coupled into a lensed-fibre and the total optical power was measured to be −9.5 dBm.

To study injection-locking of the SG-DBR laser, light from a tunable external cavity laser (which acts as the master laser) was amplified using a high-power erbium-doped fibre amplifier (EDFA) and injected into the SG-DBR laser using the lensed-fibre after passing through a variable optical attenuator, a polarisation controller and the circulator, as shown in Fig. 2. The optical power of the amplified light from the master laser was increased until the SG-DBR laser could be injection-locked to the master laser for large wavelength detunings between the master and the free-running slave lasers. To get an estimate of the optical power injected into the SG-DBR laser, a reverse bias was applied to its gain section. The photocurrent resulting from the absorption of the injected light was measured to be ∼8.8 mA, which corresponds to ∼+8.65 dBm of injected light into the slave cavity. Fig. 3*b* shows the optical spectrum of the SG-DBR laser under strong injection-locking where the wavelength of the master laser is set at different wavelengths varying from 1534.76 to 1556.79 nm (corresponding to a wavelength detuning of −8.58 and 13.6 nm, respectively). It should be noted that the ability to amplify light from the master laser to achieve strong injection-locking outside the 1530–1560 nm range was limited by the gain bandwidth of the EDFA.

The direct amplitude modulation response (S_{21}) of the SG-DBR laser was characterised using an RF electrical power of −10 dBm from the output of the VNA. As shown in Fig. 4*a*, the direct modulation bandwidth of the free-running SG-DBR laser biased at 41 mA is limited by its relaxation resonance frequency of 1.05 GHz. Enhancement of the direct amplitude modulation bandwidth of the SG-DBR laser was observed under strong injection-locking over the entire locking range. Fig. 4*b* shows the direct amplitude modulation response of the SG-DBR laser that is injection-locked at different wavelengths. In each case, the relaxation resonance frequency of the injection-locked SG-DBR laser is larger than 20 GHz, which is the highest frequency that can be measured with the VNA.

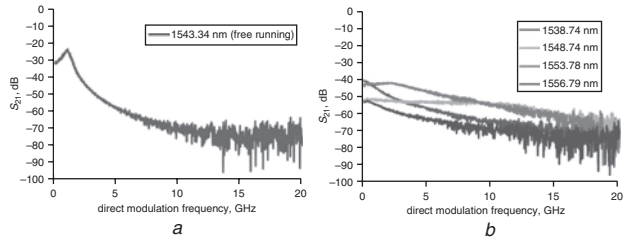

Fig. 4 *Direct amplitude modulation response*

a Free-running SG-DBR laser

b SG-DBR laser strongly injection-locked at different wavelengths

Conclusions: We have demonstrated a significant enhancement of the direct amplitude modulation bandwidth of a strongly injection-locked SG-DBR laser as the wavelength detuning between the master laser and the free-running SG-DBR slave laser is varied from −8.58 to 13.6 nm. The relaxation resonance frequency of the strongly injection-locked SG-DBR laser increases from 1.05 GHz from its free-running state to greater than 20 GHz over this wavelength detuning range.

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One or more of the Figures in this Letter are available in colour online.

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Integrated 30GHz passive ring mode-locked laser with gain flattening filter

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Abstract: We demonstrated a 30GHz integrated InGaAsP/InP ring mode-locked laser with a gain flattening filter that doubles the locking bandwidth and decreases the pulse width from 840fs to 620fs.

1. Introduction

InGaAsP/InP mode-locked lasers (MLLs) operating at 1.55µm wavelength are compact and stable pulsed sources with typically 10-100GHz repetition rates, which makes them attractive components for optical time division multiplexing (OTDM) [1], multi-wavelength sources [2], low-noise microwave oscillators [3], clock distribution systems [4], and optical samplers for electro-optic analog-to-digital conversion [5-6]. Ring MLLs based on low-cost photolithography can be integrated with a wide variety of functional elements on the InGaAsP/InP platform to build photonic integrated circuits (PICs).

Shorter pulses require wider locking bandwidth, and allow faster data rates for fiber communication, higher peak powers for clock distribution, and higher sampling rates for electro-optic analog-to-digital converters. For these reasons, there have been a multitude of studies focused on cavity design and material selection to shorten the pulse width; however we are not aware of any previous work on integrated mode-locked lasers with gain flattening filters. Gain flattening filters based on thin film dielectrics or fiber gratings are commonly used for EDFAs to correct nonuniform gain across the C-band. For this reason, there have been several studies on the use of gain flattened EDFAs in fiber mode-locked laser [7].

For mode-locked lasers with a saturable absorber region, multiple wavelengths lase simultaneously with fixed phase creating high peak-power pulses necessary to saturate the absorber. For a given material, the locked bandwidth of the mode-locked laser is limited by dispersion and gain competition due to the parabolic gain profile. By applying a filter, the net cavity gain can be flattened allowing more modes to lase. These filters can be made by standard processing on a variety of material platforms for bulk, quantum well, and quantum dot semiconductors. As dispersion is typically low for semiconductor materials and can be compensated for with an AWG [8-9], integrated gain flattening is a vital tool for dramatically increased mode-locking bandwidth.

2. Passive mode-locking at 30GHz

100µm long restricted multimode interference (MMI) couplers in a Mach-Zender interferometer (MZI) configuration were used to create an intra-cavity tunable filter as shown in figure 1. The couplers have nearly 50/50 coupling across the C-band with <1dB insertion loss, and tapered entry and exit paths to minimize reflections. A standard offset quantum well (OQW) InGaAsP/InP integrated platform is used with 7 QWs positioned above a 300nm tall 1.3Q waveguide with a confinement factor of 7.1%. A wet-etch removes the QWs for low loss passive waveguides followed by a single blanket p-cladding regrowth [10]. The total cavity length is 2600µm, the waveguide width is 1.8µm, and the total etch depth is 5µm. The device has output waveguides flared to 5µm and angled at 7° to minimize back-reflection into the cavity. The MZI filter has one 450µm gain arm with a semiconductor optical amplifier (SOA) and one 464µm phase tuning arm based on current injection to provide a ~40nm free spectral range (FSR) with a tunable extinction ratio and pole placement across the C-band. The laser threshold current was 80mA and the typical lasing power at mode-locking was ~6mW measured from the reversed biased MZI gain path.

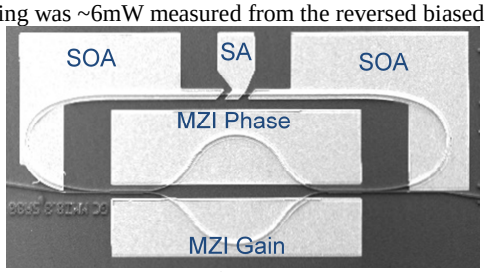

Figure 1: SEM image of mode-locked laser with an integrated MZI filter for gain flattening.

The MZI filter was turned off by applying a -5V bias to the MZI gain path which absorbed >30dB of the light propagating through it. The ring SOA drive currents and the saturable absorber (SA) bias were varied to find the most optimal pulse. The output pulse train goes through a polarization controller and erbium doped fiber amplifier (EDFA) before detection in a second harmonic generation (SHG) based Inrad autocorrelator. With the filter off, the ring SOA drive current is 158mA for -4V SA bias. The pulses are best fit by a Lorentzian distribution with 840fs FWHM shown in figure 2, along with an optical spectrum FWHM of 2nm. The filter is turned on by forward biasing the MZI gain path and adjusting the phase pad to place a zero near the previous lasing wavelength with ~1.5dB extinction ratio. With MZI SOA current of 39mA and ring SOA current of 110mA for -4.4V SA bias, the Lorentzian pulses have 620fs FWHM and an optical spectrum FWHM of 4nm, shown in figure 3. The ideal mode-locked pulses have been calculated from the measured spectral data and show good matching to a Lorentzian shape. These pulses represent the time-bandwidth limit for the locked optical spectrum. The measured pulses are 27% and 40% from this limit with the filter off and on respectively; cavity dispersion effects are likely responsible for limiting the measured pulse width, as indicated by the wider locking bandwidth producing pulses farther from ideal. The RF spectra of the mode-locked laser with the filter on is shown in figure 4 with the RF peak power >50dB above the noise floor and a -20dB linewidth of ~600kHz.

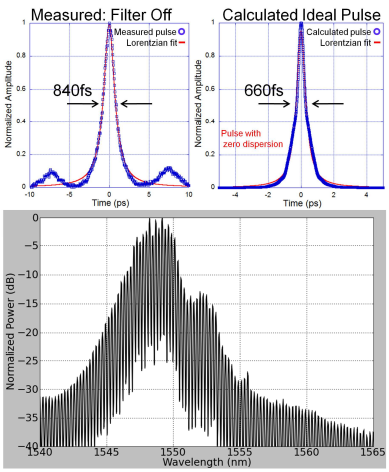

Figure 2: Filter off, measured and calculated autocorellation trace (top), optical spectrum (bottom).

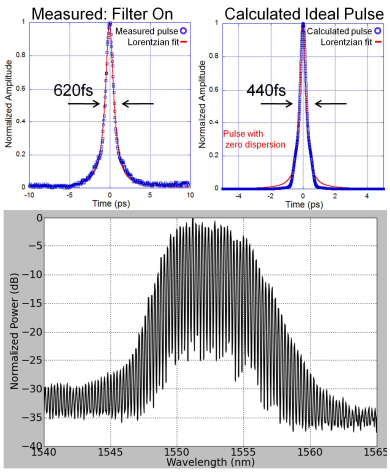

Figure 3: Filter on, measured and calculated autocorellation trace (top), optical spectrum (bottom).

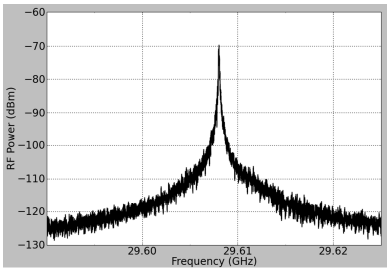

Figure 4: RF Electrical Spectrum with the filter on.

The MZI filter was characterized by injecting 3mW optical power from an external broadband ASE source into the cavity. The cavity SOAs were reversed biased to prevent resonance and nearby SOAs were turned on to provide similar levels of heating to the filter as would be experienced from the ring SOAs at lasing. The results matched well to simulations as shown in figure 5. The simulation accounted for the separate MZI phase and gain arms along with a nonuniform gain profile on the SOAs. The filter increases losses near the lasing peak; this counteracts the gain competition and effectively broadens the lasing spectra allowing more modes to lock together.

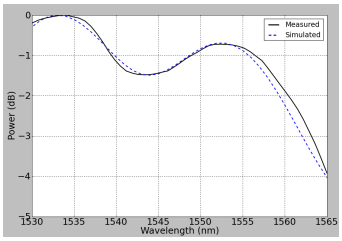

Figure 5: Measured and simulated MZI filter (39mA MZI SOA, 0mA phase pad).

An integrated ring mode-locked lasing with an intra-cavity MZI filter for gain flattening has been fabricated. The filter doubles the mode-locking bandwidth from 2nm to 4nm while decreasing the pulse width from 840fs to 620fs. The 30Ghz repetition rate, wide locking bandwidth, and narrow pulses make this device attractive for OTDM, sensing, and multi-wavelength generation, while the ring design makes it highly suitable for integration with other components in PICs.

Acknowledgment:

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II. Vertical-Cavity Surface-Emitting Lasers (VCSELs) & MBE

Wide-dynamic-range, fast-response CBr_4 doping system for molecular beam epitaxy

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The authors report the design and performance of a versatile carbon doping system for solid-source molecular beam epitaxy using carbon tetrabromide (CBr_4). This system is capable to achieve three orders of magnitude in doping by changing the CBr_4 temperature along with varying the CBr_4 leak rate into the growth chamber. The CBr_4 temperature is controlled using thermoelectric coolers and thus can be adjusted easily and quickly. The CBr_4 vapor pressure increases more than 1 decade when its temperature increases from −5 to 20 °C. The CBr_4 leak rate is controlled using six different diameter orifices connected in parallel, and the flow to each orifice can be switched on and off independently using a pneumatic valve. The fast response time of these pneumatic valves enables us to change the doping abruptly. This system is suitable for growing sophisticated structures, which require wide doping range and fast changes in doping. © *2010 American Vacuum Society.*
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I. INTRODUCTION

Compared to other *p*-type dopants in (Al)GaAs materials, such as beryllium and zinc, carbon has a very low diffusion coefficient[1] and is less dependent on the composition,[2] which make it attractive in the growths of some electronic and optoelectronic devices. Since the first successful report in 1993,[3] carbon tetrabromide (CBr_4) has become widely used as a carbon source in conventional molecular beam epitaxy (MBE). This is because high doping efficiency and high-quality films can be achieved using CBr_4. Since no carrier gas is needed for transporting CBr_4 gas, a CBr_4 doping system can be easily incorporated into MBE without modifying the existing pumping system.

For most growths, currently available CBr_4 doping systems can usually meet their growth requirements. However, these systems are not ideal for growing complicated structures which require a wide doping range and fast doping change such as vertical-cavity surface-emitting lasers (VCSELs). In order to simultaneously minimize the optical losses and electrical resistance, the distributed Bragg reflectors (DBRs) in VCSELs have to be band gap engineered. This is especially important for the *p*-DBR due to higher free carrier absorption loss and lower mobility of holes. These band-gap-engineering schemes usually involve several doping levels in the range of 10^{17}–10^{18} cm^{-3} within a DBR period, which is ~150 nm for 980 nm VCSELs.[4] Therefore, the CBr_4 doping system must be capable of changing the doping quickly to minimize the growth time. In addition, a high carrier concentration in the 10^{20} cm^{-3} is desirable for the *p*-contact layer to reduce the contact resistance. This means that the CBr_4 doping system must be operated over three orders of magnitude in doping for a single growth.

In this article, we report the design and performance of a versatile CBr_4 doping system for MBE, which addresses the requirements of wide doping range and fast doping change. Wide dynamic range is realized by changing the CBr_4 vapor pressure through a closed-loop temperature control as well as changing the CBr_4 leak rate into the growth chamber. The CBr_4 leak rate is controlled digitally by switching on and off six pneumatic valves and thus can be varied quickly.

II. SYSTEM DESIGN

Most of the CBr_4 doping systems for MBE operate similarly in principle by performing at least two main functions. One is to regulate the CBr_4 base vapor pressure, which is typically in the tens and hundreds of millitorr during operation. The other is to reduce the amount of CBr_4 injecting into the growth chamber using constrictions such as (variable) leak valves or orifices. This is necessary because the CBr_4 beam equivalent pressure less than 10^{-6} Torr is usually sufficient for most growths. Different systems use different approaches to achieve these two functions. For example, the CBr_4 base vapor pressure can be regulated directly using closed-loop pressure control or indirectly using closed-loop temperature control. The doping concentration can be ad-

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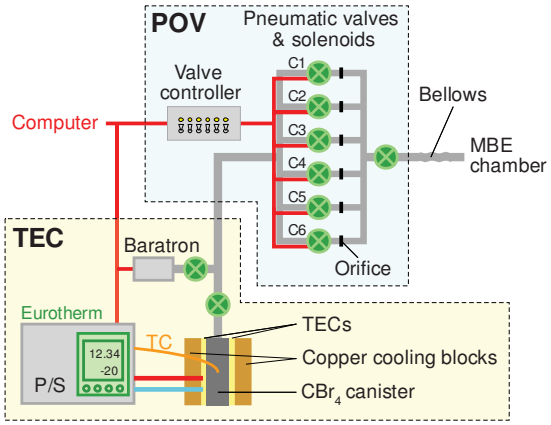

FIG. 1. (Color online) Schematic of the CBr_4 doping system.

justed by changing the CBr_4 vapor pressure or varying the leak rate, i.e., the conductance of the constrictions.

Figure 1 shows the schematic of our CBr_4 doping system, which is divided into the thermoelectric cooler (TEC) system and the parallel orifice valve (POV) system according to their functions. The TEC system is used to control the CBr_4 base vapor pressure and the POV system is used to variably reduce the amount of CBr_4 injecting to the growth chamber. In the following, we will describe these two systems in details.

A. Thermoelectric cooler system

Basically, the TEC system is a temperature-controlled CBr_4 container with the accessory electronics and plumbing as illustrated in the lower box in Fig. 1. Instead of using a water bath, the temperature of the container is controlled using TECs.[5] The core of this system is a custom-designed module shown in Fig. 2. A valved stainless steel canister, which is $25\times25\times50$ mm^3 in size, contains solid CBr_4 crystals. The canister is fairly small so that its temperature can be changed quickly. Two 25×25 mm^2 TECs are sandwiched between one side of the canister and a copper block which has cooling water running through to maintain it roughly at room temperature. There is a of total four TECs for two sides of the canister. These TECs, which have a V_{max} of 3.6 V and an I_{max} of 14.7 A at 27 °C, are electrically connected in series to have a manageable operating current. The module is wrapped with thermally insulating foam to reduce heat exchange from the environment. In addition, the whole module is enclosed in a sealed acrylic box. When the CBr_4 canister is operated below the dew point, the box has to be purged with dry nitrogen to prevent water condensation, which can thermally shorten the cold and hot sides of the TECs and significantly reduce the cooling power.

The temperature of the canister is monitored using a type-*K* thermocouple, which is spot welded on the canister and feeds into a Veeco dc power supply with a Eurotherm temperature controller. It should be noted that there are temperature gradients from the sides that the TECs touch and the monitored spot due to nonuniform cooling. In the following,

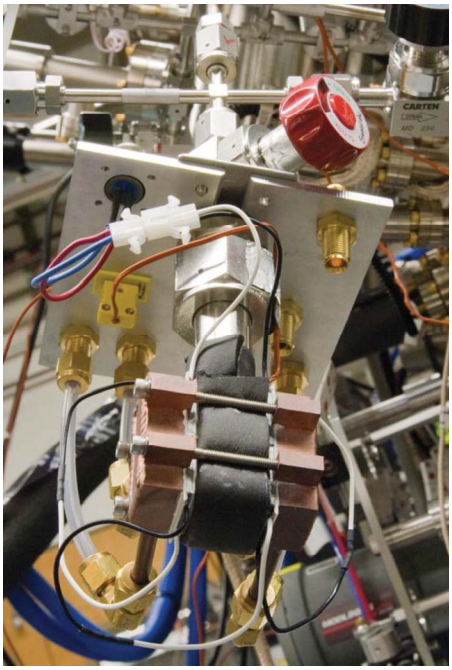

FIG. 2. (Color online) Photograph of the TEC module.

the "CBr_4 temperature" is referred to the temperature at the monitored spot unless otherwise specified. With a closed-loop control, the CBr_4 temperature can be accurately maintained within ±0.2 °C of the set point.

One of the advantages of using TECs is that heat transfer is bidirectional, which means that the TECs can either cool down or heat up the CBr_4 canister actively by reversing the direction of the current flow. However, because the power supply currently being used is unipolar, the TECs can only cool down the canister, which leads to a slower response time when warming up the canister as will be shown later.

A capacitance manometer, Baratron, was installed to monitor the CBr_4 vapor pressure when the system is in use. However, it was soon discovered that the Baratron constantly outgases hydrogen. Without any pumping, the hydrogen vapor pressure, which increases with time, contributes to the total vapor pressure read by the Baratron. Therefore, an UHV manual valve was installed to prevent hydrogen from entering the gas manifold during growth.

B. Parallel orifice valve system

Figure 3 shows a photograph of the POV system. To avoid potential inconsistency with variable leak valves at small openings, our system uses fixed orifices to achieve small conductance. As shown in the schematic in Fig. 1, the gas line from the TEC system is first split into six lines and each line has a pneumatic valve followed by an orifice with different diameters. After the orifices, these six gas lines merge together and then connect to the gas inlet on the source port through a flexible bellows. Since these air-operated pneumatic valves have a switching time in the order of hundreds of milliseconds, fast doping switching is possible.

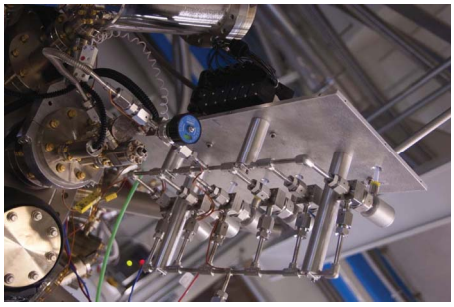

FIG. 3. (Color online) Photograph of the POV system.

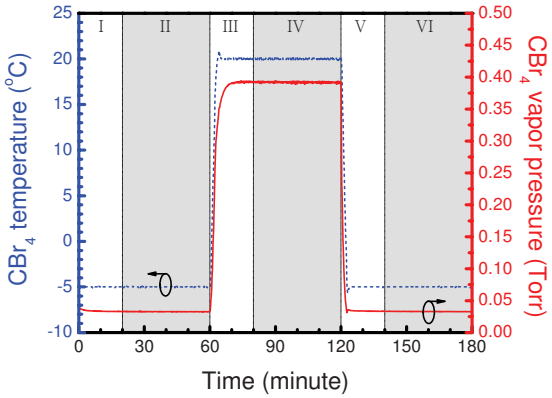

FIG. 4. (Color online) CBr_4 temperature and vapor pressure measured for 3 h. At $t=60$ m and $t=120$ m, the temperature set point was changed from −5 to 20 °C and back to −5 °C, respectively.

The idea of the POV system is quite straightforward. If these six orifices ideally have conductance of 1/2/4/8/16/32 at the given CBr_4 vapor pressure, then a total of $2^6=64$ doping levels can be achieved by permutation, provided the doping does add up. Currently, the nominal diameters of the orifices associated with pneumatic valves C1, C2, C3, C4, C5, and C6 are 250, 200, 150, 100, 75, and 50 μm, respectively. To prevent CBr_4 from condensing on the tubing, all the lines are constantly baked between 60 and 70 °C. This temperature should be low enough to avoid thermally cracking CBr_4, which should happen on the substrate.

In our system, pumps can be eliminated except through the growth chamber. This makes the system compact and also reduces the wasted source materials. This is possible because the CBr_4 vapor pressure is controlled by its temperature and can be reduced without pumping. Also, the CBr_4 flow can be completely turned off and thus does not need a pump when not in use.

III. RESULTS AND DISCUSSION

The CBr_4 doping system was characterized on a Veeco Gen III solid-source MBE system. All the calibration samples were grown at 580 °C and a growth rate of ~1 μm/h with a V/III ratio of ~30 on semi-insulating GaAs (100) substrates.

A. Thermoelectric cooler system results

For the TEC system, it is desirable that at a given CBr_4 temperature, the CBr_4 vapor pressure is stable, reproducible, and independent of the amount of CBr_4 being depleted into the growth chamber. In addition, the transient time for changing the CBr_4 vapor pressure is ideally to be short.

To evaluate the stability and transient response of the TEC system, the following experiment was performed. The CBr_4 was cooled down from room temperature to −5 °C half an hour earlier. At $t=0$, valve C5 was opened so that most of the undesired hydrogen from the Baratron can escape into the growth chamber. After 1 h, the temperature was raised to 20 °C, and finally, the temperature was lowered back to −5 °C after another 1 h. The CBr_4 temperature and vapor pressure were recorded every 10 s over the course of 3 h. The result is plotted in Fig. 4. The initial drop in the vapor pressure is due to the accumulated hydrogen being pumped out when the valve was first opened.

The CBr_4 temperatures averaged over 40 m in regions II, IV, and VI are the same as the set points and the temperature variations are within ±0.2 °C. The averaged CBr_4 vapor pressures in regions II, IV, and VI are 0.0328, 0.3920, and 0.0330 Torr, respectively. The vapor pressure increases more than ten times when the temperature increases from −5 to 20 °C. In addition, the vapor pressure variations are within ±2.5% of their averaged values, which indicates that the system is quite stable.

To see how consistent this system is, the same experiment was repeated five times at different times. Table I summarizes the averaged CBr_4 vapor pressure for three different regions over five runs. It is evident that the vapor pressure is indeed consistent at the same temperature. Although the vapor pressure in region VI is always slightly higher than that in region II, the difference is quite small and within 1%.

For a given CBr_4 temperature, its vapor pressure should ideally be maintained constant and is independent of the amount of CBr_4 being depleted into the growth chamber. Since the CBr_4 base vapor pressure is several orders of magnitude higher than the pressure after the orifices, this should be the case. To verify it, the vapor pressure at a CBr_4 temperature of −5 °C was recorded while different combinations of valves were being opened. The result is shown in Fig. 5. The difference between the worse case, i.e., all valves

TABLE I. Summary of the averaged CBr_4 vapor pressure in three 40 m periods at different CBr_4 temperatures repeated for five times.

	CBr_4 vapor pressure averaged over the region (Torr)		
	Region II (20–60 m)	Region IV (80–120 m)	Region VI (140–180 m)
Run 1	0.0329	0.3920	0.0331
Run 2	0.0329	0.3916	0.0331
Run 3	0.0327	0.3914	0.0330
Run 4	0.0326	0.3917	0.0329
Run 5	0.0328	0.3920	0.0330
Five runs averaged	0.0328	0.3917	0.0330

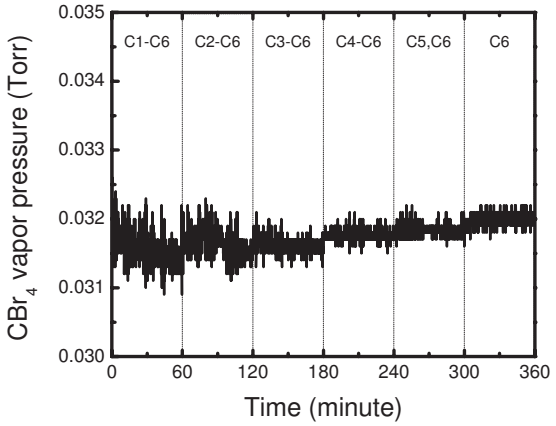

FIG. 5. CBr_4 vapor pressure with different valves being opened at a CBr_4 temperature of −5 °C. The valves that were opened for each period are labeled.

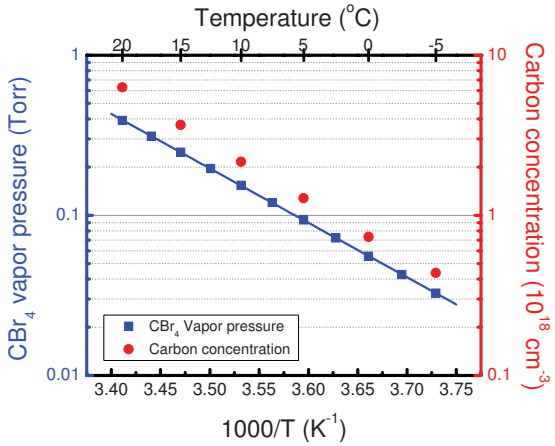

FIG. 6. (Color online) CBr_4 vapor pressure and carbon concentration measured by SIMS as a function of the CBr_4 temperature.

were opened (first region), and the best case, i.e., only the smallest valve was opened (last region), is indeed fairly small. The vapor pressure is slightly smaller than the previous value, possibly due to a lower partial pressure of hydrogen because all the valves were opened at the beginning.

To evaluate how fast the system responds to a change in the temperature set point, we analyzed the transient in regions III and V in Fig. 4. The rise time (10%–90%) and fall time (90%–10%) for the temperature changing between −5 and 20 °C are approximately 2 and 1.5 m, respectively. It should be noted that the temperature controller was optimized to provide better stability at the expense of a slower response. The rise and fall times for the vapor pressure are approximately 4 and 2 m, respectively. The reason for a slower rise time can be explained as follows. Since the equilibrium vapor pressure is determined by the lowest temperature in the canister, we need to consider how the coldest spot reaches its steady-state temperature. For active cooling, the coldest spot in the canister should be where it touches the TECs and thus, the vapor pressure drops faster. A close look at the figure reveals that the measured CBr_4 vapor pressure actually dropped faster than the vapor pressure estimated from the steady-state CBr_4 temperature (the relation between the vapor pressure and temperature will be discussed shortly). On the other hand, when the temperature set point is higher than the CBr_4 temperature, no power is provided to the TECs and the canister warms up passively. Because the heat needed to warm up the canister is transferred from the environment, the coldest spot is where the heat transfer is the least efficient and is likely not the monitored spot. When the CBr_4 temperature overshoots, the TECs start to cool down while the coldest spot has yet reached its steady-state temperature. Therefore, it takes longer time to settle due to the undesired cooling. This is why the rate of the vapor pressure increasing slowed down right after the overshoot. This spatially nonuniformity in cooling and warming up results in the asymmetry in the rise and fall times. Active heating using the TECs should improve the rise time and can be done with a bipolar power supply.

The relationship between the CBr_4 temperature and its vapor pressure is also of interest. The vapor pressure at temperatures between −5 and 20 °C in a 2.5 °C step was measured, and the result is plotted (squares) in Fig. 6. The data can be well fitted by the following equation:

$$\log_{10}(P) = 11.189 - 3398.96/T,$$

where P is the vapor pressure in Torr and T is the temperature in Kelvin. The vapor pressure at a given CBr_4 temperature is lower than what has been reported previously.[3] This can partially result from the temperature difference at the monitored and the coldest spots.

B. Parallel orifice valve system results

The POV system controls the CBr_4 leak rate into the growth chamber at a given CBr_4 vapor pressure. To predict the amount of CBr_4 leaking into the chamber, it is helpful to know the gas flow regime for the CBr_4 molecules under the operating conditions. Its mean free path is estimated to be in the order of hundreds of micron, which is close to the diameter of the orifices. Therefore, this system is operated in either the molecular flow regime or the transition flow regime, depending on the orifice sizes and vapor pressure.[6] When in the molecular flow regime, gas-wall collisions dominate. The conductance simply depends on the size of the orifices and is independent of the vapor pressure. On the other hand, the conductance in the transition flow regime also depends on the vapor pressure, and higher vapor pressure gives higher conductance.

To see how the carbon concentration varies with the CBr_4 vapor pressure, a secondary ion mass spectroscopy (SIMS) calibration sample was grown. The sample has six 200 nm GaAs:C layers grown at different CBr_4 temperatures, from 20 to −5 °C in a 5 °C step, and one 20 nm undoped GaAs layers after each GaAs:C layer. The valve that opened during the growth is C5. The SIMS result is plotted in Fig. 7. The carbon spikes at the surface and the epi-substrate interface are due to carbon contaminations from the environment. In each plateau, the concentration is fairly flat, which means

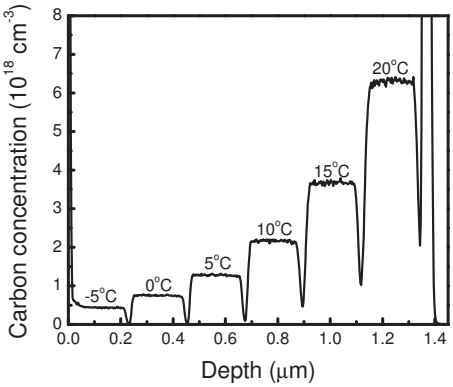

FIG. 7. SIMS profile for a structure with six GaAs:C layers grown at different CBr_4 temperatures. Only valve C5 was switched on and off during the growth. The CBr_4 temperature for each layer is labeled on the top of each plateau.

this system is quite stable. The averaged carbon concentration for each plateau is also shown as circles in Fig. 6. As the temperature increases, the carbon concentration increases faster than predicted from the vapor pressure assuming constant conductance. This can be seen in Fig. 6 that the distance between the square and circle increases at higher CBr_4 temperatures. This is because the mean free path is reduced at higher temperatures, and gas-gas collisions start to play a role in the gas flow, i.e., deviating from the molecular flow regime. The deviation should be more profound with larger orifices and higher vapor pressure.

Another SIMS calibration sample to determine the carbon concentration for different valve openings at a CBr_4 temperature of −5 °C was also grown. The result is shown in Fig. 8. The valves that were opened during each plateau are labeled on the top. The averaged carbon concentration for all the valve combinations in the sample is listed in Table II. Clearly, the CBr_4 flux from the individual valve does add up as expected since the total conductance should be the sum of the individual conductance when connected in parallel.

To see how consistent the doping concentration is, three 1-μm-thick GaAs:C calibration samples were grown on different days. The CBr_4 temperature was maintained at −5 °C

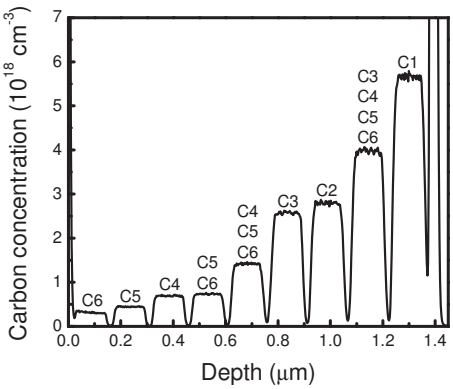

FIG. 8. SIMS profile for a structure with nine GaAs:C layers with different valves being opened. The CBr_4 temperature was kept at −5 °C. The shutters that were opened for each layer are labeled on the top of each plateau.

TABLE II. Carbon concentration for different valve openings at a CBr_4 temperature of −5 °C measured by SIMS.

Valves opened	Concentration (10^{18} cm^{-3})	Sum of individual valves (10^{18} cm^{-3})
C6	0.3	0.3
C5	0.42	0.42
C4	0.69	0.69
C5, C6	0.73	0.72
C4, C5, C6	1.42	1.41
C3	2.56	2.56
C2	2.80	2.80
C3, C4, C5, C6	3.98	3.97
C1	5.66	5.66

and valve C3 was open. The carrier densities at room temperature measured by Hall are 2.41×10^{18}, 2.41×10^{18}, and 2.47×10^{18} cm^{-3}. These values are indeed reasonably close. According to the SIMS result, the carbon concentration at the same growth condition is 2.56×10^{18} cm^{-3}, which means the electrical activation is around 95%, close to what was reported by other groups.[3]

Two more samples were grown to make sure three orders of magnitude in doping can be achieved. One was grown at a CBr_4 temperature of −5 °C with C6 open and the other was grown at a CBr_4 temperature of 10 °C with all the valves open. The carrier densities, measured by Hall, are 2.73×10^{17} and 1.14×10^{20} cm^{-3}, respectively. Almost three orders of magnitude in doping have been achieved. Lower carrier density should be possible with lower CBr_4 temperatures.

IV. CONCLUSION

A versatile CBr_4 doping system for MBE was designed, built, and characterized. By using thermoelectric coolers to control the CBr_4 temperature, accurate and stable CBr_4 vapor pressure can be achieved reproducibly. Furthermore, the vapor pressure can be changed over ten times in only 4 m. Fast switching doping is realized by independently turning on and off the flow to six orifices with different diameters using pneumatic valves. The capability to change both the CBr_4 vapor pressure and conductance to the chamber enables us to achieve three orders of magnitude in the doping concentration, making this CBr_4 doping system suitable for growing structures with sophisticated doping profiles and wide doping range.

ACKNOWLEDGMENTS

The authors would like to thank the supports and valuable discussions with the people in the MBE laboratory at the University of California, Santa Barbara.

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EFFICIENT SOURCES FOR CHIP-TO-CHIP TO BOX-TO-BOX COMMUNICATION WITHIN DATA CENTERS

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Abstract

Vertical-cavity lasers with strained active regions show increased modulation rates and reliability at lower power dissipation. However, their longer wavelength (980-1100 nm) than the standard 850 nm has inhibited their widespread adoption. Given the huge emerging markets for high-speed, high-efficiency data links, should this inhibition be overcome?

I. Introduction

Although most of the first low-threshold quantum-well Vertical-Cavity Surface-Emitting Lasers (VCSELs) were formed with strained-layer active regions having an emission wavelength in the 980 nm range [1-3], standards bodies charged with adopting them for use with multimode fiber data links, previously illuminated by 850 nm LEDs, opted to establish a standard at 850 nm where more data existed for the fibers. As the industry has grown this wavelength has become more ingrained, even as the application space has expanded well beyond the original basis for the standard.

Some, including the authors of this paper, have continued to argue for a return to the longer wavelengths due to the inherent merits of the compressively strained active regions as well as important advantages in packaging due to the transparency of the GaAs substrate. The transparent substrate enables flip-chip mounting and back-side emission, possibly with integrated micro lenses for columnated emission (i.e., Fig. 1). The key inherent advantages with compressive strain, in particular the addition of Indium to GaAs quantum-well active regions, are that one sees a reduction in material transparency current, an increase in differential gain, and a decrease in defect formation and propagation. These together lead to much more efficient devices that can operate at higher data rates and temperatures more reliably. Again, many of these advantages were clearly demonstrated in the 1990s [4-6], but as the industry was mainly focused on relatively low frequency data links, and relatively inefficient receivers were being employed, the efficiency and speed of the VCSELs were not such big issues for the mass markets.

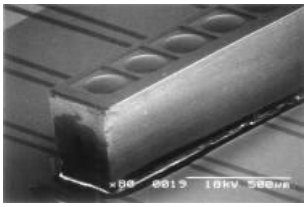

Fig. 1 SEM of flip-chipped VCSEL array with integrated 200 µm diameter microlenes

More recently, the industry has begun to focus on efficiency and speed as well as requiring very low cost. Low cost tends to equate to simple packaging, which again has been shown to be facilitated by a transparent substrate, whether in a module for chip-to-chip (e.g., Fig. 2) applications or in a package for more global interconnects. In either case, efficiency is king in a data center application. Efficiency translates to minimizing data communication power, which generally accounts for about half of the power used up in a data center.

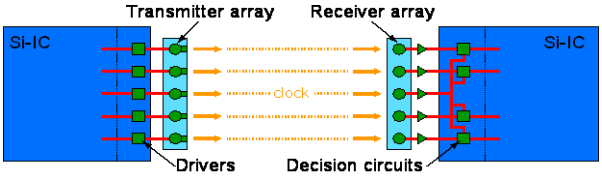

Fig. 2. Chip-to-chip optical interconnect.

Figure 3 summarizes some of the recent work with high-data rate modulation. It supports the fact that the 980 – 1100 nm VCSELs have superior temperature/speed performance. This table was contained in a paper actually focused on reliability. The older results labeled #2 and #3 in Fig. 3 suffered from relatively high series resistance, but #2 had claimed the prior record modulation efficiency of 286 fJ/bit [8] in spite of this. On the other hand, the 850 nm result of #6 represents a very well engineered device, so one would not expect much more improvement over it. We do expect still better results to be possible in the 980 – 1060 nm range as we shall discuss below.

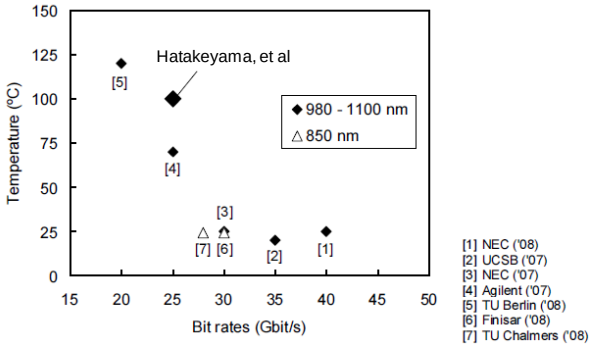

Fig. 3 High-speed direct modulation of VCSELs assembled by Hatakeyama, et al of NEC. [7]

II. Recent Work

Since our initial publication of a high-efficiency and high-speed VCSEL in 2007, as included in Fig. 3 as #2 [8], a detailed description of that VCSEL design and results has been presented in several forums [9,10]. Its schematic is shown in Fig. 4. The limiting factor in that case, besides a relatively large series resistance of 150 Ω was the appearance of additional lateral modes at a bias of approximately 1 mA, where the bandwidth was already 16 GHz. Otherwise, considerably better operation would have resulted.

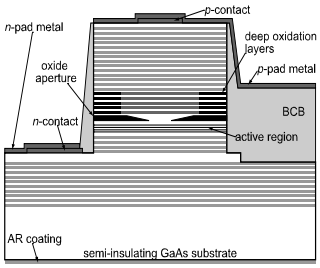

Fig. 4. Schematic of tapered oxide VCSEL that achieved 286 fJ/bit @ 35 Gb/s[8].

In order to improve upon this design several efforts have been under way. First, we have been exploring techniques to maintain single-mode operation; second, we have been working to reduce the series resistance; third, we have investigated p-modulation doping of the quantum-wells; and fourth, we have been exploring higher In content. The first two efforts are being satisfied by a change in cavity design, mostly by reducing the overall mesa diameter, but also by some other more subtle tweaks.

The effect of the p-modulation doping and increased indium content is summarized by the gain and differential gain plots of Figs. 5 & 6. Both show a remarkable improvement in all relevant parameters with indium addition. Less current is required for a given gain, and the differential gain is higher. The resonance frequency (and potential bandwidth) is proportional to the square root of the differential gain, *dg/dJ*. As can be seen there is a significant improvement in going from 850 to 980 to 1060 nm without doping. The p-doping also helps the 980 case significantly, but there is some concern that the increase in optical loss may compromise the overall performance rendering the p-doping benefit marginal.

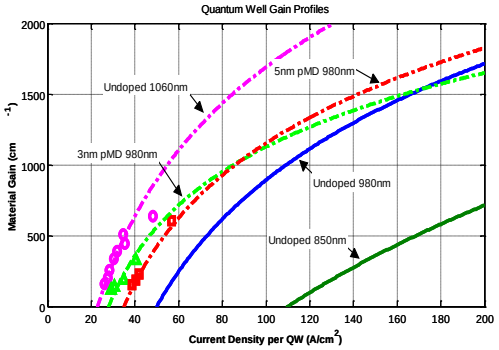

Fig. 5. Gain vs Current Density for undoped 850, 980 and 1060 nm QWs together with that of modulation-doped 980 nm QWs. Well established undoped 980 & 850nm plots from theory[11].

The potential improvement in reliability with the addition of indium is one of the most important benefits that are being sought by some researchers. Accordingly there have been some recent studies [7,12] to verify what has been assumed for many years based upon data from edge-emitting lasers and basic materials studies. The push to 1060 nm by NEC and Furukawa appears to be driven mostly by an interest in improved reliability [13]. The Furukawa study by Takaki, et al under highly accelerated conditions of T = 120˚C and J > 40 kA/cm^2, concluded that 800 years of median life at 40˚C and 6 mA could be predicted for their 1060 nm devices after some burn-in [12]. Moreover these same devices gave a new record modulation efficiency of 5.5 Gbps/mW or 182 fJ/bit.

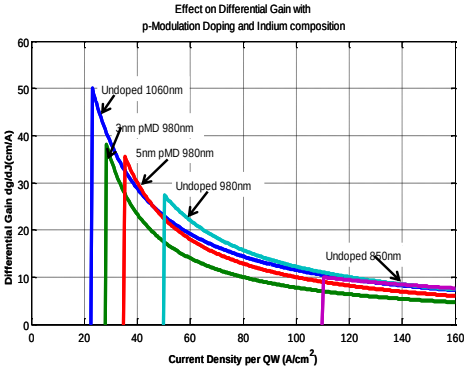

Fig. 6. Differential gains for undoped 850, 980 and 1060 nm QWs together with that of modulation-doped 980 nm QWs.

III. Conclusion

The urgent need for reliable interconnects with improved efficiency demands that the industry revisit the use of VCSELs with highly-strained active regions having wavelengths ~1060nm.

Acknowledgements

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FIRST DEMONSTRATION OF MODULATION VIA FIELD-INDUCED CHARGE-SEPARATION IN VCSELS

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Abstract — Novel three-terminal field-induced charge-separation lasers (FICSLs) in VCSEL form were designed and fabricated. The new gain modulation mechanism of hole-electron separation was demonstrated for the first time by applying a variable gate voltage with a constant injection current to the active region.

I. Introduction

High-speed, high-efficiency diode VCSELs are the cornerstones for short-haul fiber links and free-space boar-to-board optical interconnects due to their small footprints, low power dissipation, low cost, and capability of being fabricated into 2D arrays. State-of-the-art diode VCSELs lasing at different wavelengths have been reported to demonstrate above 35 Gbit/s operation and above 20 GHz bandwidth [1-3]. However, the modulation bandwidth of conventional current-modulated diode lasers is limited by double-pole roll-off of the relaxation resonance response as well as carrier transport effects [4].

In this paper, we propose a novel three-terminal field-induced charge-separation laser (FICSL). Beginning with the basic structure of a dual-intracavity-contacted diode VCSEL, a third terminal (**gate**) is added to the top n-doped DBR mirror to apply a modulation field to the active region, while the top intracavity contact is directly connected to the quantum wells of the active-n (**channel**) region for electron injection. The bottom intracavity contacted p-layer is grown beneath the active region for hole injection. A cross-sectional schematic is shown in Fig. 1. A forward DC-bias is applied between the bottom-p (**injector**) and the active-n (**channel**).

The modulation mechanism is outlined in Fig. 2a. When no bias voltage is applied on the gate, electrons and holes overlap well and the modal gain is maximized. On the other hand, when a negative bias is applied on the gate, holes are pulled toward the gate while electrons are pushed away from the gate. Consequently, the overlap between two types of carriers decreases, causing a reduction in modal gain, an increase in threshold current, and a reduction in output power for a given DC bias current.

Modeling has illustrated that this sort of modulation of the photon rate equation, rather than the carrier rate equation, results in the addition of a zero in the numerator of the small-signal response, which compensates for the dual-pole roll-off in the denominator. Also, carrier transport effects are suppressed. The net result is a vast increase in the modulation bandwidth. Additional bandgap engineering is necessary to reduce the carrier lifetime when the carriers are separated in order to flatten the small signal response as illustrated by the band diagram in Fig. 2b. Fig. 3c compares the small-signal response of a conventional diode laser using experimentally verified parameters from ref. [1] with a FICSL that has the same parameters, but takes on the design of Fig. 1. From the modeling results, one can clearly see that FICSLs benefit from the additional zero ω_z in the modulation transfer function that is lower than the relaxation resonance frequency, ω_R. As a result, FICSLs have much higher 3dB cutoff frequency than conventional

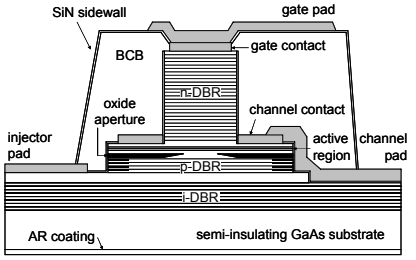

Fig. 1. Cross-sectional schematic of FICSL

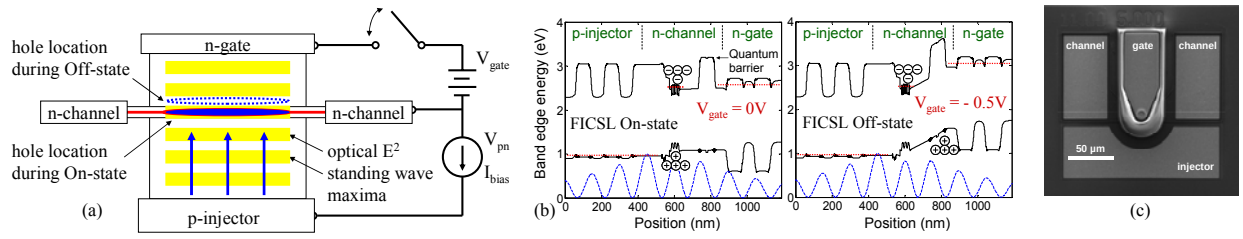

Fig. 2. (a) Operation mechanism of FICSLs showing separation of charges with bias voltage on the gate. (b) Band edge diagrams showing aligned (left figure) and separated (right figure) electron-hole pairs. (c) SEM top-view of a fabricated FICSL.

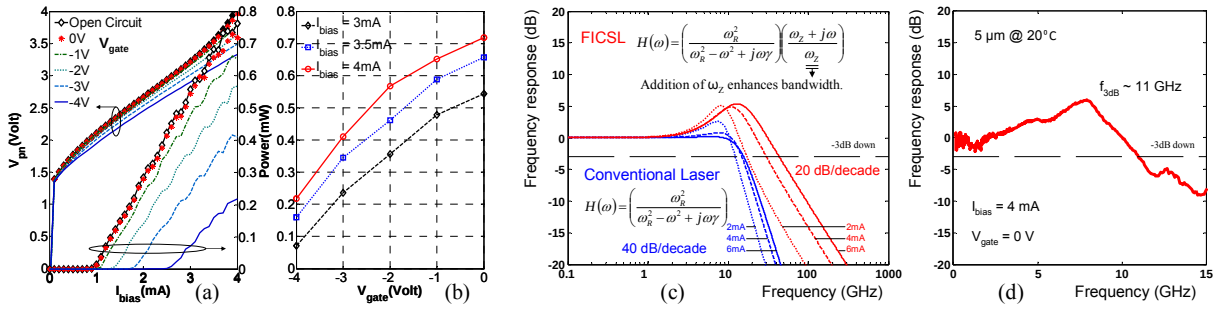

Fig. 3. (a) Room temperature CW L-I-V curves for 5μm device showing that L-I curves shift with V_{gate}. (b) L-V_{gate} curves at different I_{bias}. (c) Modeled small-signal response comparison of a conventional laser and a FICSL with same parameters and reduced carrier lifetime. Bias current I_{bias} was 2 mA, 4 mA and 6 mA. (d) Measured small-signal response for a 5 μm device.

diode lasers and slower roll-off at high frequencies (20 dB/decade vs. 40 dB/decade), making this novel field-induced charge-separation modulation extremely promising for future high-speed laser applications.

II. Device structure

The p-i-n-i-n base structure was grown on a semi-insulating GaAs (100) substrate by molecular beam epitaxy. The bottom emission design enables easy testing and flip-chip bonding to electronic ICs. The PN junction consists of a carbon-doped intracavity contact layer for p-injector, five period of p-type GaAs/AlGaAs DBR, a tapered oxide aperture layer, and three InGaAs/GaAs quantum wells with δ-doped Si in barriers as the active-n(channel) layer. The n-gate for voltage control consists of a bandgap engineered quantum barrier, Si-doped GaAs/AlGaAs DBRs and a highly-doped n-contact layer. The wafer was fabricated into double-mesa devices with high-frequency ground-source-ground (GSG) contact pads for on-wafer probing, as shown in Fig. 2c. Benzocyclobutene (BCB) was used to reduce parasitic capacitance. An anti-reflection coating was applied to reduce the reflection from the backside of the wafer.

III. Results

DC testing was done with the configuration shown by Fig. 2a. The experimental results for a 5 μm device are shown in Fig. 3a. When no bias voltage V_{gate} was applied, the FICSL demonstrated a threshold current around 1mA and output powers up to 0.8mW at an injection current I_{bias} of 4 mA. As we increased the negative bias V_{gate}, the threshold current increased while the differential quantum efficiency η_d and the output power decreased. When the bias current I_{bias} was fixed, the output power could be modulated by V_{gate}; as Fig. 3b demonstrated, with a bias current I_{bias} fixed at 3 mA, a -2±2 V swing on V_{gate} provides a 0.3±0.23 mW swing on the output. The voltage required for modulation is higher than expected due to a highly-resistive n-gate.

RF small-signal measurements were also performed to verify the modulation response. The results from a 5 μm device are shown in Fig. 3d. Due to the low output power available, performance above 15 GHz is hard to measure and the high-frequency roll-off is hard to be compared with the theoretical model. The highly-resistive n-gate also limited the RF performance and a 3dB cutoff frequency of 11 GHz was observed.

IV. Conclusion

We have demonstrated novel direct modulation mechanism via field-induced charge-separation in FICSLs that take on the form of VCSELs. By applying a field to separate the charges injected into the active region via intracavity contacts, we were able to directly modulate the gain, which promises to provide operation at higher-speeds than conventional current modulation. Experimental results verified the expected DC and RF characteristics. The highly-resistive n-gate increased the voltage required for direction modulation and decreased the RF bandwidth compared to the expected values.

V. References

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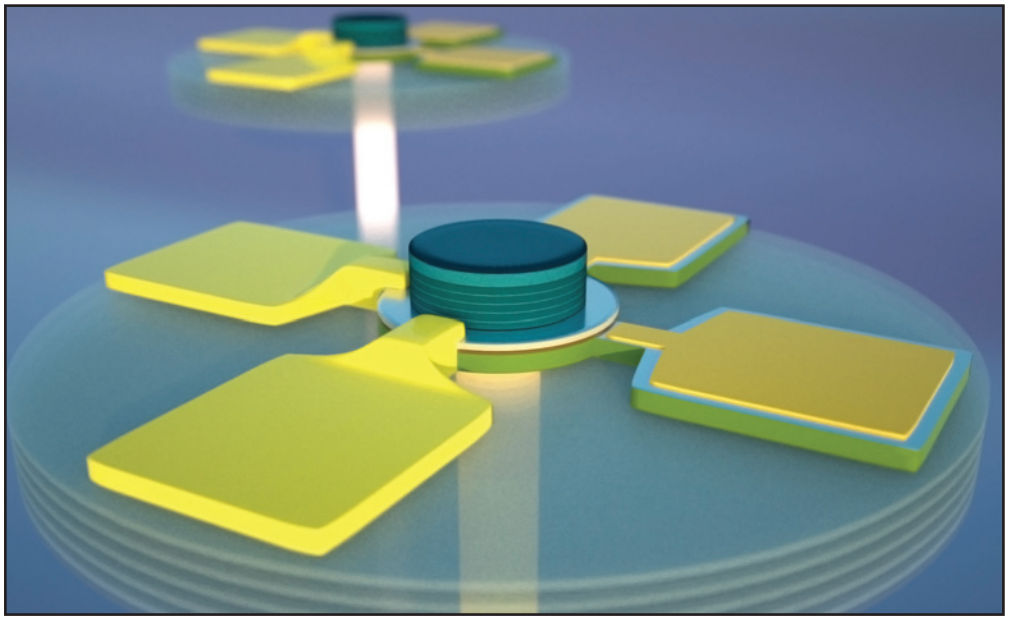
FURTHER READING
www.ece.ucsb.edu/faculty/coldren/home

Page 1619
'Large extinction ratio and low threshold dual intra-cavity contacted polarisation switching VCSELs', Y. Zheng, C.-H. Lin and L. A. Coldren

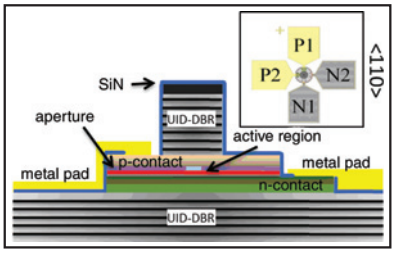
The first compact VCSEL with polarisation control shows promise for enhancing the performance of imaging and sensing systems

VCSELs take control



A vertical-cavity surface-emitting laser (VCSEL) that is capable of controlled switching between different polarisation states has been demonstrated by researchers at the University of California Santa Barbara (UCSB). The US-based team showed that, by changing the direction of the current injection in a specially designed dual intra-cavity contacted VCSEL, the output polarisation can be switched between two states. They also achieved a record low threshold current of 0.19 mA and a record high extinction ratio of >21 dB for a polarisation modulation device.

ABOVE: The VCSEL contains circular mesas that were created using a dry two-etch process, and four equally spaced vias are opened around the mesas for metal contacts
RIGHT: The epitaxial structure of the VCSEL and the orientation of the contact pads and VCSEL rotation relative to <110>



Unrealised potential

VCSELs are integral components in many applications for high-speed internet and computer communications, and they are the sources for fibre links widely used in data centres. Their small mode volume allows them to be directly modulated at very high speeds while using very little energy, and together with their small size, this makes them ideal for very-high data-rate density communication from the chip. In the near future, home-based fibre optic systems will use VCSELs to send data at high speeds between computers and home entertainment systems.

VCSELs also have great potential in many other applications that require polarisation controlled laser sources. For example, the imaging and detection of hidden objects in light detection and ranging (LiDAR) could be enhanced; and certain aerosols that show unique markers to polarised light could be easily tracked for environmental studies. In addition, by splitting the output states, data can potentially be encoded into two separate layers which increases the number of bits/symbol in next-generation optical transmission systems. Solutions to control the output polarisation have included surface gratings, asymmetric geometries or growing on off-axis wafers to force the polarisation to favour one direction over the other. However, whilst these methods have shown that polarisation stabilisation is possible, they do not offer the ability to switch to another polarisation state using the same device.

Making the switch

The dual intracavity contacted VCSEL designed by the UCSB researchers promotes asymmetric current injection along specific crystalline directions to switch the polarisation state. To improve current directionality and lower the resistance, they developed a two-etch process to fabricate the dual-intracavity contacts. The n-contact layers were electrically isolated from each other via a contact removal etch outside the mesa. The p-contact metal pads were also electrically isolated until the point of meeting the p-contact layer at the mesa. Modulation doping was used in the p-contact layer to help reduce the optical loss and this, along with the use of the intracavity contact scheme, resulted in the record low threshold current of 0.19 mA, making the VCSEL suitable for low-power applications. The large extinction ratio of >21 dB is also an advantage as it translates to a higher signal-to-noise ratio when detecting polarisation specific signatures. "These devices could conceivably be driven by a single current source whilst providing two separate polarisations," said Yan Zheng, one of the researchers in the team. "A similar system would need two separate lasers, polarising optics and drivers. The reduced size and complexity would be a great asset in densely packed data servers or in remote sensing applications where space and energy consumption is an issue."

Future directions

In their future development work, the researchers will be incorporating new designs to further electrically isolate the orthogonal current paths. They may also look at devices that incorporate both ACI and electro-optic effects. "The need for faster, more efficient optical interconnects in data centres will require new innovative lasers and this demand for high-speed data communications will spill over to the consumer market as well," said Zheng. "Streaming music, HD video and data will require reliable, low-cost and high-volume solutions. New trends in VCSEL design, such as highly strained active regions (1.1 μm), will help push high-speed operation even further while also increasing device reliability. Other advances in modulation techniques and polarisation control can help push VCSELs into new emerging markets or foster new innovative applications."

The UCSB team are also developing highly strained ultra-high-modulation-speed VCSELs and three-terminal gain-modulated VCSELs using a carrier-depletion effect.

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Large extinction ratio and low threshold dual intra-cavity contacted polarisation switching VCSELs

Y. Zheng, C.-H. Lin and L.A. Coldren

A novel dual intra-cavity contacted VCSEL capable of switching between two orthogonal polarisation states is presented. Polarisation switching is controlled by changing the current injection direction. A record-low threshold current of 0.19 mA and an extinction ratio >21dB from fit are achieved.

Introduction: Many applications ranging from consumer electronics to enterprise technologies now utilise laser sources. Vertical-cavity surface-emitting lasers (VCSELs), specifically, have shown many advantages over conventional edge-emitting lasers such as higher reliability, yield, and their ability to be put into 2D arrays. These advantages have opened up opportunities in areas such as medical imaging [1] and LIDAR [2] but polarisation controlled laser sources are required. Because the output polarisation of VCSELs does not exhibit fundamental selection rules [3], several groups have investigated asymmetric current injection (ACI) as a way to introduce gain anisotropy to control output polarisation [4–6]. That is, above threshold where there is sufficient state filling, current direction is used to provide a significant lateral carrier momentum component to control output polarisation. In this Letter we demonstrate switching between two orthogonal polarisation states via asymmetric current injection utilising a novel dual intra-cavity contacted circular mesa design. A record threshold current of 0.19 mA was achieved which is the lowest reported for a polarisation switching ACI VCSEL.

Growth and fabrication: To increase current directionality, the p- and n-contact layers were grown close together in a dual intra-cavity VCSEL structure, grown using molecular beam epitaxy (MBE), shown in Fig. 1. The device structure starts with 18 periods of unintentionally doped (UID) GaAs/AlAs on undoped (001) GaAs to form the bottom distributed Bragg reflector (DBR) mirror followed by 420 nm of Si doped GaAs for the n-contact layer. The active region consists of three 8 nm-thick $In_{0.2}Ga_{0.8}As$ quantum wells separated by 8 nm GaAs barriers surrounded by a $Al_{0.3}Ga_{0.7}As$ separate confinement heterostructure (SCH). A linearly graded AlGaAs region then forms the oxide aperture. A modulation carbon-doped GaAs p-contact layer is grown followed by 32 periods of UID$Al_{0.85}Ga_{0.15}As$/GaAs to form the top mirror.

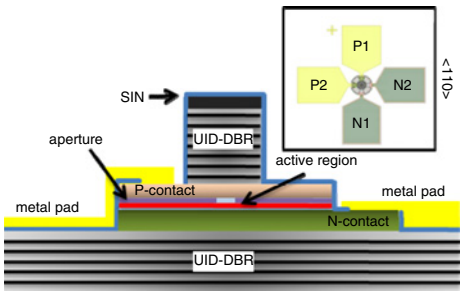

Fig. 1 *Schematic of VCSEL epitaxial structure*
Inset: Orientation of contact pads and VCSEL rotation relative to <110>

Circular mesas were created in a two-step dry-etch process that stops in the intra-cavity contact layers using a laser etch-monitor. The devices are then placed in a wet oxidation furnace to form the oxide aperture. A third etch removes the n-contact layer except from where the n-metal pads will be to help isolate orthogonal electron paths. A blanket SiN layer is deposited and four equally spaced vias are opened around the mesa for metal contacts. The pad layout is shown in the inset of Fig. 1. Completed devices have an inner mesa diameter of 13 μm and aperture of 6 μm.

Experimental results: Light output (LI) first passes through a rotating polarising lens and is then measured by a Si photodetector. The polariser transmission axis is aligned to the 0° marker on the rotational mount which is then aligned, by eye, to the $\langle 1\bar{1}0\rangle$ axis of the wafer. LI curves were taken for every 20° rotation of the polariser with either the P1-N1 or P2-N2 configuration probed. Light output of the device at a bias of 2mA is plotted against the polariser rotation angle to generate the polarisation resolved output shown in Fig. 2. The measured data for the two orthogonal current injection configurations fit very well to a sine wave with a R^2 value >0.999 and both show a polarisation rotational frequency of $2rad^{-1}$. Most importantly, the polarised outputs show a phase offset of approximately 90°, demonstrating true switching between orthogonal polarisation states.

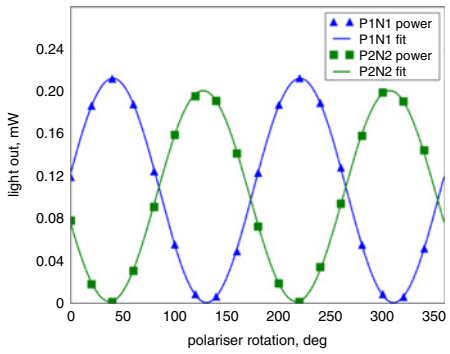

Fig. 2 *Output power at 2.0 mA showing sinusoidal dependence to polariser angle*

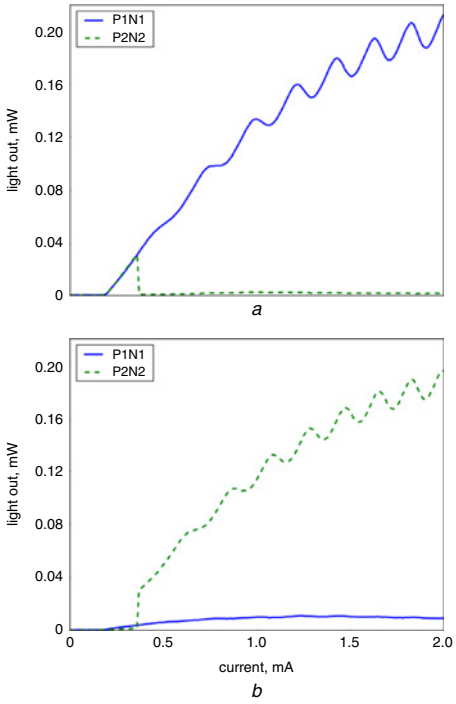

Fig. 3 *LI curves for labelled current directions with polariser transmission axis*
a 40° to $\langle 1\bar{1}0\rangle$ axis
b 120° to $\langle 1\bar{1}0\rangle$ axis

Fig. 3 shows continuous-wave (CW) light-out against current (LI) curves for two polarisation states under asymmetric current injection conditions. The threshold current is 0.19 mA for both current configurations. When injecting current between the P1-N1 pads, light output was found to be polarised close to 40° from the axis. Keeping the polariser fixed in this position and probing the orthogonal P2-N2 pads resulted in almost completely extinguishing the output. At a polariser angle of 120°, LI curves taken for both the P1-N1 and P2-N2 current injection directions are mirror opposites of that seen at 40°, shown in Fig. 3*b*. The intensity and frequency of ripples in light output increase with decreasing device size. A few devices exhibit polarisation switching at the oscillation peak or null but under 1 μs pulsed conditions these oscillations disappear. This leads us to believe that the flucuations are a result of polarisation instability from carrier heating. Maximum output power is roughly the same for both polarisations. At 2 mA bias, record extinction ratios >21dB were achieved from the fit. The near-field pattern uniformly filled the aperture and showed a diameter of roughly 13um.

Conclusion: We have demonstrated a VCSEL capable of controlled switching between polarisation states by changing the direction of current injection. The measured threshold current of 0.19 mA is the lowest reported for an asymmetric current injection polarisation switching VCSEL. A record high extinction ratio of >21dB from the fit was also achieved between orthogonal polarisation states.

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One or more of the Figures in this Letter are available in colour online.

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III. Fabrication Technology & Photonic Crystals

Deep and tapered silicon photonic crystals for achieving anti-reflection and enhanced absorption

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Abstract: Tapered silicon photonic crystals (PhCs) with smooth sidewalls are realized using a novel single-step deep reactive ion etching. The PhCs can significantly reduce the surface reflection over the wavelength range between the ultra-violet and near-infrared regions. From the measurements using a spectrophotometer and an angle-variable spectroscopic ellipsometer, the sub-wavelength periodic structure can provide a broad and angular-independent antireflective window in the visible region for the TE-polarized light. The PhCs with tapered rods can further reduce the reflection due to a gradually changed effective index. On the other hand, strong optical resonances for TM-mode can be found in this structure, which is mainly due to the existence of full photonic bandgaps inside the material. Such resonance can enhance the optical absorption inside the silicon PhCs due to its increased optical paths. With the help of both antireflective and absorption-enhanced characteristics in this structure, the PhCs can be used for various applications.

OCIS codes: (050.5298) Photonic crystals; (160.4760) Optical properties ; (220.4241) Nanostructure fabrication

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1. Introduction

Two-dimensional photonic crystals (2D PhCs) have been extensively studied as the building blocks to realize functional devices for optical networking [1], image display [2], bio-medical sensing [3], and photovoltaic applications [4]. The artificial periodic structures can be used to control the behavior of photons for its photonic bandgap (PBG) and/or light diffraction properties. Recently, as an emerging field, disordered nanopillar arrays are used to improve the efficiency of solar cells through its reduced optical reflection, enhanced absorption and enhanced carrier collection efficiency [5,6]. Tapering of nanopillars could further improve the antireflection and enhanced absorption properties [6,7]. With the help of ordered nanopillars, optical absorption can also be enhanced through multiple excitation resonances [4]. However, to develop a rapid, large-area and high-resolution fabrication scheme for realizing tapered and highly-ordered 2D nanopillars is a challenge.

In this work, we develop a simple technique for directly transferring holographically generated photoresist (PR) patterns into silicon by using a novel single-step deep reactive ion etching (SDRIE) technique. This technique can realize 2D silicon photonic crystals with a high aspect ratio, good uniformity and a tapered sidewall profile without scalloping. The resultant PhC samples are then characterized by using a spectrophotometer and an angle-variable spectroscopic ellipsometer [8–12]. Reflection spectra of this PhC structure under different incident angles and polarizations are measured for observing its antireflection and optical resonant effect. Optical resonance is mainly due to the existence of PBG inside this material. A spectroscopic ellipsometer is also used for further verifying this unique PBG phenomenon. Analysis of the PhC structure with rigorous coupled-wave analysis (RCWA) method, taking the dispersion and absorption of materials into account, is used for verifying the experimental data. It is found that such resonance will enhance the absorption inside the pillars, thus can be potentially used for PhC-based photovoltaic devices.

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2. Sample preparation

Synthesis of silicon nanopillar arrays has been investigated in the literatures using various patterning and etching techniques [13–15]. Fabrication of sub-wavelength antireflective structures with tapered sidewall profile was also studied [16]. However, most of them require a metal hard mask formed mostly by lift-off process for the following deep etching. This additional lift-off step will degrade the resolution of the patterned profile and increase process complexity. Deep reactive ion etching (DRIE) can be used for micro-electro mechanical systems (MEMS) and micro-fluidic device fabrication. Multiple-cycles of the cyclic Bosch process enable anisotropic etching of silicon with high mask selectivity (>200:1 for silicon oxide and >75:1 for photoresist) and high etching rate (several μm per min) [17]. However, this technique is not suitable for etching nanostructures due to its scalloping of the sidewalls (the peak-to-valley height is typically the scale of around several hundred nanometers). Recently, with the development of this technology, X. Wang et al. have applied Bosch etching to realize submicron trenches [18] while C.-H. Choi et al. have shown the possibility to control the sidewall profile of nanostructure array by tuning the parameters of Bosch process [19]. More recently K. J. Morton et al. have demonstrated high-aspect-ratio pillar arrays with optimized Bosch conditions and the scalloping of the sidewalls has been minimized to around 10 nm [20]. Nevertheless, due to the cyclic etching/deposition nature of Bosch process, we can still see the periodic "ripples" on the sidewalls of the best pillars. The scalloping effect will become serious for deeper pillar arrays. To prepare a photonic crystal sample for anti-reflection and/or enhanced absorption, it is desired to avoid the scalloping effect during DRIE process.

In this work, 2D periodic templates with a hexagonal lattice of elliptical geometry are realized using the holographic lithography with a double exposure and a 60-degree sample rotation over a large area [21]. The purpose of using the hexagonal lattice is to obtain a broader PBG area; even though its geometry is elliptical [22]. With an optimized process procedure, the width of the resultant patterns can be adjusted and fine tuned by controlling the total exposure energy and development time [21]. A Plamsa-Therm 770 SLR series system with a loadlock is used to transfer PhC patterns directly from the PR mask into silicon. The system allows to independently controlling the plasma density and ion energy. It is dedicated to deep etching in silicon by using the cyclic Bosch process. However, due to the alternative passivation and etching nature of the Bosch process, scalloping of the sidewalls appears in the etched patterns. We developed a SDRIE process with a controlled mixture of $Ar/SF_6/C_4F_8$ gas to attain smooth and controllable sidewalls while simultaneously keeping the advantages of high etching rate (~222 nm/min) and high mask selectivity (~85:1). Figure 1(a) shows the comparison of process flow between standard Bosch process and SDRIE process. Polymer deposition for protecting lateral sidewalls and deep silicon etching proceed simultaneously in SDRIE process. The slope of etched sidewall profile can be easily controlled by engineering the composition of gas mixture.

Figure 1(b) shows the overall process for fabricating silicon photonic crystals. A silicon substrate is cleaned and an antireflection coating (ARC) layer (XHRiC-11 ARC from Brewer Science) is deposited by spin-coating at 3000 rpm for 30 seconds. After pre-baking ARC layer on a hot plate at 165 degrees for 60 seconds, a positive PR layer is deposited at 3000 rpm for 30 seconds and soft baked at 90 degrees for 90 seconds. The sample is then transferred to the laser holography system and exposed twice with a dose of 30.24 mJ/cm^2 for each exposure. Following the double-exposure, a post-exposure bake is performed on a hot plate at 115 degrees for 120 seconds to further reduce the standing-wave effect in the resist sidewalls. The sample is then developed to attain a periodic template. Transferring the PR patterns into bottom ARC layer is then carried out by anisotropic O_2 plasma using a conventional reactive ion etching machine with an O_2 flow of 10 sccm, a pressure of 10 mTorr, and a RF voltage of 250V. Figure 2(a) shows the SEM photos of the 2D PR/ARC templates. The height, lattice constant, and ellipticity (ratio between major- and minor-axis of

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ellipse) of the resultant patterns are around 250 nm, 375 nm and 1.41, respectively. Samples with a hexagonal lattice and high uniformity are demonstrated over a large area.

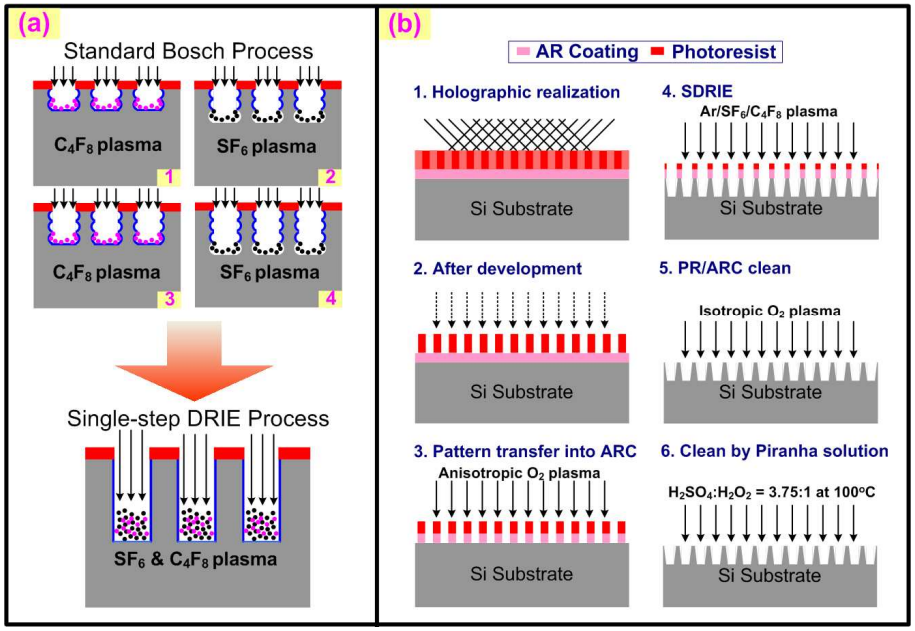

Fig. 1. (a) comparison of process flow between conventional Bosch process and SDRIE process (b) fabrication procedures of silicon photonic crystals by holographic lithography and SDRIE

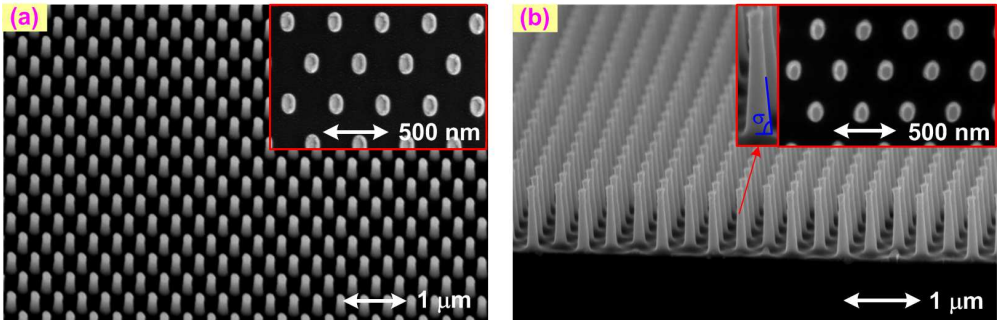

Fig. 2. SEM photos of (a) resultant 2D PR/ARC templates and (b) resultant 2D silicon photonic crystals

The substrate is then etched by SDRIE using the PR/ARC pattern as a hard mask. For the mechanism of this reactive gas mixture, isotropic etching of the silicon is carried out by SF_6/Ar plasma while sidewall protection is carried out by plasma deposition of C_4F_8. Balance between etching and deposition is the key to attain patterns with vertical sidewalls. However, in this work, less SF_6 (26 sccm) and more C_4F_8 (54 sccm) is used to obtain tapered nanostructures. For comparison, a non-tapered silicon photonic crystal sample is fabricated by using similar process conditions but with 28-sccm SF_6 and 52-sccm C_4F_8 flow rate. For both etching recipes, the pressure in the chamber is set to be 19 mTorr. The power of the RIE generator and ICP are fixed at 9 W and 850 W, respectively. Selectivity between silicon and PR/ARC mask is about 85:1 for both etching recipes. After dry etching, the remaining PR/ARC is removed by isotropic O_2 plasma with an O_2 flow of 20 sccm, a pressure of 80

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mTorr, and a RF voltage of 250V. Finally, the substrate is cleaned with a Piranha solution (H_2SO_4:H_2O_2 = 3.75:1 by volume with a lifted temperature of 100 degree Celsius).

The tapered silicon photonic crystal is 800 nm tall with a slope (the tangent of σ, the angle of slope) of 15.4, an average ellipticity of 1.6228, and a filling factor (averaged radius-to-period ratio) of 0.146, as shown in Fig. 2(b). The non-tapered reference sample is 850 nm tall with vertical sidewalls of which the slope is about 143, corresponding to an angle σ of about 89.6°. It has an average ellipticity of 1.63 and a filling factor of 0.167. The resultant PhC sample is highly uniform over the entire sample area, around 1 cm^2, as shown in Fig. 4(a). The size of the PhC patterns will be limited by the exposed area of the holographic setup.

3. Optical characterization

The optical properties of the etched samples are characterized by a spectrophotometer and an angle-variable spectroscopic ellipsometer. Figure 3(b) shows the photograph of the angle-adjustable (30° to 90°) spectroscopic ellipsometer which consists of a xenon lamp light source, a monochrometor, a beam chopper, a sample stage with a goniometer base, and a detector with a rotating analyzer. All components are connected to a control module which can be controlled via a computer. In this setup, reflection spectra under different incident angles can be measured by changing the angle θ of this system. Reflection spectra along the symmetric points of hexagonal silicon PhCs can also be obtained by adjusting the sample orientation ϕ. In this experiment, the light beam that is polarized parallel (perpendicular) to the plane of incidence, is named TM (TE) polarization, as indicated in Fig. 2(b). In contrast, TE_{phc} (TM_{phc}) refers to the direction of optical resonance of the PhCs that is parallel to the pillars (silicon substrate).

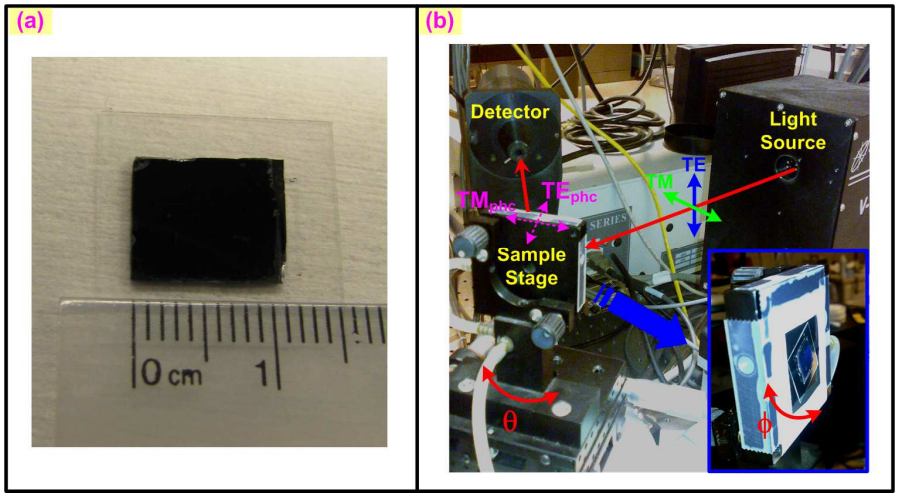

Fig. 3. (a) photo of the resultant PhC sample (b) photograph of the testing setup

Figure 4(a) shows the close-to-normal (8-degree) incident optical reflection spectrum of bare silicon, 2D PR/ARC templates on silicon, and tapered and non-tapered silicon photonic crystals that are measured by using a spectrophotometer with an un-polarized light source. Lower reflectivity of 2D PR/ARC templates is due to its lower effective index which serves as a buffer layer between air and silicon substrate. Dips at around 365 nm of wavelength as well as in the ultraviolet (UV) region are due to the absorption characteristic of the ARC. The tapered silicon photonic crystals has a much lower reflectivity than the bare silicon over a wide wavelength range due to its deeper sub-wavelength structure and gradually changed effective index between air and silicon. Slight optical resonant effect can be seen at the wavelengths of 1200 nm, 550 nm and UV region in Fig. 4(a). By combining those effects, the

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overall reflectivity of this tapered nanostructure under 8-degree incidence is below 10% in the entire UV-to-visible region and is only around 2% in the wavelengths between 500 nm and 600 nm. On the contrary, a narrower AR window and higher minimum reflectivity (~5%) is observed for the non-tapered nanostructure. This verifies that the use of tapered rods can reduce the reflection and enlarge the bandwidth of AR window due to its gradually changed effective index. The reflection spectrum of non-tapered PhCs is slightly red-shifted because of its taller and wider pillar structure.

Figure 4(b) shows the PBG diagram of the silicon PhC structure, calculated by using the 2D plane wave expansion method (2D-PWE) [23]. Due to the noncircular geometry of the silicon photonic crystals, the use of new directions to represent one quarter of the Brillouin zone (Γ-K-M-Γ-K-M'-Γ-K'-M'-Γ) is necessary for PBG calculation as well as for its characterization [22]. The broad TE_{phc}-mode PBG area shown in Fig. 4(b) indicates the existence of full PBGs in this structure. To investigate the optical resonance in this silicon PhC structure, angular dependent zeroth-order reflection spectra along these symmetry points are measured by using the testing setup shown in Fig. 3(b).

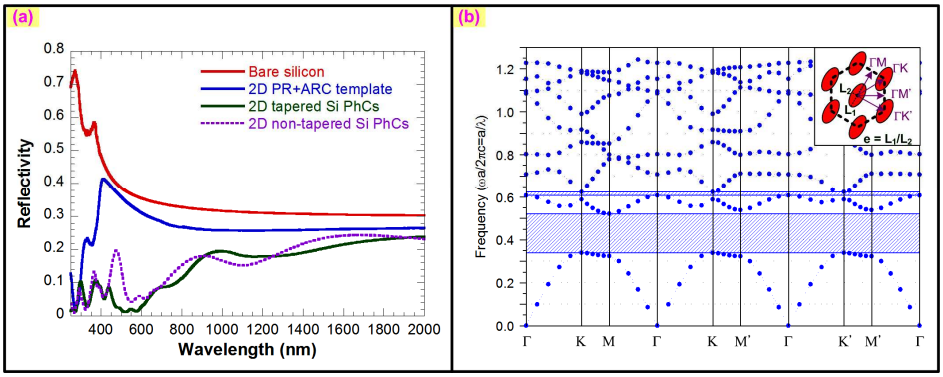

Fig. 4. (a) Measured optical reflection spectrum of bare silicon, 2D PR/ARC templates on silicon, tapered and non-tapered silicon PhCs with close-to-normal (8-degree) incidence (b) Calculated TE_{phc}-mode PBG diagram of our silicon photonic crystals

Figure 5 shows the measured angled-incident reflection spectra along symmetry points of the hexagonal silicon PhCs for the TM- and TE-polarizations. Reflection spectra of bare silicon under the same experimental conditions are also measured for comparison. Noise in the reflection spectra at the wavelength ranges between 900 nm and 1000 nm is due to the turnover of the monochrometor. The reflection of bare silicon for TE-polarization increases as the incident angle rises, while the reflection for the TM-polarized light reaches minimum at the Brewster angle (about 70 degrees). Once a tapered PhC sample is employed, the incident light will couple into the local resonance modes (TE_{phc} and TM_{phc}) of PhCs. For oblique incidence with TE-polarized light, the light will be only coupled into the TM_{phc} resonance of PhCs. Only slight resonance is found from the corresponding reflection spectra. This is partly due to the lack of full PBG for TM_{phc} mode in the nanopillar structure. Furthermore, the tapered silicon PhC has a gradually changed effective index and serves as a good buffer layer between air and silicon substrate for the TE-polarized light. This results in a broad and angular-independent antireflective window between 400 and 700 nm of wavelength. The measured reflectivity at 40- and 70-degree of incident angles in this antireflective window is below 1% and 3%, respectively. By comparing to the large reflectivity of bare silicon (around 45% and 70% at 40- and 70-degree of incident angle) for the same polarization, the tapered PhC can transmit more TE-polarized light into the silicon in both normal and angled incidence.

For TM-polarized light, the oblique incidence of light will be coupled into both TE_{phc} and TM_{phc} resonance of PhCs. The coupling efficiency of each mode depends on the incident angle. At a small incident angle, more light is coupled to the TM_{phc} mode, so the reflection

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spectrum is somewhat similar to that of a TE-polarized light. In contrast, more light is coupled into the TE_{phc} mode as the incident angle is larger. From Fig. 5(a), resonances at the wavelengths around 1100 nm and 650 nm as well as in the UV region are observed in the TM-mode reflection spectra for an incident angle of 40 degrees. The resonance becomes stronger with an incident angle of 70 degree because more light is coupled into the TE_{phc} mode. Similar resonance phenomenon is found along all symmetric points of this PhC structure. The resonance will help to trap the light inside the PhC structure and thus enhance the absorption.

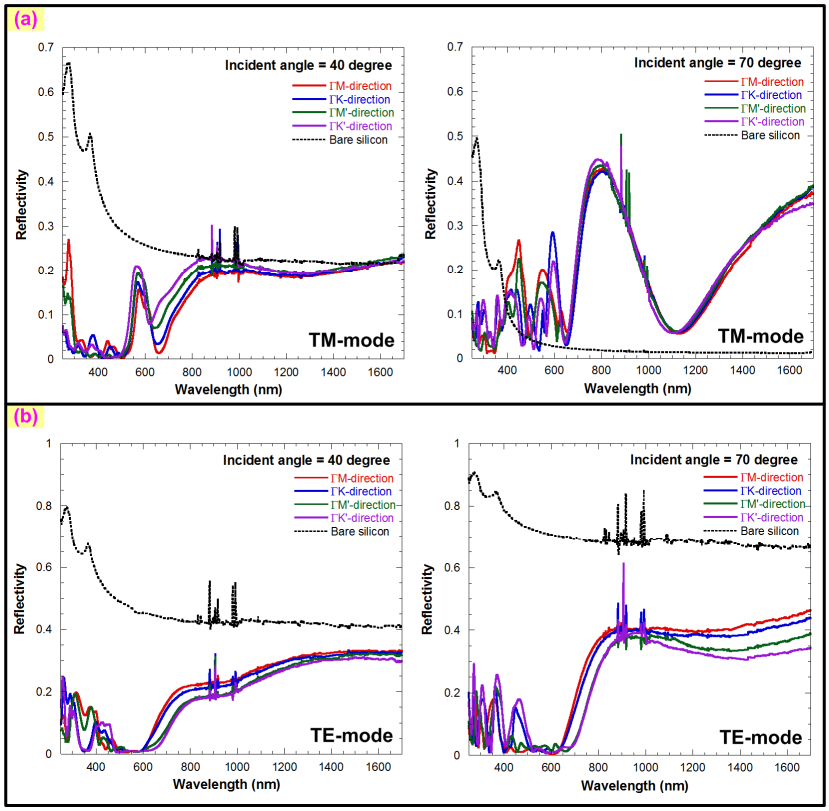

Fig. 5. Measured 40- and 70-degree angled-incident reflection spectra along symmetry points of hexagonal silicon PhCs for (a) TM- and (b) TE-polarization

Figure 6 shows the 2D contour maps of the measured reflection spectra of tapered silicon photonic crystals along ΓM-direction under different incident angles. At small incident angle, weaker resonance and low reflection is observed for both the TE- and TM-modes over the shorter-wavelength range.

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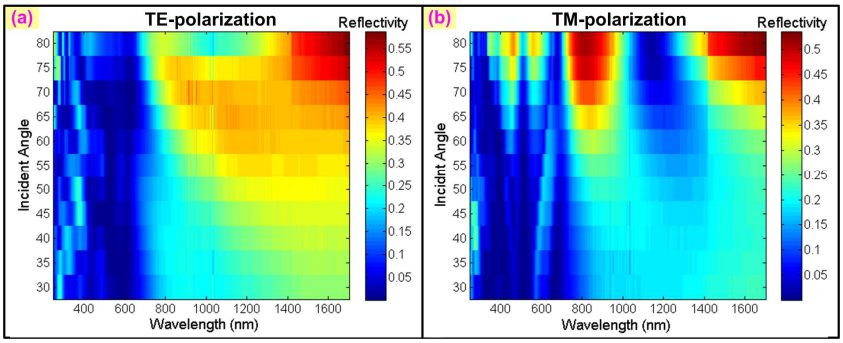

Fig. 6. 2D contour maps of measured reflection spectra of tapered silicon photonic crystals along ΓM-direction under different incident angles for (a) TE- and (b) TM-polarization incidence

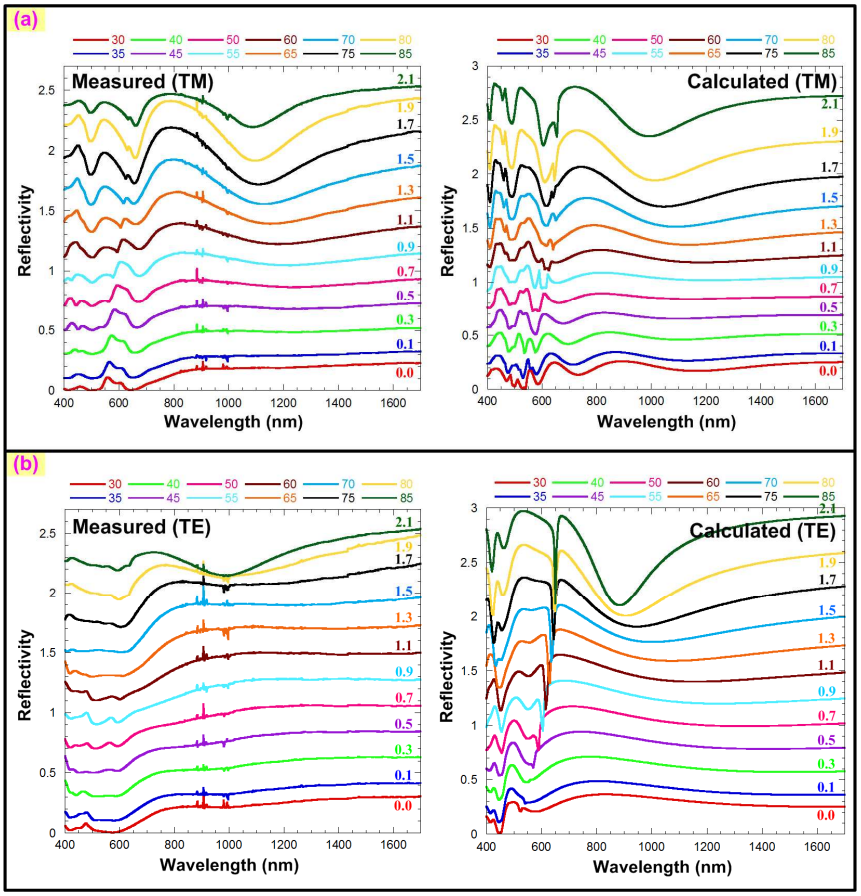

Fig. 7. Measured and calculated reflection spectra at different incident angles along the ΓM-direction of hexagonal silicon PhCs for (a) TM- and (b) TE- polarization. For clarify, the offset of curves are shown inside the plots.

The TM resonance in this structure is mainly due to the existence of PBG which causes dips in the angular reflection spectra [10]. In order to verify this effect, the PBG location is calculated by solving the Maxwell equation with rigorous coupled-wave analysis (RCWA) method. This method can account for both dispersion and absorption of materials as well as the finite-height of the fabricated silicon PhCs. The geometry of the silicon PhCs for RCWA

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simulation is set according to the real structure parameters described in Section 2 except that vertical sidewalls are assumed in the simulation model.

Figure 7 compares the measured and calculated reflection spectra under different incident angles and polarizations along the ΓM-direction of the hexagonal silicon PhCs. For clarity, the curves are offset with the value shown inside the plots. Similar behavior is found along the other symmetric points of this structure. From the dips in the measured angular reflection spectra, as shown in Fig. 7(a), the PBGs locate at the wavelengths around 650 nm and 1100 nm [10]. There is a good agreement between the experimental and calculated spectra, although measured reflection spectra show weaker resonances, especially for the TE-polarization. This is due to the tapered sidewall of the real structure which reduces the resonant effect. According to the calculated distribution of electric field in the reflection plane of this structure, the electric field for the TE_{phc} resonance confines inside the pillars while that for the TM_{phc} resonance falls between the pillars. The TM_{phc} resonance will be greatly reduced in a tapered structure. Thus for oblique TE-mode incidence, optical resonance effect is greatly reduced since all of the light will couple into TM_{phc} resonance. On the other hand, the antireflective effect due to the gradually changed effective index of this structure is dominant for the TE incidence and provides a broad and relatively angular-independent antireflective window in the visible region.

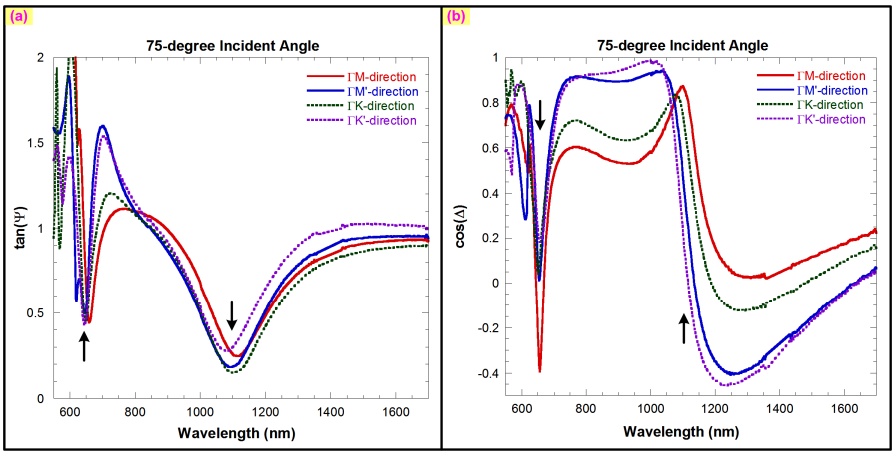

Fig. 8. Measured spectra of PBG ellipsometry parameters (a) tan(ψ) and (b) cos(Δ) along symmetry points of the hexagonal silicon PhCs. Arrows shown in the plots indicate the PBG positions.

We also use the spectral ellipsometry for characterizing the PBG of PhCs [11,12]. The ellipsometry measures two of the four Stokes parameters, which are denoted by ψ and Δ. The polarization state of the light incident upon the sample can be decomposed into a TE and a TM component. The reflection of the TE and TM components are denoted by R_{TE} and R_{TM}, respectively. The ellipsometry measures the ratio of R_{TE} and R_{TM}, $\rho = R_{TM}/R_{TE} = \tan(\Psi)e^{i\Delta}$. Here, tan(ψ) is the amplitude ratio and cos(Δ) is the phase difference through the material-light interaction. The measured ellipsometry parameters along the symmetry points of hexagonal silicon PhCs are shown in Fig. 8. For oblique incidence, the reflection of different polarized light would manifest differently in their corresponding spectra. The TE_{phc} bandgap leads to higher out-of-plane diffraction for the TM-polarized light [10], resulting in lower reflection and thus lower tan(ψ) value. Meanwhile, the TM-polarized light would increase its optical paths and corresponding lower cos(Δ) value [11]. The reflection caused by the TE_{phc}-mode PBG would then appear as a dip and a steep slope in the tan(ψ) and cos(Δ) spectra, respectively [11,12]. We indeed find similar phenomenon at the wavelengths of 650 nm and 1100 nm along the symmetry points, as indicated by the arrows in Fig. 8, verifying the existence of full TM PBGs inside the PhCs.

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One of the potential applications for tapered PhC materials is the photovoltaic devices. The angle dependence of the reflectivity can affect the energy conversion of fixed outdoor solar-cell panels, because the angle of solar irradiation varies during a day. The use of surface random textures or AR coatings can also reduce the reflectivity of the Si surface, but their AR effects have strong angle dependence, which may result in a large variation of the output power for solar cells irradiated at oblique angles. With the proposed tapered PhCs, antireflection can be obtained for both TE- and TM-polarized light with relative small-angled incidence (0-45 degree) since most of light will couple into the TM_{phc} mode of PhC. The broadband and angular-independent AR window is beneficial for coupling the input energy to solar cells. Absorption enhancement will become dominant for TM-polarized light with a large incident angle (> 45 degree) since more light will couple into TE_{phc} mode of PhC and cause optical resonance. The optical resonance, which increases the total optical paths, is vital for increasing light absorption at longer wavelengths where the absorption coefficient is small, especially for thin Si-film substrates. Meanwhile, the AR effect can still be attained for the TE-polarized light with a large incident angle. One of the possible device architectures that utilize both the antireflection and absorption effects of PhCs is to employ P-N junction inside the pillars such that the light will always touch the active layer and contribute to the photocurrent. Though the dry-etched surface may have higher surface recombination velocities and plasma-induced damage, surface passivation and/or controlled wet-chemical damage removal etches can be used to reduce the defects [24].

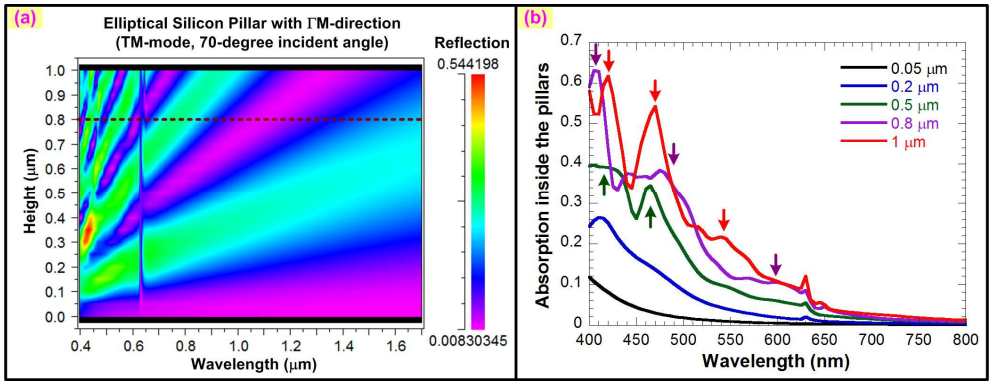

Fig. 9. Calculated 70-degree angled-incident (a) reflection and (b) absorption spectra of silicon PhCs in the TM polarization for different pillar heights. The lattice constant of PhC pillars is set to 375 nm.

4. Discussion

We further investigate the effects of pillar height on the resonance phenomenon of this silicon PhCs by using the RCWA method. The pillars are still assumed to have vertical sidewalls. Figure 9 shows the calculated reflection and absorption spectra versus pillar height for the TM polarization at an incident angle of 70 degrees. There is a dip at around 640 nm of wavelength throughout all reflection spectra in Fig. 9(a), thus enhancing the absorption as shown in Fig. 9(b). This is probably due to the multiple excitation resonance which was reported recently [4]. There are several dips in the reflection spectra that strongly depend on the pillar height. These are caused by the existence of PBG. The dash line shown in Fig. 9(a) indicates the case for the fabricated 800-nm tall PhC structures. The overlap of dips that are caused by the multiple excitation resonance and PBGs are found in Fig. 9(a). The enhancement on the optical absorption is stronger for taller pillars, especially for the wavelengths within the PBGs. Arrows shown in Fig. 9(b) indicate the locations of PBGs. For the case of 0.8 μm tall PhC pillars, optical absorption at 500-600 nm wavelength bands is enhanced. Since the location of dips in the measured reflection spectra shown in Fig. 7(a) are

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similar to the calculated ones, we can expect that the enhanced absorption in the fabricated PhC pillars also follows the calculated curve shown in Fig. 9(b).

Figure 10 shows the calculated reflection and absorption spectra against the lattice constant for the TM polarization at an incident angle of 70 degrees. It can be found from Fig. 10(a) that the multiple excitation resonance depends strongly on the lattice constant of the PhC structure. On the contrary, the PBG position can be fine tuned by simply changing the lattice constant of the PhCs. The PBG moves toward longer wavelength as we increase the lattice constant of the PhCs, thus red-shifting the enhanced absorption, as shown in Fig. 10(b). Arrows shown in Fig. 10(b) indicate the location of PBGs. However, the PBGs disappear in the UV-to-visible region as the lattice constant of PhCs is larger than 500 nm. Therefore, PhCs with a lattice constant of less than 450 nm are considered to be a better choice for enhancing the optical absorption over the visible wavelengths.

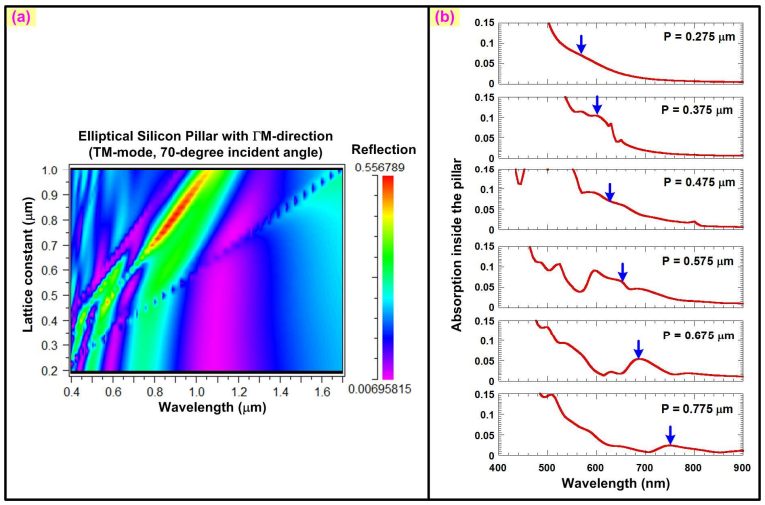

Fig. 10. The variation of the calculated (a) reflection and (b) absorption spectra of silicon PhCs with the lattice constant (P), along the TM polarization at 70-degree incident angle. The height of PhC pillars is set to 800 nm.

5. Conclusion

We fabricated deep and tapered silicon photonic crystals and demonstrated their anti-reflection and enhanced absorption characteristics. To realize such structures with high resolution and fast process time, we developed a technique to directly transfer the holographic generated PR/ARC patterns into silicon by using a novel SDRIE scheme with a controlled mixture of $Ar/SF_6/C_4F_8$ gas. Tapered and tall (800-nm high) silicon photonic crystals with smooth sidewall surface (no scalloping), an averaged ellipticity of 1.6228, and a filling factor of 0.146 is realized with high uniformity over the entire sample area.

Reflection spectra of this PhC structure under different incident angles and polarizations are measured for observing its optical characteristics. For small incident angles, the PhCs has low reflectivity over the visible wavelengths for both TE and TM modes. The tapered PhC structure that has a gradually changed effective index serves as a good buffer layer between air and silicon, resulting in a broad antireflective window. This effect is especially beneficial for the TE-polarized light, and the antireflective window can be obtained over a large incident angle. On the other hand, strong optical resonances for TM-mode are found in this structure, which is mainly due to the existence of full PBGs inside the material. This PBG phenomenon is further verified by the spectroscopic ellipsometry. Such strong resonance will greatly enhance the optical absorption inside silicon PhCs. According to the RCWA simulation results, enhanced optical absorption is found for taller silicon PhC pillars, especially for the wavelengths within the PBGs, and can be fine tuned by changing the lattice

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constant of the PhCs. PhCs with a lattice constant of less than 450 nm are considered to be a better choice for enhancing the optical absorption over the visible wavelengths. With the help of both antireflective and absorption-enhanced characteristics in this structure, this PhC material can be used for various applications.

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Realization of silicon nanopillar arrays with controllable sidewall profiles by holography lithography and a novel single-step deep reactive ion etching

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ABSTRACT

A simple and efficient approach for fabricating silicon nanopillar arrays with a high aspect ratio and controllable sidewall profiles has been developed by using holographic lithography and a novel single-step deep reactive ion etching. During the etching process, scalloping of the sidewalls can be avoided while reserving the high mask selectivity and high etching rate. Besides, the sidewall angle of resultant patterns can be adjusted by tuning the composition of the gas mixture of single-step DRIE process. We further fabricate a tapered silicon nanopillar array and observe its photonic bandgap property. We believe that the good optical performance of this tapered silicon nanopillar array realized by the proposed approach shows the promising of this process for various applications.

INTRODUCTION

Silicon nanopillar arrays have been extensively used in many emerging technologies including bio-medical sensing [1], chemical sensing [2], and electronic field emission [3] via a large surface-to-volume ratio, optical wave-guiding [4, 5] via photonic bandgap properties, field effect transistors [6] via sub-100-nm single-crystalline silicon features, and antireflection coating on silicon [7, 8] via a lower effective index. Except for bottom-growth techniques, a sequence of patterning and etching processes is usually required to realize nanostructures in semiconductors. For patterning, most of nanostructures are realized using electron-beam lithography, covering only a small area. The disadvantages of being time consuming and with very low throughput are also the shortcomings for this technique. Nanoimprint lithography shows potential to replicate patterns with high throughput. But the key concerns of overlay, defects, and template patterning will distort the profile of the resultant patterns and degrade its uniformity. On the other hand, holographic lithography is an attractive method for periodic pattern generation with high regularity over a large area. Holographic system only requires easy-attainable and relatively inexpensive optical components to generate uniform interference patterns without using any mask. For etching, numerous methods have been reported for attaining high-aspect-ratio nanostructures. However, most of them require a metal hard mask formed mostly by lift-off process for the following deep etching [9-12]. This addition lift-off step will degrade the resolution of the profile and increase process complexity. Recently, self-masked dry etching technique is proposed by depositing nanosized clusters formed by reactive gas mixtures [13, 14]. However, the resultant nanostructure arrays are lack of regularity. Deep reactive ion etching (DRIE) is mainly used for micro-electro mechanical systems (MEMS) and microfluidic device

fabrication. Multiple-cycles of the two-step Bosch process enable anisotropic etching of silicon with high mask selectivity (>200:1 for silicon oxide and >75:1 for photoresist) and high etching rate (several μm per min) [15]. However, this technique is not suitable for etching nanostructures due to its scalloping of the sidewalls (the peak-to-valley height is typically the scale of around several hundred nanometers). Recently, with the development of this technology, X. Wang et al. have applied Bosch etching to realize submicron trenches [16] while C.-H. Choi et al. have shown the possibility to control the sidewall profile of nanostructure array by tuning the parameters of Bosch process [17]. More recently K. J. Morton et al. have demonstrated high-aspect-ratio pillar arrays with optimized Bosch conditions and the scalloping of the sidewalls have been minimized to around 10 nm [18]. Nevertheless, due to the alternative etching/deposition nature of Bosch process, we can still see the periodic "ripples" on the sidewalls of the best pillars to date. The scalloping effect will become serious with increased etching depths of patterns.

In this work, we have realized two-dimensional (2D) resist templates by using holography lithography with a double exposure and a rotation of samples before the second exposure. An analysis model is developed and an antireflection layer is used for eliminating the back-reflection from the substrate. To keep the advantages of high mask selectivity and high etching rate in the Bosch process but avoiding its scalloping effect, we have developed a mean of directly transferring photoresist patterns into silicon by using a single-step deep reactive ion etching (SDRIE) with a controlled mixture of $Ar/SF_6/C_4F_8$ gases. The influence of the composition of gas mixture to the resultant profile is also investigated. Optical characterization of SDRIE-realized silicon nanopillar array is also performed.

FABRICATION APPROACHES

Holographic realization of resist template

For 2D resist template realization, a holography setup based on a two-beam interference principle shows much attractive due to its simplicity and flexibility. A hexagonal array with a circular shape can be realized by triply exposing the same interference pattern with the sample rotated by 0°, 60° and 120°, respectively. Unfortunately, this method suffers from the alignment issue for realizing hexagonal structures in large area [19]. On the contrary, if a double exposure of two-beam interference is executed at 0° and 60°, one can fabricate 2D periodic structure with a hexagonal lattice of elliptical geometry. Figures 1 (a) and (b) show the interference patterns of the 1^{st} and 2^{nd} exposure steps on the sample. A 60-degree tilted interference pattern is obtained by rotating the sample before 2^{nd} exposure. The resultant 2D intensity distribution on the sample and the final pattern after development are shown in Figure 1 (c) and (d), respectively. Although the shape of resultant pattern is elliptical, there still exists a broad photonic bandgap inside this structure [19]. The width of the resultant patterns can be adjusted and fine tuned by controlling the total exposure energy and development time [20]. The relatively simple fabrication procedures and experimental setup of this method will improve the manufacturing yield, thus reducing the cost.

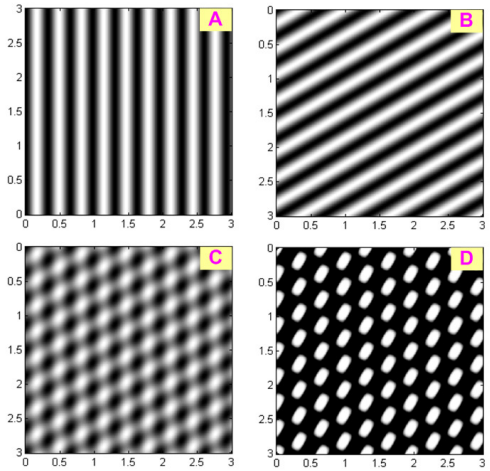

Figure 1 Schematic diagram of process procedures for realizing hexagonal 2D resist template by means of two-beam interference principle with double-exposure steps.

Single-step deep reactive ion etching

For silicon etching, we use a Plamsa-Therm 770 SLR series system with a loadlock for deep etching silicon pillars. The system has an inductively coupled plasma (ICP) coil and a capactively coupled substrate RF supply to independently control plasma density and ion energy in the system. This system is dedicated to deeply etching in silicon for MEMS structures using conventional Bosch process which cycles between a polymer deposition cycle using C_4F_8 gas (no substrate bias) and an etching cycle using a SF_6 mixture with substrate bias. However, due to the isotropic etching nature of SF_6 dry etching, scalloping of the sidewalls results from this process. We have developed a SDRIE process with a controlled mixture of $Ar/SF_6/C_4F_8$ gas to avoid this scalloping issue while simultaneously keeping the high etching rate and high mask selectivity. Figure 2 shows the comparison of process flow between conventional Bosch process and SDRIE process. Polymer deposition for protecting lateral sidewalls and deep silicon etching proceed simultaneously in SDRIE process. With an optimized gas mixture for balancing the deposition and etching rate, pillars with vertical sidewalls can be realized.

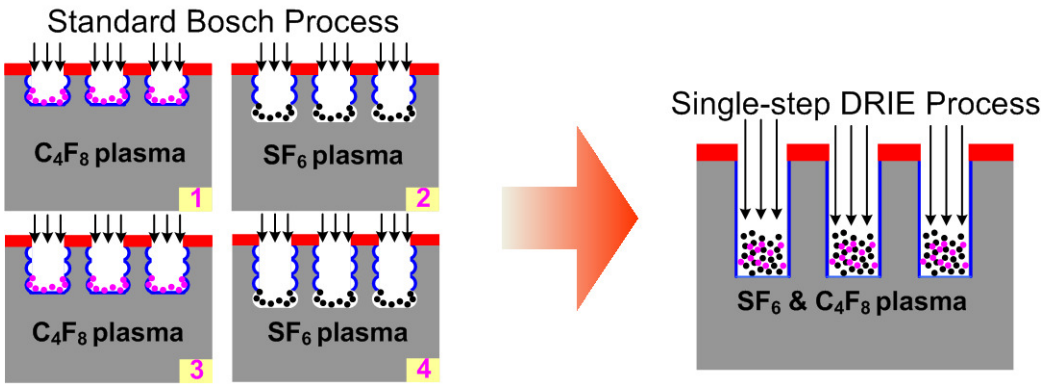

Figure 2 Comparison of process flow between conventional Bosch process and SDRIE process

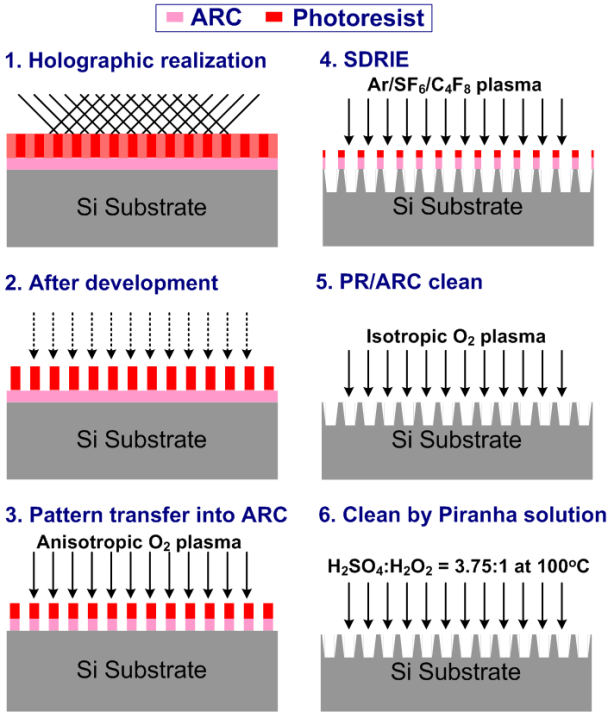

Figure 3 Fabrication procedures of silicon nanopillar arrays by holographic lithography and SDRIE process

Fabrication procedures of silicon nanopillar arrays

Instead of using a thin photoresist (PR) layer (~20 nm) for holography [17] which may limit the final etched height of silicon pillars, a thick PR template with a periodicity of 350 nm and an aspect ratio of 2 is fabricated uniformly over a large area with the help of antireflection coating [20]. Figure 3 shows the overall process for fabricating silicon nanopillar arrays by holographic lithography and SDRIE process. A silicon substrate is cleaned by ultrasonification in acetone and iso-propanol and blown dry with nitrogen gas. An antireflection coating (ARC) layer is deposited by spin-coating at 3000 rpm for 30 seconds. After pre-baking the ARC layer on a hot plate at 165 degrees for 60 seconds, a positive PR layer is deposited at 3000 rpm for 30 seconds and soft baked at 90 degrees for 90 seconds. The sample is then transferred to the laser holography system and exposed twice with a dose of 30.24 mJ/cm^2 for each exposure. Following the double-exposure, a post-exposure bake is performed on a hot plate at 115 degrees for 120 seconds to further reduce the standing-wave effect in the resist sidewalls. After that, the sample is dipped into developer for 10 seconds to attain a periodic structure. After development, the sample is clean by rinsing it in de-ionized water. The sample is finally hard-baked to complete the cross-linking process. Transferring PR patterns into bottom ARC layer is then carried out by anisotropic O_2 plasma using a conventional reactive ion etching (RIE) machine with an O_2 flow of 10 sccm, a pressure of 10 mTorr, and a RF voltage of 250V. The substrate is then etched by SDRIE using the PR/ARC pattern as a hard mask. After SDRIE, the remaining PR/ARC is removed by isotropic O_2 plasma with an O_2 flow of 20 sccm, a pressure of 80 mTorr, and a RF voltage of 250V. Finally, the substrate is cleaned with a Piranha solution (H_2SO_4:H_2O_2 = 3.75:1

by volume with a lifted temperature of 100 degree Celsius). The resultant structures are then characterized using a scanning electron microscope (SEM).

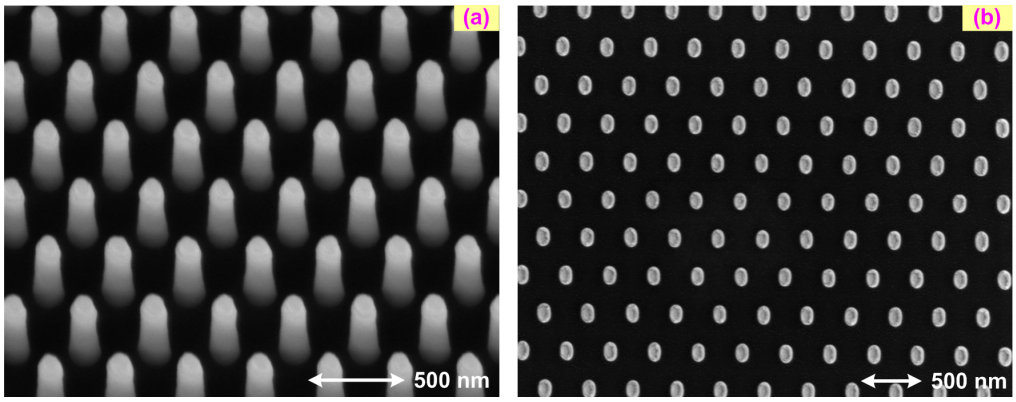

Figure 4 (a) Tilted and (b) top SEM views of resultant 2D PR/ARC templates

Results and discussion

Figure 4 shows the tilted and top SEM views of resultant 2D PR/ARC templates after holographic exposure and anisotropic O_2 plasma etching. The diameters of the resultant patterns are around 147 and 104 nm for major- and minor-axis of ellipse, respectively. The height of this template is around 250 nm. Samples with a hexagonal lattice, high uniformity and vertical sidewalls are demonstrated over a large area.

For pattern transferring into silicon, different mixtures of reactive gases are used to understand how it will affect the resultant slope of sidewall profiles. Detail process conditions are listed in Table 1. Sidewall angle is defined as the inner angle of the pillar. The cross-section and tilted SEM views of the corresponding samples are shown in Figure 5. For the mechanism of this reactive gas mixture, isotropic etching of the silicon is carried out by SF_6 plasma while sidewall protection (lateral etching suppression) is carried out by plasma deposition of C_4F_8. Balance between etching and deposition steps is the key to attain high-aspect-ratio patterns with vertical sidewalls. In this experiment, we fix the flow of Ar gas and the total flow of C_4F_8 and SF_6 to 20 and 80 sccm, respectively. The pressure in the chamber is set to be 19 mTorr. The power of RIE generator and ICP are fixed at 9 W and 850 W, respectively. The flow of C_4F_8 increases from 50 to 54 sccm while the flow of SF_6 decreases from 30 to 26 sccm. Total etching time for each process condition is varied in order to attain pillars with almost the same height. The different etching rate is due to different flow combinations of C_4F_8 and SF_6 gas mixture (More SF_6 or less C_4F_8 will have higher silicon etching rate). Due to excess SF_6, the width of the resultant pattern in Figure 5 (a) changes from 113 nm at the top to 62.7 nm at the bottom, resulting in a sidewall angle of 92.4 degree. On the contrary, with excessive C_4F_8, the width of the resultant pattern in Figure 5 (c) changes from 31.3 nm at the top to 157 nm at the bottom, resulting in a sidewall angle of 84.1 degree. Almost vertical sidewalls on the resultant patterns can be realized with balanced etching/deposition rate. The widths of the resultant pattern in Figure 5 (b) are almost the same between the top (109 nm) and the bottom (117 nm), resulting in vertical sidewalls with a sidewall angle of 89.6 degree. The etching rate of silicon under this

process recipe is around 222 nm/min. It should be noted that smooth sidewalls on the resultant patterns are observed in Figure 5, showing that SDRIE can really avoid the scalloping effect. Samples under those SDRIE conditions are highly uniform over a large area. Besides, Figure 5 also shows that the sidewall angle can be adjusted by tuning the composition of gas mixture. We currently achieve an 8-degree tunable range of sidewall angles for this 350 nm spaced 2D nanostructure. This profile tuning range is limited by the width of nanostructure.

Table 1 Profiles of resultant patterns under different DRIE process conditions

Silicon nanopillars	SDRIE process conditions				Resultant profiles	
	Time (min)	C_4F_8 (sccm)	SF_6 (sccm)	Ar (sccm)	Height (μm)	Sidewall Angle (degree)
Sample (a)	3	50	30	20	1.2	92.4
Sample (b)	5	52	28	20	1.11	89.6
Sample (c)	14	54	26	20	1.22	84.1

* The pressure is set to be 19 mTorr. The power of RIE generator is fixed at 9 W while the power of the ICP is fixed at 850 W.

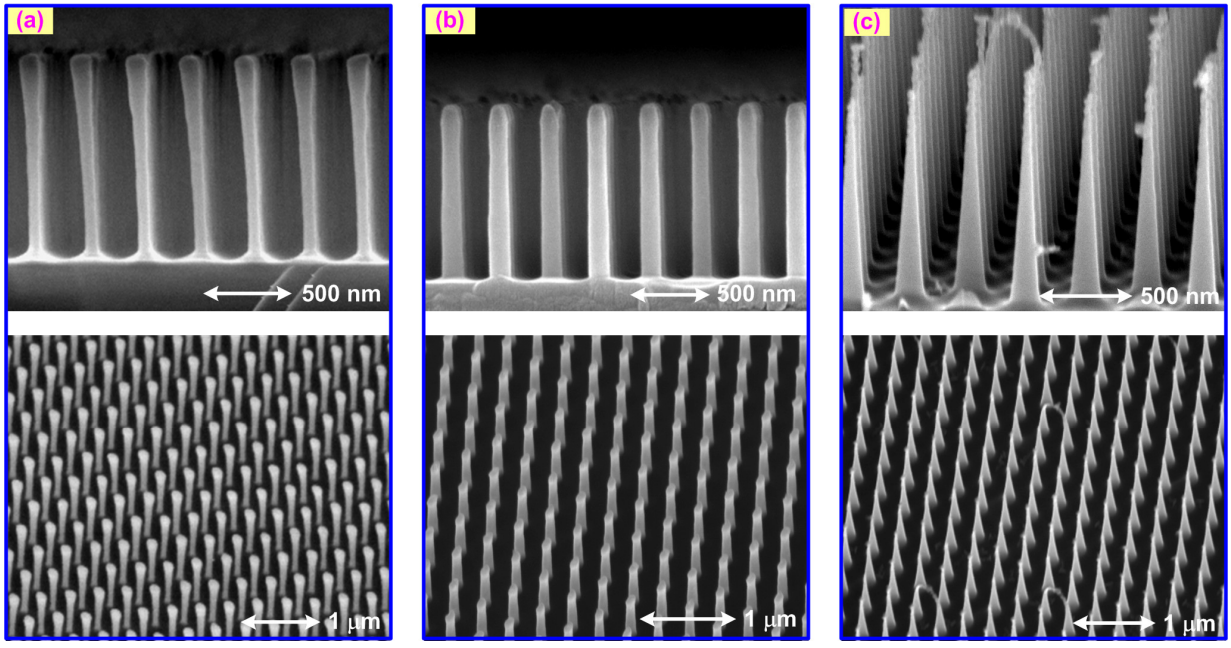

Figure 5 Cross-section and tilted SEM views of resultant profiles under different process conditions

Mask selectivity is also an important factor for the SDRIE process. Figure 6 (a) shows the cross-section SEM view of the original PR template after holographic exposure and development. The thickness of PR pattern and ARC layer are 270 nm and 120 nm, respectively. After transferring patterns from PR into ARC layer by anisotropic O_2 plasma etching, the height of the

resultant template is around 250 nm, as shown in Figure 4. Figure 6 (b) shows the cross-section SEM view of the resultant pattern after SDRIE process using the process recipe of sample (b) in Figure 5. After attaining a tall 1.11 μm silicon pillar array, the thickness of the remaining PR/ARC is still about 237 nm, corresponding to a high mask selectivity of ~85:1. It should be noted that the hard-baking of the PR and ARC before SDRIE process is the key to attain high mask selectivity between silicon and PR/ARC. The diameters of the resultant silicon pillars are around 115 and 82 nm for major- and minor-axis of ellipse, respectively. By comparing those values with that of the original PR/ARC templates, the lateral etching rate using vertical-etched recipe of SDRIE is around 4-6 nm/min.

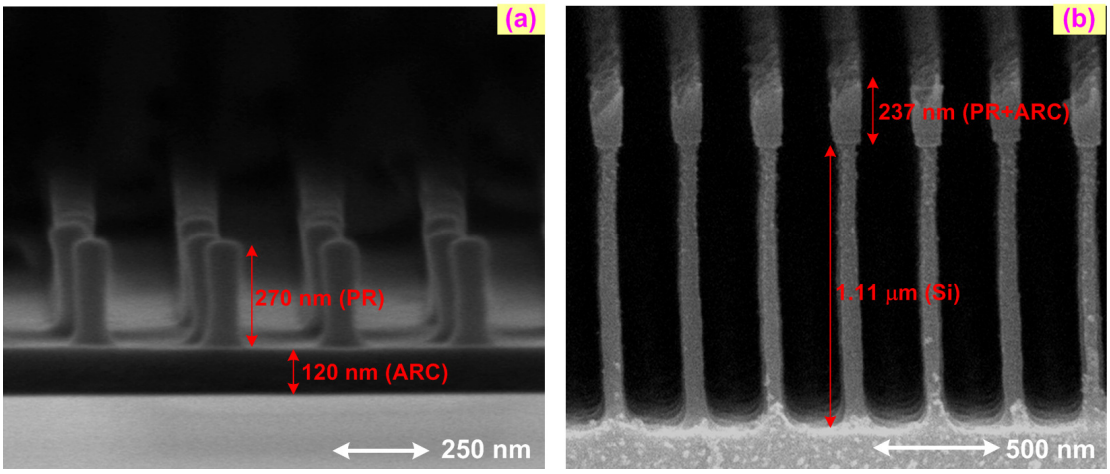

Figure 6 Cross-section SEM views of (a) the original resist template after holographic exposure and development and (b) the resultant pattern after SDRIE process using the process recipe of sample (b) in Figure 5.

TAPERED SILICON NANOPILLARS AND ITS OPTICAL PROPERTY

As we mention that the slope of etched sidewall profile can be easily controlled by engineering the composition of gas mixture. Realization of tapered silicon nanopillar array becomes possible. To verify the good quality of the resultant patterns, we fabricate a tall 800 nm silicon nanopillar array with a hexagonal lattice of elliptical geometry, a sidewall angle of 86.3 degree (tapered sidewall profile), smooth sidewalls, an averaged ellipticity of 1.6228, and a filling factor (radius-to-period ratio) of 0.146 for testing its optical property. In this case, less SF_6 (26 sccm) and more C_4F_8 (54 sccm) is used during SDRIE process to obtain tapered nanostructures. Figure 7 (a) shows the SEM picture and the photograph of the resultant silicon nanopillar array sample. This resultant nanostructure is highly uniform over the entire sample area, around 1 cm^2. Superior antireflection and enhanced absorption property of this tapered silicon nanopillar array has been mentioned in our previous work [21]. Here, the same sample is used as an example for showing the good optical performance of SDRIE-realized structure. We will focus on the photonic bandgap property of this tapered silicon nanopillar array.

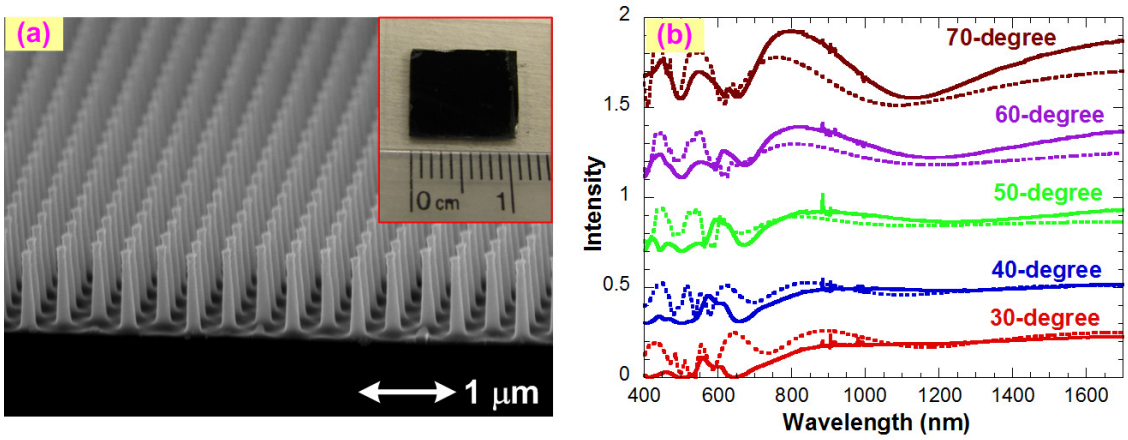

Figure 7 (a) SEM picture and photograph of resultant silicon nanopillar array sample (b) Measured (solid) and calculated (dash) reflection spectra at different incident angles along the ΓM-direction of hexagonal silicon nanopillar array for TM-polarization. The curves are offset for clarity.

Optical characterization of this resultant nanostructure is performed by using an angle-variable spectroscopic ellipsometer. Reflection spectra of this nanostructure under different incident angles and polarizations are measured for observing its optical resonant effect. It is believed that the TM resonance in this structure is mainly due to the existence of PBG which causes dips in the angular reflection spectra. In order to verify this effect, the PBG location is calculated by solving the Maxwell equation with rigorous coupled-wave analysis (RCWA) method, taking both dispersion and absorption of materials into account. The geometry of the silicon nanopillars for RCWA simulation is set according to the real structure as shown in Figure 7 (a) except the slope of sidewalls which is set to be vertical in the simulation model. Figure 7 (c) compares the measured and calculated reflection spectra under different incident angles and polarizations along the ΓM-direction of the hexagonal silicon nanopillar array for TM-polarization. The curves are offset for clarity. Similar behavior is found along the other symmetric points of this structure. From the dips in the measured angular reflection spectra, the PBGs locate at the wavelengths around 650 nm and 1100 nm. There is a good agreement between the experimental and calculated spectra, although measured reflection spectra show weaker and much complex resonances. We believe that this is due to the tapered sidewall of the real structure which reduces the resonant effect.

Spectroscopic ellipsometer is also used for further verifying this unique PBG phenomenon. The measured ellipsometry parameters along the ΓM symmetry direction of hexagonal silicon nanopillar array under different incident angles are shown in Figure 8. Parameters $\tan(\psi)$ and $\cos(\Delta)$ represent the reflection ratio between the TM and TE polarizations and the phase difference through the material-light interaction, respectively. For oblique incidence, the reflection of different polarized light would manifest differently in their corresponding spectra. Theoretically, the reflection caused by the TM photonic bandgap would appear as a dip and a steep slope in the $\tan(\psi)$ and $\cos(\Delta)$ spectrum, respectively. We indeed find similar phenomenon at the wavelengths of 650 nm and 1100 nm along the symmetry points, verifying the existence of full TM PBGs inside the material.

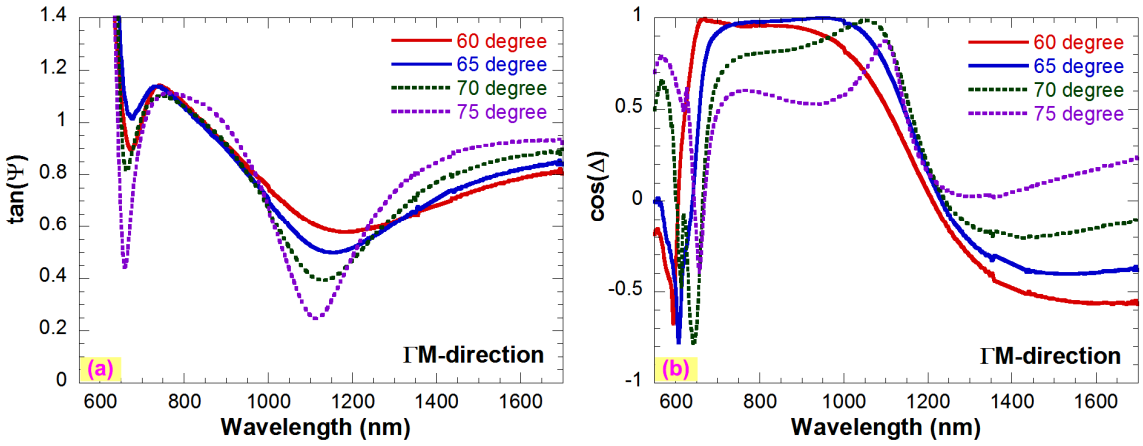

Figure 8 Measured spectra of PBG ellipsometry parameters (a) tan(ψ) and (b) cos(Δ) along ΓM symmetry direction of the hexagonal silicon nanopillar array under different incident angles.

CONCLUSIONS

We have developed a simple and efficient approach for making silicon nanopillar arrays with high regularity and uniformity over a large area. We have demonstrated that 2D resist templates realized by holographic lithography can be used as the hard mask for the following silicon etching process. Instead of using conventional Bosch process, a single-step DRIE with a controlled mixture of $Ar/SF_6/C_4F_8$ gas is used to attain smooth and controllable sidewalls on the resultant patterns while simultaneously keeping the advantages of high mask selectivity and high etching rate. A tall 1.11 μm silicon nanopillar array with an aspect ratio of > 10 and vertical sidewalls (the sidewall angle is about 89.6 degree) is realized with high regularity and uniformity. The sidewall angle of resultant patterns can be adjusted by tuning the composition of the gas mixture of SDRIE process. An 8-degree tunable range of sidewall angle is achieved in the 350 nm spaced two-dimensional nanostructure.

We further fabricate a tapered and 800 nm tall silicon nanopillar array with a sidewall angle of 86.3 degree for testing its optical property. Optical characterization of this nanostructure is performed by using an angle-variable spectroscopic ellipsometer. Reflection spectra are further verified by performing a RCWA simulation. From the dips in the measured angular reflection spectra and the dip and steep slope in the measured spectra of PBG ellipsometry parameters, full photonic bandgaps are found inside this material. We believe that the good optical performance of this tapered silicon nanopillar array realized by the proposed approach shows the promising of this process for various applications.

ACKNOWLEDGMENTS

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Antireflection and Enhanced Absorption in Tapered Silicon Photonic Crystals

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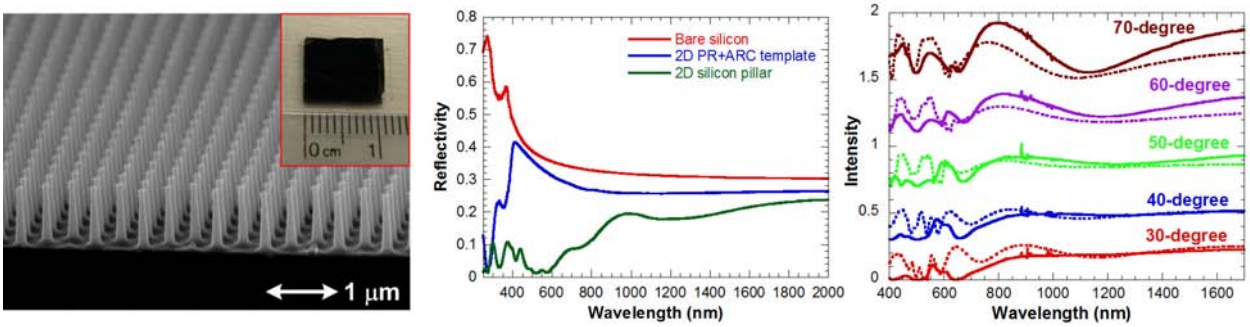
Abstract: Tapered silicon photonic crystals provide a broad and wide-angle antireflective window and strong optical resonances for enhanced absorption for TE- and TM-polarized light, respectively, showing the potential for improving the performance of photovoltaic devices.

OCIS codes: (050.5298) Photonic crystals; (160.4760) Optical properties ; (220.4241) Nanostructure fabrication

1. Introduction

Two-dimensional photonic crystals (2D PhCs) have been extensively studied as the building blocks to realize functional devices for optical networking, image display, bio-medical sensing, and photovoltaic applications. Recently, as an emerging field, disordered nanopillar arrays are used to improve the efficiency of solar cells through its reduced optical reflection, enhanced absorption and enhanced carrier collection efficiency [1, 2]. Tapering of nanopillars could further improve the antireflection and enhanced absorption properties [2, 3]. To our best knowledge, the effects of the photonic bandgap (PBG) property of 2D PhCs on the reduced optical reflection and/or enhanced absorption are rarely discussed in the literature. In our previous work, we developed a technique for directly transferring holographically generated photoresist/antireflection coating (PR/ARC) patterns into silicon by using a novel single-step deep reactive ion etching (SDRIE) technique to realize 2D silicon photonic crystals with a high aspect ratio, good uniformity and a tapered sidewall profile without scalloping [3]. However, the optical property of such structures was not resolved yet. In this work, we characterize the resultant PhC samples by using a spectrophotometer and an angle-variable spectroscopic ellipsometer. Reflection spectra of this PhC structure under different incident angles and polarizations are measured for observing its antireflection and optical resonant effect. Optical resonance is mainly due to the existence of PBG inside this material. A spectroscopic ellipsometer is also used for further verifying this unique PBG phenomenon. We also analyze the PhC structure with rigorous coupled-wave analysis (RCWA) method, taking the dispersion and absorption of materials into account, for comparison with the experimental data. It is found that such resonance will enhance the absorption inside the silicon PhC structure, thus increasing the efficiency as applying this structure for solar energy conversion.



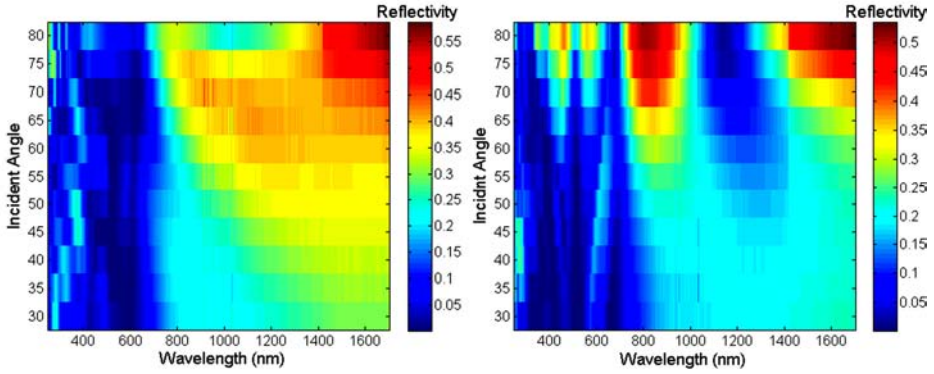
(a) (b) (c)

Figure 1 (a) SEM picture and photograph of resultant silicon photonic crystal sample (b) Measured optical reflection spectrum of bare silicon, 2D PR/ARC templates on silicon, and tapered silicon PhCs with 8-degree incidence (c) Measured (solid) and calculated (dash) reflection spectra at different incident angles along the ΓM-direction of hexagonal silicon PhCs for TM-polarization. The curves are offset for clarity.

2. Sample preparation

2D periodic templates with a hexagonal lattice of elliptical geometry are realized using the holographic lithography with a double exposure and a 60-degree rotation of samples over a large area. The purpose of using the hexagonal

lattice is to obtain a broader PBG area; even though its geometry is elliptical. With an optimized process procedure, we have shown that the width of the resultant patterns can be adjusted and fine tuned by controlling the total exposure energy and development time [4]. We developed a SDRIE process with a controlled mixture of Ar/SF6/C4F8 gas to attain smooth and controllable sidewalls while simultaneously keeping the advantages of high etching rate (~222 nm/min) and high mask selectivity (~85:1). Polymer deposition for protecting lateral sidewalls and deep silicon etching proceed simultaneously in SDRIE process. The slope of etched sidewall profile can be easily controlled by engineering the composition of gas mixture [3]. A tall 800 nm silicon photonic crystal with a positive slope (+65 nm/ m) of sidewall profile, smooth sidewalls, an averaged ellipticity of 1.6228, and a filling factor (radius-to-period ratio) of 0.146 is realized as shown in Figure 1(a). The resultant PhC sample is highly uniform over the entire sample area, around 1 cm^2. The size of PhC patterns is limited by the exposed area of the holographic setup.



(a) (b)

Figure 2 Measured reflection spectra of tapered silicon photonic crystals along ΓM-direction under different incident angles for (a) TE- and (b) TM-polarization

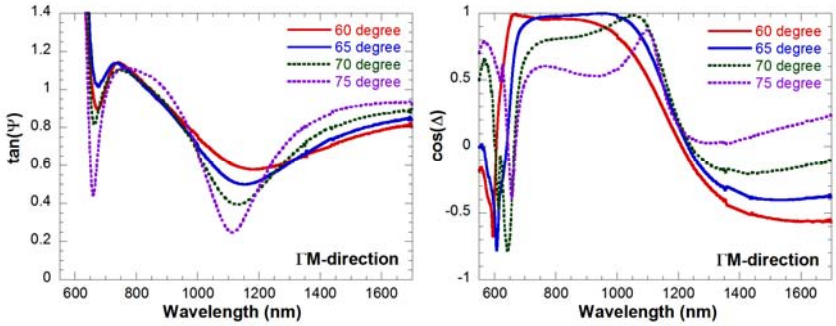
3. Optical characterization

Figure 1(b) shows the close-to-normal (8-degree) incident optical reflection spectra of bare silicon, 2D PR/ARC templates on silicon, and tapered silicon photonic crystals that are measured by using a spectrophotometer. Lower reflectivity of 2D PR/ARC templates is due to its lower effective index which serves as a buffer layer between air and silicon substrate. Dips at around 365 nm of wavelength as well as in the ultraviolet (UV) region are due to the absorption characteristic of the ARC. For the tapered silicon photonic crystal, lower reflectivity is due to its deeper sub-wavelength structure and gradually changed effective index between air and silicon. Slight optical resonant effect can be seen at the wavelengths of 1200 nm, 550 nm and UV region. By combining those effects, the overall reflectivity of this nanostructure is below 10% in the entire UV-to-visible region and is only around 2% in the wavelengths between 500 nm and 600 nm. It is believed that the TM resonance in this structure is mainly due to the existence of PBG which causes dips in the angular reflection spectra. In order to verify this effect, the PBG location is calculated by solving the Maxwell equation with rigorous coupled-wave analysis (RCWA) method, taking both dispersion and absorption of materials into account. The geometry of the silicon PhCs for RCWA simulation is set according to the real structure as shown in Figure 1(a) except the slope of sidewalls which is set to be vertical in the simulation model. Figure 1(c) compares the measured and calculated reflection spectra under different incident angles and polarizations along the ΓM-direction of the hexagonal silicon PhCs for TM-polarization. The curves are offset for clarity. Similar behavior is found along the other symmetric points of this structure. From the dips in the measured angular reflection spectra, the PBGs locate at the wavelengths around 650 nm and 1100 nm. There is a good agreement between the experimental and calculated spectra, although measured reflection spectra show weaker and much complex resonances. We believe that this is due to the tapered sidewall of the real structure which reduces the resonant effect.

Figure 2 shows the measured reflection spectra of tapered silicon photonic crystals along ΓM-direction under different incident angles. Optical characteristics of silicon PhCs are totally different than that of bare silicon. For TM-polarization, antireflective effect and slight optical resonance happen for smaller incident angles. However, the resonance becomes stronger for larger incident angles since now more light can see the periodicity of this structure, as shown in Figure 2(b). Similar resonance phenomenon is found along all symmetric points of this PhC structure.

The resonance will help to trap the light inside the PhC structure and thus enhance the absorption. Contrary to the strong resonance for the TM-incidence, only slight resonance is found for TE-incidence, as shown in Figure 2(a). This is partially due to the lack of full PBG for TE-polarized light in this tapered nanopillar structure. On the other hand, this tapered silicon PhC structure with a gradually changed effective index now serves as a good buffer layer between air and silicon substrate for the TE-polarized light, resulting in a broad and angular-insensitive antireflective window between 400 and 700 nm of wavelength. The measured reflectivity at 40- and 70-degree of incident angles in this antireflective window is below 1% and 3%, respectively. As compared to the high reflectivity of bare silicon (around 45% and 70% at 40- and 70-degree of incident angle) for the same polarization, this material will be able to transmit more TE-polarized light into the silicon in both normal and angled incidence.

Spectral ellipsometry is also used for further verifying this unique PBG phenomenon. The measured ellipsometry parameters along the ΓM symmetry direction of hexagonal silicon PhCs under different incident angles are shown in Figure 3. Parameters tan( ) and cos(Δ) represent the reflection ratio between the TM and TE polarizations and the phase difference through the material-light interaction, respectively. For oblique incidence, the reflection of different polarized light would manifest differently in their corresponding spectra. Theoretically, the reflection caused by the TM photonic bandgap would appear as a dip and a steep slope in the tan( ) and cos(Δ) spectrum, respectively. We indeed find similar phenomenon at the wavelengths of 650 nm and 1100 nm along the symmetry points, verifying the existence of full TM PBGs inside the PhCs.



(a) (b)

Figure 3 Measured spectra of PBG ellipsometry parameters (a) tan( ) and (b) cos(Δ) along ΓM symmetry direction of the hexagonal silicon PhCs under different incident angles

3. Conclusions

Reflection spectra of this PhC structure under different incident angles and polarizations are measured for observing its optical characteristics. Strong optical resonances for TM-mode are found in this structure, which is mainly due to the existence of full PBGs inside the material. This PBG phenomenon is further verified by the spectroscopic ellipsometry. Such strong resonance will greatly enhance the optical absorption inside silicon PhCs. On the contrary, with a gradually changed effective index, this structure serves as a good buffer layer for the TE-polarized light between air and silicon, resulting in a broad and angle-insensitive antireflective window in the visible region. With the help of both antireflective and absorption-enhanced characteristics in this structure, we believe that this PhC material can be used for various applications, including but not limited to the enhancement on the conversion efficiency of photovoltaic devices.

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Holographic realization of hexagonal two dimensional photonic crystal structures with elliptical geometry

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A complete investigation of holographic photonic crystal structures has been conducted. From both theoretical and experimental results, profiles of resultant patterns under different process conditions can be estimated and controlled. The use of antireflection layers is crucial for realizing submicron photonic crystals with good uniformity over a large area. We successfully realize submicron-scale photonic crystal templates on silicon substrates with an aspect ratio of 2.5 and good quality by a laser holography technique. The samples are highly uniform in an area of $>2\times2$ cm^2 and present good reproducibility. A lift-off process is performed to transfer inversed pillar patterns into a chromium hard mask for the following dry etching into silicon substrates. A single-step deep reactive ion etching with controlled mixture of $Ar/SF_6/C_4F_8$ gases is used to directly transfer pillar patterns into silicon. Transferred patterns with a high aspect ratio and vertical sidewalls (no scalloping) are demonstrated over a large area. © *2010 American Vacuum Society.*
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I. INTRODUCTION

A photonic crystal (PhC) is an artificial periodic structure that controls the behavior of photons. Since its first introduction by Yablonovitch[1] and John,[2] PhCs have been used to realize functional devices for optical networking, image display, biomedical sensing, and solar cells for the past decades. However, due to the extreme difficulty to integrate three-dimensional PhCs with other optoelectronic devices, most researchers have been focusing on the two-dimensional (2D) PhC structures. The use of e-beam lithography to realize 2D PhC structures with accurately controlled feature size is a direct and common solution. However, the disadvantages of being time consuming and having low throughput and high cost are serious shortcomings for this technique. Although nanoimprint lithography may be potentially a flexible and high-throughput solution, the key concerns of overlay, defects, and template patterning may affect the resultant pattern and its photonic bandgap (PBG) properties. On the other hand, laser holography lithography based on two-beam interference principle, has been successfully applied over 1 decade to manufacture periodic structures for a wide variety of uses. It is an attractive method for periodic pattern generation over a large area with high throughput and low cost. Although it is much harder to accurately control the location and feature size of submicron-scale periodic structures in this method, photonic crystals with slight structural variations are still suitable for many applications due to its relative wide PBGs.[3]

Some groups indeed realized 2D periodic pillars or holes by means of laser holography technique.[4–13] However, most results were fabricated either on a silicon substrate with a larger micron-level periodicity or on a glass substrate with a submicron periodicity. To our knowledge, very few groups have really attained submicron holographic PhCs on a silicon substrate. A factor that may have contributed to this is the serious back-reflection (or so-called standing wave effect) between air and silicon substrates (the refractive index is 5 for 325 nm of incident wavelength), which would otherwise degrade the process latitude. To overcome this bottleneck, a buffer material between air and silicon substrates as an anti-reflection (AR) layer is necessary to relax the back-reflection issue.

In this work, we focus on theoretical and experimental investigation of holographic photonic crystal structures on silicon substrates. Hexagonal 2D photonic crystals with an elliptical geometry are realized by laser holography with a double-exposure and a rotation of sample. An analysis model is developed to calculate the back-reflection and try to minimize it by using an AR coating layer. Thanks to the nonlinear nature of positive photoresist (PR), 2D periodic holes and pillars can be realized by controlling the total exposure energy onto the surface of photoresist. How the profile is affected under different development time is also investigated. After successfully realizing photonic crystal templates, a lift-off process is performed to transfer pillar patterns into a chromium hard mask with inversed structures for the following reactive ion etching (RIE) into silicon substrates. A single-step deep reactive ion etching (DRIE) with controlled

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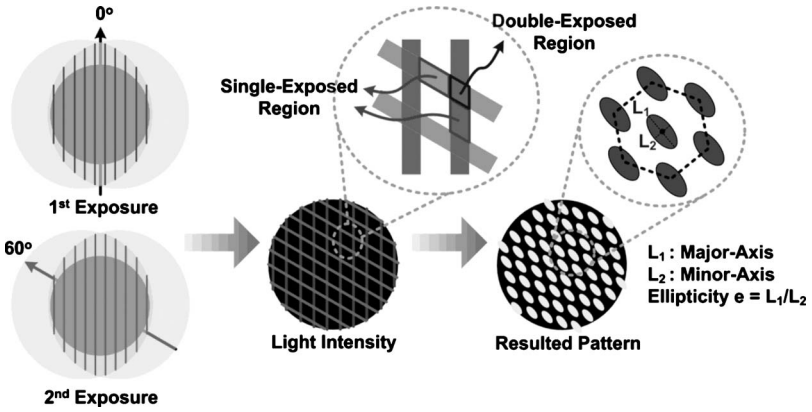

FIG. 1. Schematic diagram of process procedures for realizing hexagonal 2D photonic crystals by means of two-beam interference principle with double-exposure steps.

mixture of $Ar/SF_6/C_4F_8$ gases is used to directly transfer pillar patterns into silicon with a high aspect ratio and vertical sidewalls (no scalloping).

II. HOLOGRAPHIC CONCEPTS

As with conventional holography, using single-exposure of three-beam interference to obtain a two-dimensional interference pattern was theoretically[14] and experimentally[13] discussed. However, this method suffers from complicated process setup since the resultant pattern depends on both the propagation and polarization parameters of each beam. A holography setup based on a multiple exposure of two-beam interference principle is attractive due to its simplicity and flexibility.[4,8] A hexagonal array with a circular shape can be realized by triply exposing the same interference pattern with the sample rotated by 0°, 60° and 120°, respectively.[8,12] However, this method may suffer from an alignment issue for realizing submicron hexagonal 2D structures over a large area.[3] On the contrary, if double exposure of two-beam interference is executed at 0° and 60°, one can fabricate 2D periodic structure with a hexagonal lattice of elliptical geometry.[3,4,6,8,10,12] Although the shape of resultant pattern is elliptical, there still exists a photonic bandgap in this structure.[3] The relatively simple fabrication procedures and experimental setup of this method will improve the manufacturing yield, thus reducing the cost.

Figure 1 shows the schematic diagram of process procedures for realizing hexagonal 2D photonic crystals by means of two-beam interference principle with double-exposure steps. The sample is exposed to a one-dimensional interference stripe with a sinusoidal intensity profile at 0° and 60°. On the resultant 2D intensity distribution, the area covered only by one of exposure steps is referred to single-exposed region while the area overlapped by both exposure steps is the double-exposed region. The nonexposed region refers to the area where almost no exposed energy falls during both exposure steps. With a carefully controlled process, it is possible to realize a hexagonal lattice with an elliptical geometry. The ellipticity (e) of the resultant pattern is defined as the ratio between the length of major-axis (L_1) and minor-axis (L_2) of the ellipse.

III. THEORETICAL MODELING

Before fabricating two-dimensional periodic structures, a simulation model to calculate the profiles of holographically recorded patterns is necessary to initially understand the effects of each process parameter. The profile of recorded structures in photoresist depends on the light exposure pattern, photoresist sensitization and development. In the case of double-exposure in two-beam interference, the light exposure pattern can be described by

$$I_{\phi_1}(x,y) = 2I\cos^2[\mathrm{OPD}\times(x\cos\phi_1 + y\sin\phi_1)],$$

$$I_{\phi_2}(x,y) = 2I\cos^2[\mathrm{OPD}\times(x\cos\phi_2 + y\sin\phi_2)],$$

$$I_{\mathrm{total}}(x,y) = I_{\phi_1}(x,y) + I_{\phi_2}(x,y), \tag{1}$$

where I is the intensity of laser beam; OPD is the optical path difference which is defined by $\mathrm{OPD} = \pi[\sin(\theta_1) + \sin(\theta_2)]/\lambda$, where θ_1 and θ_2 are the incident angle of beam 1 and beam 2, and λ is the incident wavelength; ϕ_1 and ϕ_2 are the rotating angles of sample in the first and second exposure steps. Thus the total exposure pattern can be obtained by adding the intensity distribution $I(\phi_1)$ and $I(\phi_2)$ of the first and second exposure energies. The photosensitization process was mathematically represented by writing the inhibitor concentration m as a function of irradiance.[15]

$$m_{xy}(z) = \exp[-CI(x,y)\Delta T], \tag{2}$$

where C is the kinetic exposure rate constant and ΔT is the exposure time. In this article, we use normalized exposure energy $CI(x,y)\Delta T$ for obtaining the inhibitor concentration which ranges from 0 (complete exposed) to 1 (unexposed). The dissolution rate V of the photoresist in a developer can be described as[16]

$$V_{xy}(z) = V_{\max}\frac{(a+1)[1-m_{xy}(z)]^n}{a+[1-m_{xy}(z)]^n} + V_{\min}, \quad a = \frac{n+1}{n-1}(1-m_{\mathrm{th}})^n, \tag{3}$$

where $V_{\max}$ and $V_{\min}$ are the dissolution rates of the fully exposed and nonexposed photoresists, respectively (they are determined by the concentration of developer); a is a function of the inhibitor concentration threshold m_{th} at the onset

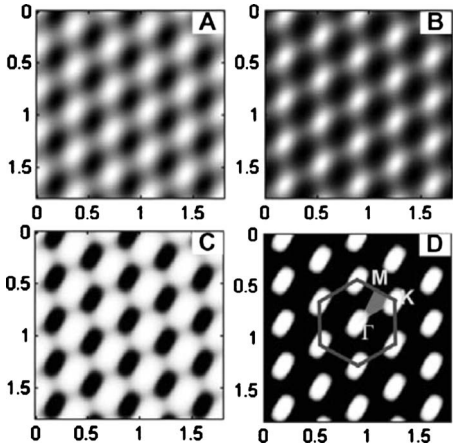

FIG. 2. (a) Light intensity distribution under double-exposure of two-beam interference. (b) Inhibitor concentration in the exposed photoresist during the photosensitization process. (c) Dissolution rate of the exposed photoresist in a developer. (d) Resultant patterns after development. Two-dimensional periodic patterns with a hexagonal lattice of elliptical pillars can be realized.

of dissolution, and n is the number of molecules of the product of the photoreaction that reacts with the developer to dissolve a resin molecule. Therefore, the remaining photoresist thickness $z(x,y,t)$ can be obtained by a simple integration of the dissolution rate $V(x,y,z)$.

$$z(x,y,t) = z(x,y,t_0) - \int_0^t V(x,y,z)dt. \tag{4}$$

Figure 2 shows the step-by-step transition process for the generation of two-dimensional hexagonal pillars. Parameters used in this model are shown in Table I. Due to the double-exposure process, there exist three different intensity levels (double-exposed region, single-exposed region, and nonexposed region) in the light intensity distribution which may result in three different exposure energies. Thanks to the nonlinear nature of the photoresist,[17] we can slightly overexpose to let the double- and single-exposed regions have almost the same cross-link effect to eliminate this problem. With optimal process condition, a well-defined arrayed pattern can be holographically realized.

Although the exposure pattern is sinusoidal, we can still produce a photoresist pattern with a squarelike profile by developing in strong nonlinear conditions. On the other hand, a sinusoidal profile will be expected if the development is in linear conditions because the isotropy of wet development produces a narrowing on the top of the structures.[16] That is, for the case of low exposure energy and high concentration developer, we cannot obtain isolated patterns since the dissolution rate in single- and double-exposed regions is still low and the resultant profile under high concentration developer (or long development time) becomes sinusoidal. However, if high exposure energy and low concentration developer (or short development time) is used for the same purpose, isolated patterns with vertical sidewalls become possible due to the sufficient dissolution rate in both single- and double-exposed regions such that the isotropic wet etching effect is eliminated.

Periodic pillars can be realized holographically by using a positive photoresist,[5–7] while arrayed holes can be fabricated by using a negative photoresist.[8,9,11,12] However, the use of negative photoresist suffers from fabrication problems including the resolution limit and the fact that it is harder to be removed by wet etching. On the other hand, if we utilize the nonlinearity nature of positive photoresist, we can obtain periodic holes by carefully controlling the exposure doses to have above-threshold dissolution rate in the double-exposed region and below-threshold dissolution rate in the single- and nonexposed regions. After development, only the photoresist in the double-exposed region can be removed and two-dimensional periodic holes can be realized. If the total exposure energy is enough to have above-threshold dissolution rate in both double- and single-exposed regions, two-dimensional periodic pillars will be realized. Figure 3 shows the evolution of the calculated profiles as the normalized exposure energy increases. When the normalized exposure energy is below 0.8 (above 1.2), the resultant pattern is a periodic hole (pillar) structure. The transited structure is observed when the exposure energy is between 0.8 and 1.2. From the calculated profile under 0.6 normalized exposure energy, we can find that the photoresist in the double-exposed region is totally removed, while that in the single-exposed region is almost remained, forming perfect hole patterns. There is a maximum thickness of photoresist for fabricating perfect holes or pillars with controlled exposure dose onto the photoresist.

TABLE I. Parameters for simulation of profiles of holographic photonic crystals.

Parameter	Symbol (unit)	Value
Incident wavelength	λ (nm)	325
Incident angle	θ_1, θ_2 (deg)	30, 30
Rotating angle of sample	ϕ_1, ϕ_2 (deg)	0, 60
Normalized exposure energy	$CI(x,y)\Delta T$ (a.u.)	variable
Number of molecules of the product of the photoreaction	n	6
Dissolution rate of the nonexposed and full-exposed photoresist	V_{min}, V_{max} (nm/s)	0.15, 45
Inhibitor concentration threshold at the onset of dissolution	m_{th}	0.61
Thickness of photoresist	T (nm)	200
Development time	DT (s)	Variable

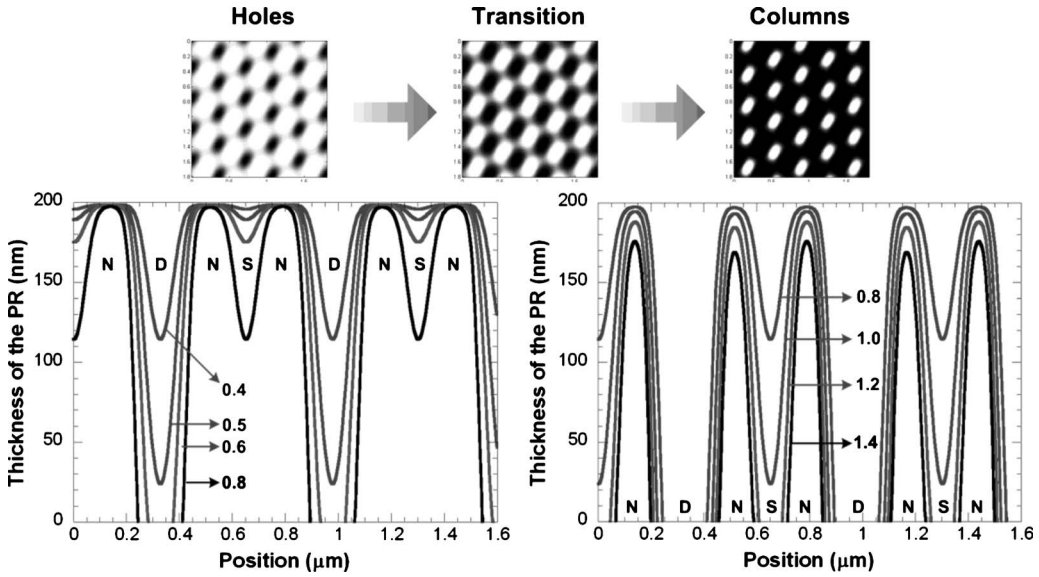

FIG. 3. Evolution of the calculated profiles with the normalized exposure energy (the numbers in the figure) for positive photoresist films double exposed to an interference pattern. By carefully controlling the total exposure doses, two-dimensional periodic holes or pillars can be realized by using a positive photoresist. Development time in this figure is set to 8 s (N: nonexposed region, S: single-exposed region, and D: double-exposed region).

Figure 4 shows the calculated profiles under different exposure doses. Periodicity of the hexagonal patterns in this calculation is set to 420 nm. Hollow-square and solid-circle symbols in Fig. 4 show the diameters of holes and pillars, respectively, while the hollow-circle and solid-diamond symbols show the ellipticity of holes and pillars, respectively. An increased (decreased) diameter of holes (pillars) for both major and minor axes of elliptical structure is expected as the exposure energy increases. From the overlap point of diameter curves, we know the maximal air fill factor (the ratio between the averaged radius of ellipse and the periodicity of resultant pattern) of holographic patterns is about 40% for both holes and pillars. The calculated ellipticity of the resultant patterns is about 1.73 throughout all exposure conditions. How the profile of the resultant patterns is affected under different development time is also investigated theoretically. Once the exposure energy is determined, sufficient development time is necessary to completely generate patterns. The aspect ratio of the resultant pattern will increase as the development time increases. The width of the pillars will be reduced as the aspect ratio reaches its maximum value. With neglectable back-reflection issue, there is only about 2 nm/s reduction rate for overdeveloped process.

Photonic bandgap maps of the calculated profiles under different exposure energies are shown in Fig. 5. Due to the noncircular geometries of the resultant patterns, the addition of new directions to represent one-quarter of the Brillouin zone is necessary.[6] Detailed discussion can be found in previous works.[3,6] As we expected, there exist TM-mode (electric field in plane) gaps in hole arrays, while TE-mode (mag-

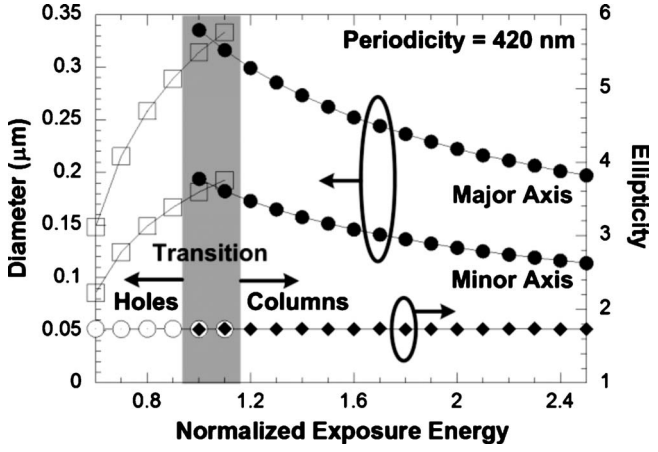

FIG. 4. Calculated profiles under different exposure energies. (Hollow-square and solid-circle symbols show the diameters of holes and pillars, respectively, while hollow-circle and solid-diamond symbols show the ellipticity of holes and pillars, respectively.)

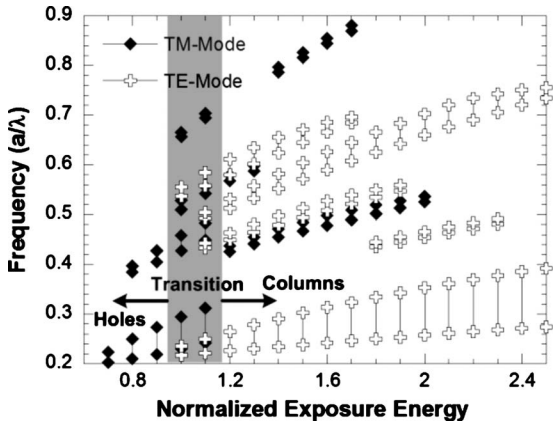

FIG. 5. Photonic bandgap maps of the calculated profiles under different exposure energy. (Solid-diamond and hollow-cross symbols show the TM- and TE-mode gaps, respectively.)

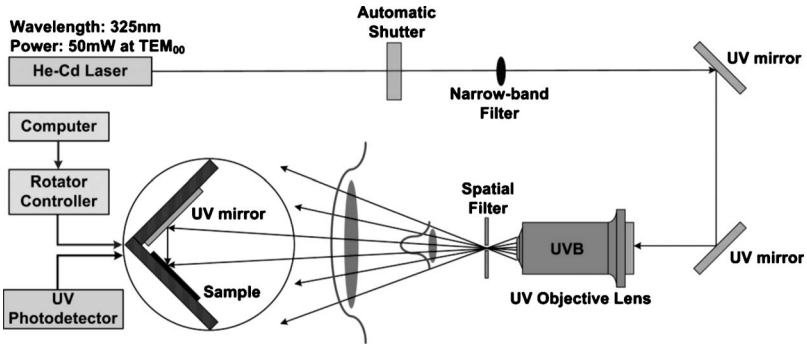

FIG. 6. Schematic diagram of our laser holography system

netic field in plane) gaps dominate pillar arrays. The gap size is affected according to the geometry of resultant patterns depending on the exposure energy.

IV. EXPERIMENTAL DEMONSTRATION

Figure 6 shows the schematic diagram of our holographic setup which consists of a light source, a narrow-band filter, an UV objective lens, a spatial filter, and a sample stage. The light source is a 50 mW He–Cd laser emitting at a wavelength of 325 nm in a single transverse mode. A 325 nm laser-line filter with 1.2 nm bandwidth and >80% transmission is used to guarantee the pure light from the He–Cd laser. An UV objective lens and a spatial filter are used to enlarge the total area of the light field at the sample stage and to block the noise from the laser source. At the sample stage, an UV-mirror and a sample holder plate are fastened together at 90°. All of the components in this holography system are transparent at 325 nm. By simply adjusting the stage orientation with respect to the direction of the laser beam, the periodicity of the resultant patterns can be easily controlled.

A. Realization of PhC templates with the help of AR coating

Due to the presence of an additional interference fringe parallel to the surface of sample, called standing waves, the use of high refractive-index substrates generate serious back-reflection problems to the lithography. This problem may be even stronger if the applied photoresist film is thicker than one-half period of the standing wave pattern. To reduce the contrast of the standing wave, some materials with the right thickness are proposed as AR coating layers.[18] The use of dielectric materials such as silicon dioxide or silicon nitride with an accurate thickness can also be served as the buffer layer to eliminate the back-reflection problem. However, reflectivity variation due to imperfect AR layers is an uncertain factor in the process. Commercial bottom AR coating materials are available from photoresist manufacturers. Such coatings provide a gradual variation of refractive index between the photoresist and substrate to reduce the back-reflection from the interface as well as to absorb the transmitted light, leading to wider thickness tolerance for the AR coating layers.

To calculate the back-reflection into the resist layer, we developed an analytical model by using a transfer matrix and modified transmission and reflection coefficients,[19] given the real and imaginary parts of the index of refraction for the materials and the incident angle θ of the two laser beams. Figure 7(a) shows the reflectivity variation under different thicknesses of AR coating layers with an incident wavelength of 325 nm. The structure of the test sample is also shown in the inset of Fig. 7(a). Back-reflection of the real photoresist/ARC/silicon sample with an incident angle of 30° is also calculated. Thickness and refractive index of the AR coating and photoresist layer are characterized by an ellipsometer (Rudolph AutoEL-III) and thin-film measurement system (Filmetrics F20-UV).

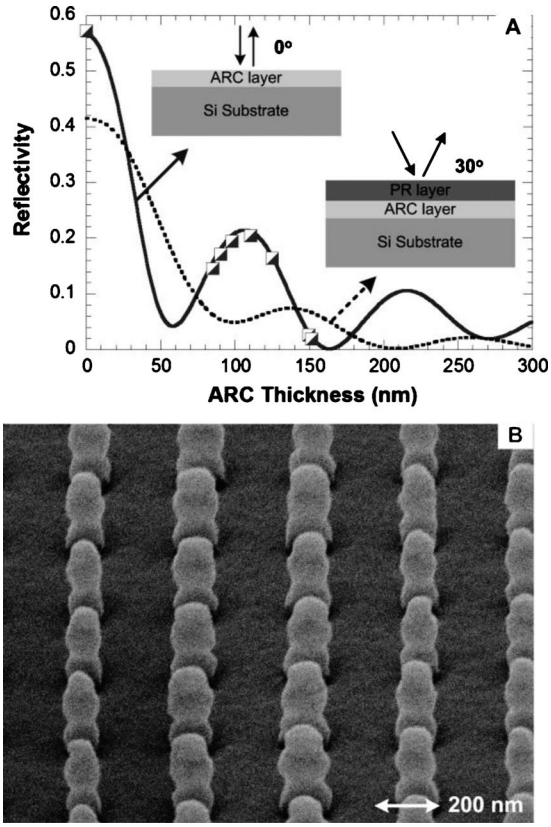

FIG. 7. (a) Reflectivity variation under different thickness of AR coating layer with an incident wavelength of 325 nm. The structure of the test sample is shown in the inset of the figure. (Solid and dot curves are simulation results while square symbols are experimental data. (b) 200 nm thick PhC templates using an 80 nm thick AR coating layer. Sidewall distortion on the resultant patterns caused from back-reflection can be clearly seen.

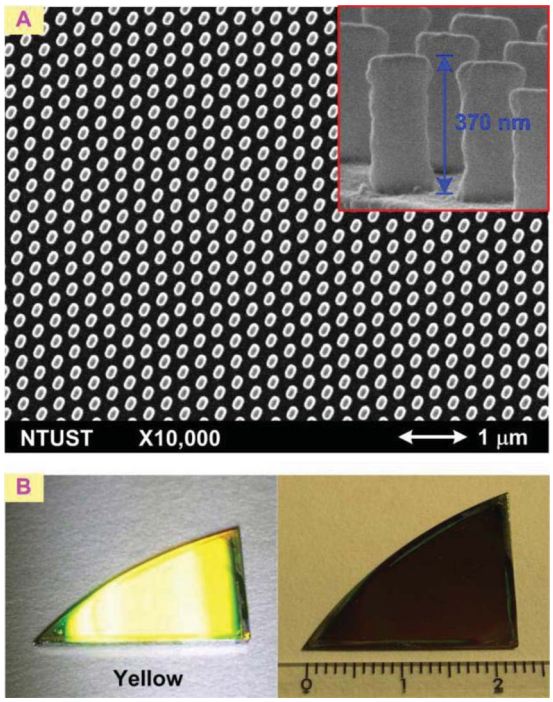

FIG. 8. (Color online) (a) SEM pictures of fabricated two-dimensional hexagonal pillars. 370 nm thick PhC templates with a high aspect ratio and vertical sidewalls are realized using a 160 nm thick AR coating layer. (b) Photographs of the resultant samples under tilted angles of illumination. Bright and uniform diffracted light throughout the sample proves a good quality of the resultant patterns. The samples are highly uniform in an area of $>2\times2$ cm^2 and present good reproducibility.

Without the help of AR coating, it is difficult to fabricate submicron patterns on silicon substrates due to serious back-reflection problem. Although photoresist with a thickness of half standing wave period can be used to avoid pattern distortion or collapse, only ~50 nm thick PhC templates is not sufficient as a mask for pattern transferring. 200 nm thick patterns can be realized using an 80 nm thick AR coating layer between photoresist and silicon substrate, as shown in Fig. 7(b). However, we can clearly see the distortion on the sidewalls of resultant patterns due to insufficient reduction of back-reflection.

370 nm thick PhC templates with an aspect ratio of 2.5 and vertical sidewalls are demonstrated with the help of a 160 nm thick AR coating layer, as shown in Fig. 8(a). Fabrication flow for this well-defined template is investigated as follows. Silicon substrate is cleaned by ultrasonification in acetone and isopropanol and blown dry with nitrogen gas. A 160 nm AR coating layer (Brewer Science XHRiC-11 ARC) is deposited by spin coating with a solution at 1500 rpm for 70 s. After prebaking the AR coating layer on a hot plate at 165° for 60 s, a 370 nm positive photoresist layer (OHKA THMR-M100) is deposited at 2000 rpm for 30 s and soft baked again at 90° for 90 s. The sample is then transferred to the laser holography system and exposed twice with a dose of 30.24 mJ/cm^2 for each exposure. Following the double-exposure, a postexposure bake (PEB) is performed on a hot plate at 115° for 120 s to further reduce the standing-wave effect. After that, the sample is dipped into standard 2.38% TMAH photoresist developer (AZ-300MIF) for 10 s to attain a periodic structure. After development, the sample is rinsed in de-ionized water and finally hard baked at 100° for 60 s to complete the cross-linking process. Figure 8 shows the SEM pictures and photographs of the resultant 2D hexagonal pillars. By using a flashlight to illuminate the PhC sample with a tilted angle in the directions perpendicular to double-exposure directions, a bright diffracted light throughout the sample and a change in color under different angles of illumination is observed, as shown in Fig. 8(b), indicating that the resultant PhC structure is well orientated throughout the sample with high uniformity and superior quality. The samples are highly uniform in an area of $>2\times2$ cm^2 and present good reproducibility.

B. Resultant profiles under different process conditions

In order to investigate the resultant profiles under different exposure energy, eight 200 nm thick hexagonal photonic crystal samples are fabricated with a development time of 5 s and exposure times of 100, 110, 120, 130, 150, 170, 190, and 210 s for each exposure, corresponding to the exposure doses of 14.4 mJ/cm^2 (sample A), 15.84 mJ/cm^2 (sample B), 17.28 mJ/cm^2 (sample C), 18.72 mJ/cm^2 (sample D), 21.6 mJ/cm^2 (sample E), 24.48 mJ/cm^2 (sample F), 27.36 mJ/cm^2 (sample G), and 30.24 mJ/cm^2 (sample H). Other process conditions such as PEB are the same as described in Sec. IV A except the rotational speed for the spin-on photoresist (5000 rpm for 30 s). Figure 9 shows the experimental profiles under different exposure doses. SEM pictures of the corresponding structures are shown around the analytical plot, which shows the diameter and ellipticity of the resultant patterns with the exposure energy.

We can find that air-hole patterns (samples A–C) can be realized with lower exposure energy while periodic pillars (samples E–H) can be realized with higher exposure energy. As the exposure energy increases, the diameters of holes increase for both axes of elliptical structure. An increase of the ellipticity of holes is observed. This may be mainly due to the slightly difference of exposure energy between the first and second exposure steps. The difference of exposure energy between the two exposure steps is due to nonuniform exposure and the rotation of sample. For pillar patterns, the diameters decrease for both axes of the ellipse as the exposure energy increases. The ellipticity of the pillars is always around 1.47 for different exposure energies. The reason for the ellipticity difference between experimental (Fig. 9) and theoretical (Fig. 4) results may be due to the other process effects such as PEB, which was not considered in our simulation model.

The effect of development time for the resultant profiles is also investigated here. Four 200 nm thick hexagonal photonic crystal samples are fabricated with an exposure energy of 21.6 mJ/cm^2 and development times of 5 s (sample A), 10 s (sample B), 15 s (sample C), and 20 s (sample D). Figure 10 shows the experimental profiles under different development

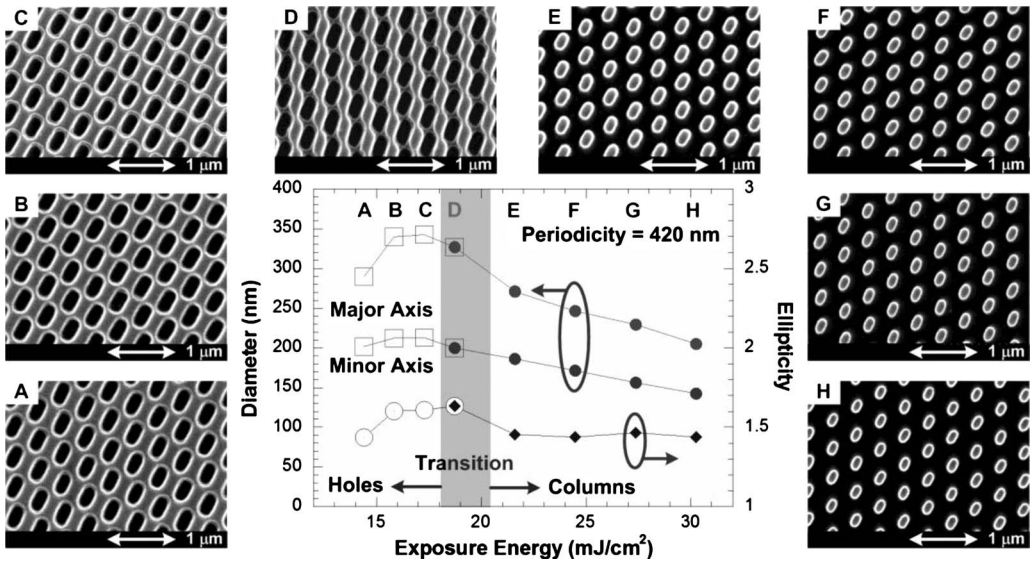

FIG. 9. Experimental profiles under different exposure energy. Eight uniformly hexagonal photonic crystal samples are fabricated with a lattice constant of 420 nm. SEM pictures of the corresponding structures are shown around the analytical plot which shows the diameter and ellipticity of the resultant pattern with the exposure energy. (Hollow-square and solid-circle symbols show the diameters of holes and pillars, respectively, while hollow-circle and solid-diamond symbols show the ellipticity of holes and pillars, respectively.)

time. SEM pictures of the corresponding structures are shown above the analytical plot, which shows the diameter and ellipticity of the resultant pattern with the development time. The width of the pillars is reduced as the development time increases. The reduction rates for the major and minor axes of ellipse are about 2.8 and 1.7 nm/s, which agree with our theoretical results. The difference of reduction rate between two axes of ellipse may be also due to the slightly difference of exposure energy between the first and second exposure steps. Such low reduction rate for overdeveloped process is also due to the help of good AR coating. From Figs. 9 and 10, we can find that the fabrication tolerance for holographic realizing 2D photonic crystals by double exposure process is very wide in terms of exposure energy and development time. The total exposure energy will determine the geometry of resultant patterns. Development time will not affect the patterns a lot.

C. Pattern transfer into silicon

Polymeric periodic arrays may seem unlikely to yield useful photonic structures since the refractive index of such ma-

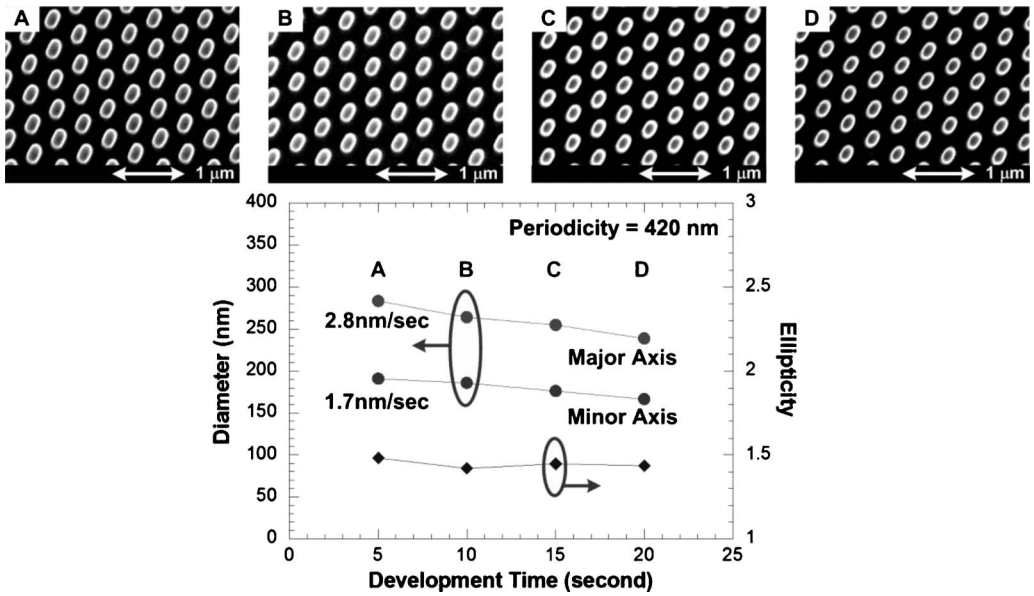

FIG. 10. Experimental profiles under different development time. Four 200 nm thick hexagonal photonic crystal samples are fabricated with a lattice constant of 420 nm. SEM pictures of the corresponding structures are shown above the analytical plot which shows the diameter and ellipticity of the resultant pattern with the development time. (Solid-circle symbol shows the diameter of pillars while solid-diamond symbol shows the ellipticity of the pillars.)

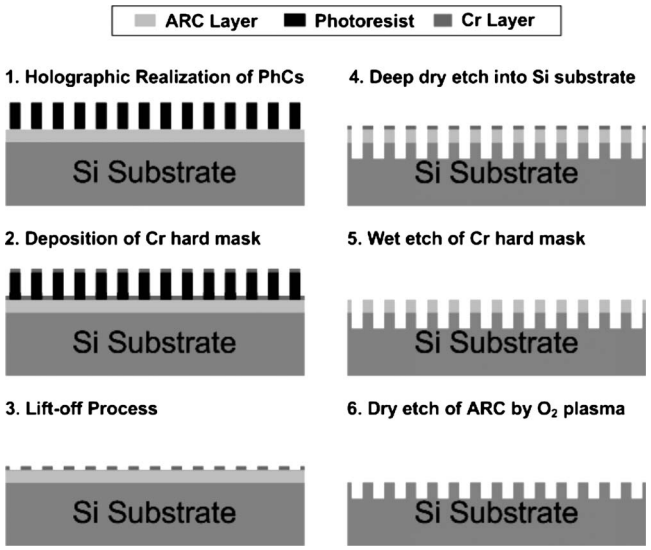

FIG. 11. Sequence of the experimental steps for transferring PhC patterns into silicon substrate by means of lift-off process and etching technique.

terials are substantially less than those of the more traditionally used solid-state materials such as silicon. Thus they are usually used as intermediate templates to create photonic lattices with higher index materials. To deep transfer the patterns into silicon substrate, a hard mask such as chromium (Cr) is often used to provide high etching selectivity for the following deep etching process but metal hard mask patterning can be difficult. It is also possible to transfer patterns into metal layer by wet etching process. However, undercutting due to isotropic etching makes wet etching useless for nanometer-scale patterns. Another way to transfer the patterns is to perform a lift-off process but the resultant patterns will be inversed.

We perform a lift-off process to transfer patterns into a chromium hard mask layer for the following dry etching into silicon substrate. The fabrication flow of pattern transfer is shown in Fig. 11. SEM pictures of the resultant patterns after Cr evaporation (procedure 2 of Fig. 11), lift-off using a blue-tape (procedure 3 of Fig. 11), and dry etching into silicon (procedure 6 of Fig. 11) are shown in Fig. 12. After preparing a 370 nm thick hexagonal PhC template with a lattice constant of 375 nm by means of laser holography method, as described in Sec. IV A, a 35 nm chromium film is deposited onto the photoresist template by angled e-beam evaporation to generate a hard mask layer, as shown in Fig. 12(a). Since the resultant patterns are not clean by conventional lift-off method using an acetone solution (removed Cr patterns are usually sticked back onto the samples), the following lift-off process is carried out by using a blue tape to stick the photoresist patterns away from the samples. Although some photoresist patterns are left on the samples after lift-off, they can be easily removed by wet etching or O_2 plasma since no Cr mask lies on the top of photoresist. The resulting patterns are much clean and uniform by this method as shown in Fig. 12(b). Dry etching the patterns into the AR coating layer and silicon substrate is then carried out using a conventional RIE machine with a CF_4 flow of 5 SCCM (SCCM denotes cubic centimeter per minute at STP), 100W rf power, and a pressure of 80 mTorr. After performing 15 min of dry etching procedure, the photonic crystal pattern is then transferred through the 160 nm AR coating layer and into the silicon substrate to a maximum depth of about 650 nm. Since there is still Cr on the surface, deeper etching is possible. To remove the remaining Cr and AR coating layers on the surface of the sample, a wet etching process is used to remove the Cr layer, while oxygen plasma is then used to clean the residual AR coating layers. Figure 12(c) shows the side-view of the transferred silicon PhC structures. Highly uniform photonic crystals on silicon substrates with a high aspect ratio (>4) and vertical sidewalls are demonstrated over a large area.

Contrary to conventional schemes for PhC pattern transfer, a novel DRIE is developed and utilized for etching PhC pillar patterns into silicon substrates. DRIE is mainly used for microelectromechanical systems and microfluidic device fabrication. Multiple cycles of the two-step Bosch process enable anisotropic etching of silicon with high mask selectivity (>200:1 for silicon oxide and >75:1 for PR) and high etching rate (several μm/min). However, this technique is not suitable for etching nanostructures due to its scalloping of the sidewalls (the peak-to-valley height is typically the scale of around several hundred nanometers). Recently, with the development of this technology, Choi *et al.*[20] directly transferred 20 nm thick photoresist patterns into silicon with controlled sidewall profiles using a Bosch process. More recently, Morton *et al.*[21] realized silicon pillar array with an aspect ratio of >50:1 and a peak-to-valley height (scalloping) of ~10 nm using a Bosch process with an optimized

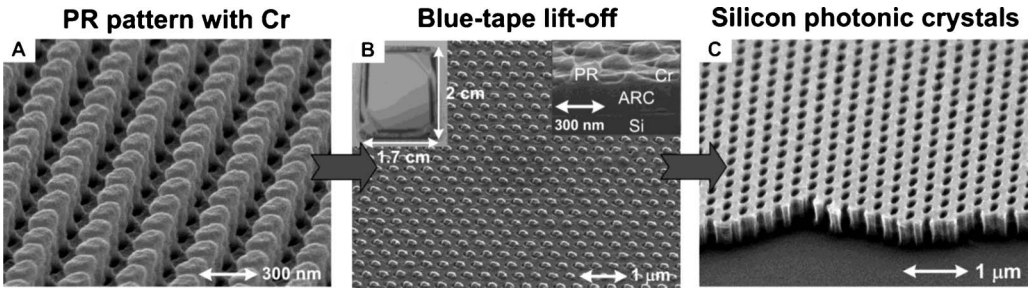

FIG. 12. SEM pictures of the resultant patterns after (a) Cr evaporation (procedure 2 of Fig. 11), (b) lift-off using a blue-tape (procedure 3 of Fig. 11), and (c) dry etching into silicon (procedure 6 of Fig. 11)

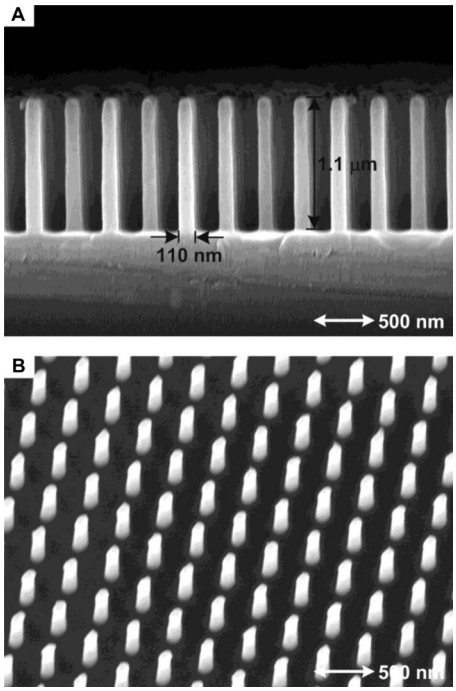

FIG. 13. Cross-sectional and tilted SEM views of vertical silicon nanopillars with an aspect ratio of 10 using a single-step deep reactive ion etching and controlled mixture of $Ar/SF_6/C_4F_8$ gases.

etching conditions. However, the scalloping of the sidewalls cannot be avoided due to the cyclic deposition/etching nature of the Bosch process, resulting in periodic ripples on the sidewalls. We have developed a means of directly transferring photoresist patterns into silicon using a single-step DRIE and controlled mixture of $Ar/SF_6/C_4F_8$ gases. With an optimized gas mixture for balancing the deposition (C_4F_8 flow) and etching rate (SF_6 flow), pillars with vertical sidewalls can be realized. During the etching process, the scalloping of the sidewalls can be avoided while reserving the high mask selectivity ($\sim 85:1$) and relatively high etching rate (222 nm/min). Figure 13 shows the cross-sectional and tilted SEM views of the transferred patterns. Silicon nanopillar arrays with an aspect ratio of 10 and vertical sidewalls are achieved with high uniformity over a large area. Systematic analysis of this novel DRIE process is under development and will be discussed in elsewhere.

V. CONCLUSION

A complete investigation of holographic photonic crystal structures has been conducted. Hexagonal photonic crystals with an elliptical geometry can be realized by performing a double-exposure of laser holography method. Theoretical and experimental results show that two-dimensional periodic holes or pillars can be realized depending on the total exposure energy onto the surface of positive photoresist layer. The photonic band diagrams for the PhC structures under different exposure doses are also analyzed. Width reduction of the resultant patterns under different development time is also investigated. An analysis model is developed and an antireflection layer is used for eliminating the back-reflection from the substrate. Optimized process procedures for holographically realizing photonic crystals on a silicon substrate with good quality are addressed. Submicron photonic crystal templates with an aspect ratio of 2.5 and vertical sidewalls are demonstrated. The samples are highly uniform in an area of $>2\times 2$ cm^2 and present good reproducibility.

A lift-off process is performed to transfer inversed pillar patterns into a chromium hard mask for the following deep dry etching into silicon substrates using a conventional RIE machine. A single-step DRIE with controlled mixture of $Ar/SF_6/C_4F_8$ gases is used to directly transfer pillar patterns into silicon. Transferred patterns with a high aspect ratio and vertical sidewalls are demonstrated by those methods over a large area. We believe that holographic photonic crystals will be a low-cost choice for a variety of industry applications, including efficiency enhancement of light emitting diodes and solar cells, biomedical sensing, and photonic integrated circuits.

ACKNOWLEDGMENTS

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Fabrication of Highly-ordered Silicon Nanowire Arrays with Controllable Sidewall Profiles for Achieving Low Surface Reflection

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***Abstract* — A novel and simple approach is demonstrated for fabricating silicon nanowire arrays (SNWAs) with controllable sidewall profiles. A single-step deep reactive ion etching (SDRIE) is used to transfer the holography patterned photoresist template to silicon or silicon-on-insulator substrates. With the SDRIE etching process, scalloping of the sidewalls can be avoided while reserving the high mask selectivity and high etching rate. The sidewall angle of resultant patterns can be adjusted by tuning the composition of the gas mixture of the process. A modified SDRIE process with a linearly-changed gas flow is further developed to extend its capability. A post high-energy argon plasma treatment is used to create sharp tips on the top of SNWAs and to increase the filling factor. Broadband antireflective (AR) window with a low reflectivity can be realized from tall SNWAs with high filling factor. Depositing silicon dioxide over SNWAs can further enhance the AR performance. The position and bandwidth of the AR window can be controlled by tuning the SNWA parameters.**

***Index Terms* — silicon nanowire array, single-step deep reactive ion etching, holography lithography, antireflection**

I. Introduction

SILICON nanowire arrays (SNWAs) have been extensively used in many emerging technologies including bio-medical sensing [1], chemical sensing [2], electronic field emission [3], optical wave-guiding [4, 5], field effect transistors [6], and photovoltaic devices [7-9]. Except for bottom-growth techniques, a sequence of patterning and etching processes are usually required to realize nanostructures in semiconductors. Most of nanostructures are patterned using electron-beam lithography, which has the disadvantages of being time consuming and low throughput. On the other hand, holographic lithography is an attractive method for periodic pattern generation with high uniformity over a large area. For transferring the SNWA patterns to semiconductor structures, numerous etching schemes have been reported for attaining high-aspect-ratio nanostructures. Most of them require a metal hard mask for the following deep etching [10-13]. The metal hard mask may require an additional lift-off step that will degrade the profile resolution and increase process complexity. Recently, self-masked dry etching technique is proposed by depositing nano-clusters formed by reactive gas mixtures [14, 15]. However, the resultant nanostructure arrays are lack of regularity. Deep reactive ion etching (DRIE) is mainly used for micro-electro mechanical systems (MEMS) and microfluidic device fabrication. Multiple-cycles of the two-step Bosch process enable anisotropic etching of silicon with high mask selectivity (>200:1 for silicon oxide and >75:1 for photoresist) and high etching rate (several μm per min) [16]. The major concern for using this technique to etch nanostructures is the scalloping of the sidewalls where the peak-to-valley height can be in the scale of several hundred nanometers. Recently, researchers have demonstrated the use of Bosch etching to realize submicron structures [17, 18] and silicon nanopillar arrays with a high aspect ratio and reduced scalloping of the sidewalls [19]. However, the scalloping effect is still a critical issue for etching deeper nanowires.

In this work, we have realized two-dimensional (2D) resist templates by using the holography lithography [20]. We developed a single-step deep reactive ion etching (SDRIE) scheme to directly transfer the photoresist (PR) patterns into silicon based structures. The effects of various process parameters are investigated in order to control the resultant profile. A modified SDRIE process is developed for obtaining tall SNWAs. A tip sharpening scheme is also developed to realize tapered nanowires with large filling factor. The anti-reflection characteristics of the SNWAs realized with the new fabrication schemes are then measured and discussed.

II. Single-Step Deep Reactive Ion Etching

We developed a novel SDRIE technique for fabricating silicon nanowire arrays by simply using the PR template as the hard mask. For the etching of silicon nanowires, we use a Plasma-Therm 770 SLR series system with a loadlock for deep etching silicon pillars. The system has an inductively coupled plasma (ICP) coil and a capacitively coupled substrate RF

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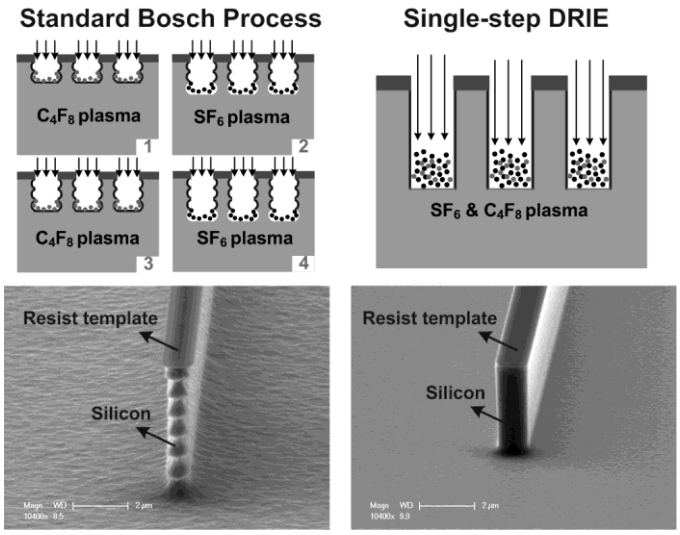
supply to independently control the plasma density and ion energy in the system. This system can be used to deeply etch silicon by means of the conventional Bosch process which cycles between a polymer deposition cycle using C_4F_8 gas without substrate bias and an etching cycle using a SF_6 mixture with substrate bias. Due to the isotropic etching nature of SF_6 dry etching, it causes scalloping on the sidewalls. We developed a SDRIE process with a controlled mixture of $Ar/SF_6/C_4F_8$ gas to avoid this scalloping issue while simultaneously achieve high etching rate and high mask selectivity. Polymer deposition for protecting lateral sidewalls and deep silicon etching proceed simultaneously in the SDRIE process.

The difference in the etched profiles between the conventional Bosch process and SDRIE can be clearly observed from Figure 1 for etching a 2-μm wide waveguide. Detailed information of the process condition is listed in Table 1. Although higher etching rate (~2.3 μm/min) and higher selectivity (~88.46) can be obtained in the Bosch process, serious scalloping occurs on the sidewalls (~265 nm) of the resultant profile. On the contrary, patterns with smooth and vertical sidewalls become possible by using the SDRIE process.



(a) (b)

Figure 1 Schematic of etching process and the resultant profiles for (a) Bosch and (b) SDRIE process

The use of SDRIE to fabricate SNWAs includes two steps: holographic lithography and SDRIE. We use a 270 nm thick PR template rather than a thin one [18] as the mask for deep etching. The SNWAs have a square lattice with a lattice constant of 350 nm. High uniformity can be achieved over a large area with the help of an antireflection coating (ARC). Transferring PR patterns into the bottom ARC layer is carried out by using the anisotropic O_2 plasma using a conventional reactive ion etching (RIE) machine with an O_2 flow of 10 sccm, a pressure of 10 mTorr, and a RF voltage of 250V. The substrate is then etched by SDRIE using the PR/ARC pattern as a hard mask. After SDRIE, the remaining PR/ARC is removed by the isotropic O_2 plasma with an O_2 flow of 20 sccm, a pressure of 80 mTorr, and a RF voltage of 250V. Finally, the substrate is cleaned with a Piranha solution (H_2SO_4:H_2O_2 = 3.75:1 by volume) at a lifted temperature of 100 degree Celsius. The resultant structures are then characterized using a scanning electron microscope (SEM).

In order to control the SNWA profile, we will report the effects on the resultant profile by varying the process conditions. For comparisons, the reference process condition is set as the flow rate of Ar, SF_6, C_4F_8 being 20, 26, 54 sccm, respectively, the dc-bias power of 9 W, ICP power of 800 W, and the chamber pressure of 19 mTorr.

A. Effect of $Ar/SF_6/C_4F_8$ gas mixture

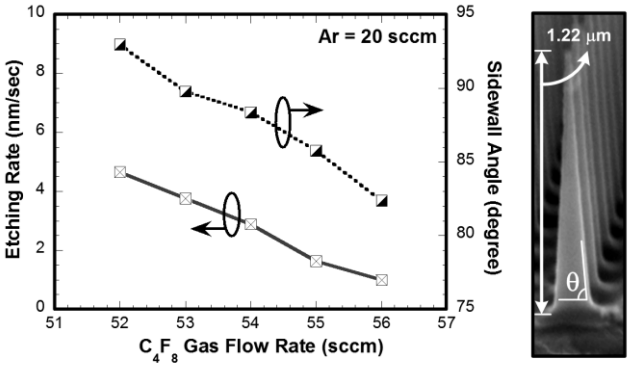
The gas mixtures will affect the etching rate and slope of nanowire sidewalls. The incorporation of Ar gas during the SDRIE process is to stabilize the helium gas in the system. The contribution of additional physical bombardment by Ar gas to the silicon etching rate in the SDRIE process is relatively small. Therefore, in this experiment we vary only the relative flow rate of SF_6 and C_4F_8 from the reference condition. The total flow rate of SF_6 and C_4F_8 is fixed at 80 sccm. Figure 2 (a) shows the silicon etching rate and the corresponding sidewall angle against the gas flow rate of C_4F_8. The C_4F_8-dominated (SF_6-dominated) process condition has lower (higher) silicon etching rate and smaller (larger) sidewall angle. Here the sidewall angle is defined as the inner angle of the pillar, as shown in Figure 2 (b). When the etching and deposition processes are balanced, high-aspect-ratio patterns with vertical sidewalls can be obtained. On the other hand, pillars with a tapered profile and a sharp tip can be realized by increasing the flow rate of C_4F_8. Undercut can appear in the pillars as the SF_6 flow rate rises, which may lead to the collapse of patterns. In our previous report, we have demonstrated hexagonal-oriented SNWAs with almost the same height but different sidewall angles by tuning the gas mixture and etching time [21]. Here, the etching time is fixed at 3 minutes for obtaining the variation of etching rate and SNWA profile under different gas mixture. Lower C_4F_8 (SF_6) flow rate results in lower (higher) silicon etching rate and smaller (larger) sidewall angles. Around 10 degree sidewall tunable angle is achieved, verifying that tall SNWAs with controlled profiles can be realized by adjusting the gas mixture.

Table 1 Etching conditions of Bosch process and SDRIE and the corresponding resultant profiles

Dry etching	Time (min)	$C_4F_8/SF_6/Ar$ (sccm)	Pressure (mTorr)	ICP/Bias (W)	Height (μm)	Scalloping (nm)	Selectivity
Bosch process	2	0/100/40 70/0/40	23	825/13	4.6	265.5	88.46
SDRIE	10	52/28/20	19	850/9	3.15	0	16.52

B. *Effect of chamber pressure*

The chamber pressure can also affect the etching rate and slope of nanowire sidewalls. SNWA samples are fabricated by varying only the chamber pressure from the reference condition. The etching time is fixed at 5 minutes. Figure 3 shows the silicon etching rate and the SNWA sidewall angle against the chamber pressure. The silicon etching rate is increased with the chamber pressure due to the increased fluorine radical density [22, 23]. However, the increased fluorine radical density also causes the undercut-etching problem. The saturation of silicon etching rate happens as the pressure is higher than 19 mTorr.



(a) (b)

Figure 2 Etching rate and sidewall angle, as defined in (b), for different C_4F_8 gas flow rate.

C. *Effect of dc-bias and ICP power*

The degree of dissociation of fluorine is of primary importance in determining etching rate and profile shapes. As the electromagnetic field induced by the ICP source power, a low source power process can lead to neutral-driven etching rather than ion-driven etching. From our experimental results, the etching rate is relatively insensitive to the ICP source power.

To study the influence of dc-bias power on the SDRIE process, SNWA samples are fabricated by SDRIE with the reference process condition except that the dc-bias power is set as 4, 7, 9, 11 and 13 W, respectively. The etching time is fixed at 3 minutes. Figure 4 shows the etching rate and selectivity of SDRIE under different dc-bias power. Lowering the physical bombardment on the wafer surface induced by the ion acceleration leads to isotropic etching with undercut-etching. By increasing the dc-bias power, the addition of physical etching enhances the etching rate of silicon and PR/ARC and minimizes the silicon lateral etching rate, which will eliminate the pattern shrinkage. However, in case that the physical etching process dominates, the etching selectivity decreases as the dc-bias power rises. Besides, the sidewalls become rough as a high dc-bias power is applied in the SDRIE process. The compromised value for the dc-bias power of SDRIE is around 9 to 11 W, which will provide an etching rate of around 3 nm/sec, a selectivity of around 16, and smooth sidewalls.

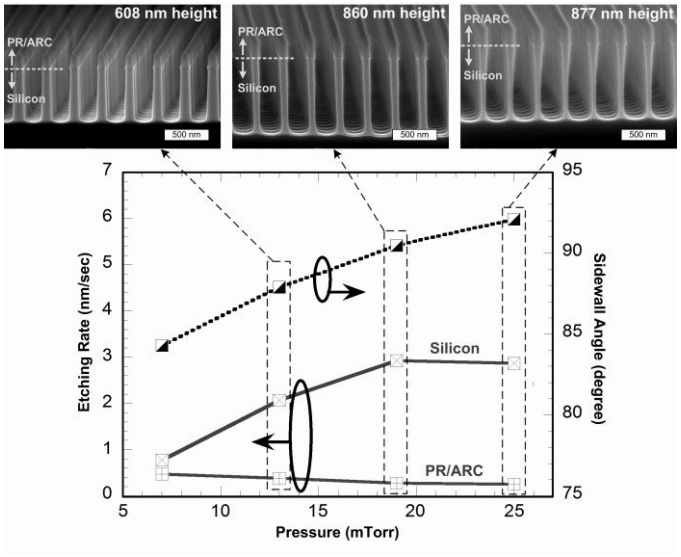


Figure 3 Silicon etching rate and SNWA sidewall angle against the chamber pressure

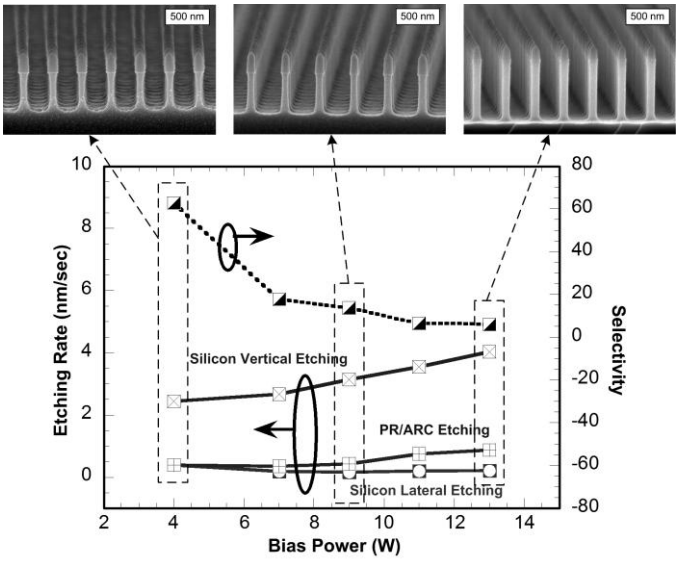


Figure 4 Etching rate of SDRIE and the sidewall angle of resultant patterns under different flow composition of SF_6 and C_4F_8 gas mixture

III. Modified SDRIE and Tip Sharpening

A. *Modified SDRIE with linearly-changed gas flow*

Low silicon surface reflection can be realized with the help of tall nanostructure arrays [24]. Tapered profile of nanostructures could further improve the antireflective properties [25]. The goal of this work is to realize tall SNWAs with tapered rods and moderate filling factor (radius-to-lattice-constant ratio). Although the SDRIE process is good for making silicon nanopillar arrays with a high aspect ratio and smooth sidewalls, the issues of pattern shrinkage, RIE-lag [22], and undercut etching may limit the process flexibility. We can realize tall nanostructures by increasing the etching time of SDRIE. However, as the etching proceeds deeper, the etching rate in the vertical direction will be decreased due to the RIE-lag effect.

Thus, it will require a longer etching time to achieve taller pillar structure. However, the pattern shrinkage becomes serious for a long etching process due to the lateral etching of the PR and silicon. For example, the SDRIE A and B processes, as listed in Table 2, result in very narrow pillars as the height exceeds 900 nm. Thus, it is difficult to realize tall nanowire structures while maintaining a large filling factor by using the SDRIE process. It can be clearly seen from Figure 3 that the lateral undercut is serious in tall nanostructures since it is hard for both the etching (SF_6) and protection (C_4F_8) gases to flow into the high-aspect-ratio nanostructures. From Figure 2, more C_4F_8 gas flow for sidewall passivation is needed to achieve vertical sidewalls. The reduced total gas flow inside tall nanostructures will result in the SF_6-dominated etching process, thus cause lateral undercut etching in the bottom of pillars. Serious lateral undercut may lead to the collapse of patterns.

From Figure 4, the pattern shrinkage problem can be reduced by increasing the physical bombardment (increase the dc-bias power) and decreasing the chemical etching (decrease/increase the SF_6/C_4F_8 gas flow). To verify this point, we change the bias power from 9 W to 13 W and the SF_6/C_4F_8 gas mixture from 26/54 sccm to 25/55 sccm. The process condition and resultant profile is listed as "SDRIE C" process in Table 2. After 5-minute etching, a 906 nm tall silicon pillar can be realized to have an improved filling factor of 0.13 and vertical sidewalls.

In order to obtain SNWAs with larger filling factors, we demonstrate here a "modified SDRIE" process, as listed in Table 2, by linearly changing the gas flow. During the process, the flow rate of C_4F_8 (SF_6) changes linearly from 55 (25) sccm to 55.8 (24.2) sccm in five steps. Silicon nitride (SiNx) is used as the hard mask for deep silicon etching. A stronger hard mask is also good for maintaining the width of the resultant patterns. Pattern transfer from PR/ARC into SiNx is carried out by anisotropic CHF_3 plasma etching. The etching time in each step is set to 1.5 minutes. Higher bias power (13 W) is used to eliminate the pattern shrinkage. The resultant profile after each step of the process is shown in Figure 5 and the corresponding parameters are summarized in Table 2. The pillar height can reach 632 nm after 3-minute etching (after step 2). A 1340 nm tall and tapered SNWA with an aspect ratio of 10.89 and a filling factor of 0.18 is obtained with a total etching time of 7.5 minutes (after step 5).

B. Tip-sharpening Process

Another approach for making nanotip array is to utilize the post tip-sharpening process. Tip sharpening can be performed by using high-energy argon plasma treatment after the SDRIE etching. In the experiment, two set of SNWA samples with almost the same sample area are fabricated by the SDRIE process to have a height of 464 nm (sample A) and 880 nm (sample B), respectively. These samples are then exposed to the plasma atmosphere for 20 minutes with an argon gas flow of 20 sccm, a chamber pressure of 80 mTorr. The RF bias voltage is varied from 50 V to 500 V for observing the tip sharpening process.

Figure 6 shows the SEM photos of resultant profiles after post argon plasma treatment for different RF bias voltages. It can be found that a bias voltage of 50 V for the tip sharpening process has little effect on the resultant pattern profiles. The top of the pillars become rounded as the bias voltage is raised to 200 V. The tip-sharpening of Si pillars happens with a bias voltage of 350 V or larger. We believe that the tip sharpening effect is due to the existence of higher electric field at the pillar edges, resulting in an enhanced sputtering rate there. However, the height of resultant patterns decreases as the bias voltage increases because of the enhanced physical bombardment, as shown in Figure 7. It is interesting to find that the width of resultant patterns increases with the bias voltage. This might be due to the fact that the silicon material of pillar arrays is sputtered out and attached on the sidewalls, resulting in an increase in the filling factor of SNWAs.

Table 2 Comparison between the original and modified SDRIE process

Etching processes		SDRIE process conditions				Resultant profiles		
		Time (min)	C_4F_8 (sccm)	SF_6 (sccm)	Bias power (W)	Height/Width (nm)	Filling Factor	Sidewall Angle (degree)
SDRIE A		5	54	26	9	978/30.2	0.04	90.6
SDRIE B		7	54	26	9	1390/24	0.03	90.3
SDRIE C		5	55	25	13	906/93.5	0.13	90
Modified SDRIE	Step 2	1.5 per Step	55 ↓ 55.8	25 ↓ 24.2	13	632/150	0.21	90.5
	Step 3					849/139	0.20	89.6
	Step 4					1110/130	0.19	89.1
	Step 5					1340/123	0.18	88.4

* The pressure, ICP power and Ar gas flow are fixed at 19 mTorr, 800 W and 20 sccm, respectively. Original SDRIE process uses PR/ARC as the hard mask. Modified SDRIE process uses silicon nitride as the hard mask.

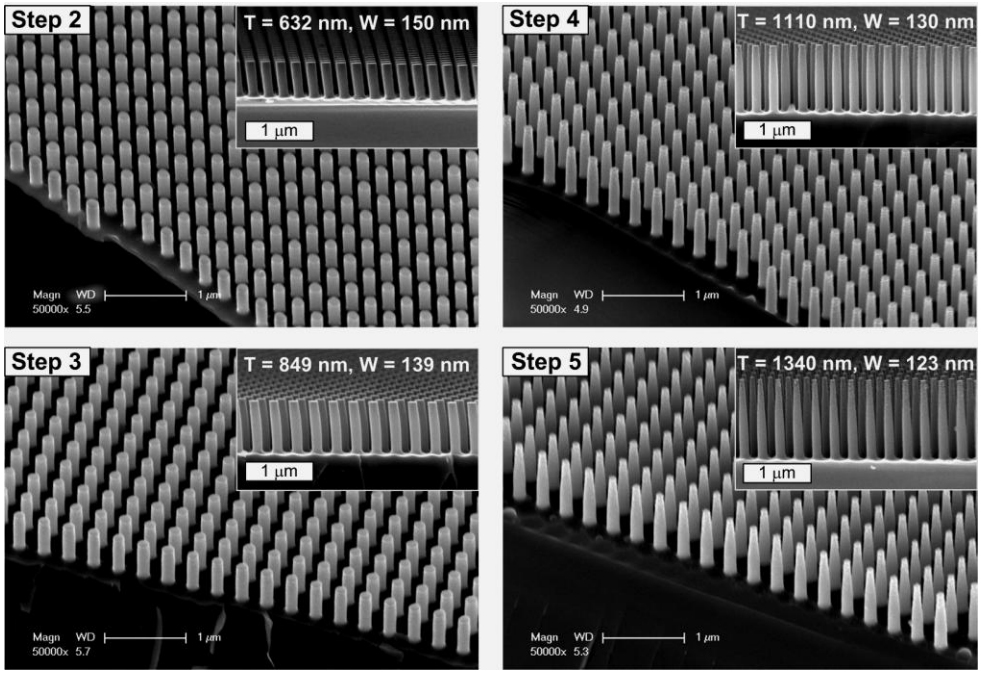


Figure 5 SEM views of resultant profiles after each step of the modified SDRIE with linearly-changed C_4F_8/SF_6 gas flow

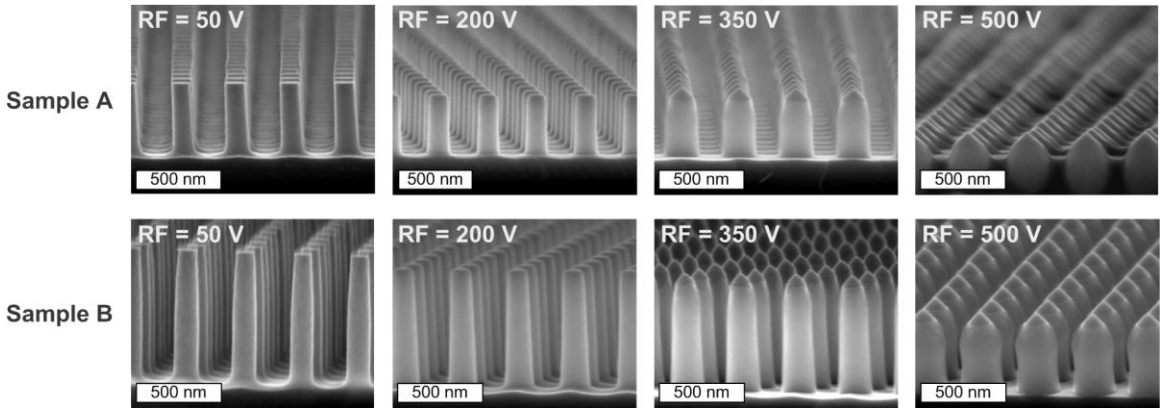


Figure 6 SEM views of resultant SNWA profiles (Sample A and B) after post argon plasma treatment with different RF bias voltages.

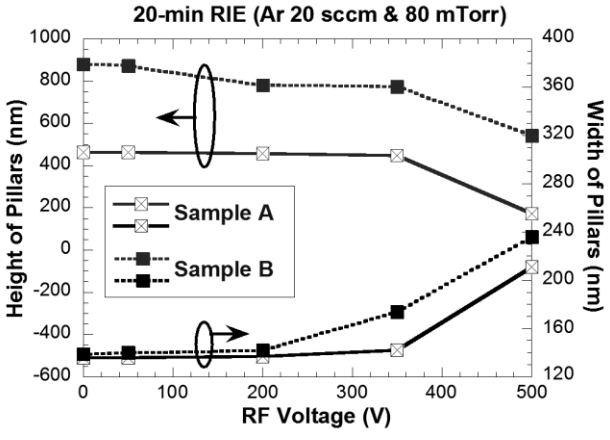


Figure 7 The height and width of resultant profiles (Sample A and B) after post argon plasma treatment with different RF bias voltages.

IV. Optical Reflection

A. *Modified SDRIE realized SNWAs*

We have fabricated tall SNWAs with moderate filling factor by using the modified SDRIE process. Optical reflection spectra of the resultant SNWA samples are characterized using a spectrophotometer (Filmetrics F20-UV). Figure 8 shows the reflection spectra of the SNWAs after each step of the modified SDRIE process. Since the resultant SNWAs are not tall enough after Step 2 of the modified SDRIE, the reflection can be as high as 25% in the visible region. The antireflection effect is improved as the SNWAs become taller and tapered. The reflectivity between 550 nm and 700 nm of wavelength can be as low as 0.2% for the SNWAs after Step 5 of the modified SDRIE. The reflectivity can be less than 7% over the whole visible region.

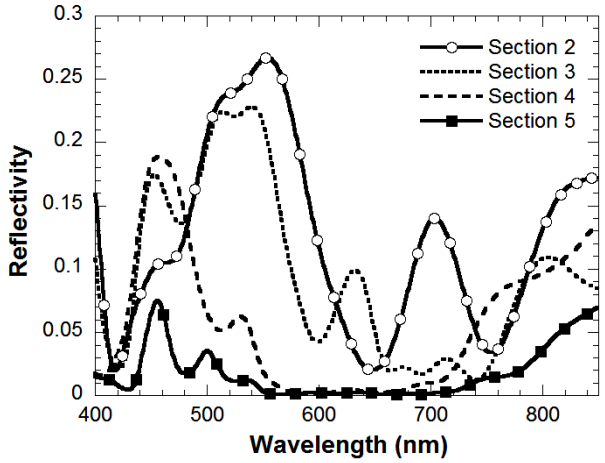


Figure 8 Measured reflection spectra of SNWAs after each step of the modified SDRIE with linearly-changed C_4F_8/SF_6 gas flow, as listed in Table 2.

B. SNWAs after argon plasma treatment

The argon plasma treatment after SDRIE etching can be used to sharpen the tips of SNWAs and to increase their filling factor. Figure 9 shows the reflection spectra of the SNWAs after argon plasma treatment with different RF bias voltages for Sample A and B in Figure 6 and 7. Since the original SNWAs of Sample A are relatively short, low reflectivity can only be obtained over a narrow wavelength range. The lowest reflectivity for the original Sample A is around 3% at 625-nm wavelength. The reflection spectrum of sample A after 200 V argon treatment is slightly improved to be around 2.4%. For Sample A after 500 V argon treatment, the height and width of the resultant SNWAs change to 173 nm and 211 nm, respectively, with sharp tips on the top. Due to the shallow nanostructures, the resultant SNWAs lose the photonic crystal property but provide surface roughness effect, resulting in an around 10% reflectivity throughout the visible region.

For the taller sample B, the minimum reflectivity is around 1.2% in the visible region. The reflectivity is slightly reduced to be around 1% after 200 V argon treatment. The height and width of resultant SNWAs change dramatically to 543 nm and 236 nm, respectively, after 500-V argon bombardment. With sharp tips on the top and enlarged filling factor, 33.7%, the low-reflectivity window is red shifted. The reflectivity is increased for shorter SNWAs.

C. SiO_2 coated SNWAs on silicon-on-insulator substrate

The SNWAs reported in previous sections are fabricated on bare silicon substrate. In this section, we address the properties of SNWAs on silicon-on-insulator (SOI) wafers, which are often used for fabricating optical integrated circuits or thin-film optoelectronic devices. The SOI wafer contains a 2 μm thick silicon dioxide as the intermediate layer and a 6 μm thick silicon layer on the top. SNWA samples are fabricated using the SDRIE process. Figure 10 shows the reflection spectra of the bare SOI, 250 nm tall PR/ARC templates on SOI, 700 nm tall SNWAs on SOI, and the 700-nm tall SNWAs coated with a 186 nm thick SiO_2 film. The SiO_2 film is deposited by plasma-enhanced chemical vapor deposition (PECVD) over the tall SNWAs to serve as a buffer layer between SNWAs and air.

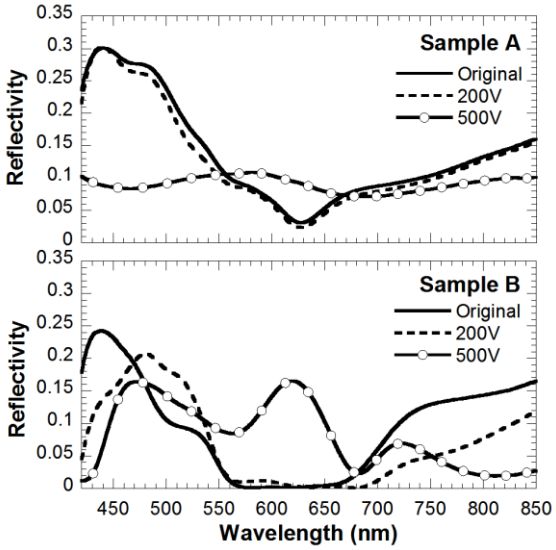


Figure 9 Measured reflection spectra of Sample A and B in Figure 7 after post argon plasma treatment with different RF bias voltage.

Lower reflectivity of PR/ARC templates on SOI is due to its lower effective index which serves as a buffer layer between air and silicon substrate. Reduced reflectivity over the UV wavelengths is due to the absorption characteristic of the ARC film. SNWAs on the SOI substrate can provide lower reflectivity than the bare SOI wafer over a wide wavelength range due to its deeper sub-wavelength structure. The overall reflectivity of this nanostructure is below 20% in the entire UV-to-visible region and is around 2.5% in the wavelengths between 500 nm and 550 nm. The reflectivity is further reduced by depositing a SiO_2 film on top of the SNWAs. The reflectivity is below 10% over the entire UV-to-visible region and below 1% for the wavelengths between 500 nm and 600 nm. It verifies that SNWAs coated with a SiO_2 film of right thickness can also improve the AR performance. Since SOI wafer contains Si-SiO_2-Si structures, multi-cavity resonance can be observed in

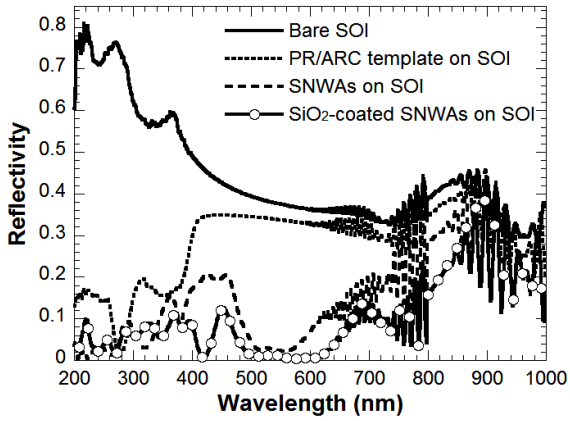


Figure 10 Measured reflection spectra of bare SOI, 250 nm tall PR/ARC templates on SOI, 700 nm tall square SNWAs on SOI, and the 700-nm tall SNWAs coated with a 186 nm thick SiO_2 film

the longer-wavelength side of the reflection spectra.

D. Change of antireflective spectra with SNWA parameters

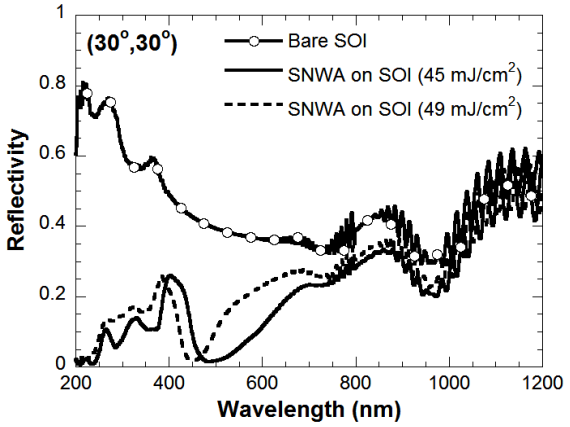
To figure out how the SNWA parameters affect the characteristic of AR window, we fabricated several SNWA samples on SOI substrate to have different widths, lattice constants, and heights. Figure 11 (a) shows the reflection spectra for SNWAs with different holography exposure time that leads to different pillar widths. The SNWAs with smaller pillar width have blue-shifted reflection spectrum and reduced bandwidth of AR windows. Figure 11 (b) compares the reflection spectra for SNWAs with different lattice constants. Again, the low-reflectivity window becomes narrower and moves to shorter wavelengths for the SNWAs with a smaller lattice constant. The trend shown in Figure 11 (a) and (b) agrees with the rigorous coupled-wave analysis (RCWA) simulation results. Figure 11 (c) shows the reflection spectra for the SNWAs with different SDRIE etching time that result in different pillar heights. The RCWA simulation indicates that taller SNWA results in the broadening and red-shifting of the anti-reflection spectrum. However, for SNWAs realized by the SDRIE process, pattern shrinkage in taller SNWAs leads to smaller pillar width because of the lateral silicon etching. Thus the overall reflection spectrum is broadened but blue-shifted, as shown in Figure 11 (c). The effects of the SNWA parameters on the antireflection property of SNWAs are summarized in Table 3.

Table 3 Optical property variation for different SNWA parameters

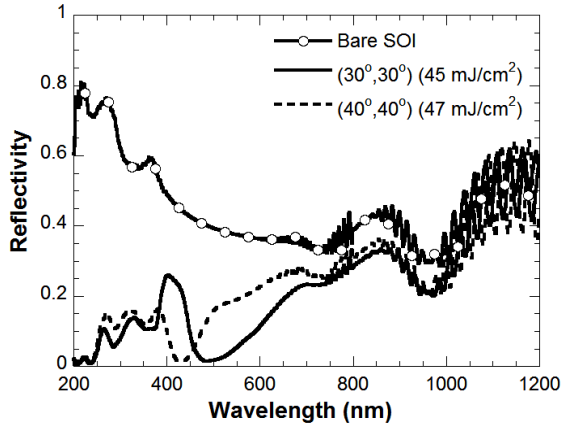
SNWA parameters	Simulated AR spectrum	Measured AR spectrum	AR bandwidth
Pillar height ↑	Red shift	Blue shift	Increased (↑↑)
Pillar width ↑	Red shift	Red shift	Increased (↑)
Lattice constant ↑	Red shift	Red shift	Increased (↑)

V. CONCLUSION

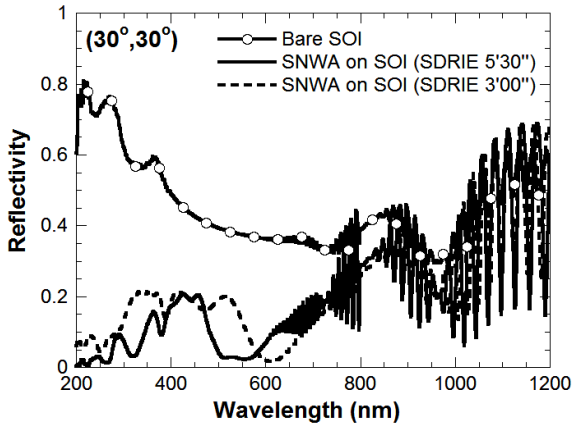
A novel and simple approach for fabricating tall SNWAs with high uniformity is demonstrated. PR templates realized by the holographic lithography can be used directly as the hard mask for the SDRIE etching. The SDRIE process with a controlled mixture of $Ar/SF_6/C_4F_8$ gas can be used to attain smooth and controllable sidewalls on the resultant SNWA patterns while simultaneously keeping the advantages of high mask selectivity and high etching rate. The sidewall angle of resultant patterns can be adjusted by adjusting the composition of the gas mixture of SDRIE process. A modified SDRIE process with a linearly-changed gas flow is developed to solve the undercut-etching issue, to eliminate the pattern shrinkage by using a higher dc-bias power and a stronger hard mask. The high-energy argon plasma treatment after SDRIE etching can be used to increase the filling factor and create sharp tips on SNWAs. This post-etching process can be used to amend the reflection spectra of SNWAs.



(a)



(b)



(c)

Figure 11 (a) Measured reflection spectra of 330 nm spaced square SNWAs on SOI substrate with different exposure time during holography for obtaining different pillar widths. (b) Measured reflection spectra of SNWAs on SOI substrate with different lattice constants. (c) Measured reflection spectra of square SNWAs on SOI substrate width different SDRIE etching time for obtaining different pillar heights.

We also demonstrate that SNWAs coated with a SiO_2 film can be used to obtain good AR performance, which is comparable to what we have achieved from tapered SNWAs [8]. How the SNWA parameters affect the characteristic of AR window is also investigated. With increased height, width and lattice constant of SNWAs, the AR window will be widened and red-shifted. The highly-ordered SNWAs fabricated with the SDRIE process and the post-etching treatment can be used for reducing surface reflection with high controllability.

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